# Lab 5 : Event Simulator

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Table with pipeline

| Program | Instructions | Cycles | Stalled times | Wrong paths | Throughput |
|---|---|---|---|---|---|
| Evenodd | 6 | 14 | 4 | 0 | 0.4285 |
| Prime | 29 | 45 | 7 | 5 | 0.6444 |
| Palidrome | 49 | 93 | 33 | 7 | 0.52688 |
| Fibonnaci | 78 | 120 | 22 | 16 | 0.65 |
| Descending order | 277 | 469 | 100 | 88 | 0.59 |

Table with Event simulator and pipeline

| Program | Instructions | Cycles | Stalled times | Wrong paths | Throughput |
|---|---|---|---|---|---|
| Evenodd | 6 | 312 | 4 | 0 | 0.01923 |
| Prime | 29 | 1348 | 7 | 5 | 0.02151 |
| Palidrome | 49 | 2375 | 33 | 7 | 0.02063 |
| Fibonnaci | 78 | 3855 | 22 | 16 | 0.020233 |
| Descending order | 277 | 15639 | 100 | 88 | 0.01777 |

## Observations :

1.The number of times OF stalls (Data Hazards) and the number of times wrong paths are taken (Control Hazards) remains same as earlier because only the number of cycles taken to read/write from memory and execute has changed. It does not effect data hazards and control hazards.

2.The number of cycles will be different because in the earlier case, we assumed that all the stages takes one cycle to complete its functionality but now we have introduced latency so all stages will take different number of cycles to complete its execution.As we have increased the latency, the number of cycles have increased drastically. As the main memory latency is 40 cycles, the total number of cycles are greater than 40 times the number of instructions.

3.The thorughput has decreased because of the increase in latency. The throughput in terms of instructions per cycle is approximately equal to 0.02 for all the cases which is appriximately 25 times less than the earlier implementation with unit latency.