Lab 5 : Event Simulator with Cache

Imtiyaz Ahmad : 170020037
P Sathwik : 170020034

Table 1:

When Li cache is 1KB and Ld cache keeps varying in size with fixed latency = 2cycles

Ld size (in Bytes)	even or odd	prime	palindrome	fibonacci	descending
4	326	768	997	1753	6091
8	326	768	997	1753	5531
32	326	768	997	1753	4171
128	326	768	997	1753	4171
256	326	768	997	1753	4171
512	326	768	997	1753	4171
1024	326	768	997	1753	4171

Table 2:

When Ld cache is 1KB and Li cache keeps varying in size with fixed latency = 2cycles

Li size (in Bytes)	even or odd	prime	palindrome	fibonacci	descending
4	326	1408	2437	4033	144151
8	326	1408	2437	4033	144151
32	326	768	997	2353	10731
128	326	768	997	1753	4171
256	326	768	997	1753	4171
512	326	768	997	1753	4171
1024	326	768	997	1753	4171

Table 3:

When Ld cache is 1KB and Li cache is 1KB and latency keeps on varying in size

Latency	even or odd	prime	palindrome	fibonacci	descending
1	319	738	946	1664	3805
2	326	768	997	1753	4171
4	340	828	1099	1931	4903
8	368	948	1303	2287	6367
12	396	1068	1507	2643	7831