8-bit DAC Design

Report submitted as a

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Course project

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ABSTRACT

In this project, we have implemented 8-bit DAC as an application of current mirrors. We have used Simple Cascode current mirror, Sooch's cascode current mirror and low voltage Sooch's cascode current mirror to implement current sources. Several non-linearities are pointed out in the design and simulation part along with their possible reasons. Finally we test our DAC circuit by sampling a sine wave, using digital input to DAC and retrieving back the analog signal. FFT analysis is also performed to highlight the linearity. We obtained a voltage swing of 600mV, with a load of 50Ω.

The MATLAB codes for sampling the sine wave and generating digital inputs for both sine wave and ramp, along with the LtSpice schematics and the complete project is archived here : [Shubham & Harsh (2021)]

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Chapter 1

Objective

The objective of this project is to design a 8-bit Digital to Analog Converter(DAC) as an application of current mirrors. The DAC implemented will use following topologies for implementing current sources :

- Cascode Current mirror,
- Sooch's Cascode[Sooch (1985)] or Low Voltage Sooch's Cascode.

Upon designing the DAC, qualitative FFT analysis for digital sine wave input to understand linearity issues.

1.1 Design parameters :

We will be using PTM 65nm CMOS SPICE models for simulation. For Circuit simulation we have used LTspice and for scientific computing we have used MATLAB.

Given Specifications :

Given specifications		
Supply Voltage (V)	Output Swing(peak-to-peak) (mV)	Load resistance (Ω)
1.2	600	50

DAC Topology :

Binary Weighted, Current switching or current steering

Chapter 2

DAC Topology

We want to convert a 8-bit digital signal, to a analog voltage/current signals. We first try to convert the 8-bit digital signal to analog current, which eventually can be converted to voltage if required.

2.1 Basic Topology (Current Switching)

The basic topology which is easily accomplished has following idea behind :
$I_{out} = D_0 \times I_o + D_1 \times 2I_o + D_2 \times 2^2 I_o + D_3 \times 2^3 I_o + ... + D_7 \times 2^7 I_o$, where I_o is the unit value of the binary weighting. The idea is illustrated in the figure (Fig. 2.1). We have implemented this topology, however this topology has few shortcomings and

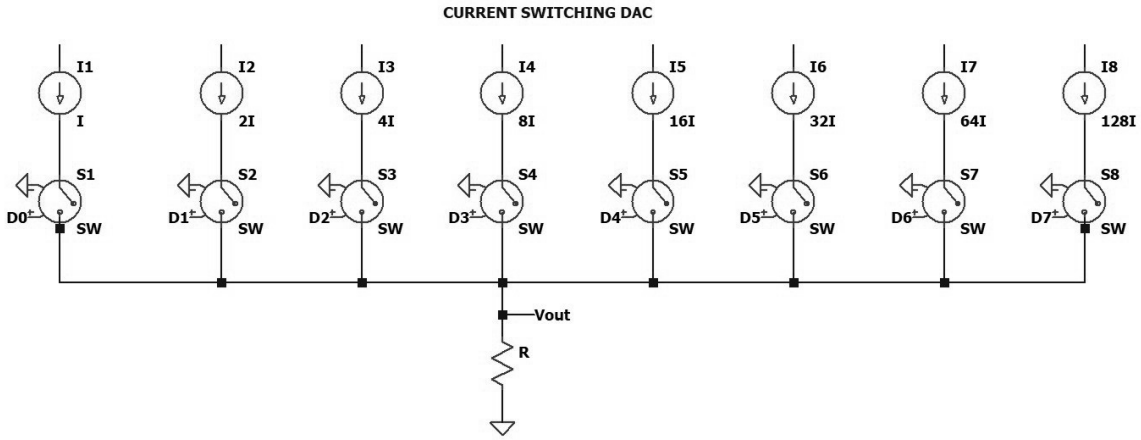

Figure 2.1: Current Switching DAC

not implemented practically. Due to the switching nature the parasitic capacitance in current sources charges and discharges leading to transient behaviours and spikes, to name one of the dynamic errors. [Razavi (2018)].

2.2 Current steering topology

The current steering topology does not suffer from transient behaviour of capacitance as there is no switching action so, no charging -discharging, furthermore we get a differential output naturally. The following figure (Fig. 2.2) demonstrates the topology. Here, the 2 switches at each current source are toggled by complementing digital

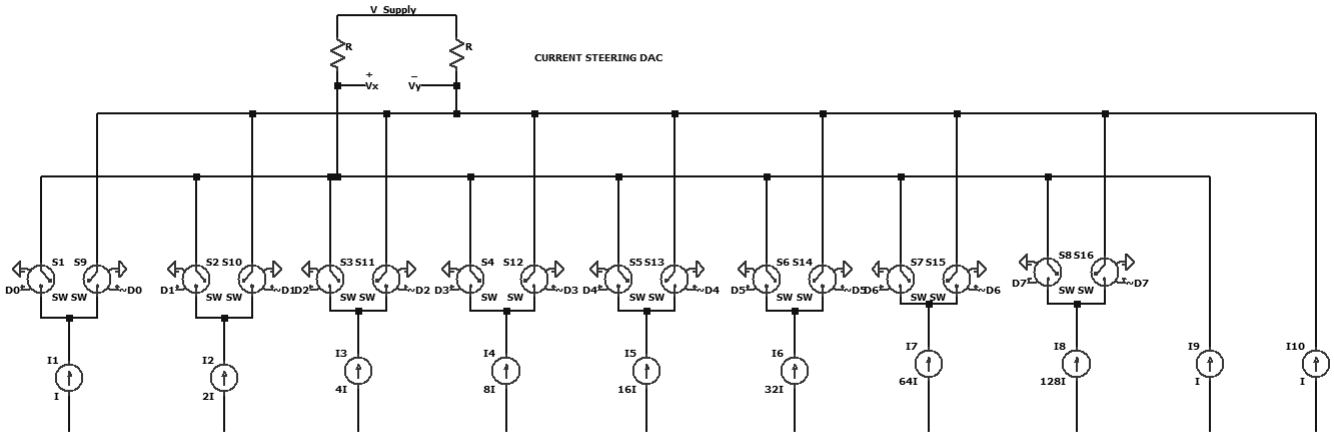

Figure 2.2: Current Steering DAC

signals, i.e. when one switch is on the other remains off and vice-versa. Also, we can observe that we get differential output, i.e even harmonics will be absent. So we may expect higher linearity in current steering DAC than current switching.
The maximum current through a branch is $256I_o$ while at the same time other branch has minimum current of I_o, where I_o is unit current. So, the differential voltage output ranges from $-255I_oR$ to $255I_oR$, with a step of $2I_oR$, i.e it represents 255 distinct voltage levels.

Chapter 3

Current Sources

The DAC is implemented as an application of current mirrors. In this chapter, we present different current mirror biasing circuits we used, and their characteristics.

3.1 Cascode Current Mirror

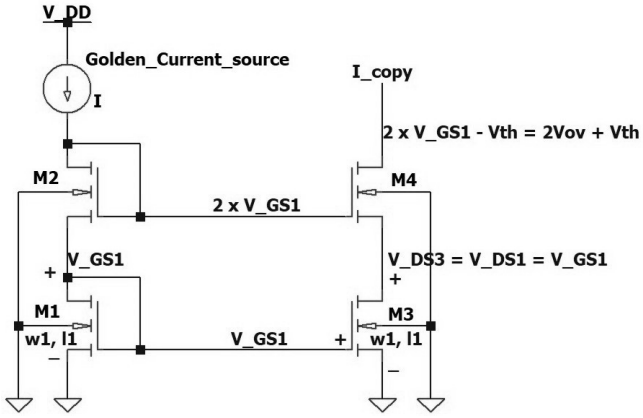

Figure 3.1: Cascode Current Mirror

From the figure (Fig. 3.1), we can observe following characteristics of cascode current mirror circuit :

Characteristics of Cascode Current mirror	
Compliance voltage	$2V_{OV} + V_{th}$
Accuracy	100%(99.9%)*
R_{out}	$g_{m_4} r_{o3} r_{o4}$

* due body effect and other non-idealities.

3.2 Sooch's Cascode and Low voltage Sooch's cascode

Sooch's cascode [Sooch (1985)] improves compliance voltage, while maintaining high output impedance and high accuracy. Low voltage Sooch's cascode has 2 stages in biasing circuit, therefore it has more power consumption but supply voltage is reduced. Following figure (Fig. 3.2) illustrates this. Following the voltage calculations

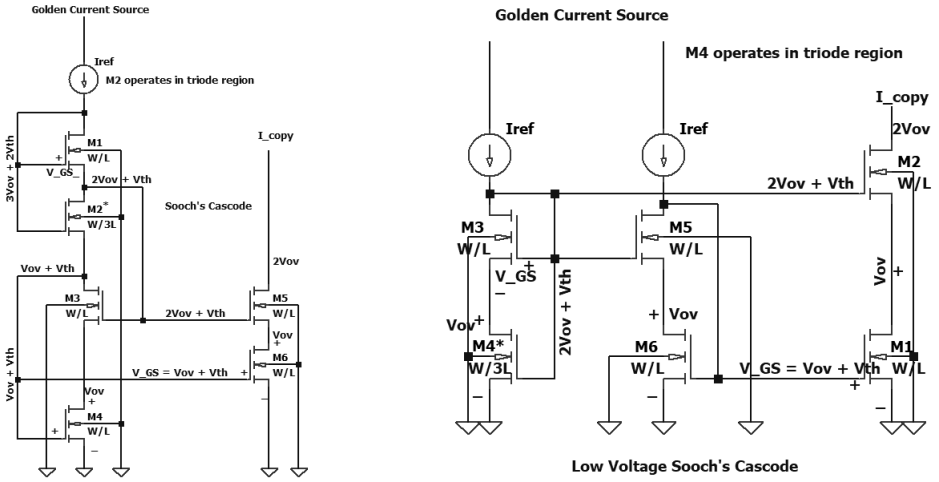

Figure 3.2: Sooch's Cascode[Left] & Low Voltage Sooch's Cascode[Right]

in the figure (Fig. 3.2), we can observe that $M2$ in Sooch's and $M4$ in low voltage Sooch's mirror operate in triode region and have a $\frac{1}{3} \times \frac{W}{L}$ ratio for obtaining : $V_{DS4} = V_{dsat}$ and $V_{GS3} = V_{dsat} + V_{th}$.

3.3 Problems encountered by using Simple Current Mirror biasing

Following problems can be encountered readily by using simple current mirror biasing:

- Low Accuracy in Mirroring : Due to channel length modulation. There is high possibility of not getting required accurate steps and voltage swings. There is also a high possibility to observe *major carry transition*, even at lower number of bits.

- Low Output Resistance : In DAC topology the output resistances changes when different cells turn on, .i.e $R_{eff} = R_L || \frac{r_{o,eff}}{m}$, when m cells turns on. So, voltage levels may differ.[Razavi (2018)] This non-linearity is reduced by high $r_{o,eff}$.

Chapter 4

Calculations, Design and Simulations

In this chapter, we discuss the calculation, design, simulation and qualitative analysis.

4.1 Calculation

Current Switching DAC

We get the value of I_{LSB} from our design constraint of having maximum output swing as 600mV, thus when all the branches are delivering current maximum voltage across the resistor R is 600mV :
$2^N * I_{LSB} * R = 600mV$ where N = 8
$I_{LSB} = \frac{600mV}{2^8 * 50\Omega} = 47\mu A$.

Current Steering DAC

Calculation of I_{LSB} unit current source :
$V_{max} = 0.5V_{peak-peak} = \frac{600mV}{2} = 300mV$, — (1)
Maximum analog voltage level = $V_{max} = 255I_oR$, where $R = 50\Omega$ — (2)
$\implies I_{LSB} = 23.44\mu A$.

4.2 Design

Design of Current Switching DAC

We are using Low Voltage Sooch Cascode as the biasing circuit. PMOS transistors are used as they act as a current source. The size of the transistors in the the biasing circuit are choosen to maintain the ratio: $(\frac{W}{L})_{Mb} = \frac{1}{3}(\frac{W}{L})_{Ma}$ to ensure low compliance voltage and perfect mirroring. For the transistors meant to carry $I_{LSB}, 2I_{LSB}.....2^{(N-1)}I_{LSB}$ their sizes have to be scaled accordingly. Instead of increasing the width of transistors to reach the desired ratio we use number of transistors in parallel depending on the current they have to carry keeping size of each unit the same. This is done to lower the noise, improve linearity and reduce the problems arising due to mismatches between them.

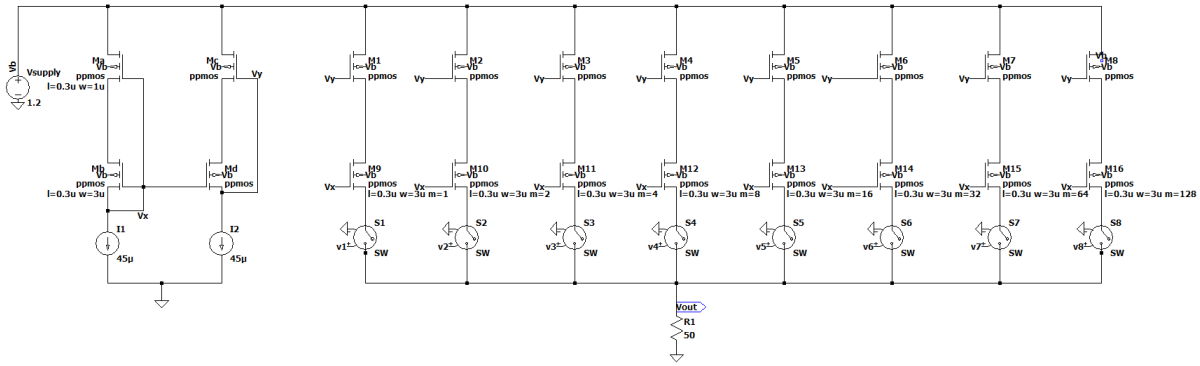

Figure 4.1: Current Switching DAC

Design of Current Steering DAC

L of transistors are chosen to be $300nm(\simeq 5 \times 65nm)$, to prevent channel length modulation and other short channel effects. W is chosen to be $6\mu m$.
For simple cascode current mirror, proper biasing circuit is used as shown in figure (Fig. 3.1). For low voltage Sooch's cascode the transistor which operates in triode region has $\frac{1}{3}$rd W/L ratio, so W for that transistor($M4$ in Fig. 3.2) is chosen to be $2\mu m$. The number of fingers are chosen to get the binary weights of currents in each current mirror. Since, the voltage swing required is easily obtained, no tweaking is required with the values of cascode transistors in each current source.

For the steering circuit design we have used 2 switches, which are toggled by digital bits(acts like a SPDT switch).

Schematics

Following current steering circuit was used in DAC design :

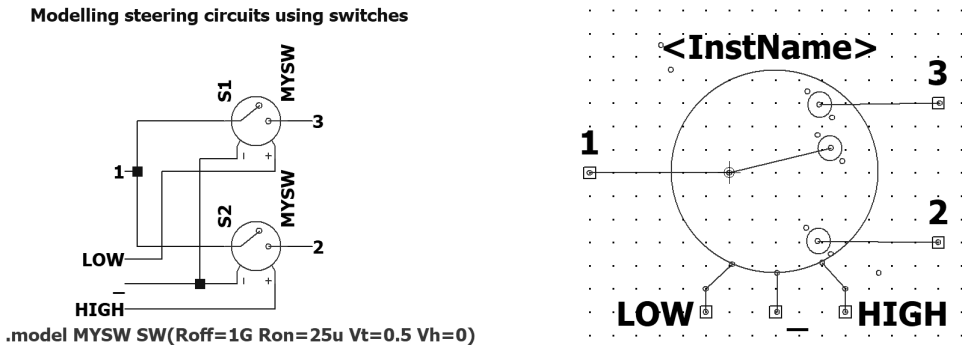

Figure 4.2: Schematic of Steering circuit[Left] & Symbol of Schematic[Right]

Following are the schematic of current steering DACs, Fig. 4.3 and Fig. 4.4 :

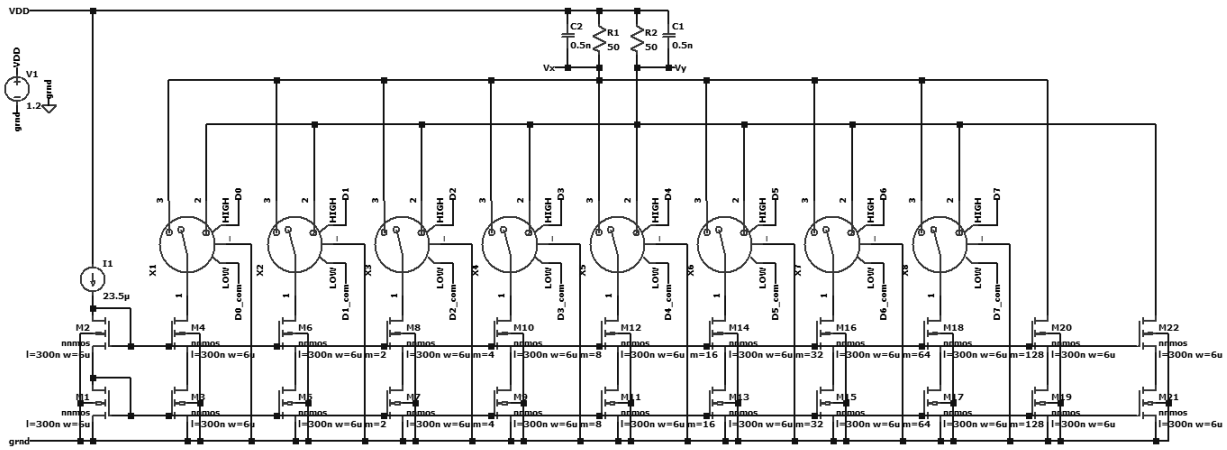

Figure 4.3: Schematic of current steering DAC, with cascode current mirrors

Getting digital inputs into circuit : We used PWL text file input for voltage sources, which were generated by MATLAB. Inputs were taken by including the schematic in Fig. 4.4 into main schematic.

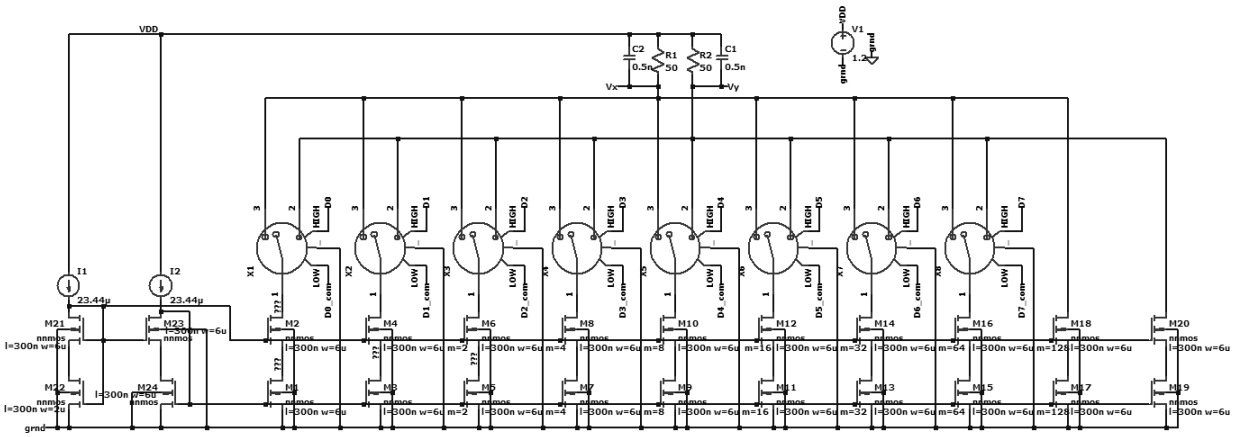

Figure 4.4: Schematic of current steering DAC, with Low voltage Sooch's cascode current mirrors

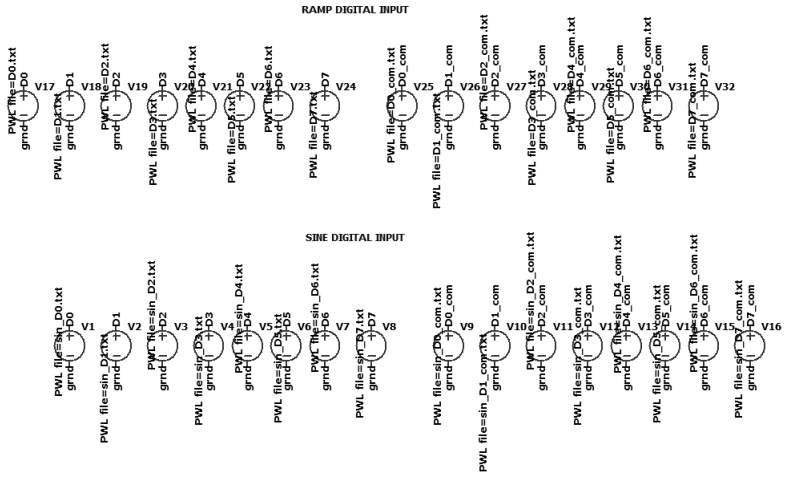

Figure 4.5: Digital inputs

MATLAB Codes for Generating digital bits :

Codes are included in the following Github repository : [Shubham & Harsh (2021)]. The repository also contains the code for **sampling a sine wave** for its reconstruction using DAC.

4.3 Simulation

Current switching DACs

Capacitors are used to smoothing the plots(enough to remove unusual spikes), acting as a low pass filters.

Ramp input :

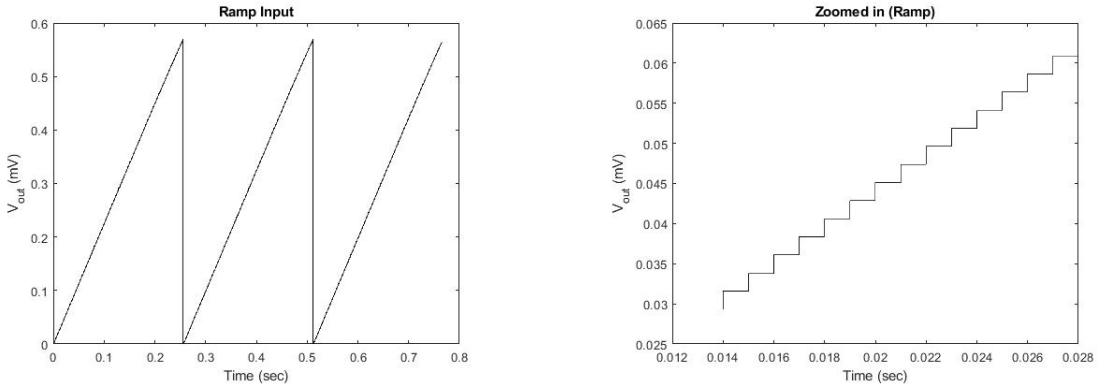

Figure 4.6: Current Switching DAC's

Sinusoidal digital input :

Digital input of sine wave is provided. The frequency of sine wave is $f = 732.42Hz$, sampled at the rate of $f_s = 1MHz$, satisfying nyquist's rate. For FFT analysis 2^{12} samples are taken. Following plots are shown in the figure Fig. 4.7 and Fig. 4.8.

The FFT analysis in the Fig. 4.8 a peak at $f = 732Hz$, but multiple other peaks are observed nearby. This is non-linearity present in the circuit. We expect this non-linearity to vanish if we use differential output.

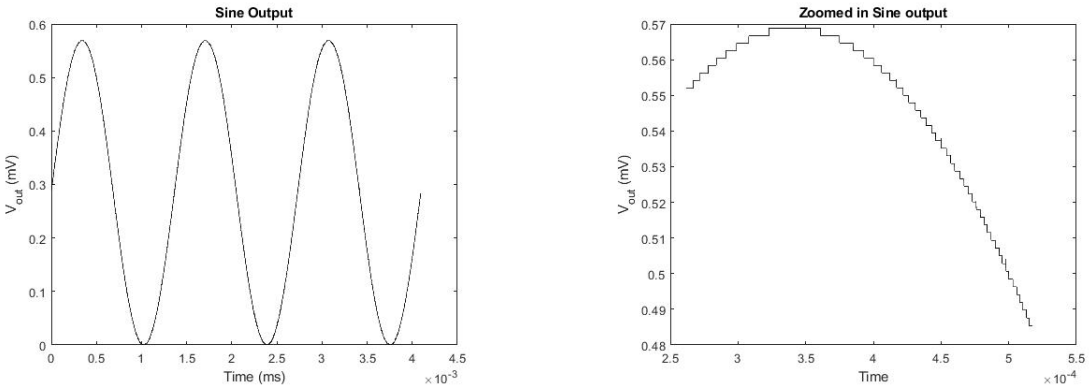

Figure 4.7: Current switching DAC, Sine output

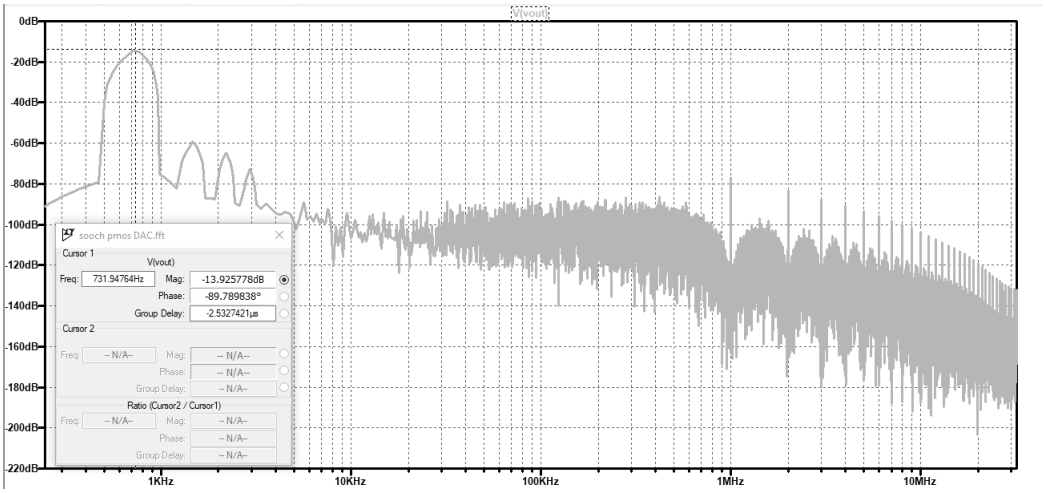

Figure 4.8: Sine output FFT Analysis, Zoomed In

Current steering DACs

Capacitors are used to smoothing the plots(enough to remove unusual spikes), acting as a low pass filters.

Ramp input :

Observing carefully, we find that the output swing is not exactly $600mV$ for Simple Cascode Current mirror DAC (Fig. 4.9), whereas it is $\simeq 600mV$ for Low voltage Sooch's Cascode DAC (Fig. 4.10). Also the step-size in former is less accurate than latter. The reason is the accuracy, we can conclude that Low Voltage Sooch's Cascode accurately copies current.

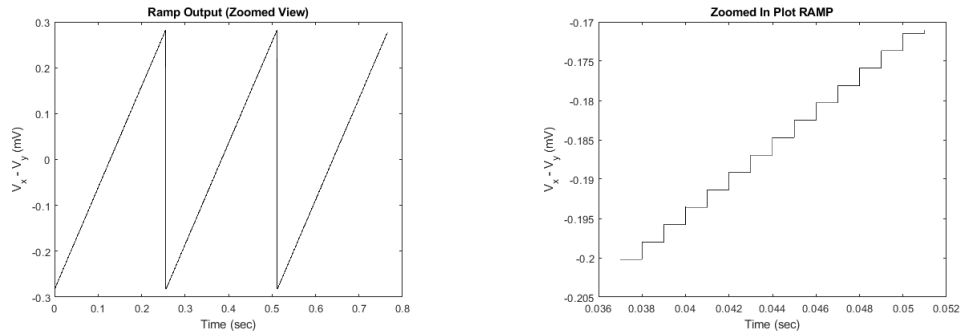

Figure 4.9: Simple Cascode Current mirror DAC

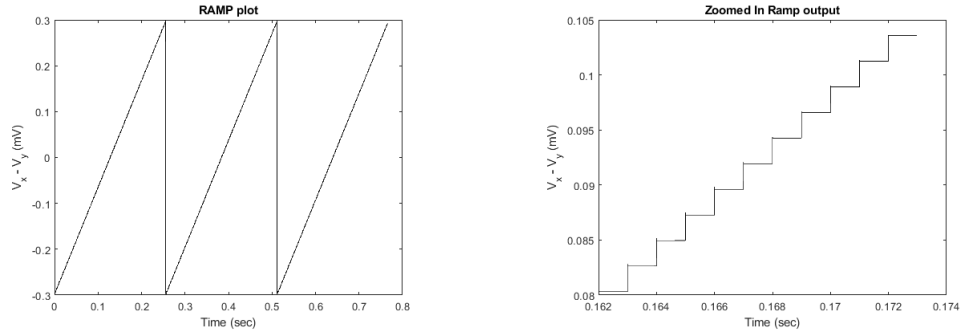

Figure 4.10: Low Voltage Sooch's Cascode Current mirror DAC

Sinusoidal digital input : Digital input of sine wave is provided. The frequency of sine wave is $f = 732.42Hz$, sampled at the rate of $f_s = 1MHz$, satisfying nyquist's rate. For FFT analysis 2^{12} samples are taken. Following are the plots Fig. 4.11 and Fig. 4.12 :

From the FFT analysis we clearly get the $732Hz$ peak which is the frequency of sine wave, .i.e we successfully recovered the sampled wave. A similar FFT plot is observed for the Low voltage sooch's cascode DAC. Another point to obeserve is that, we have a single peak, hence more linearity than current switching DAC.

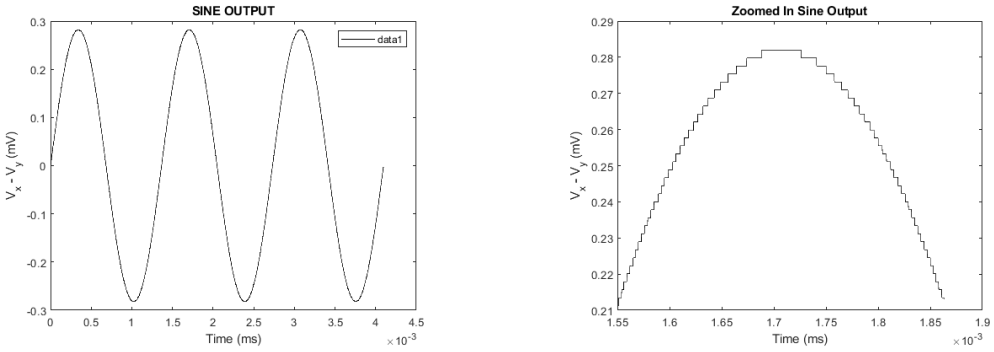

Figure 4.11: Simple Cascode Current mirror DAC, Sine output

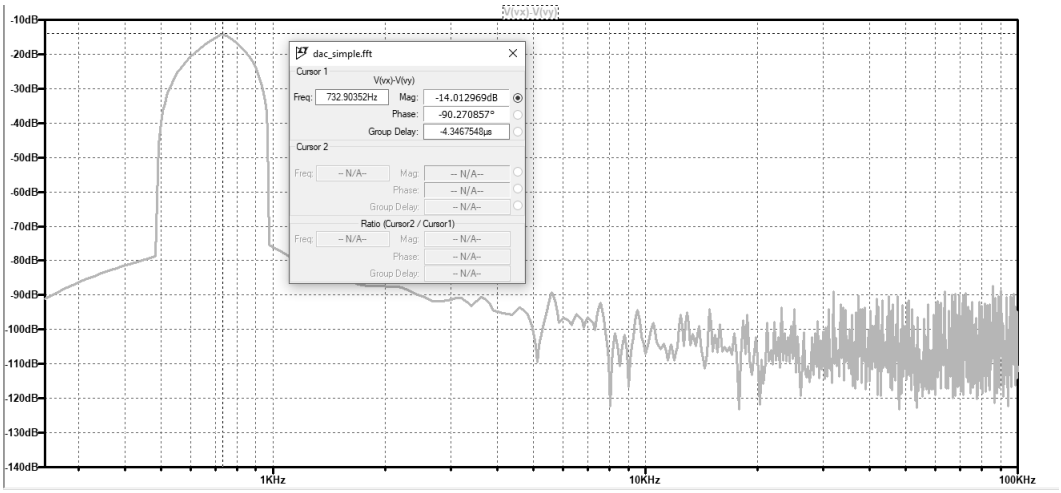

Figure 4.12: Sine output FFT Analysis, Zoomed In

Chapter 5

Observations and Conclusion

We present our observations in the following points :

- Sooch's cascode current mirror or Low voltage Sooch's cascode current mirror has higher accuracy of mirroring currents than simple cascode current mirror. So, we can observe accurate swings and step size as desired.
- Current Steering DAC is practically more feasible than current switching due to several reasons [Razavi (2018)] :
    1. **Transients during charging and discharging of capacitors in the current source :** We can observe that without using low pass filter in output, there are significant number of spikes in current switching than current steering(no spikes in our simulation) shown in Fig. 5.1. This is because when switch is off, the capacitor discharges through the current source, when again switch is turned on, the capacitor momentarily draws significant amount of current to charge.

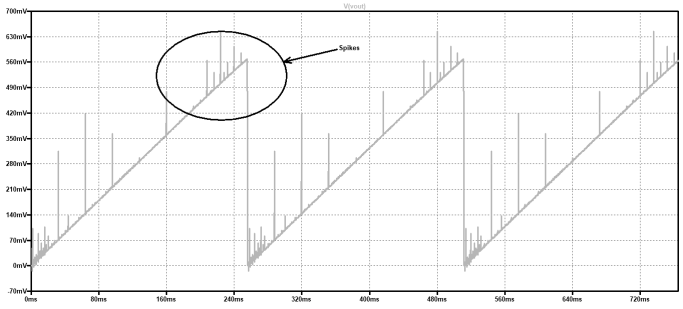

Figure 5.1: Spikes in Current switching DAC

2. **Non-linearity** : In the FFT plot of current switching DAC (Fig. 4.8), we observed multiple peaks, this is due to non-linearity present in circuit. One way to remove other harmonics is to use differential output and get linearity. The same is reflected in FFT plot of current steering DAC (Fig. 4.12).

5.1 Scope of future work :

- Analytical verification of qualitative results obtained.
- Implementing the current steering circuits and switches using MOS transistors.
- Implementing the complex architectures to prevent glitches and errors.
- Implementing the bandgap reference circuits for golden current source.

Bibliography

Razavi, B. (2018), 'The current-steering dac [a circuit for all seasons]', *IEEE Solid-State Circuits Magazine* **10**(1), 11–15.

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Sooch, N. S. (1985), 'Mos cascode current mirror'. US Patent 4,550,284.