BATCH- BTECH SEM 3

SEC. – A and B

COA (CS1134) LAB

Assignment set -3

1. Develop a VHDL model to design a four bit Parallel in parallel out register using D flip flop components. Use an enable and reset input pin to enable and reset the registers.
2. Develop a VHDL model to design a four bit Serial in Serial out register using D flip flop components. Use an enable and reset input pin to enable and reset the registers.
3. Develop a VHDL model to design a four bit Parallel/Serial in Serial out register using D flip flop components. Use an enable and reset input pin to enable and reset the registers. Use a mode input pin to decide whether the input mode is serial or parallel.
4. Develop a VHDL model to design a four bit ripple counter using D flip flop components. Use an enable and reset input pin to enable and reset the counter.