

BATCH- BTECH SEM 3

SEC. – A and B

## COA (CS1134) LAB

### Assignment set -2

Q1. Design a VHDL model for a hardwired 4-Bit comparator using dataflow architecture.

Q2. Design a VHDL model for a 3 to 8 Decoder (with an enable) using Dataflow Architecture. Thereby Design a VHDL model for a 4 to 16 Decoder using 3 to 8 decoders designed earlier using Structural Architecture.

Q3. Design a VHDL Model for an Octal to Binary Encoder with 8 input Bits and three output bits. Each input Bit represents one Octal number.

Q4. Design a VHDL model for 8-1 and 2-1 multiplexer. Using these models develop a VHDL model for 16 -1 multiplexer (Use structural architecture).