Problem Sheet for Practice

Note: This problem sheet is for your practice. You don't have to submit it for grading. You are strongly advised to solve it for your own benefit. Try to solve it individually first. However, if you are unable to solve some problem, don't hesitate to take help of your friends. Group study goes a long way towards learning. I expect you NOT to look at lecture slides BEFORE attempting ANY question.

Q1. Draw the truth tables for following functions: (Note: ' represents NOT)

(a) ABC+ AB'C' +A'BC'
(b) ABCD+ A'B'C'D'

Q2. Draw the Karnaugh Map for the following functions and minimize the functions, if possible.

(a) ABC+ AB'C' +A'B'C'+A'BC
(b) AB+BC+A'B

Q3. Prove or disprove the following (with or without truth tables)

(a) A.(B+C)= A.B+A.C

(b) A+AB = A

(c) A+A'B = A+B

(d) (A+B)' = A'.B'

(e) (A.B)' = A+B

Q.4 Consider the following program segments: (Memory addresses are given on left)

```
    Main
      {…….
1000      Call  B
1001      Call  C
1002      …….
      }
Subroutine B
    {……..
2000    Call  C
2001    Return
    }
Subroutine  C
  { …….
3000  Return
}
```

Show the contents of stack after each call and return.

Q. 5: Consider a single bus organization of CPU (only one component can write on the common data bus in any cycle). Write the signals in each cycles for the following instructions (starting from the instruction fetch till End signal).

(a) I1: ADD [A], [B], [1000] ;Add contents of memory location pointed by Register B with Contents of location 1000 and store the result in memory location pointed by register A.

(b) I2: BRA [A] ; Jump to the location pointed by register A.

Q. 6. Let us assume that the CPU has only these two instructions and CPU uses hardwired control. Draw the Circuits for the Signals (i) End (ii) PC_in (iii) PC_out (iv) MAR_in (v) MDR_out.

Q. 7. Implement 2-input EX-OR gate using (a)Only NOR gates (b) Only NAND Gates

Q. 8. Represent following numbers using IEEE representation

(a) 125.625 in Single Precision.

(b) -0.03125 in Double Precision

Hint: Remember Excess Notation

Q. 9. Multiply -34 by -13 using Booth's algorithm (in Binary)

Q. 10. Divide 347 by 13 using (a) Restoring Division (b) Non-restoring division

Q. 11. Which statements are True for RISC architectures:

(i) Primary goal is to speedup individual instruction
(ii) Small Code Sizes
(iii) Multiple-clock instructions
(iv) "LOAD" and "STORE" are **independent instructions**
(v) Easy to apply pipelining.

Q.12. What the Conjuctive Normal Form and Disjunctive Normal form of a Function? What are minterm and maxterm in a function

Q. 13. Write all possible Boolean functions with two Inputs "a" and "b".

Q. 14. What are the advantages and disadvantages of Single Bus, Two Bus and Three Bus CPU organizations.

Q 15. Convert $(12345)_{10}$ to Base 14 (Symbols 0-9, A,B,C,D).