BATCH- BTECH SEM 3

SEC. – A and B

COA (CS1134) LAB

Assignment set -1 (extended)

Q1. Design a VHDL model using dataflow architecture for half adder and full adder .

Q2. Design a VHDL Model of a full adder using half adder components .

Q3. Design a VHDL model for a four bit full adder using full adder components .

Q4. Design a VHDL Model for a four bit adder subtractor using :-

- Use 2's compliment subtraction.
- Use a control bit to decide addition/Subtraction.
- Make sure to take care of the carry out in case of addition/subtraction.

Q5. Design a VHDL model for a 4 bit Carry Lookahead Adder using Full adder components. Generate all the carries in parallel except the final one.