MAMBO: Dynamic Binary Modification on RISC-V

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MAMBO
=
First optimised DBM framework for RISC-V

What is DBM?

(Also, DBI and DBT)

Valgrind

QEMU

(And MAMBO)

What is DBM?

Dynamic – Working at runtime

Binary – Natively compiled user-space code

Modification – Alteration of applications

+

Instrumentation – Inserting additional functionality

Translation – Translating one instruction set into another

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DBM Use Cases

DBM Use Cases

Program analysis

Callgrind (Valgrind)

Memory error detection

Memcheck (Valgrind), Dr. Memory (DynamoRIO), Memcheck (MAMBO)

Dynamic binary translation

QEMU, Apple Rosetta, TANGO

Why MAMBO?

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Why MAMBO?

Optimized for RISC-V 64-bit, ARM 32-bit & ARM 64-bit
- Low overhead
- **Only available DBM optimized for RISC-V**

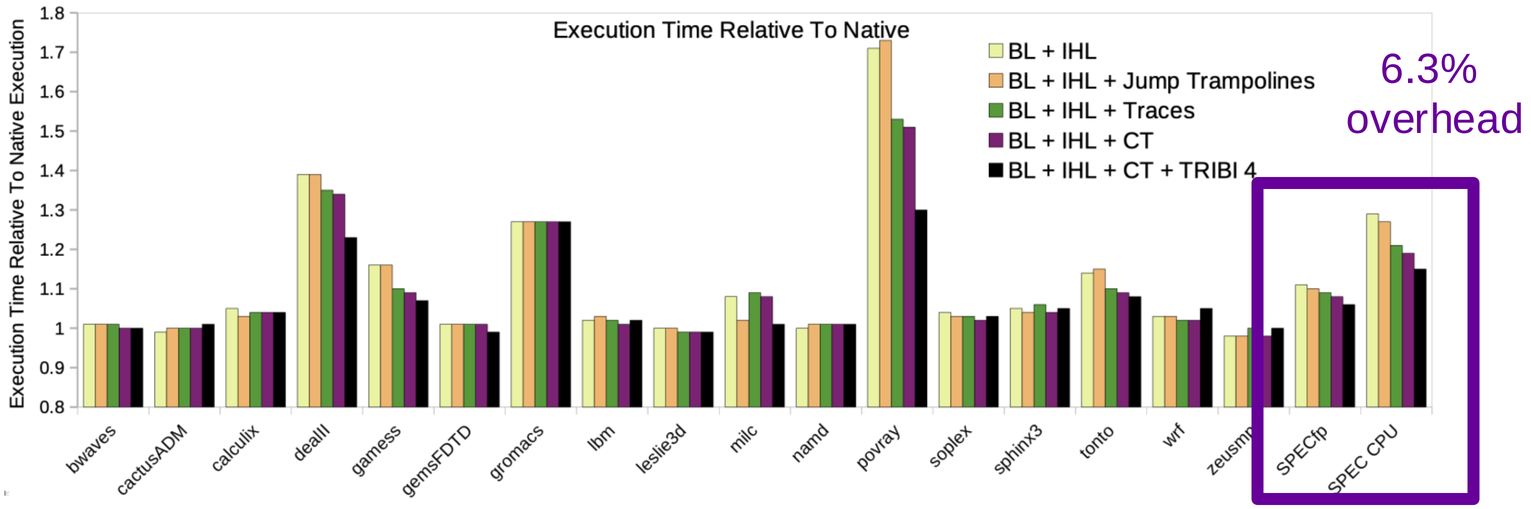
Low complexity
- Relatively small codebase (~20k LoC)

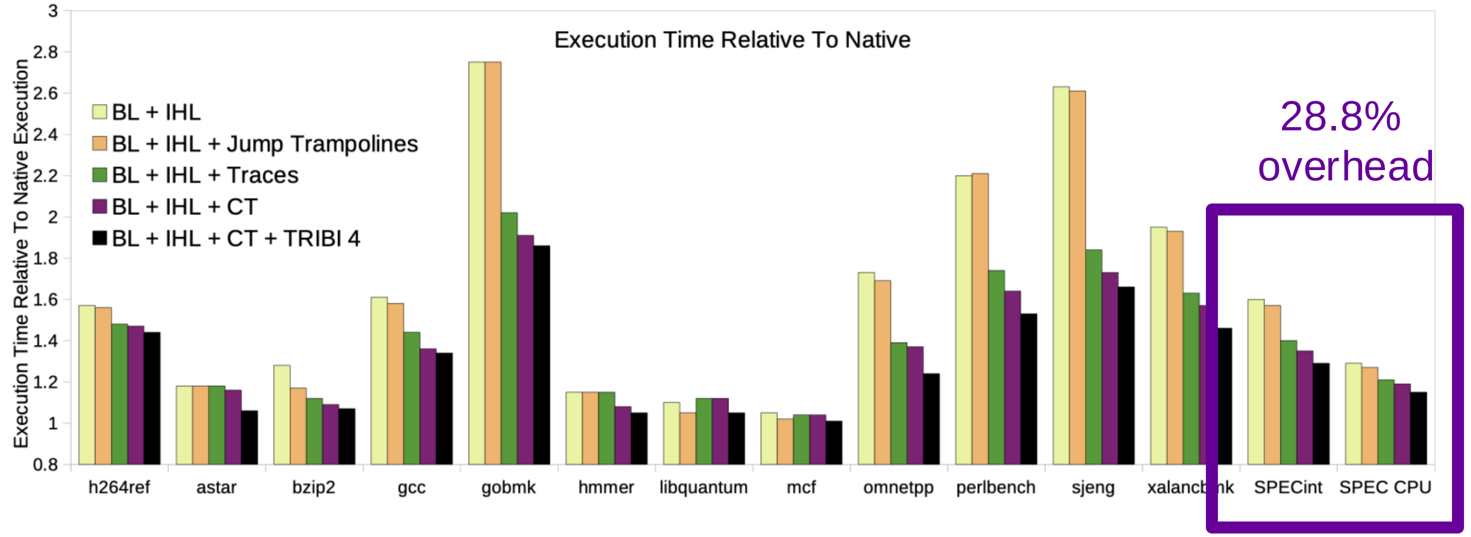
Simple plugin API
- Architecture agnostic helper functions for portable plugins

Not a toy!

Why MAMBO on RISC-V?

Why MAMBO on RISC-V?



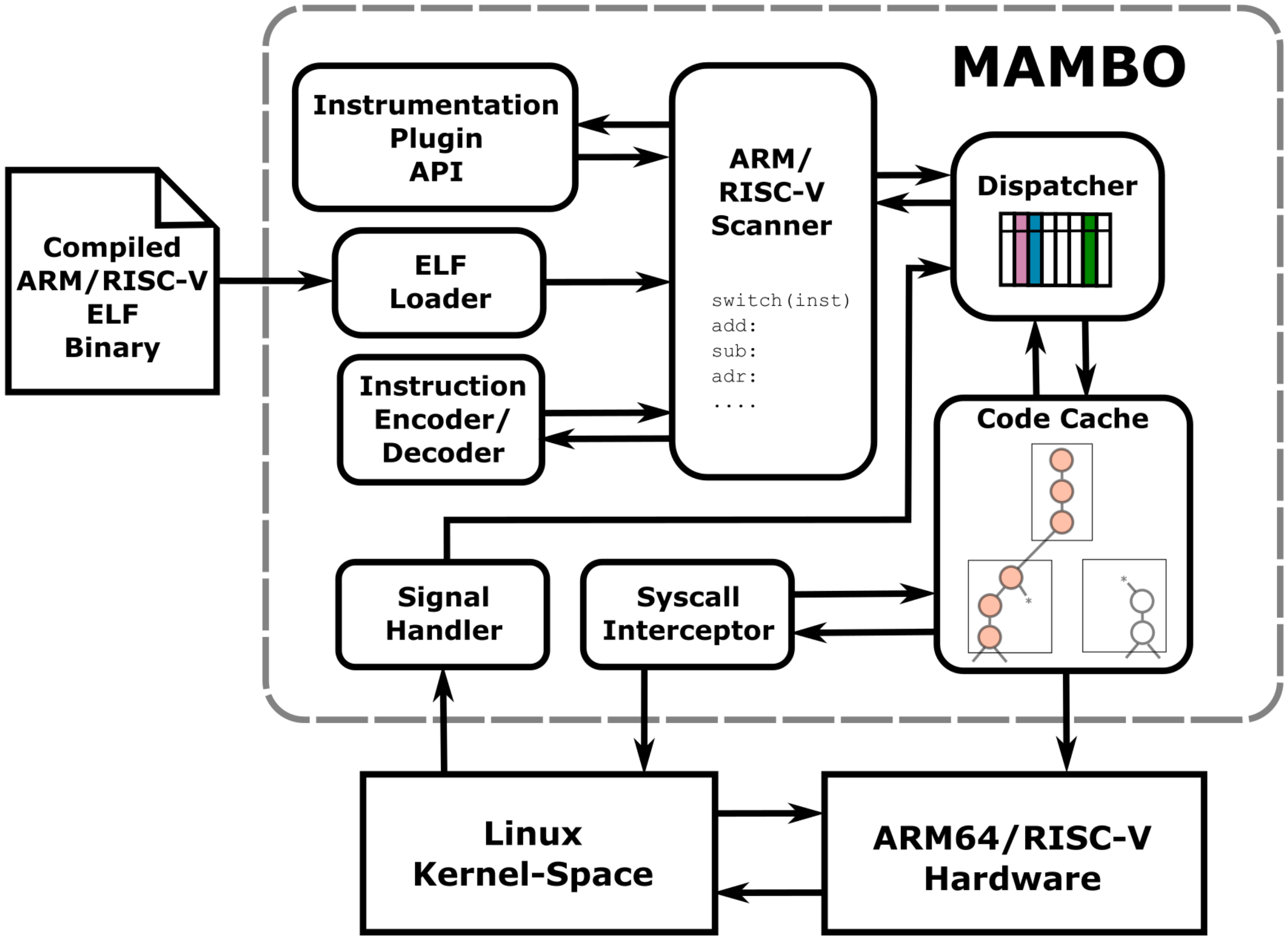


Slowdown relative to native execution for SPEC CPU2006 – RISC-V 64GC.

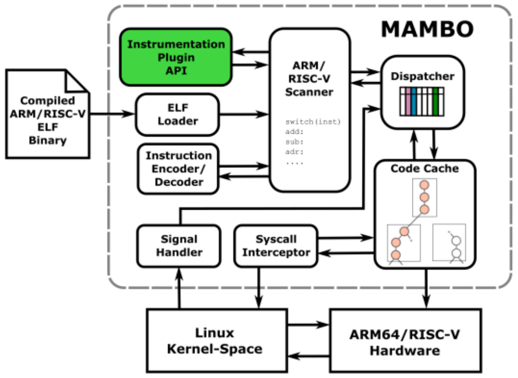
Kressel et al. Evaluating the Impact of Optimizations for Dynamic Binary Modification on 64-bit RISC-V.

MAMBO Architecture

MAMBO Architecture



Introduction to MAMBO plugin API



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Example Use Cases

Example Use Cases

Code analysis

Building CFG

Code generation

Insertion of new functionality

Code modification

Reimplementation of library functions

Code instrumentation

Performance counters and metrics

Runtime event handling

Tracking thread creation/destruction

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Event Driven Programming Model

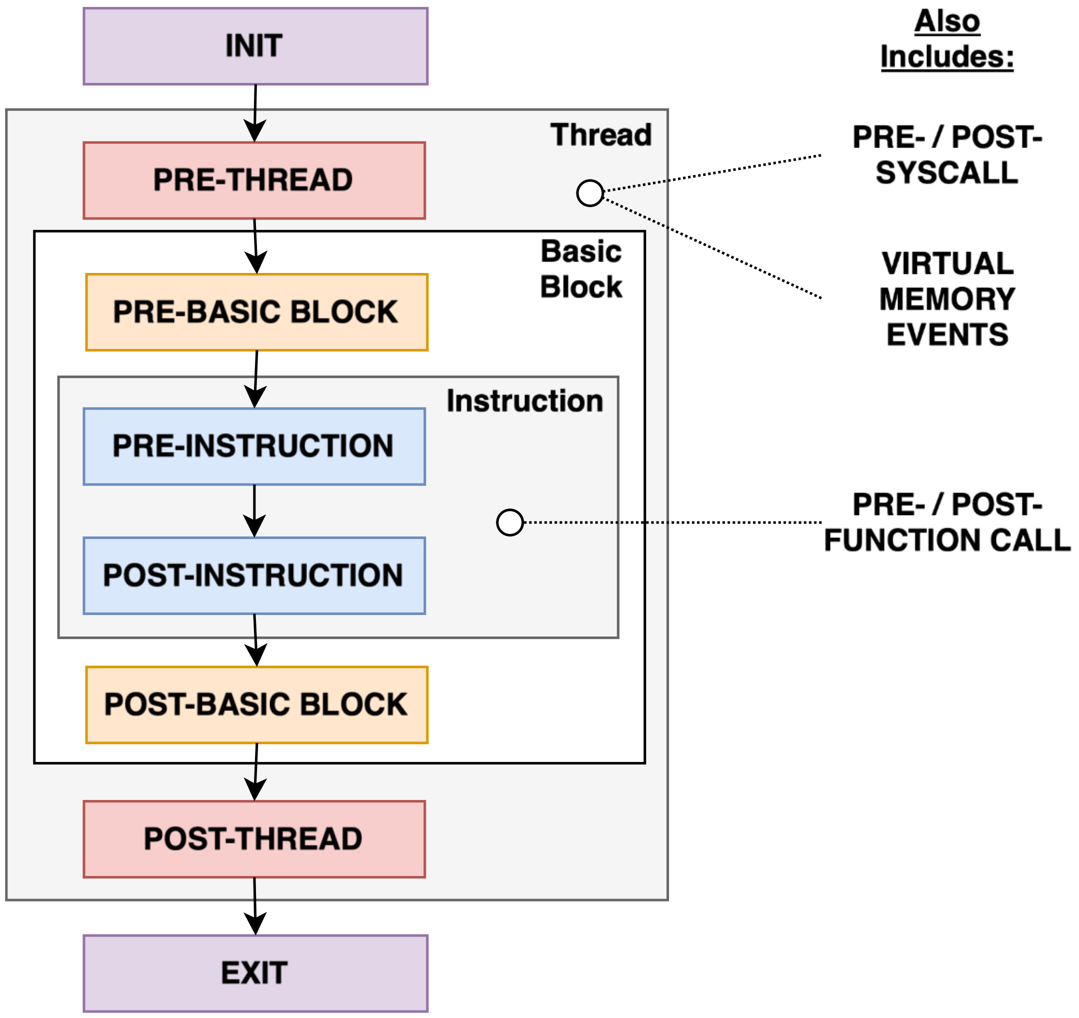
Event Driven Programming Model

User defined functions are registered as callbacks

MAMBO executes callbacks when the event is encountered

Fine-grained (e.g., per-instruction), medium-grained (e.g., per-basic block) and coarse-grained (e.g., per-thread) instrumentation

Event Driven Programming Model



MAMBO API

MAMBO API

Callback registering functions

Code analysis

Instrumentation functions

Various helper functions

Both architecture dependent and independent functions

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Lessons Learned from RISC-V Port

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Lessons Learned From RISC-V Port

Limited range of direct branches

Restrictions placed on atomic Load Reserved (LR) and Store Conditional (SC)

Thread pointer as a general-purpose register (x4)

MAMBO Roadmap

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MAMBO Roadmap

Foster an open-source community
- Collaborations and contributions welcome

Improve Documentation

More tools
- Data race detector

Keep up with RISC-V (and ARM)

Current research projects
- Cybersecurity
- Binary lifting

CODE OPEN SOURCE ON GITHUB

BEEHIVE-LAB / MAMBO

(APACHE 2.0 LICENSE)

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Thanks!

UK Research and Innovation

ROYAL ACADEMY OF ENGINEERING

THE ROYAL SOCIETY

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Engineering and Physical Sciences Research Council

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Hardware Donations

SiFive

Deep Computing