

# Digitizing the Schumann Electronics PLL Analog Harmonizer



*Isaiah Farrell*

A final project dissertation submitted in partial fulfilment  
of the requirements for the degree of

**Master of Science (MSc)**  
*Acoustics and Music Technology*

Acoustics and Audio Group  
Edinburgh College of Art  
University of Edinburgh

August 2023

Supervisor : Dr. Stefan Bilbao



## Abstract

The Schumann Electronics PLL is a hardware guitar effect that utilizes low-level digital clocking techniques and op amp saturation to generate square wave signals at two locked frequencies derived from the fundamental of the input signal. This effect can be implemented digitally through cascading stages of virtual analog modelling and algorithmic approximations of integrated circuits used in the effect. In this work, sections with discrete components are modelled using standard virtual analog modelling techniques. Integrated circuits, not including operational amplifiers, are analyzed and approximated with simplified algorithms. Techniques are outlined for approximating phase-locked loops, decade counters, and Schmitt triggers, allowing for the simulation of the effect. The resultant algorithm has been implemented in MATLAB and behaves subjectively similar to the original hardware, with satisfactory frequency locking behavior and signal qualities. Areas for further improvement arise in the VCO stage of the PLL IC and artifacts from aliasing affecting the output and sensitivity of VCO, the latter is remedied with oversampling. Further work may address these areas to bring more stability to the device in a VST implementation.



# **Declaration**

I do hereby declare that this dissertation was composed by myself and that the work described within is my own, except where explicitly stated otherwise.

Isaiah Farrell  
August 21, 2023



# Acknowledgements

Firstly I would like to thank Professor Stefan Bilbao for his guidance throughout the development of this project. I would also like to acknowledge the guitar pedal building communities and forums on the internet, whose open discussion and pursuit of knowledge have helped in this project as well as contributing to my appreciation of effects building, both in the hardware and digital domains. Finally, I would like to thank the academic staff and fellow AMT and Sound Design students for a rewarding year of study.



# Contents

<b>Abstract</b>	i
<b>Declaration</b>	iii
<b>Acknowledgements</b>	v
<b>Contents</b>	vii
<b>List of figures</b>	ix
<b>List of tables</b>	xi
<b>1 Introduction</b>	1
1.1 General background . . . . .	1
1.2 History of the PLL . . . . .	2
1.3 Sounds of the PLL . . . . .	2
1.4 Interface of the PLL . . . . .	3
1.5 Virtual Analog and Digital Logic Methods . . . . .	4
1.6 Aims and Implementation Challenges . . . . .	5
1.7 Results . . . . .	5
<b>2 Circuit Topology and Digital Implementation</b>	7
2.1 Overview of the Schumann PLL Circuit . . . . .	7
2.1.1 Filtering and Analog Saturation . . . . .	8
2.1.2 Digital System . . . . .	9
2.2 Methods for linear virtual analog modelling . . . . .	12
2.3 Input Filtering . . . . .	14
2.4 Saturation and Schmitt Trigger . . . . .	18
2.5 Phase-Locked Loop . . . . .	23
2.5.1 The Phase Frequency Detector . . . . .	24
2.5.2 PLL Loop Filter . . . . .	26
2.5.3 The VCO . . . . .	28
2.6 Decade Counter . . . . .	29
2.7 Output Volume and Filtering . . . . .	31
2.7.1 Wave Shape Filter . . . . .	33

<b>3 Results and Analysis</b>	<b>35</b>
3.1 Analog Filtering and Saturation Behavior . . . . .	35
3.2 Phase and Frequency Locking Behavior . . . . .	37
3.2.1 Loop Filter Control Voltage and PFD Input Analysis . . . . .	39
3.3 Subjective Analysis . . . . .	41
<b>4 Conclusions</b>	<b>43</b>
4.1 Future Work and Improvements . . . . .	43
<b>A Hardware Implementation of the Schumann PLL</b>	<b>45</b>
A.1 Power Section . . . . .	45
A.2 PCB Design and Assembly . . . . .	45
<b>B Component Values and Full Schematics</b>	<b>47</b>
B.1 Analog Input Stage . . . . .	47
B.2 Digital and Output Stage . . . . .	49
B.3 Power Stage . . . . .	51
<b>C Final Project Proposal</b>	<b>53</b>
C.1 Background . . . . .	53
C.2 Project Aims . . . . .	53
C.3 Proposed Methodology . . . . .	54
C.3.1 Integrated Circuits . . . . .	54
C.3.2 Circuit Topology . . . . .	55
C.3.3 Real-time Modelling . . . . .	56
C.4 Timeline . . . . .	56
C.4.1 Milestones . . . . .	56
C.4.2 Gantt Chart . . . . .	57
<b>Bibliography</b>	<b>57</b>

# List of Figures

1.1	Physical Schumann PLL effect interface [1]	4
2.1	Block diagram of the effect signal path	8
2.2	Simplified circuit diagram of the analog input processing [2]	9
2.3	Basic PLL functions and configuration of a 4046 PLL [3]	10
2.4	Simplified Circuit diagram of the digital processing [2]	11
2.5	Two-stage analog input filtering and amplification	14
2.6	Output from the first filter stage	17
2.7	Output from second filter stage (input from first stage)	17
2.8	Frequency warping from trapezoid rule in the first preamp stage, 10kHz to 40kHz bounds, 192kHz sample rate. Code implementation displayed as solid lines, analytical solution as dashed lines	18
2.9	Frequency warping from trapezoid rule in the second preamp stage, 10kHz to 40kHz bounds, 192kHz sample rate. Code implementation displayed as solid line, analytical solution as dashed line	18
2.10	Open loop op amp saturation stage with offset control	19
2.11	Open loop op amp saturation plots at trigger extremes and center	20
2.12	Open loop op amp saturation plot in non-oscillatory offset state	20
2.13	Behavior of a Schmitt Trigger inverter with a noisy input signal [4]	21
2.14	Schmitt Trigger hysteresis curve [5]	21
2.15	Schmitt Trigger threshold voltage plot [5]	22
2.16	Schmitt Trigger output with op amp clipping and sinusoidal input.	23
2.17	Phase-Locked Loop system block diagram	24
2.18	D Flip-Flop logic diagram	24
2.19	Output behavior of the PFD [6]	25
2.20	PLL external loop filter schematic	27
2.21	PLL loop filter plot, switched capacitors	28
2.22	4046 VCO Functional Block Diagram [6]	29
2.23	Timing diagram for CD4017 [7]	30
2.24	Configuration of decade counters in the Schumann PLL [2]	30
2.25	Schumann PLL output stage schematic	32
2.26	Plot of output filter transfer function at variable resistances	33
3.1	Square wave saturation time domain analysis	36
3.2	Square wave saturation harmonic analysis	37
3.3	PLL Frequency division behavior, set to lower perfect 5 from input frequency, marked by dotted line	37

3.4	PLL Frequency division behavior, set to raise 2 octaves from input frequency, marked by dotted line . . . . .	38
3.5	Loop Filter general sinusoidal input behavior . . . . .	39
3.6	Loop Filter initial state pulses (Sinusoidal Input) . . . . .	40
3.7	Loop Filter locked state pulses (Sinusoidal Input) . . . . .	40
3.8	PLL Input Phase Locking analysis . . . . .	40
A.1	Interface of the Schumann PLL clone . . . . .	46
A.2	PCB and potentiometer wiring of the Schumann PLL Clone . . . . .	46
B.1	Analog input stage schematic [2] . . . . .	47
B.2	Digital stage and analog output schematic [2] . . . . .	50
B.3	Power stage schematic [2] . . . . .	51
C.1	PLL Schematic by digi2t and jonasx26 [2] . . . . .	54

# List of Tables

2.1	Behavioral truth table for the PLL PFD . . . . .	25
B.1	Component values for the analog input stage B.1 . . . . .	48
B.2	Component values for the digital and output stages B.2 . . . . .	49
B.3	Component values for the power stage B.3 . . . . .	51



# Chapter 1

## Introduction

### 1.1 General background

Since the innovation of the electric guitar, guitarists have curated their instruments and amplifiers to define their characteristic sound. This concept extends further into history and throughout other instruments, but in the past century guitarists have shown to be the leading curators of a tone that defines them and their musical style. This endeavor has facilitated a large industry and community surrounding effects for guitar, beginning with accidental saturation of vacuum tubes in early amplifiers and rapidly growing in the 1960s with off-board circuits that sit in the signal path between the guitar and the amplifier. These circuits are commonly referred to as effects pedals or "stomp boxes". This adoption of effects pedals has created an ecosystem of electronics engineers with a desire for audio experimentation and guitarists looking for a unique tone to make them stand out [8].

The builders of these pedals come from varied backgrounds, and hobbyists have long been a part of the landscape [9]. This has given way to the label of "boutique pedals" or pedals that are usually made in (very) small quantities, usually by a single pedal builder or small team. Often these boutique operations begin with guitarists altering existing mass-produced circuits for their own personal use, eventually familiarizing themselves to the point of producing new circuits. Small effects makers have carved out a place of importance in the effects community, developing unique circuits that many larger manufacturers would not take risks on.

These unique effects have varied as one-off and small run effects would become popular and adopted into the mass market. Fuzz is one of the earliest examples of an effect that did not seek to emulate a "natural" sound, like earlier reverb effects. Fuzz effects use feedback to saturate transistors, creating a harsh, squared off waveform. These effects were developed after guitarists were seeking distorted tones because of sounds from damaged amp speakers and broken transformers making it onto recordings and sought after. This trend grew through the rock era and gave way to more

sophisticated circuits [8].

## 1.2 History of the PLL

The Schumann PLL [1], standing for Phase-locked loop - the integrated circuit that drives the pedals functionality, is a boutique effect that builds upon the functionality of fuzz pedals, bringing the effect into an experimental setting and using unconventional methods of saturation. The pedal is an analog guitar harmonizer, using a guitar input to generate three square waves, one from a saturated input signal, a harmonic and a sub-harmonic square wave locked to the frequency of the input signal.

These pedals were developed and built by John Schumann in New York City and sold for a short time in the early to mid 2000s [10]. They were rumored on forums to be used by Radiohead's bassist in the mid-2000s [11], and have spawned a number of replicas and inspired pedals in recent years, creating a cult following of PLL-style effects. Schumann claimed that the effect was in development for two years before it was produced, with guitar tracking taking the longest to develop due to its harmonic-rich input. Schumann further claimed in an interview with Tape-Op Magazine that the effect is purposely difficult to tune for use and meant to be treated as somewhat of an instrument of its own, commenting on his resentment of effect pedal manufacturers limiting the range of controls, saying that those effects are for the "lowest common denominator" [12].

The pedals were slow to make, with a relatively large number of components for a boutique pedal, a complex process for the etched enclosure, and wiring the knobs [12]. Because of this process and short production time, there are not many of these pedals in existence and they currently sell for thousands of dollars on the second-hand market [13]. For this reason, and because these pedals will only grow more scarce, the effort to create a digital model of this effect is worthwhile. The already digital sounding nature of the hardware effect lends itself to the digital domain, and the possibilities for expansion made available from modelling the effect justify the effort.

## 1.3 Sounds of the PLL

The effect is a unique glitchy-sounding fuzz harmonizer that can be tuned to ramp up into the locked tone or waver in and out of its frequency locking. As seen in 1.1, the pedal has sets of controls that work together to tune the sound and behavior of the pedal. It primarily utilizes integrated circuits that are commonly implemented to manipulate clock signals in digital circuits. This style of signal manipulation uses logic circuits that necessitate a one-bit digital input signal, this is derived from the input by clipping the signal into a square wave. The signal is never subject to sophisticated digital processing (i.e. high quality A/D conversion and algorithmic processing), but

utilizes one-bit analog to digital conversion and treatment of digital output as an analog output signal.

The primary signal path of the pedal involves pre-amplification followed by square wave saturation. The saturated signal is then fed into a logic chip that generates a phase-aligned, frequency multiplied copy of the signal. This multiplied signal is then further divided to achieve a sub-harmonic. The saturated input, multiplied, and divided signals are then added together and filtered to create a harsh, harmonically rich tone that sits somewhere between a fuzz and a synthesizer tone. The tracking controls on the pedal allow the user to achieve unique characteristics in the generated tones, such as smoothing the tracking to achieve a portamento-like effect or limiting tracking to induce a vibrato in the generated signals. Even through simple manipulation of the generated frequencies a user can achieve octave-locked lead guitar tones or even complex harmonies. There were even plans to release a sequencer to play the pedal as an instrument, designated by an input marked "arpeggiator" on the side of the original pedals, but no such unit was made available to the public [1].

## 1.4 Interface of the PLL

The interface of the Schumann PLL is significantly more complex than a standard effect pedal. The pedal has ten standard potentiometers, five of which are in a rheostat (variable resistance) configuration, two 1p12t rotary switches, and three DPDT toggles. The controls on the interface can be broken up into five categories, input sensitivity, pitch tracking, harmonic setting, phase, and output controls. Each of these stages have multiple settings that sometimes change behavior based on others in their group.

The first stage of controls is input sensitivity, which consists of the PRE AMP and TRIGGER controls on the pedal (figure 1.1). These settings control how the instrument signal is fed into the digital logic portion of the circuit, with the PRE AMP controlling input amplification and filtering, while TRIGGER controls the duty cycle of the input-derived square wave.

The second stage of controls determine the quality of the pitch tracking in the harmonic generation portion of the pedal. The LOOP TRACK, RESPONSE, and LOOP SPEED controls determine the values of an analog RC filter that smooths control voltage passed to the harmonic VCO (voltage controlled oscillator). These filtering controls interact with the LAG TIME knob that adjusts the internal gain of the VCO.

The third stage of controls are the two primary dials on the interface. These rotary switches set the frequency of the harmonic and sub-harmonic tones locked to the input signal. Internally the switches connect to two digital counters in the unit, MULTIPLIER sets the frequency multiplication interval of the clipped input signal, while DIVIDER sets the frequency division of the output from the frequency multiplied VCO.



Figure 1.1: Physical Schumann PLL effect interface [1]

The fourth stage of the pedal is the simplest, with only two ON-ON toggle switches labeled MULTIPLIER PHASE and DIVIDER PHASE. These switches simply invert the phase of the multiplied and divided synthesized signals.

The fifth and final stage of the interface consists of the five knobs on the right side of the interface, which determine the levels and output filtering of the effect. SQUARE WAVE, MULTIPLIER, and DIVIDER set the gain relationship between the three generated square waves. WAVE SHAPE controls a low pass filter on the units output, and MASTER determines the output level of the pedal. It is important to note that the maximum output of this pedal is set to 11.85V which is significantly higher than most pedals.

## 1.5 Virtual Analog and Digital Logic Methods

The Schumann PLL is marketed as an "analog" guitar effect, however, the circuit uses mixed signal digital analog integrated circuits [2]. These chips integrate digital logic and analog functionality. While the pedal does not delve into modern digital conventions, i.e. Digital Signal Processing, it uses low level digital processes for simple operations such as phase comparison and counting [3] [7].

These simple digital processes are implemented with CMOS integrated circuits, specifically 4000 series ICs developed in the 1970s [14]. Complementary metal-oxide-semiconductor, or CMOS, is a fabrication process that uses p-type and n-type MOSFETs to implement digital logic in integrated circuit designs [4]. This approach allows for low level digital circuits with a high degree of responsiveness. These chips

have a low transition time, usually in the order of tens to hundreds of nanoseconds. When using these circuits in the processing of analog audio signals this suggests that there is not a need for component-level analog modelling of CMOS, since they transition at a substantially higher rates than typically would be captured in audio rate sampling [5], but rather capturing the breadth of their functionality through a digital logic implementation. As such, in this digitization effort these circuits are simply implemented with conditional logic in accordance with their data sheets, with limited consideration for any component-level modelling (with exceptions in the case of external analog filters that the circuits rely on).

## **1.6 Aims and Implementation Challenges**

The following items represent the goals for this project,

- Find the state space representations of the analog portions of the effect, implement with trapezoidal integration
- Derive algorithmic solutions to the digital logic circuits in the effect, implement with logic statements in MATLAB.
- Combine analog and logic blocks into a functional algorithmic digital effect.
- Develop PCB from schematic and build an hardware clone of the guitar pedal.
- Compare pedal and digital implementation subjectively and with Fourier analysis.

The challenges of the effect digitization are as follows,

- Determine what portions of the effect can be modeled with conventional virtual analog approaches and what could accurately be modeled with logic algorithms.
- Accurately developing logic stages that process the virtual analog output accurately to the hardware effect, minimizing the loss of signal character from digitization.
- Dividing the large analog stages into smaller sub-circuits that are easier to calculate the state space matrices of.

## **1.7 Results**

The result of this project has been the successful development of a mixed signal analog and digital circuit in MATLAB, with adequate subjective correlation to the analog hardware. Linear analog circuits were implemented with trapezoidal integration from the state space form. Nonlinear analog saturation (one open loop op amp) was

## **CHAPTER 1. INTRODUCTION**

implemented with a simple square wave saturation algorithm, and subsequent CMOS logic ICs were implemented with standard conditional logic statements in MATLAB.

The full analysis of the behavior of the pedal can be read in 4. Behavior of the phase locking is shown to be adequate and mapped to the behavior of the analog circuit. This behavior extends to control outliers such as vibrato at a low LOOP TRACK setting. These behaviors suggest an accurate model of the effect.

Some issues and opportunities for further work were encountered, primarily the issue of aliasing. Due to the low computational requirements of the effect this can be remedied by oversampling without significant computational cost. Future work may be completed in a real-time C++ implementation of the effect, as well as a more sophisticated model of the VCO, which is currently implemented with a variable frequency sine wave.

# Chapter 2

## Circuit Topology and Digital Implementation

This chapter discusses the approaches to digitizing the circuit from the schematic. General approaches to digital logic design and conventional virtual analog modelling of discrete component circuits are covered, as well as an in-depth analysis and methods for each of the functional stages of the circuit and their implementation in code.

### 2.1 Overview of the Schumann PLL Circuit

The general signal path of the effect circuit is shown in figure 2.1, separated into processes used to achieve the characteristic saturation, frequency multiplication and division in the physical circuit.

The first stage of the circuit consists of analog pre-amplification and filtering, using two op amp stages, one of which is user defined. This output feeds into a saturating op amp with a signal offset control. This control acts as a duty cycle control for the output square wave.

The output from the analog stage is passed through a 1-bit analog to digital converter and into the phase-locked loop portion of the circuit, which houses a phase detector and voltage controlled oscillator, and employs an external low pass filter. This output signal is fed back through into the phase detector after being frequency divided though the multiplier counter. The VCO output is also passed through another counter that is set to the divider frequency as well as the output summation. The three signals are summed and fed through a low-pass output filter, and to the output. As a note, this block diagram neglects any volume controls.

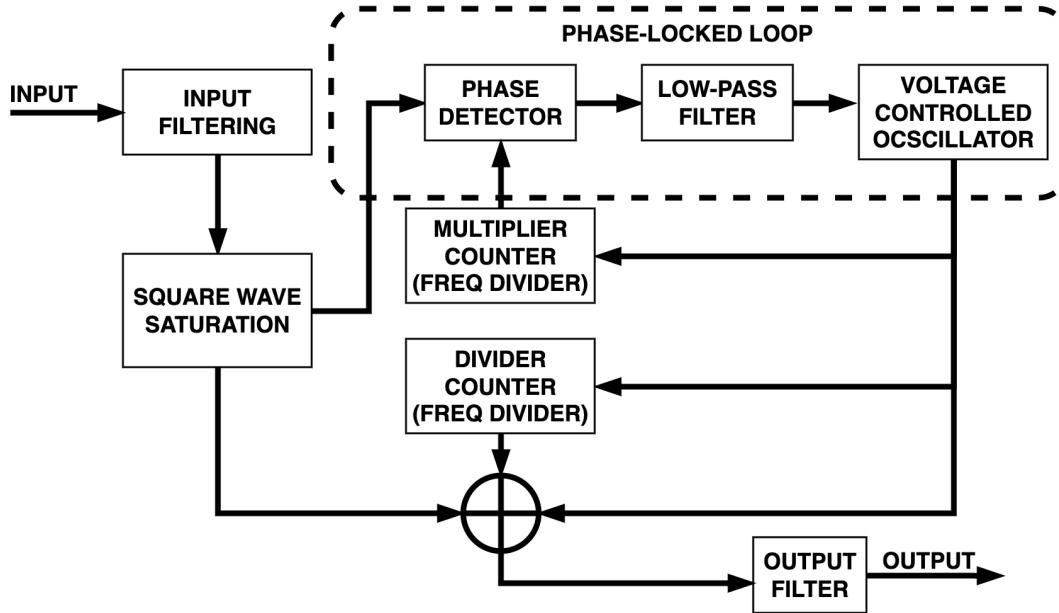


Figure 2.1: Block diagram of the effect signal path

### 2.1.1 Filtering and Analog Saturation

The figure 2.2 displays the analog input circuit in the effect. This circuit can be separated into three stages, the first stage extends from the AC signal input through the output of the first op amp. The second extends from the output of the first op amp through the input to the third op amp, and the third stage includes the input to the third op amp and the power circuit connected to the inverting input of the third op amp.

The first stage of the analog processing begins with a passive RC (resistor and capacitor) band-pass filter. This configuration also has voltage divider behavior (taking note of the two resistors in series from the input to ground). This filtered signal is passed into the non-inverting input of an op amp with an active band-pass filter configuration. This configuration consists of a non-inverting op amp integrator amplifier with an additional polarized capacitor to accentuate high-pass behavior in the filter.

The general purpose of these stages are to significantly amplify the input signal, letting the user bring the low level signal from the guitar pickups, around 200mV to the 10V range. The secondary function of the stage is to filter out the low and high frequencies of the input signal to preserve the fundamental of the guitar tone in the generated square wave. This filtering improves the tracking in the frequency-locked synthesized signals. Finally, the analog saturation stage allows the user to set a DC offset in the signal before it is amplified and hard-clipped, this changes the tonal quality of the output signal. Overall, the circuit conditions the instrument input and outputs

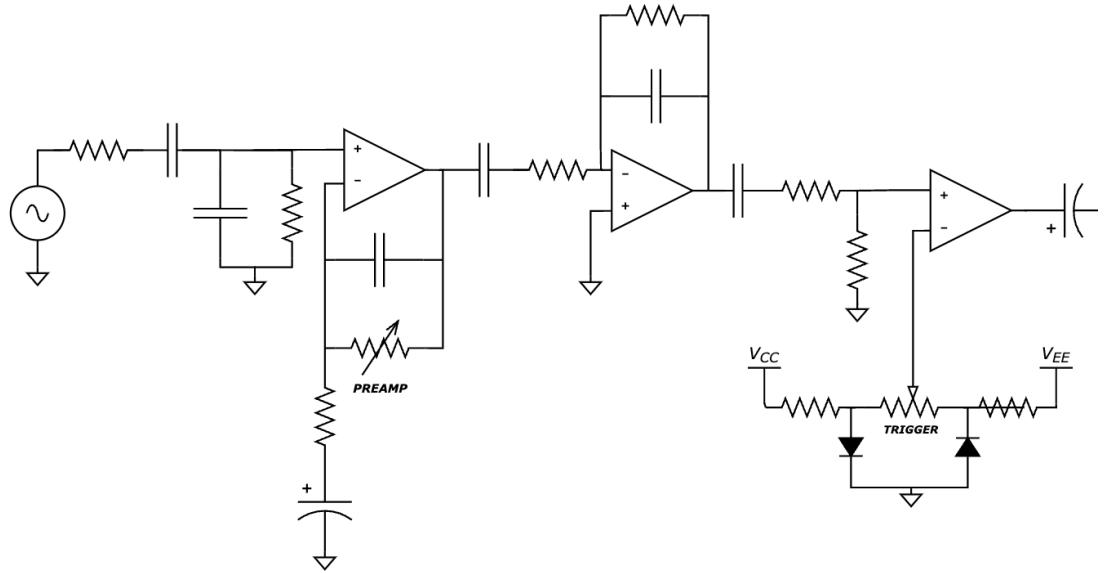


Figure 2.2: Simplified circuit diagram of the analog input processing [2]

a bipolar square wave.

### Simple supplemental filters

The effect circuit also utilizes passive analog circuits outside of the input stage. These two circuits, pictured connected to the PC2 and VCO IN pins of the PLL chip (figure 2.17) and after the output buffer, are both variable RC low-pass filters (figure 2.4). These filters have low-pass functionality, yet preserve feedthrough signal due to the resistance to ground. The filter connected to the PLL filters the control signal sent from the phase detector to the VCO, with the user controlled filter behavior altering the tracking of the PLL output. The second serves as an output filter for the summed signal, and removes the high frequency harshness that can result from digital square waves.

#### 2.1.2 Digital System

The Schumann PLL circuit utilizes 4000 series CMOS logic ICs. These chips allow the pedal to execute low-level digital logic functions in the generation of multiplied frequency signals.

The first of these chips is the 40106 CMOS Hex Schmitt Trigger Inverter [5]. The original pedals use the 74HC14N [15], but this IC is not rated to operate at a 12V supply, so a more stable option with near identical functionality, a higher supply voltage, and most importantly a data sheet with documented functionality at the real supply

voltage, is selected to replace it for analytical reasons. This chip has dual functionality, primarily it converts an analog signal to a digital one, working as a more sophisticated comparator circuit with noise rejection, and switching between 0V and the supply voltage of the IC. Secondarily, it inverts the input signal in the digital domain, this is how the MULTIPLIER PHASE and DIVIDER PHASE controls operate. The repeated use of these inverters ensure the quality of the digital signals throughout the circuit because of their resistance to noise.

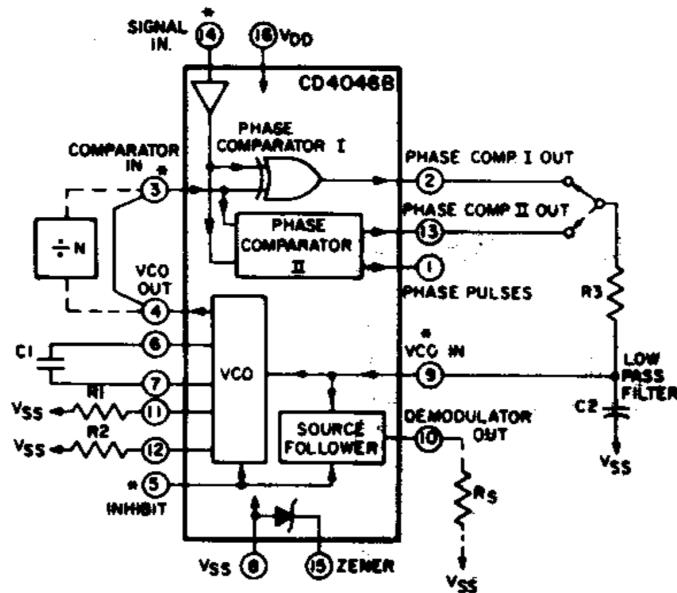


Figure 2.3: Basic PLL functions and configuration of a 4046 PLL [3]

The second integrated circuit designates the primary functionality of the circuit, and also gives it its name. The 4046 CMOS Micropower Phase-Locked Loop [3] is a phase detector and VCO (voltage-controlled oscillator) that locks onto the phase of an input signal. The basic blocks of the IC are shown in 2.17, the primary blocks utilized are the Phase Comparator II, a CMOS digital logic circuit, and the VCO, a mixed signal voltage controlled amplifier that outputs a digital square wave. The two phase comparator blocks differ in their behavior. Phase Comparator I uses an exclusive-OR gate to output pulses based on the leading and lagging edges of the signals, however the signal that is leading or lagging is not differentiated within the circuit output. The Phase Comparator II uses a more complex logic design, discussed in depth in 2.6, that will output a positive pulse with a leading input signal, a low pulse with a lagging input signal, and incorporates a high impedance off state, which will simply prompt the discharge of the loop filter capacitors as the VCO control voltage.

The final digital IC is the 4017 CMOS Counter/Divider [7]. The circuit utilizes two of these chips to adjust the frequency of the synthesized signals. The circuit is a 5-stage

## 2.1. Overview of the Schumann PLL Circuit

Johnson counter with ten decoded outputs [16]. These circuits count the rising edges of the incoming clock signal (this can be any periodic square wave) and iterate through the 10 output pins, outputting a pulse on the pin according to the number of rising edges detected. The counters are reset by sending a pulse into the reset pin. This is done by routing one of the counter outputs into the reset pin. With this configuration the counter will output a single pulse for every n cycles of the input signal. This equates to a frequency divided output signal. The exact configuration of the logic circuit and implementation in code is discussed in detail in 2.7.

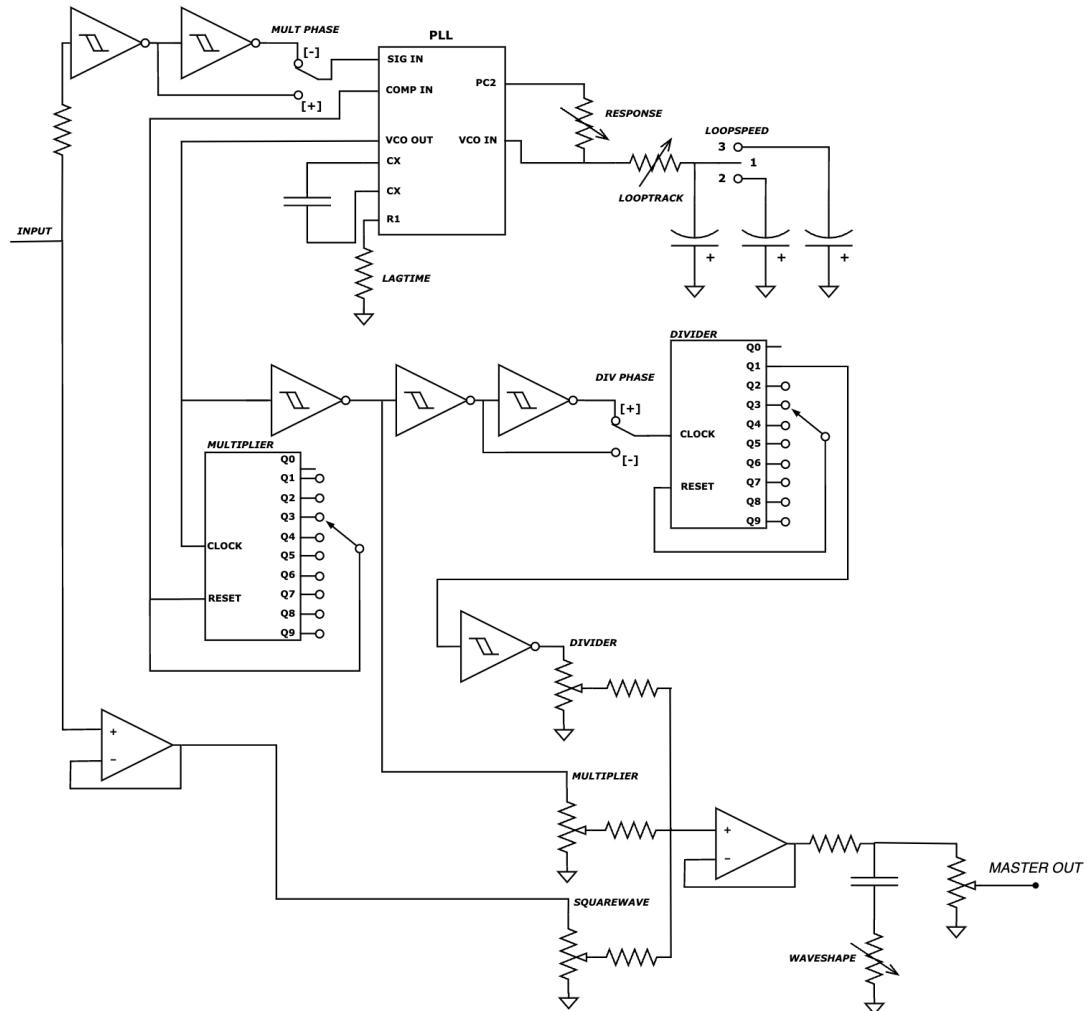


Figure 2.4: Simplified Circuit diagram of the digital processing [2]

## 2.2 Methods for linear virtual analog modelling

Analog circuits are a continuous time system. The representation of these systems digitally requires a method of discrete integration over the input voltages to calculate the output of the system. For circuits without memory these systems can be calculated through simple algebraic equations represented in the circuit. More commonly, circuits will utilize components that store current or voltage, the most utilized of these components are capacitors and inductors. In a digital system this behavior requires a modelling approach with memory, since the system must account for the energy already stored in a component.

State-space modelling is a conventional approach to efficiently model analog circuits. The system is represented using a system of differential equation, with each equation mapped to the voltage differential through an energy storing component (only capacitors in the case of this project), and relating these to the current state of the system. These equations represent the behavior of the circuit in continuous time [17]. The following equation is the most common configuration to represent the state of a non-linear system, which captures the characteristics necessary for the analog portion of the Schumann PLL.

$$\dot{\mathbf{x}}(t) = \mathbf{Ax}(t) + \mathbf{Bu}(t) \quad (2.1)$$

$$\mathbf{y}(t) = \mathbf{Cx}(t) + \mathbf{Du}(t) \quad (2.2)$$

Where  $\mathbf{u}$  is the input vector,  $\mathbf{A}$  is the state matrix,  $\mathbf{x}$  is the state vector,  $\mathbf{B}$  is the input matrix,  $\mathbf{C}$  is the output matrix,  $\mathbf{D}$  is the feedthrough matrix, and  $\mathbf{y}$  is the output matrix. In the specific case of the circuit modelled in the Schumann PLL, the input and output vectors are both one-dimensional. The state matrix  $\mathbf{A}$  is represented by an  $n \times n$  matrix where  $n$  is the number of capacitors present in the system, since there are no inductors in the analyzed circuits. The input and output matrices  $\mathbf{B}$  and  $\mathbf{C}$  are represented by a  $n \times 1$  and  $1 \times n$  matrix, respectively. The state vector  $x$  is an  $n \times 1$  matrix. Finally, the feedthrough matrix  $D$ , input vector  $u$ , and output vector  $y$  are represented by scalar values.

The state vector represents the current state of system, the elements in this vector store the current voltages across capacitors in the circuit, serving as a memory element. The state and input matrices represent the interactions of the components with these stored capacitor voltages and the input voltage. The output matrix designates the composition of the output signal from the current state, and the feedthrough matrix designates any part of the input voltage fed through, or not affected by the energy-storing components in the circuit. The input and output vectors simply represent the

input and output voltages from the circuit.

To implement this state space with code, the continuous time state space solution must be discretized. To find the solution in a discrete time system trapezoid rule will be employed. Integrating over one sample period  $T$ ,

$$\int_{(n-1)T}^{nT} \dot{\mathbf{x}}(t) dt = \int_{(n-1)T}^{nT} \mathbf{Ax}(t) + \mathbf{Bu}(t) dt \quad (2.3)$$

The right hand integral can be approximated with the trapezoid rule, which approximates  $\dot{\mathbf{x}}(t)$  as a straight line between  $n - 1$  and  $n$  [18]. Substituting  $x^n = x(nT)$  results in the following equation.

$$x^n - x^{n-1} \approx \frac{T}{2}(\mathbf{A}(x^n + x^{n-1}) + \mathbf{B}(u^n + u^{n-1})) \quad (2.4)$$

$$(\mathbf{I} - \mathbf{A}k/2)x^n = (\mathbf{I} + \mathbf{A}k/2)x^{n-1} + \frac{\mathbf{B}k}{2}(u^n + u^{n-1}) \quad (2.5)$$

$$x^n = (\mathbf{I} - \mathbf{A}k/2)^{-1}((\mathbf{I} + \mathbf{A}k/2)x^{n-1} + \frac{\mathbf{B}k}{2}(u^n + u^{n-1})) \quad (2.6)$$

Where  $k$  is equivalent to the sampling frequency  $\frac{1}{T}$  and  $\mathbf{I}$  is the identity matrix of equivalent dimension to  $\mathbf{A}$ . Equation 2.6 can be used at each sample to update the state vector  $\mathbf{x}$  to be used in the output equation 2.2. The following Algorithm 1 demonstrates an implementation of this method in code.

---

**Algorithm 1** Linear State Space Simulation
 

---

```

k = 1/SampleRate
N = Number of Samples in u
AkMinverse = (I - A * k/2)
AkP = (I + A * k/2)
Bk = (B * k/2)
x = 0
for n = 1:N do
    x = AkMinverse * (AkP * x + (Bk) * (u(n) + u(n - 1)))
    y(n) = C * x + D * u(n)
end for
    
```

---

In the design of the algorithm there must be considerations made for user defined parameters, and optimization of the code around those limitations. For example, if the state matrix  $\mathbf{A}$  contains user defined values, it must be recalculated in a real time simulation. This recalculation may be conducted at a slower control rate, or in a secondary function that cycles when values are changed by a user. Optimizations that can be made in the exception of these include the pre-computation of  $(\mathbf{I} - \mathbf{A}k/2) * (\mathbf{I} + \mathbf{A}k/2)$  and  $(\mathbf{I} - \mathbf{A}k/2) * (\frac{\mathbf{B}k}{2})$  before the primary function loop.

## 2.3 Input Filtering

The first section of the circuit is the analog input filter and preamp. This portion of the circuit is comprised of two op amp stages performing filtering and signal amplification. For state update purposes and minimizing the re-calculation of state matrices due to user defined variables, this section is split into two sub-sections. The first of these subsections is a four-capacitor system that performs bandpass filtering and user designated amplification. The second subsection is a similar construction, but limits the passband cutoff frequencies further and amplifies the signal by a fixed amount.

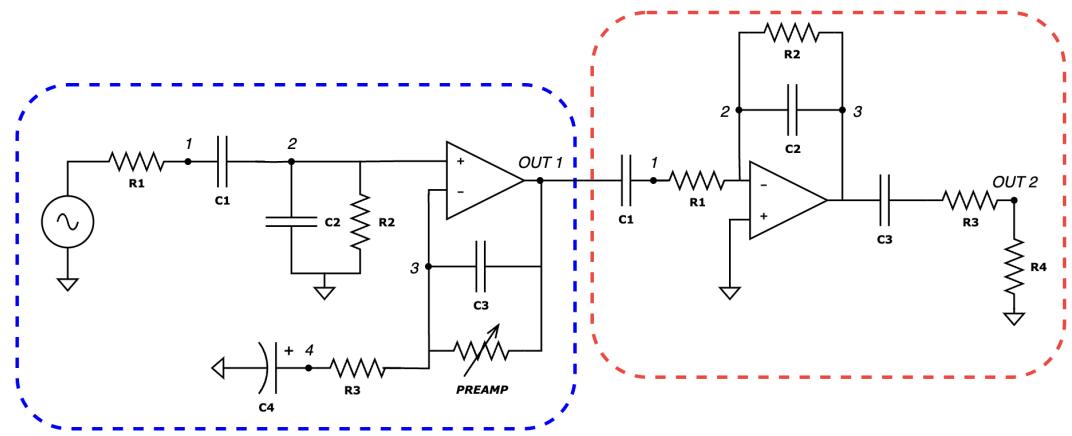


Figure 2.5: Two-stage analog input filtering and amplification

The first section of the analog filtering stage can be seen outlined in blue in figure 2.5. This circuit can further be separated into two functional blocks. The first step of the circuit is a passive band pass stage. The R1 and C2 pair act as a conventional RC lowpass filter, while the C1 and R2 pair act to highpass the input signal. Finally the R1 and R2 pair has a slight voltage divider effect on the signal, however, due to the relationship between the resistors the signal is not reduced by a significant amount relative to the amplification in the second stage, exhibiting only a 7.25% reduction in voltage. In fact, this portion of the circuit has little effect in comparison to the active filter it feeds into. This second block of the first stage is a non-inverting integrator amplifier, with an added lowpass filter C3. This circuit bandpasses the signal with capacitor C4, amplifies it with the voltage divider configuration of the variable PRE AMP resistance and R3, and as mentioned further lowpasses the signal with capacitor C3.

The nodes presented in figure 2.5 can be used to find the system of differential equations of the circuit, using Kirchoff's Current Law to perform nodal analysis [4]. The following represents the system derived from this method.

$$\dot{v}_{C_1} = v_{C_2} \quad (2.7)$$

$$\dot{v}_{C_2} = -\left(\frac{1}{C_1 C_2 R_1 R_2}\right) v_{C_1} - \left(\frac{C_1(R1+R2)+C_2 R_2}{C_1 C_2 R_1 R_2}\right) v_{C_2} + \left(\frac{1}{C_1 C_2 R_1 R_2}\right) v_{in} \quad (2.8)$$

$$\dot{v}_{C_3} = \left(\frac{R_1 C_1}{C_4 R_3}\right) v_{C_2} - \left(\frac{1}{R_{preamp} C_3}\right) v_{C_3} - \left(\frac{1}{R_3 C_3}\right) v_{C_4} \quad (2.9)$$

$$\dot{v}_{C_4} = \left(\frac{R_1 C_1}{C_4 R_3}\right) v_{C_2} - \left(\frac{1}{R_3 C_4}\right) v_{C_4} \quad (2.10)$$

Finally, we can calculate the output voltage at OUT 1 by considering a resistor from the output to ground and using KCL to compute the voltage at the node, resulting in the following output equation.

$$v_{out} = (R_1 C_1) v_{C_2} + v_{C_3} \quad (2.11)$$

From this, the method shown in section 2.2 can be used to construct the state space matrices for the system.

$$\mathbf{A} = - \begin{bmatrix} 0 & -1 & 0 & 0 \\ \frac{1}{C_1 C_2 R_1 R_2} & \frac{C_1(R1+R2)+C_2 R_2}{C_1 C_2 R_1 R_2} & 0 & 0 \\ 0 & -\frac{R_1 C_1}{C_4 R_3} & \frac{1}{R_{preamp} C_3} & \frac{1}{R_3 C_3} \\ 0 & -\frac{R_1 C_1}{C_4 R_3} & 0 & \frac{1}{R_3 C_4} \end{bmatrix} \quad (2.12)$$

$$\mathbf{B} = \begin{bmatrix} 0 \\ \frac{1}{C_1 C_2 R_1 R_2} \\ 0 \\ 0 \end{bmatrix} \quad (2.13)$$

$$\mathbf{C} = \begin{bmatrix} 0 & R_1 C_1 & 1 & 0 \end{bmatrix} \quad (2.14)$$

$$\mathbf{D} = 0 \quad (2.15)$$

The second stage of the analog input preamp is outlined in red in figure 2.5. This stage consists of an op amp integrator amplifier and an output high-pass filter voltage divider configuration. The amplification in this stage is significantly higher than the first as well as the attenuation outside of the passband, resulting in a significantly bandpassed output. The input capacitor C1 attenuates the low frequency content of

the signal from the prior stage. To calculate the state space solution of this stage, the same method used in the first stage will be applied. The resulting system of equations represents the behavior of the second input preamp stage.

$$\dot{v}_{C_1} = -\frac{1}{R_1 C_1} v_{C_1} + \frac{1}{R_1 C_1} v_{in} \quad (2.16)$$

$$\dot{v}_{C_2} = \frac{1}{R_1 C_2} v_{C_1} - \frac{1}{R_2 C_2} v_{C_2} - \frac{1}{R_1 C_2} v_{in} \quad (2.17)$$

$$\dot{v}_{C_3} = \frac{1}{R_1 C_3} v_{C_1} - \frac{1}{R_2 C_3} v_{C_2} - \frac{1}{(R_3 + R_4) C_3} v_{C_3} + \frac{1}{R_1 C_3} v_{in} \quad (2.18)$$

The output equation is calculated to be of the following form

$$\dot{v}_{out} = -\frac{R_4}{R_3 + R_4} v_{C_2} + \frac{R_4}{R_3 + R_4} v_{C_3} \quad (2.19)$$

From this, the method shown in section 2.2 can once again be used to construct the state space matrices for the system.

$$\mathbf{A} = \begin{bmatrix} -\frac{1}{R_1 C_1} & 0 & 0 \\ \frac{1}{R_1 C_2} & -\frac{1}{R_2 C_2} & 0 \\ \frac{1}{R_1 C_3} & -\frac{1}{R_2 C_3} & -\frac{1}{(R_3 + R_4) C_3} \end{bmatrix} \quad (2.20)$$

$$\mathbf{B} = \begin{bmatrix} \frac{1}{R_1 C_1} \\ -\frac{1}{R_1 C_2} \\ -\frac{1}{R_1 C_3} \end{bmatrix} \quad (2.21)$$

$$\mathbf{C} = \begin{bmatrix} 0 & -\frac{R_4}{R_3 + R_4} & \frac{R_4}{R_3 + R_4} \end{bmatrix} \quad (2.22)$$

$$\mathbf{D} = 0 \quad (2.23)$$

With the state space matrices represented with 2.12-2.15 and 2.20-2.23, the filters may be implemented in MATLAB with Algorithm 1. From this implementation the resulting frequency responses are obtained (Figures 2.6 and 2.7).

### 2.3. Input Filtering

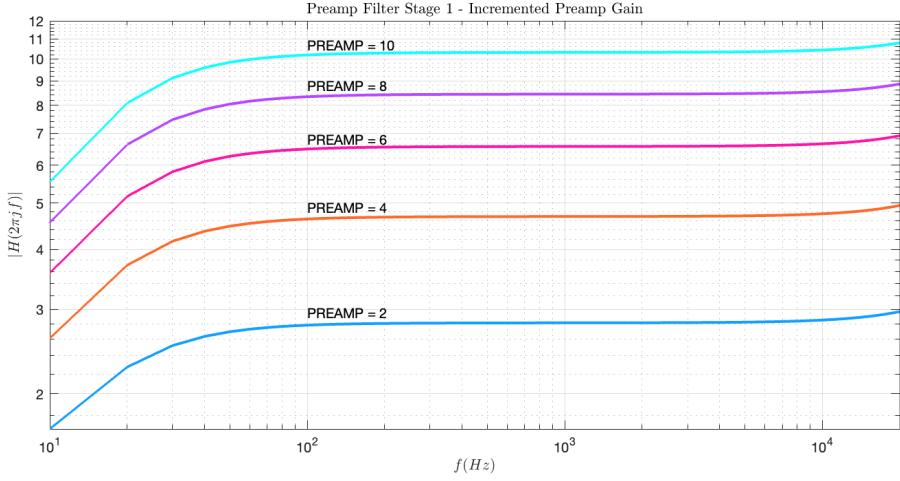


Figure 2.6: Output from the first filter stage

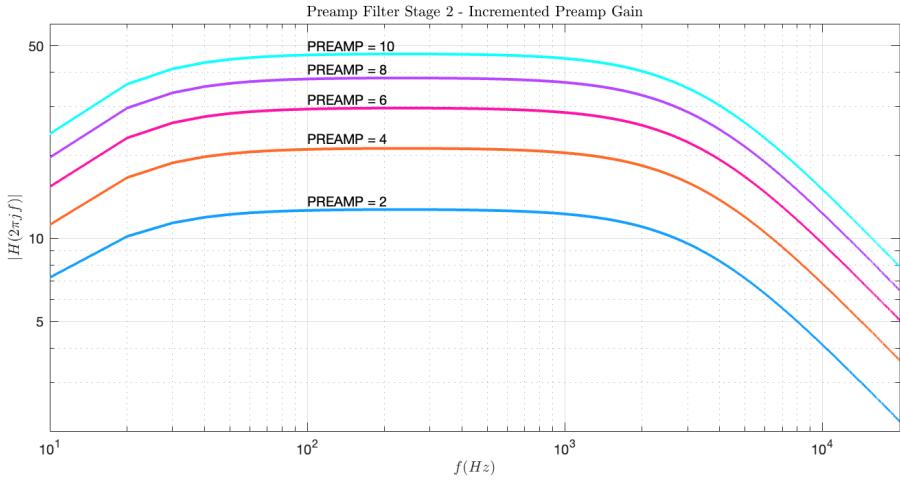


Figure 2.7: Output from second filter stage (input from first stage)

Figure 2.6 demonstrates the highpass behavior of the first stage, however, the low-pass (overall bandpass) behavior of the system is not apparent. This lack of attenuation is due to the high frequency warping due to the trapezoid rule implementation. This is only significantly present in the first stage, Figures 2.8 and 2.9 express the deviation from the analytical solution. These deviations occur only above 10kHz, with the most significant warping occurring above the audible frequency spectrum. The second stage, shown in figure 2.7 demonstrates the significant increase in amplitude, as well as the greater high frequency attenuation in the circuit.

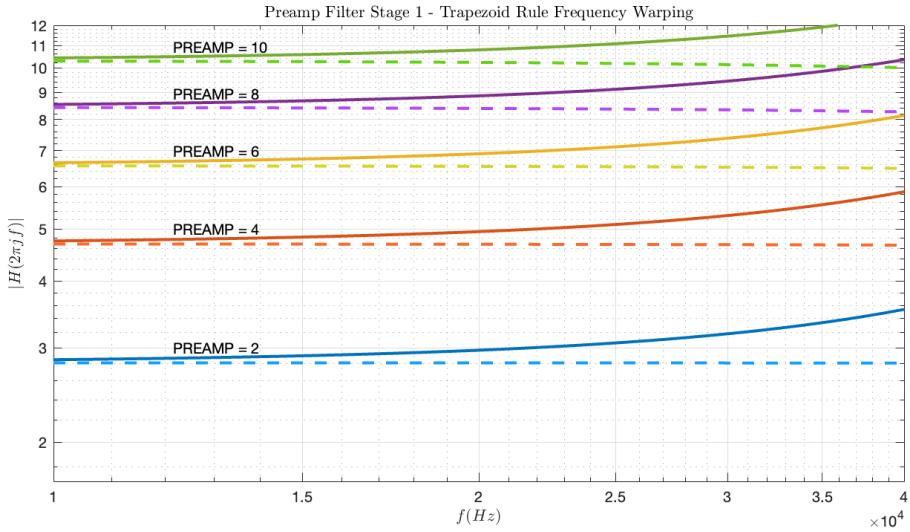


Figure 2.8: Frequency warping from trapezoid rule in the first preamp stage, 10kHz to 40kHz bounds, 192kHz sample rate. Code implementation displayed as solid lines, analytical solution as dashed lines

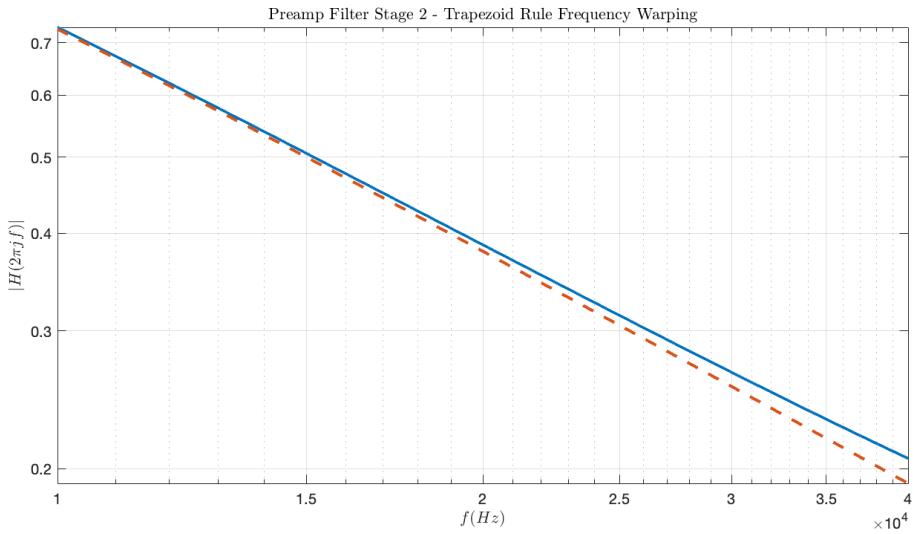


Figure 2.9: Frequency warping from trapezoid rule in the second preamp stage, 10kHz to 40kHz bounds, 192kHz sample rate. Code implementation displayed as solid line, analytical solution as dashed line

## 2.4 Saturation and Schmitt Trigger

The circuit utilizes two stages of saturation in series. The first stage is an open loop op amp with a DC offset control. Figure 2.10 shows the actual component level stage in the circuit and its equivalent voltage control.  $V_{CC}$  and  $V_{EE}$  are the  $\pm 11.85V$  rails of the circuit, and  $R_1 = R_2 = R_{Trigger}$ . The diodes ensure the correct polarity of the

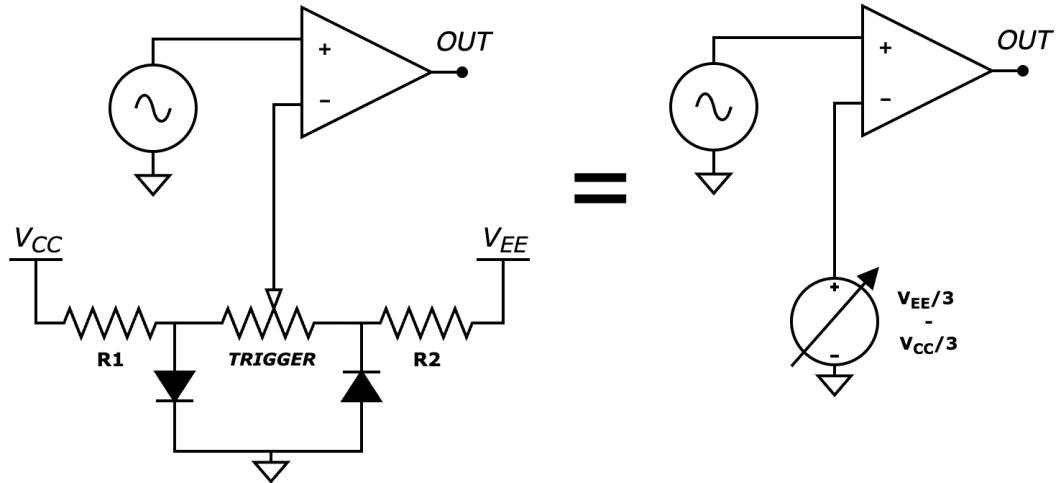


Figure 2.10: Open loop op amp saturation stage with offset control

connected voltage. The following equation represents the user controlled DC voltage divider.

$$v_{Trigger} = V_{CC} + (V_{EE} - V_{CC}) \left( \frac{R_1 + R_{V_{CC}}}{R_1 + R_2 + R_{Trigger}} \right) \quad (2.24)$$

Where  $R_{V_{CC}}$  is the resistance of the TRIGGER potentiometer connected to  $R_1$ . With potentiometer position  $TRIGGER = 0 : 1$ , this system can be represented as a variable voltage with the following equation

$$v_{TRIGGER} = V_{CC} \left( \frac{1 - TRIGGER}{3} \right) + V_{EE} \left( \frac{-TRIGGER}{3} \right) \quad (2.25)$$

The open loop op amp may not be modeled with simply an ideal op amp, since the signal is amplified to a voltage greater than the physical voltage supply capability of the op amp. This discrepancy in calculated and physically available voltage results in the saturation of the op amp, or the hard clipping of the signal at the supply limits. Considering the following digital stages of the circuit, and the difficulty of accurately modelling op amp models, this clipping will simply be applied by a simple limiting algorithm at the supply voltages.

The open loop configuration of the op amp has the following equation

$$v_{ol} = A_o(V_+ - V_-) \quad (2.26)$$

Where  $A_o$  is the open loop gain of the op amp. For the TL074 op amp used in the circuit, this value is  $125dB$ . Accounting for the supply voltage and variable trigger voltage, the following represents the output of the Schumann PLL op amp saturation stage from the open loop output voltage  $v_{ol}$ .

$$v_{out} = \begin{cases} V_{CC} & \text{if } v_{ol} > V_{CC} \\ v_{ol} & \text{if } V_{EE} \leq v_{ol} \leq V_{CC} \\ V_{EE} & \text{if } v_{ol} < V_{EE} \end{cases} \quad (2.27)$$

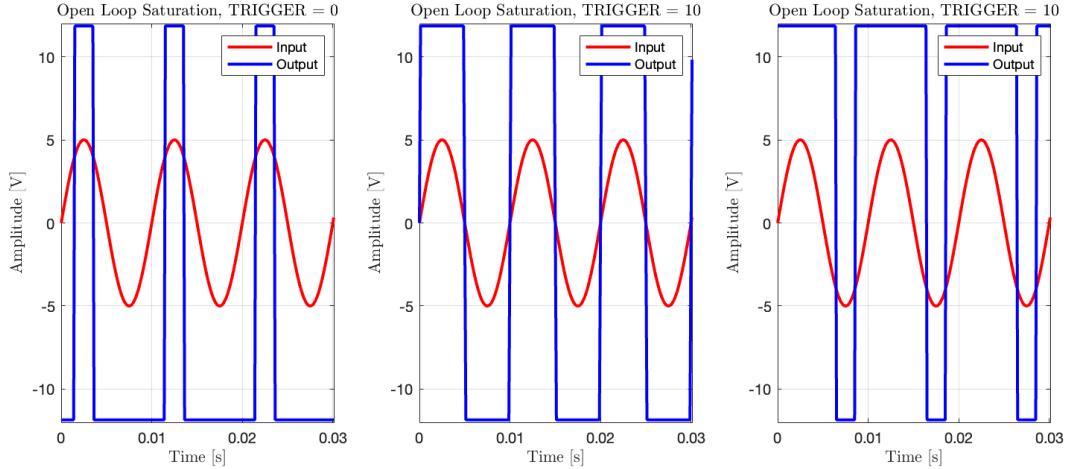


Figure 2.11: Open loop op amp saturation plots at trigger extremes and center

From this equation we can simulate the behavior of the op amp. The plotted output of these equations at three trigger settings is seen in figure 2.11. With a sinusoidal input, the trigger controls the duty cycle of the output square wave. While a guitar input is not sinusoidal, the trigger still acts as a pulse width modulation, or PWM, control. It is important to note that a trigger set higher than the amplitude of the input will result in a constant dc saturation without oscillation, this phenomena is demonstrated in figure 2.12.

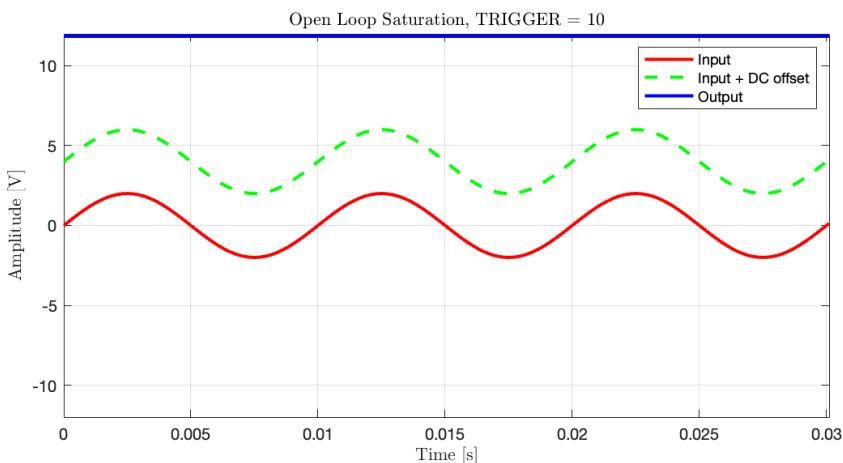


Figure 2.12: Open loop op amp saturation plot in non-oscillatory offset state

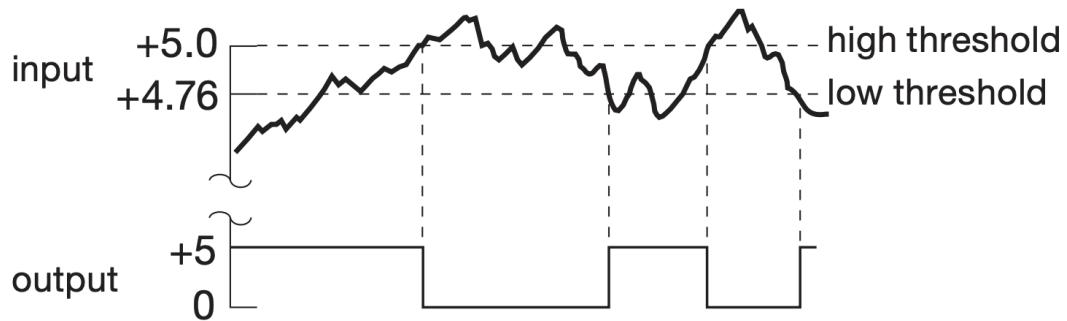


Figure 2.13: Behavior of a Schmitt Trigger inverter with a noisy input signal [4]

The second stage of saturation, and also a component found throughout the circuit, is the Schmitt trigger. The package used in the circuit is the 40106 CMOS Hex Schmitt Trigger Inverter [5], a package with six Schmitt trigger inverters. The Schmitt trigger is a threshold level detecting circuit. The circuit behaves similarly to a comparator, outputting a fixed voltage when the input signal exceeded a certain threshold. Unlike a comparator, where the threshold is simply set to one point to output a voltage (and any signal below that voltage resulting in no output), a Schmitt trigger uses a property called *hysteresis* [4].

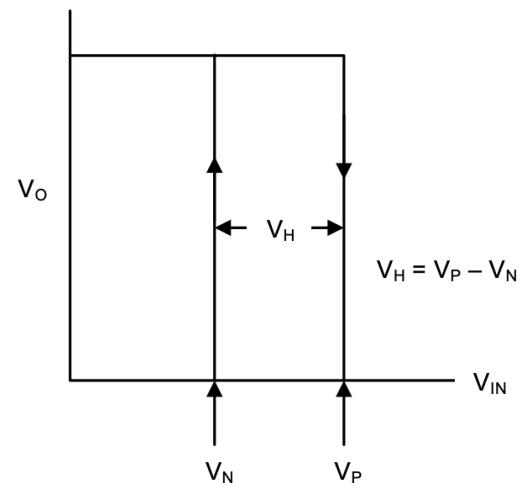


Figure 2.14: Schmitt Trigger hysteresis curve [5]

Hysteresis uses positive feedback in a circuit to set two threshold voltages in a comparator circuit, taking into account the current voltage and its recent history. These thresholds are set to the point where the output triggers a high voltage, and the return point where the output returns to zero. For example, if a signal exceeds the voltage to toggle the output on, it will not turn off again until the input is lower than the low

threshold voltage, and vice versa. This behavior is demonstrated in figure 2.13, note that this is a plot for a Schmitt Trigger inverter, so a high signal produces a low output.

The hysteresis behavior can be plotted in the form of figure ??, where  $V_N$  is the lower threshold voltage,  $V_P$  is the high threshold voltage, and  $V_O$  is the supply voltage to the IC.

The Threshold voltages for the 40106 Schmitt Trigger IC can be found from the supply voltage with the following plot (figure 2.15). The supply voltage in the Schumann PLL is 11.85V, the resulting threshold voltages are  $V_P = 6.5V$  and  $V_N = 4.5V$  [5].

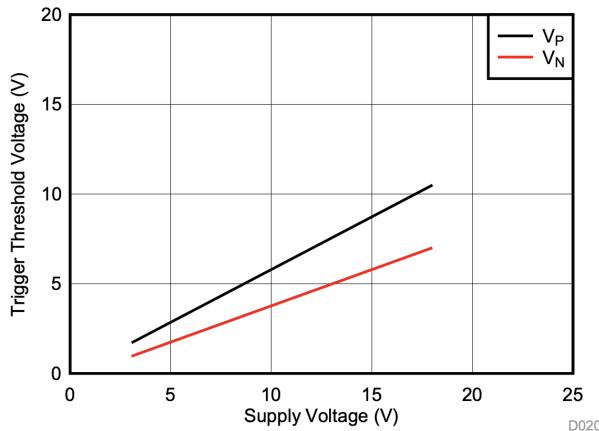


Figure 2.15: Schmitt Trigger threshold voltage plot [5]

The digital implementation of a Schmitt Trigger is a system with one step of memory to mimic the feedback behavior of the trigger. This enables the system to reference the current state of the system to determine the updated state.

---

**Algorithm 2** 40106 Schmitt Trigger Digitization

---

$N$  = Number of Samples in  $u$

$V_{previous} = 0$

**for**  $n = 1:N$  **do**  $V_{in} = u(n)$

**if**  $V_{in} \geq V_P$  AND  $V_{previous} < V_P$  **then**  
         $y_{out}(n) = 0$   
    **end if**

**if**  $V_{in} \leq V_N$  AND  $V_{previous} > V_N$  **then**  
         $y_{out}(n) = V_{supply}$   
    **end if**

$V_{previous} = V_{in}$

**end for**

---

The algorithm 2 represents the digital implementation approach with the properties of the Schmitt Trigger. The transition time of the trigger (duration from low to high output when triggered) is typically  $45\text{ns}$  for the 40106 IC [5]. This is not necessary to model digitally with audio rate sampling.

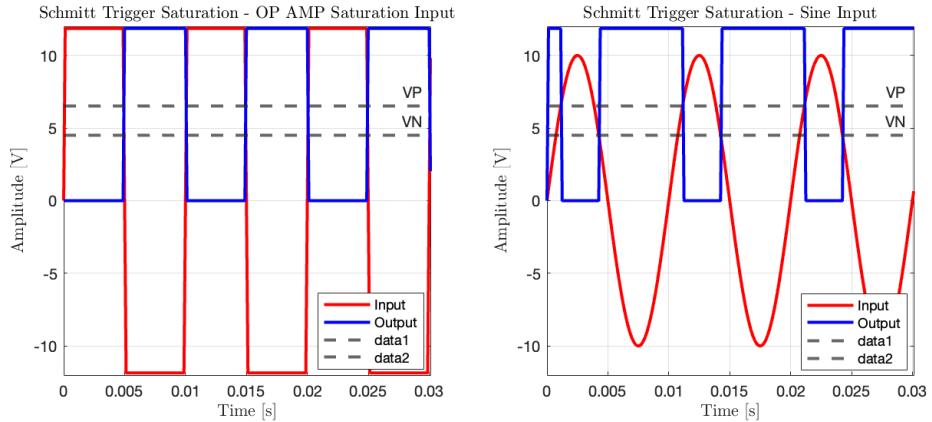


Figure 2.16: Schmitt Trigger output with op amp clipping and sinusoidal input.

The application of this algorithm 2 is presented in 2.16. The output from the open loop op amp saturation stage, the real signal path in the Schumann PLL, shows the bipolar op amp signal and the inverted output. The primary function of this operation is the straightening of the clock edges and generating a 1-bit signal for digital processing (removing the negative voltage content). The second plot demonstrates the Schmitt trigger hysteresis behavior with a sinusoidal input, showing the transition of the output at the threshold points.

## 2.5 Phase-Locked Loop

The Phase-locked loop, or PLL, is a mixed-signal control system that serves as the primary component for frequency multiplication in the Schumann PLL circuit. The system uses phase detection and a VCO to generate a signal that is phase related to the input signal. The stages and signal path of the PLL are shown in 2.17.

The PLL IC used in the design of the Schumann PLL is the CD4046B CMOS Micropower Phase-Locked Loop, introduced by RCA in the 1970s - commonly used for clock multiplication in early digital electronics. The IC consists of a low-power linear voltage controlled oscillator and two types of phase comparators. In addition to the on-board functions, the PLL circuit requires two primary functions. The first of these functions is the loop filter, which smooths the output of the phase detector for the VCO input. The second is a method of frequency dividing the VCO output signal - this functionality is completed by a counter outlined in detail in section 2.6. The sub-component analysis and implementation is discussed in the following subsections.

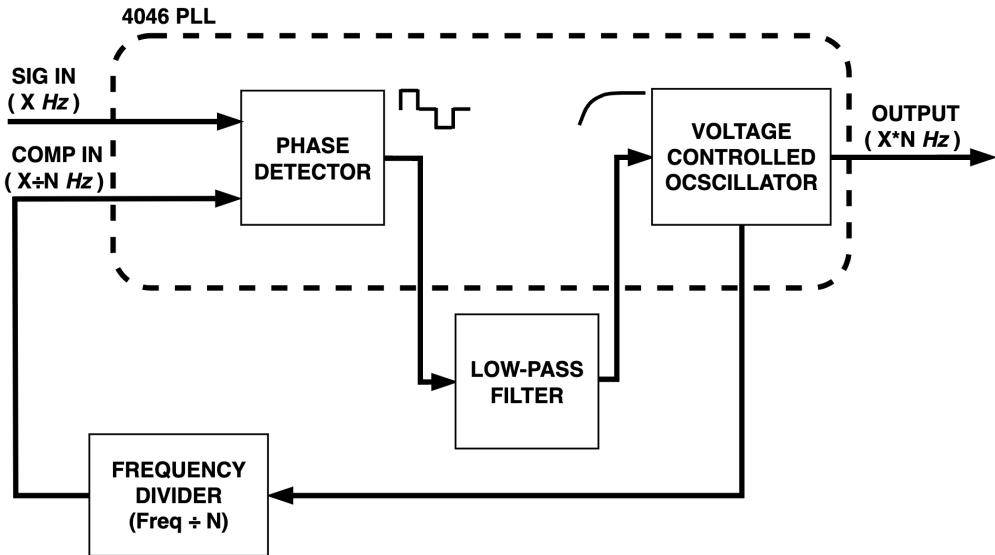


Figure 2.17: Phase-Locked Loop system block diagram

### 2.5.1 The Phase Frequency Detector

The input stage of the phase-locked loop is the phase detector. The 4046 IC contains two frequency comparators, the type II phase phase comparator is used in the Schumann PLL design. The Phase Comparator II circuit is an edge controlled digital memory network [3] also known as a Phase Frequency Detector (PFD) [6]. This method of phase detection uses a logic circuit (shown in figure 2.18), acting only on the rising edges of the two signal inputs. The logic circuit outputs a control signal via a p-MOS and n-MOS charge pump configuration, this pulls the voltage output up or down by opening the transistor path to the voltage supplies ( $V_{CC}$  and ground).

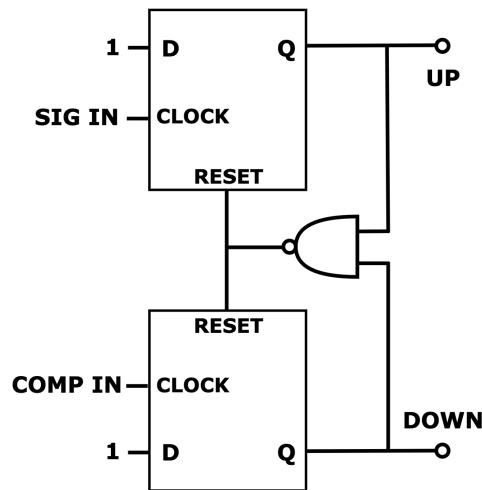


Figure 2.18: D Flip-Flop logic diagram

The system detects phase discrepancies in the rising edges of the input signals SIG IN and COMP IN (Feedback from the VCO out), outputting a high voltage when the COMP IN signal lags behind the SIG IN signal and a low voltage when the SIG IN signal lags behind the COMP IN signal. This creates a real-time adjustment in the voltage fed to the VCO, adjusting the frequency of the output and "locking" the output to the input signal. This output generation is outlined in figure 2.19.

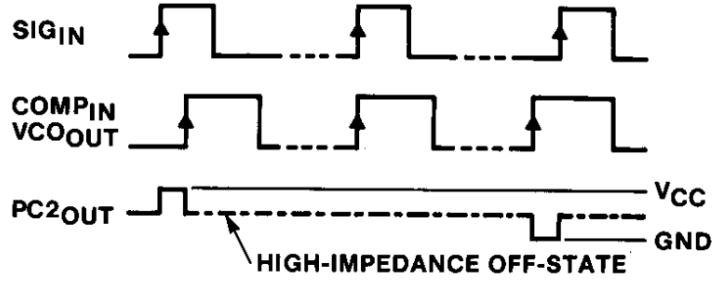


Figure 2.19: Output behavior of the PFD [6]

The logic system is made up of three components, two D Flip-Flops and one AND gate. The D Flip-Flops are configured such that the D input is constantly high, and will toggle on with the first detected clock edge. After the edge triggers the on state output from Q, the output will only reset to zero after both outputs toggle on, resulting in the triggering of the AND gate, seen in the table 2.1. When neither output is on, both transistors are closed and there is no output voltage and a high impedance, rendering the circuit disconnected from the connected loop filter.

SIG <sub>IN</sub>	COMP <sub>IN</sub>	Q <sub>UP</sub>	Q <sub>DOWN</sub>
1	0	1	0
0	1	0	1
1	1	0	0
0	0	No Change	No Change

Table 2.1: Behavioral truth table for the PLL PFD

Algorithm 3 represents the digital implementation for square wave edge detection and output the signal of the PFD, where  $Q_{UP}$  and  $Q_{DOWN}$  are the D Flip-Flop outputs and  $HIZ$  designates the high impedance off state for reference in the loop filter algorithm.

---

**Algorithm 3** 4046 PC II (Phase Frequency Detector)

---

```

 $N = \text{Number of Samples in } u$ 
 $COMP_{IN_{PREV}} = 0$ 
 $SIG_{IN_{PREV}} = 0$ 
for n = 1:N do
    if  $SIG_{IN} > 0$  AND  $SIG_{IN_{PREV}} = 0$  then
         $Q_{UP} = 1$ 
    end if
    if  $COMP_{IN} > 0$  AND  $COMP_{IN_{PREV}} = 0$  then
         $Q_{DOWN} = 1$ 
    end if
    if  $Q_{UP}$  AND  $Q_{DOWN} = 1$  then
         $Q_{UP} = 0$ 
         $Q_{DOWN} = 0$ 
    end if
    if  $Q_{UP} = 1$  then
         $x_{ctrl}(n) = V_{DD}$ 
    end if
    if  $Q_{DOWN} = 1$  then
         $x_{ctrl}(n) = 0$ 
    end if
    if  $Q_{UP}$  AND  $Q_{DOWN} = 0$  then
         $HIZ = 1$ 
    end if
     $COMP_{IN_{PREV}} = COMP_{IN}$ 
     $SIG_{IN_{PREV}} = SIG_{IN}$ 
end for

```

---

### 2.5.2 PLL Loop Filter

The loop filter is the second stage of the PLL system. The primary purpose of it is the low pass filtering (smoothing - in practice) of the variable square wave output of the PFD. This smoothing results in a variable dc voltage to designate the frequency of the VCO output. The usual filter suggested by the 4046 data sheet [3] is a basic RC low pass, however the Schumann PLL uses an RC configuration with a voltage divider and feedthrough pictured in 2.20.

The components of the filter consist of two user defined variable voltages (implemented with rheostat potentiometer configurations), RESPONSE and LOOP TRACK and a switchable capacitance with LOOP SPEED. This allows a user to control the amount of unfiltered signal fed through, and the tracking speed and variance of the VCO. Generally, RESPONSE controls how fast the effect locks onto a note, and LOOP TRACK controls how accurately the system locks onto a note, with lower settings giving the tracking a vibrato quality. The LOOP SPEED selection designates the frequency ramp and decay time, with setting 1 having the shortest ramp up and 3

having the longest, this is correspondent to the size of the capacitor and the time it takes to discharge.

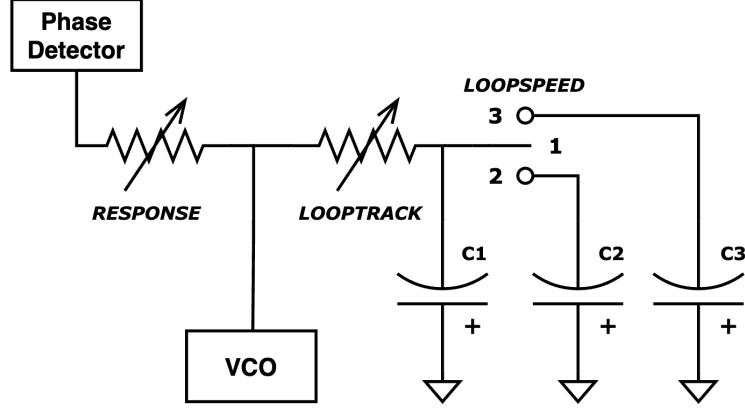


Figure 2.20: PLL external loop filter schematic

With the linear behavior of the loop filter, the modelling method outlined in section 2.2 can be applied. With the switchable capacitors, there may be two capacitors in parallel to ground. These pairs of capacitors can be represented as a single capacitor with the sum of any connected capacitance [4], since capacitors in series connected to the same nodes may be treated as one. This summation also reduces the energy-storing components in the circuit to one, therefore the state space matrix  $\mathbf{A}$  will have  $1 \times 1$  dimensions. The following state equations are used to model the system.

$$\mathbf{A} = \frac{-1}{(R_{response} + R_{looptrack})C_{loopspeed}} \quad (2.28)$$

$$\mathbf{B} = \frac{1}{(R_{response} + R_{looptrack})C_{loopspeed}} \quad (2.29)$$

$$\mathbf{C} = 1 - \frac{R_{looptrack}}{R_{response} + R_{looptrack}} \quad (2.30)$$

$$\mathbf{D} = \frac{R_{looptrack}}{R_{response} + R_{looptrack}} \quad (2.31)$$

The above equations are relevant for the simulation under an input signal from the PFD. Under the condition where the charge pump is closed there is a high impedance at the input. This is equivalent to a break in the circuit at the phase detector input. Therefore under this condition the only output to the VCO is the discharged voltage from the capacitors. With this, there is a secondary output filter matrix that excludes the input, state, and feedthrough matrices. This leaves the following system of state equations.

$$\mathbf{A} = \frac{-1}{(R_{looptrack})C_{loopspeed}} \quad (2.32)$$

$$\mathbf{C} = 1 \quad (2.33)$$

These can be implemented with algorithm 1 with the addition of a filter switching condition using the  $HIZ$  condition from algorithm 3. Figure 2.21 demonstrates the effect of the switching LOOP SPEED capacitors, not demonstrated in the plot is the additional charge and discharge time corresponding to the lower cutoff frequency in the transfer function.

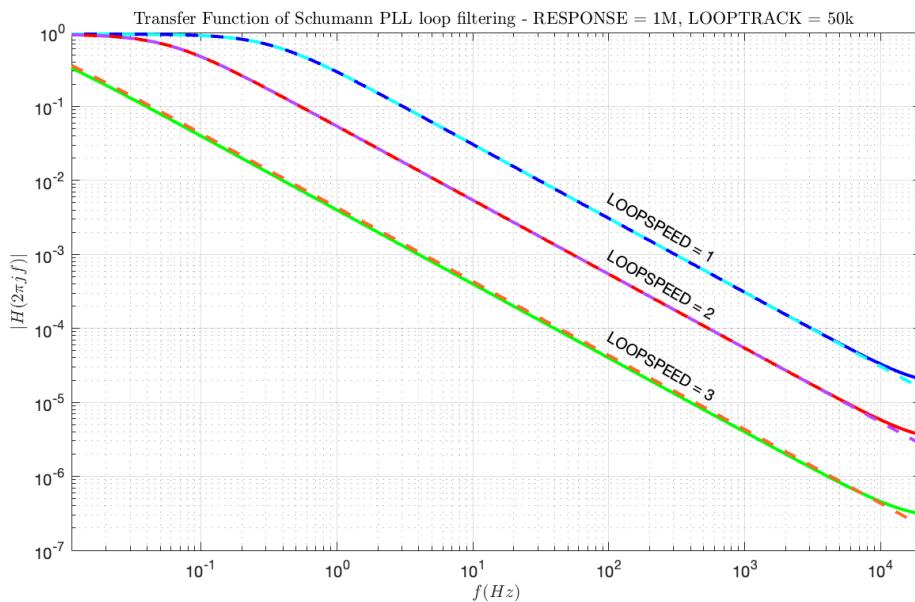


Figure 2.21: PLL loop filter plot, switched capacitors

### 2.5.3 The VCO

The final sub-component of the PLL is the voltage controlled oscillator (VCO). This uses the filtered control voltage from the phase comparator to generate a square wave at a designated frequency. The 4046 VCO is linear and designed to require low input voltages. As seen in the schematic figure 2.4, the PLL requires an external capacitor and resistor to function. These components correspond to R1 and C1 in figure 2.22.

These components designate the VCO behavior, with the variable LAGTIME resistance (R1) controlling the center frequency of the frequency tracking and the external capacitor controlling bandwidth. From the 4046 application report, these component values can be used to obtain a voltage to frequency coefficient (eqn. 2.35).

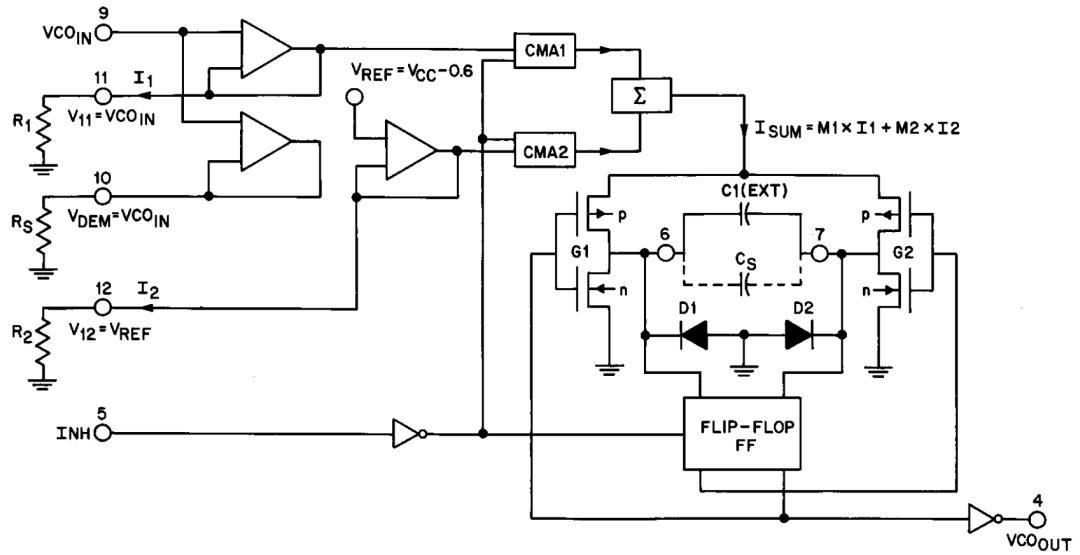


Figure 2.22: 4046 VCO Functional Block Diagram [6]

$$V_{ramp} = \frac{V_{CC}}{10} + .6 \quad (2.34)$$

$$f_{osc} = \frac{6.2(VCO_{IN}/R_1)}{2C_1V_{ramp}} \quad (2.35)$$

With this coefficient, the system can be approximated through the generation of a variable frequency sinusoid with that coefficient converted from  $Hz$  to radians. This sinusoid will then be used to extrapolate a square wave with the same frequency (i.e. when the sine is greater than 0, set it equal to 1), this approach provides a digital clock that accounts for the PLL component values, without the component level modelling of the mixed signal VCO.

$$VCO_{sin}(t) = \sin(2\pi f_{osc} t) \quad (2.36)$$

$$VCO_{OUT}(t) = \begin{cases} 1 & \text{if } VCO_{sin}(t) > 0 \\ 0 & \text{if } VCO_{sin}(t) \leq 0 \end{cases} \quad (2.37)$$

## 2.6 Decade Counter

The decade counter is the final digital component used in the Schumann PLL circuit. This chip performs the clock frequency division used for the sub-frequency and PLL feedback frequency generation. The IC used in the effect is the CD4017 CMOS counter, a 5-stage johnson counter with 10 decoded outputs [7]. The logic circuit detects

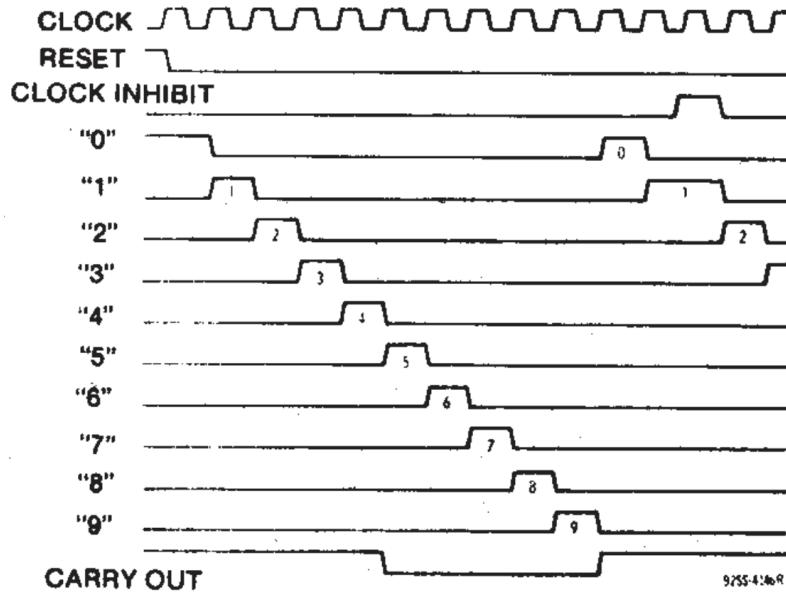


Figure 2.23: Timing diagram for CD4017 [7]

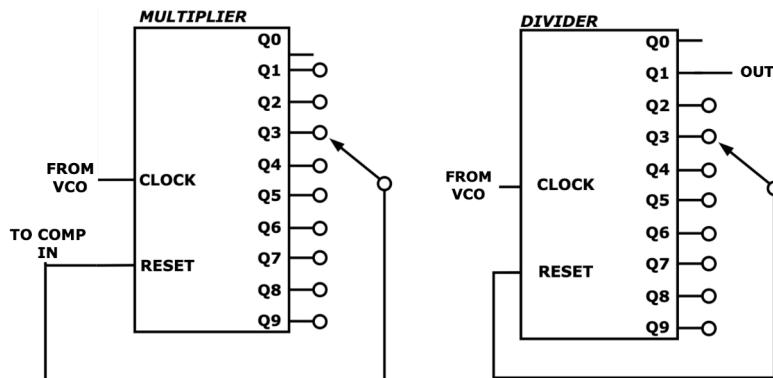


Figure 2.24: Configuration of decade counters in the Schumann PLL [2]

incoming rising clock edges, iterating through ten outputs. The timing diagram for the chip is documented in figure 2.23. The timing of the output is dependant on the rotary position and configuration of the counters, shown in figure 2.24, the two decade counters in the circuit have slightly differing configurations.

Both decade counters are configured with a rotary selector routing one of the clock outputs to reset the counter, this will prompt iteration through the cycle, repeating at the designated output. The difference in configuration is the source of the output signal and the range of frequency division. The MULTIPLIER counter, found in the feedback path of the PLL, and routes the reset pulse to the COMP IN of the PLL PFD. This configuration results in a consistent output pulse width unrelated to the input frequency. This pulse width in the pedal is .15ms, observed from the hardware

copy of the pedal (appendix B). The DIVIDER decade counter is configured to always output on the first detected clock edge after reset, and is reset by a subsequent input clock. This generates an output signal with a pulse width equal to one full clock cycle. The primary functional difference in user operation is the lack of a unison frequency selection for the DIVIDER configuration, this is reflected in the pedal interface in figure 1.1.

The counters may be implemented with conditional processing and timing processes in MATLAB. Algorithms 4 and 5 outline the overall framework and differences in implementation between the two counter configurations.

---

**Algorithm 4** 4017 MULTIPLIER Counter Implementation

---

```

 $u$  = INPUT SIGNAL
 $PulseCount$  = 0
 $Count$  = 0
 $TARGET$  = Rotary Setting
 $State_{out}$  = 0
 $Trigger$  = 0
 $NP$  =  $PulseTime * SampleRate$ 
 $N$  = Number of Samples in  $u$ 
for  $n = 1:N$  do
    if  $u(n) > u(n - 1)$  then
         $Count = Count + 1$ 
        if  $Count == TARGET$  then
             $State_{out} = 1$ 
             $Count = 0$ 
             $Trigger = 1$ 
        end if
    end if
    if  $Trigger == 1$  then
         $PulseCount = PulseCount + 1$ 
        if  $PulseCount == NP$  then
             $PulseCount = 0$ 
             $Trigger = 0$ 
             $State_{out} = 0$ 
        end if
    end if
end for
```

---

## 2.7 Output Volume and Filtering

The output of the effect after the digital processing consists of a summing amplifier configuration and a low pass filter controlled by the WAVE SHAPE knob on the effect interface. The circuit output schematic, pictured in figure 2.25, shows the components of the output stage.

---

**Algorithm 5** 4017 DIVIDER Counter Implementation

---

```

 $u$  = INPUT SIGNAL
 $Count = 0$ 
 $TARGET$  = Rotary Setting
 $State_{out} = 0$ 
 $Trigger = 0$ 
 $N$  = Number of Samples in  $u$ 
for  $n = 1:N$  do
    if  $u(n) > u(n - 1)$  then
         $Count = Count + 1$ 
        if  $Trigger == 1$  then
             $Trigger = 0$ 
             $State_{out} = 0$ 
        end if
        if  $Count == TARGET$  then
             $Count = 0$ 
        end if
    end if
end for

```

---

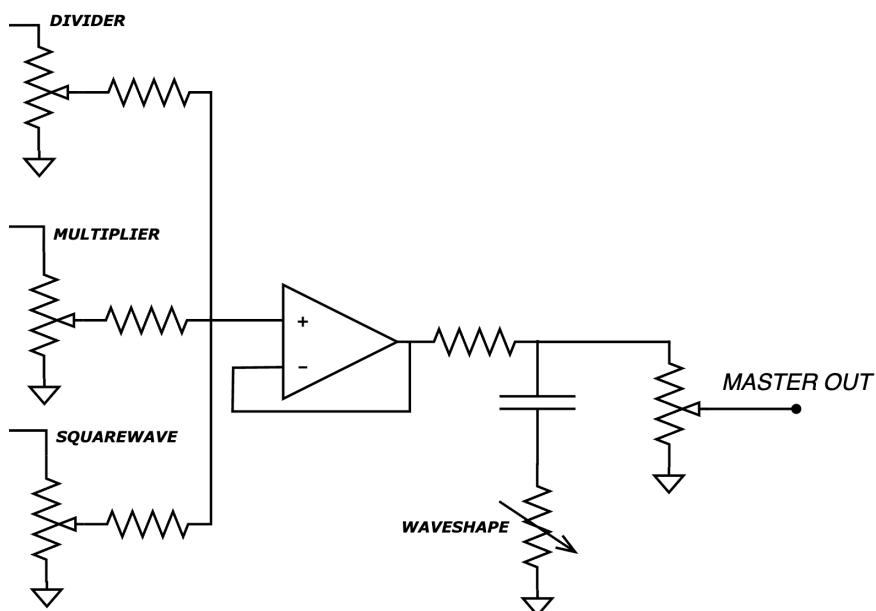


Figure 2.25: Schumann PLL output stage schematic

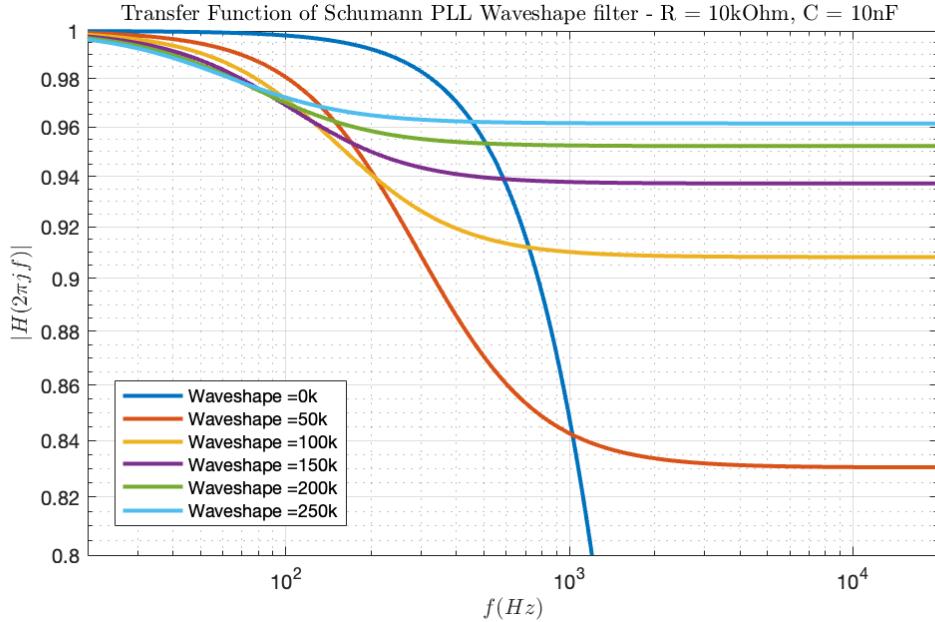


Figure 2.26: Plot of output filter transfer function at variable resistances

Each square wave signal has a voltage divider volume control before the summing amplifier, allowing the user to scale the outputs relative to each other. It is important to note that the SQUARE WAVE output signal is output from the initial open-loop op amp saturation stage. As such, the signal is a bipolar square wave, unlike the DIVIDER and MULTIPLIER clock signals. Additionally, the op amp pictured is a single source voltage supplied to a LM660CN [19] CMOS Quad Operational Amplifier, this op amp supports peak to peak voltage swing, but will not output any voltage below 0V because of its single supply voltage. To achieve this in the digital implementation, the signals must be added and then the summed voltage clipped using a conditional statement.

### 2.7.1 Wave Shape Filter

The output lowpass filter pictured in figure 2.25 is functionally the same as the low pass filter design in the loop filter, and may be modelled identically with equations 2.28-2.31. The filter has only one user defined variable, the variable resistance to ground, and controls the ratio of low-passed signal to fed through signal. Figure 2.26 documents the variable cutoff and high frequency attenuation from the variable filter resistance.



# Chapter 3

## Results and Analysis

To measure the performance of the model, it has been compared against a physical copy of the effect produced in conjunction with the digitization process (see appendix A for build details). This method of analysis is most effective in this style of synthesis circuit, where there is a substantially more complex process than common fuzz or overdrive circuits with only basic wave shaping functionality.

The computational performance of the system in the MATLAB implementation is sufficient for a future real-time implementation, with an average processing time of  $.117s$  processing time per second of audio sampled at  $192kHz$  and  $.028s$  processing time per second of audio sampled at  $48kHz$ . Without further development in output anti-aliasing methods, it is recommended to oversample to  $192kHz$  for the best audio performance, however due to the layered signals in the effect and the characteristically harsh sound, subjectively the system does not suffer significantly when computed at a  $48kHz$  sampling rate.

This analysis is divided into three primary categories. The first is the square wave saturation and filtering circuit, which includes the output filter as well, but does not address any phase locking behavior. This is correspondent to the SQUARE WAVE output path in the effect. The second area of analysis is the phase and frequency locking behavior of the effect, this behavior is crucial to the characteristic sound of the effect. This section will also briefly discuss the behavior of phase locking through the VCO control voltage input analysis. Finally, a discussion of subjective qualities and effectiveness of the digitized effect when subjected to real guitar input. This section also includes a guide to attached audio files.

### 3.1 Analog Filtering and Saturation Behavior

The basic square wave fuzz effect on the signal input is generated through the op amp clipping stage outlined and simulated in 2.4. When isolated (i.e. PLL-generated tones are bypassed with MULTIPLIER and DIVIDER controls) the effect will pass through a

### CHAPTER 3. RESULTS AND ANALYSIS

single supply op amp and the lowpass filter discussed in 2.7. The resultant output with a  $200\text{Hz}$  sine wave input is shown in the time and frequency domains in figures 3.1 and 3.2, respectively. From the time domain plot, these signals are nearly identical, with the peaks of the square waves following the same slope from the WAVE SHAPE filtering behavior. The primary discrepancy is seen at the rising and falling edges of the waves, where the hardware effect displays significant rippling from the Gibbs Phenomenon [20]. This artifacting is most likely due to the recording rate of hardware effect, which has band-limited the signal.

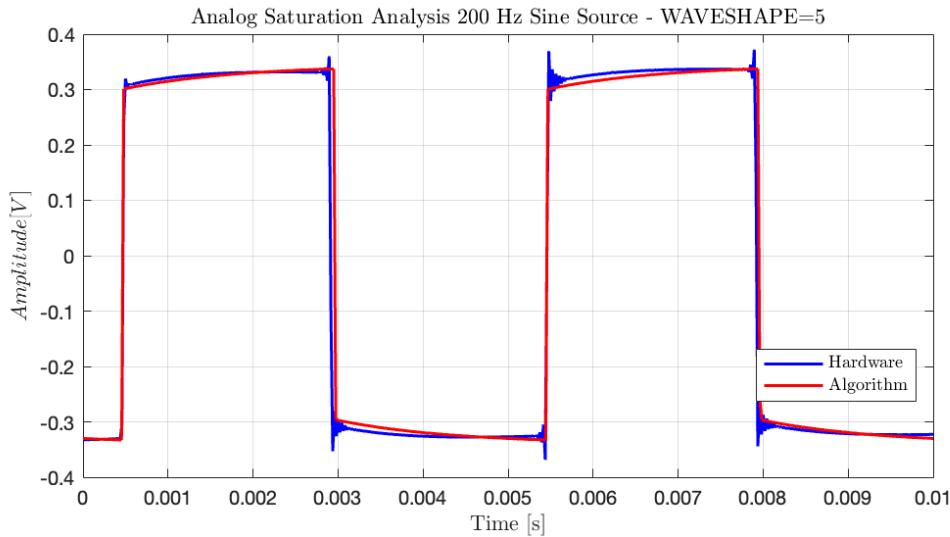


Figure 3.1: Square wave saturation time domain analysis

In the frequency domain, the harmonic content of the two signals is aligned. There is some additional harmonic content in addition to the primary square wave harmonics that are less present in the algorithmic implementation, however the primary harmonics of the square wave are maintained. It is also important to note one of the primary advantages the software implementation has over the hardware that can be observed in the plot, which is the significantly lower noise floor than a hardware fuzz circuit.

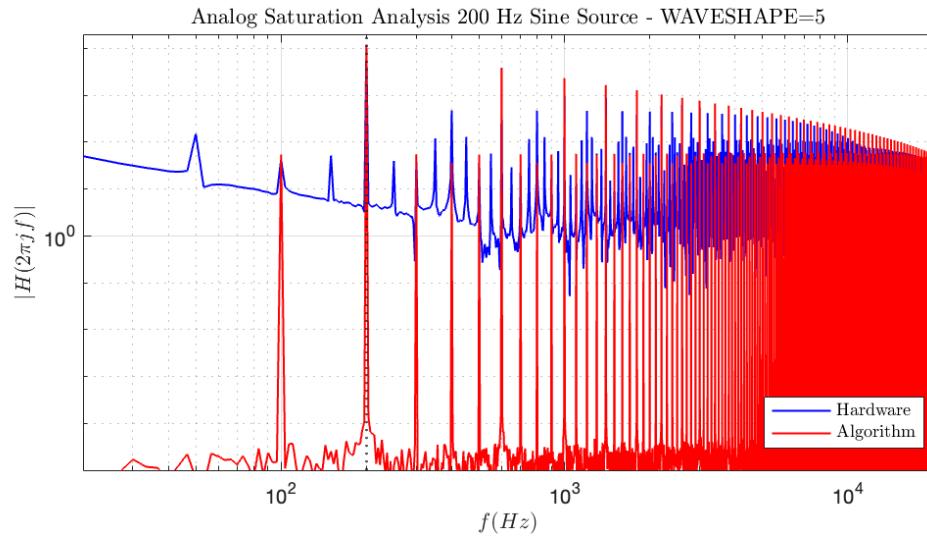


Figure 3.2: Square wave saturation harmonic analysis

### 3.2 Phase and Frequency Locking Behavior

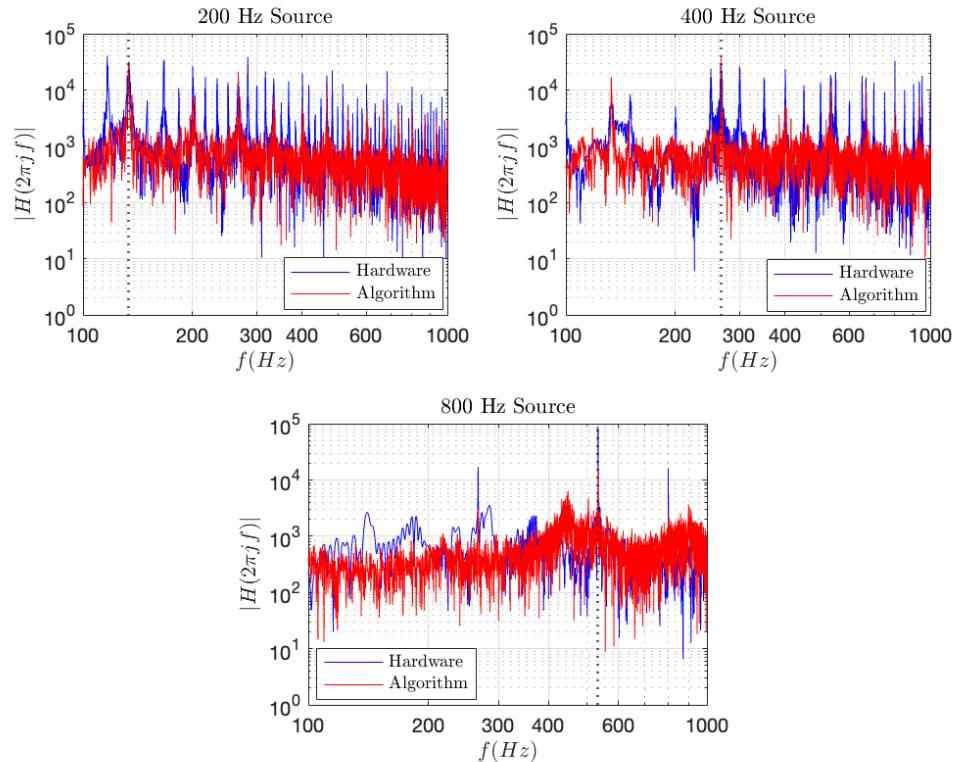


Figure 3.3: PLL Frequency division behavior, set to lower perfect 5 from input frequency, marked by dotted line

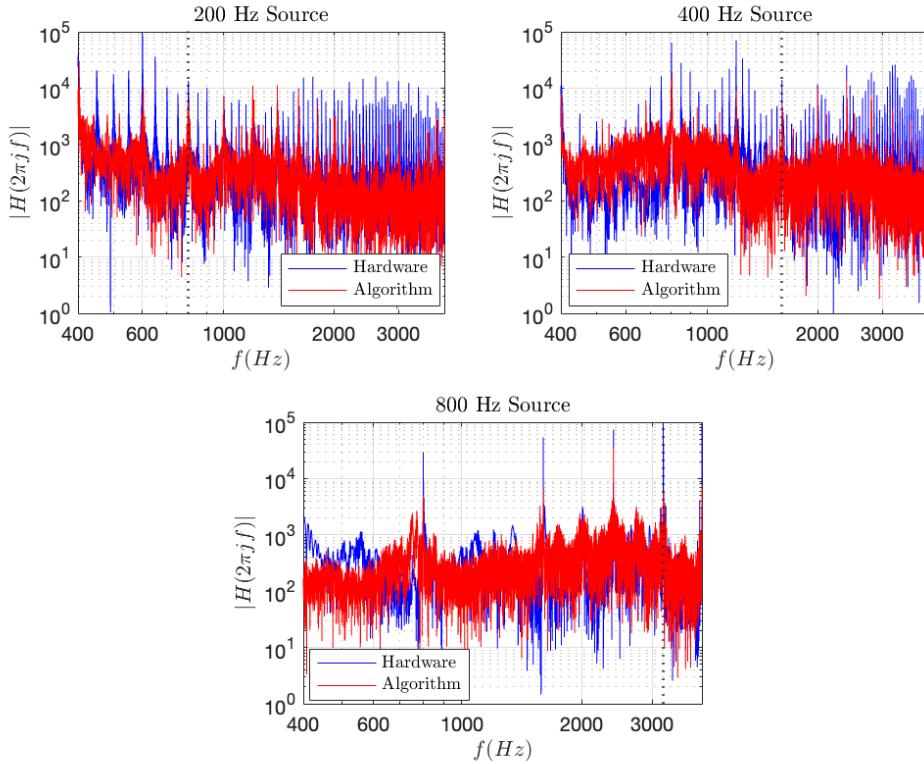


Figure 3.4: PLL Frequency division behavior, set to raise 2 octaves from input frequency, marked by dotted line

The frequency locking behavior is crucial for the functionality and overall tonality of the Schumann PLL, since this is the feature the circuit is built around, with the square wave processing existing to perform the CMOS logic processing. The behavior of PLL frequency locking is efficient and consistent with the hardware implementation across the mid-range frequency spectrum, the expected use case for input fundamental tones.

Examples from the frequency division and multiplication outputs are shown at various frequencies compared to the hardware copy in figures 3.3 and 3.4. All plots show strong correlation between peaks in the hardware and algorithmic implementations. The behavior of the decade counter in the multiplier configuration has a strong effect on timbre and PLL system behavior, which has been replicated in the multiplier behavior, this can be seen via inspection in figure 3.4, with the highest peak sitting at a lower frequency than the dotted line marking the expected multiplied frequency in both the hardware and algorithmic implementations.

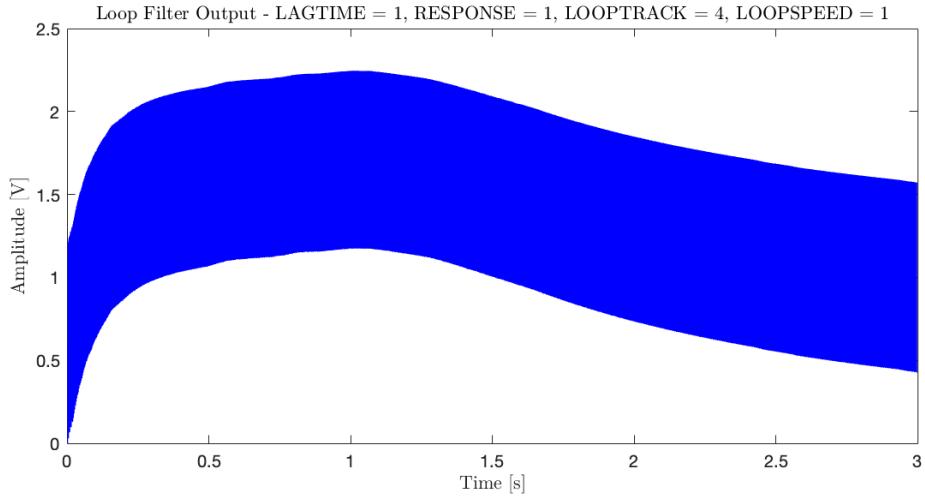


Figure 3.5: Loop Filter general sinusoidal input behavior

### 3.2.1 Loop Filter Control Voltage and PFD Input Analysis

The operation of the PLL is dependent on the behavior of the Loop Filter [3] and multiplier counter [7] (feedback clock divider) that convert pulse information from the PFD and divide VCO output for frequency locking, respectively. The effective execution of these behaviors is crucial in the achievement of phase locking in the circuit. Firstly, considering the VCO input (output from loop filter) in figure 3.5, the general behavior of the PFD and loop filter combination can be observed. The control voltage rapidly rises from zero, locking onto a tone, then slowly tapers off and applies self correction when it varies or the input frequency changes. This is observed in the smooth roll-off in control voltage from 1s to 3s in the plot. The waveform present modulating the smooth DC control voltage is the PFD output, fed through to the VCO due to the loop filter topology. This can be observed closely in figures 3.6 and 3.7, taken from different times in the simulation. Near the beginning of the simulation, when the frequency has not locked yet, the pulses are observed to be long in duration, representative of the PFD behavior under an input signal frequency discrepancy (outlined in figure 2.19). The tapering control voltage is also consistent with the expected behavior, consisting of only short pulses characteristic of phase locked (or very nearly phase locked) inputs.

These behaviors are consistent with that expected from the system, and is reinforced by the phase locking demonstrated in the frequency domain analysis of the SIG IN and COMP IN (multiplier counter output) from the algorithm, showing the two signals to be frequency aligned. The additional harmonic content present in the signal is directly resultant from the variable duty cycle of the feedback counter configuration seen in 2.24, which outputs a positive pulse of a fixed duration independent of frequency. This expected behavior reinforces the validity of the generated multiplied and divided signal outputs.

### CHAPTER 3. RESULTS AND ANALYSIS

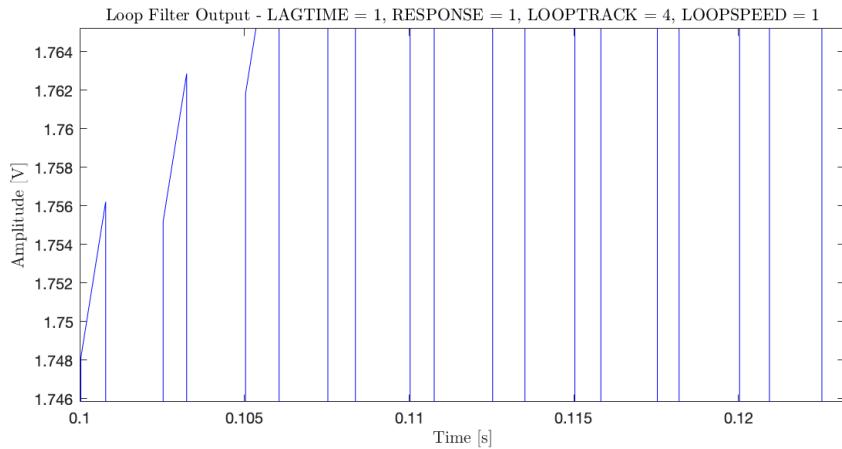


Figure 3.6: Loop Filter initial state pulses (Sinusoidal Input)

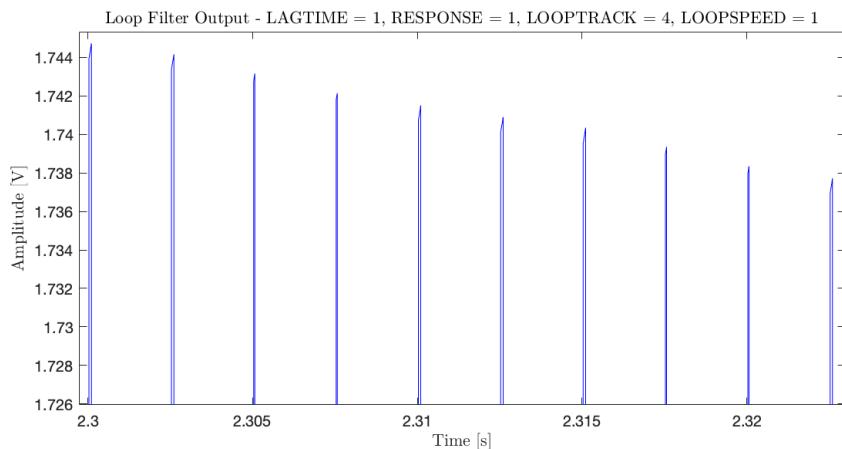


Figure 3.7: Loop Filter locked state pulses (Sinusoidal Input)

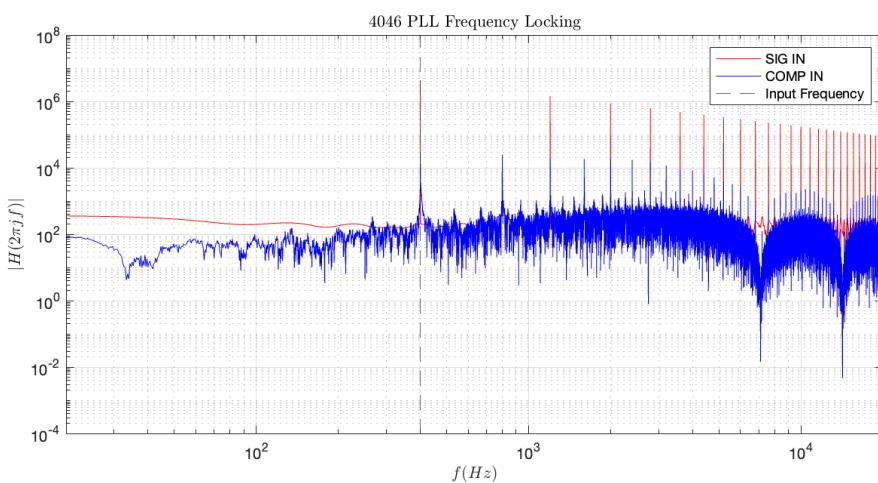


Figure 3.8: PLL Input Phase Locking analysis

### 3.3 Subjective Analysis

The subjective comparison of the digital implementation and the hardware effect is necessary in a complex system where some features may be unaccounted for in harmonic and time domain analysis. Included with this report are sounds with use case samples of audio from the algorithm and hardware. Samples from the hardware were routed through an audio interface and re-recorded, while digital samples were recorded with source audio in the attached MATLAB script. In both  $48kHz$  and  $192kHz$  sampling rates, the guitar audio performs effectively when directly compared to the physical pedal. The lowest similarity of the signals is found in the frequency multiplied signal, where the digital model seems to have a longer response time than the hardware. This may be remedied by future work in a full, component-level model of the PLL VCO.

The following list of attached audio files comprises a range of use cases and effect settings to compare the full performance of the algorithm and hardware. Hardware was recorded at a  $48kHz$  sampling rate, algorithm processed samples were generated at  $48kHz$  and  $192kHz$  sampling rate and downsampled to  $48kHz$ . More audio samples may be found at [www.anachrome.art/tech/dsp/pll](http://www.anachrome.art/tech/dsp/pll)

#### Audio Example 1: Low Register Guitar Input

- LOW-GUITAR\_48k\_AUDIO\_IN.wav
- LOW-GUITAR\_48k\_HARDWARE.wav
- LOW-GUITAR\_192k\_RENDER.wav
- LOW-GUITAR\_48k\_RENDER.wav

#### Audio Example 2: Full Range Guitar Input

- FULLRANGE-GUITAR\_48k\_AUDIO\_IN.wav
- FULLRANGE-GUITAR\_48k\_HARDWARE.wav
- FULLRANGE-GUITAR\_192k\_RENDER.wav
- FULLRANGE-GUITAR\_48k\_RENDER.wav



# Chapter 4

## Conclusions

In this paper, an analysis of the Schumann Electronics PLL and approach to modelling the mixed signal system was presented. State space matrices and the trapezoid rule were utilized to simulate linear input amplification and analog filters in the effect, while digital logic algorithms were developed from the behavioral information found within data sheets of the CMOS logic integrated circuits in the effect. These digitized component algorithms were configured according to the pedal schematic and a full implementation in MATLAB was developed. The output from the algorithm were analyzed and discussed in chapter 3, with satisfactory behavior and similarity in output to the hardware effect.

### 4.1 Future Work and Improvements

As this is a novel attempt to model a lesser-known guitar effect, there are still possible improvements to be made upon the methods and resulting algorithm presented with this effort. Two primary steps could be taken to most accurately model the system. The first of these steps is a more in-depth analysis and algorithm to model the charging and discharging of the VCO stage and its square wave generation. Currently this is modeled as a sine wave with a linear voltage to frequency relationship used as a reference for a generated square wave. This current approach allows the system to function with reasonable accuracy, but a component level implementation may prove to more accurately model this system. Secondly, an approach to reduce aliasing other than oversampling could be applied to the system, difficulties in implementation may arise from the nature of the conditional logic algorithms applied in the system that are used to generate waveforms. Further research must be done in approaches to band-limit square waves that are generated with iterative conditional systems. These improvements could further improve performance and algorithm accuracy for a full real-time VST implementation of the effect.



## Appendix A

# Hardware Implementation of the Schumann PLL

In addition to the digital replication of the pedal developed in the primary chapters, a hardware effect, or "clone" of the Schumann PLL was also constructed. The effect was constructed for the purpose of subjective and mathematical analysis of the circuit behavior compared to the algorithm developed. This has proven to be necessary due to the limited recordings of this pedal in studio quality, as most of the demonstrations currently available are recorded at a poor quality.

### A.1 Power Section

The primary discrepancy between the digital implementation (with circuit analysis in the primary document) and the hardware construction of the pedal is the consideration for the power supply. In a digital construction simple DC voltage sources may be used, but a physical device must operate from one power source. Since the device requires  $\pm 11.85V$  bipolar power. This is efficiently done with an external AC power supply and an on-board AC to DC converter. The hardware effect requires a 12V AC power supply, and utilizes a full wave voltage doubler topology (stabilized with voltage regulators) to output the required bipolar DC voltage. The schematic for the configuration is seen in Appendix section B.3.

### A.2 PCB Design and Assembly

The hardware effect was designed and built with the components and circuit layout specified in appendix B. The printed circuit board was designed in KiCad with a 4 layer board, consisting of a top route layer, ground plane, split bipolar power plane, and bottom route layer. This design is more sophisticated than the original circuit board in the Schumann PLL, which used a two 2-layer layer boards with mixed power, ground,

## Appendix A. Hardware Implementation of the Schumann PLL

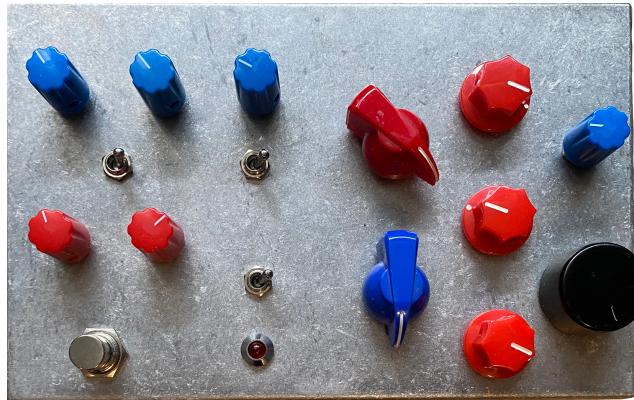


Figure A.1: Interface of the Schumann PLL clone

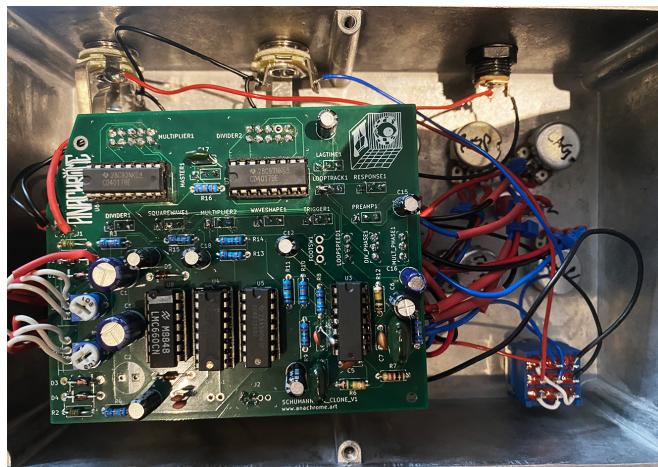


Figure A.2: PCB and potentiometer wiring of the Schumann PLL Clone

and signal routing. This 4 layer approach allows for more efficient layout design and power routing, with the ground plane providing better noise control compared to 2-layer designs, since every signal path will run over a ground plane, and every component has a short path to ground if needed. In guitar effects these considerations are not immediately consequential as they are typically low power and slow signal circuits (e.g. there is no possibility of antenna behavior), but it still constitutes best practice for circuit design.

All potentiometers, switches and rotaries were solder lug panel mount components, and required jumper wires from the controls to the board. This method, while the same as the original pedal, is fairly labor intensive, with the modern standard being board mounted components. This would be difficult to achieve with a single board due to differing component depths, with the rotary selectors protruding significantly deeper than the potentiometers in the enclosure. The board and controls were mounted in a Hammond 26827PSLA enclosure with  $188 \times 120 \times 57\text{mm}$  dimensions. Finally, the effect was powered with a  $240V\text{AC}$  to  $12V\text{AC}$  power supply.

## Appendix B

# Component Values and Full Schematics

### B.1 Analog Input Stage

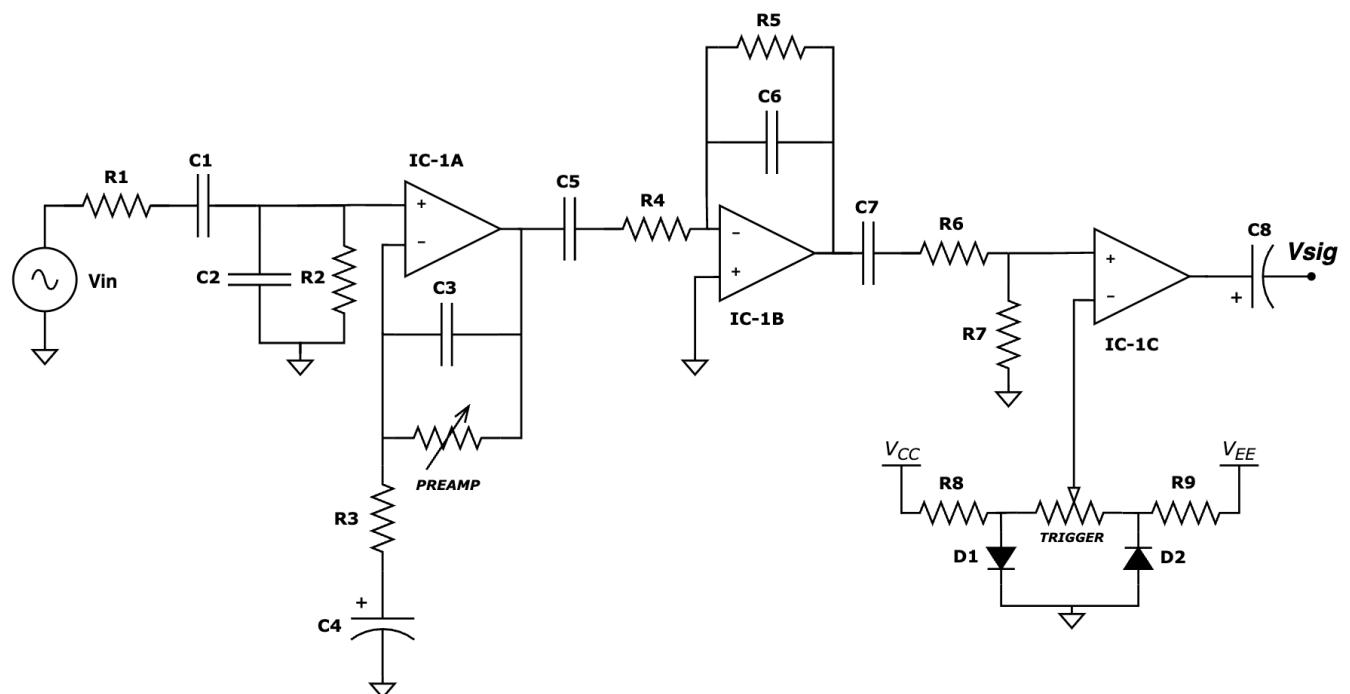


Figure B.1: Analog input stage schematic [2]

**Appendix B. Component Values and Full Schematics**

Table B.1: Component values for the analog input stage B.1

RESISTORS	CAPACITORS
R1 : 10kΩ	C1 : 10μF
R2 : 150kΩ	C2 : 10pF
R3 : 110Ω	C3 : 100pF
PREAMP : A10kΩ	C4 : 10μF
R4 : 200kΩ	C5 : 220nF
R5 : 1MΩ	C6 : 47pF
R6 : 10kΩ	C7 : 100nF
R7 : 100kΩ	C8 : 10μF
R8 : 10kΩ	
R9 : 10kΩ	
TRIGGER : B10kΩ	
INTEGRATED CIRCUITS	DIODES
IC-1 : TL074	D1 : 1N4001
	D2 : 1N4001

## B.2 Digital and Output Stage

Table B.2: Component values for the digital and output stages B.2

RESISTORS	CAPACITORS	INTEGRATED CIRCUITS
R10 : 150kΩ RESPONSE : B2MΩ LOOPTRACK : A500kΩ LAGTIME : B10kΩ DIVIDER : A100kΩ R11 : 1MΩ MULTIPLIER : A100kΩ R12 : 1MΩ SQUAREWAVE : A100kΩ R13 : 1MΩ R14 : 10kΩ WAVESHAPE : B250kΩ MASTER : A100kΩ	C9 : 20nF C10 : 470nF C11 : 2.2μF C12 : 33μF C13 : 10nF	IC-1 : TL074 IC-2 : 40106 IC-3 : 4046 IC-4 : 4017 IC-5 : 4017 IC-6 : LM660CN

**Appendix B. Component Values and Full Schematic**

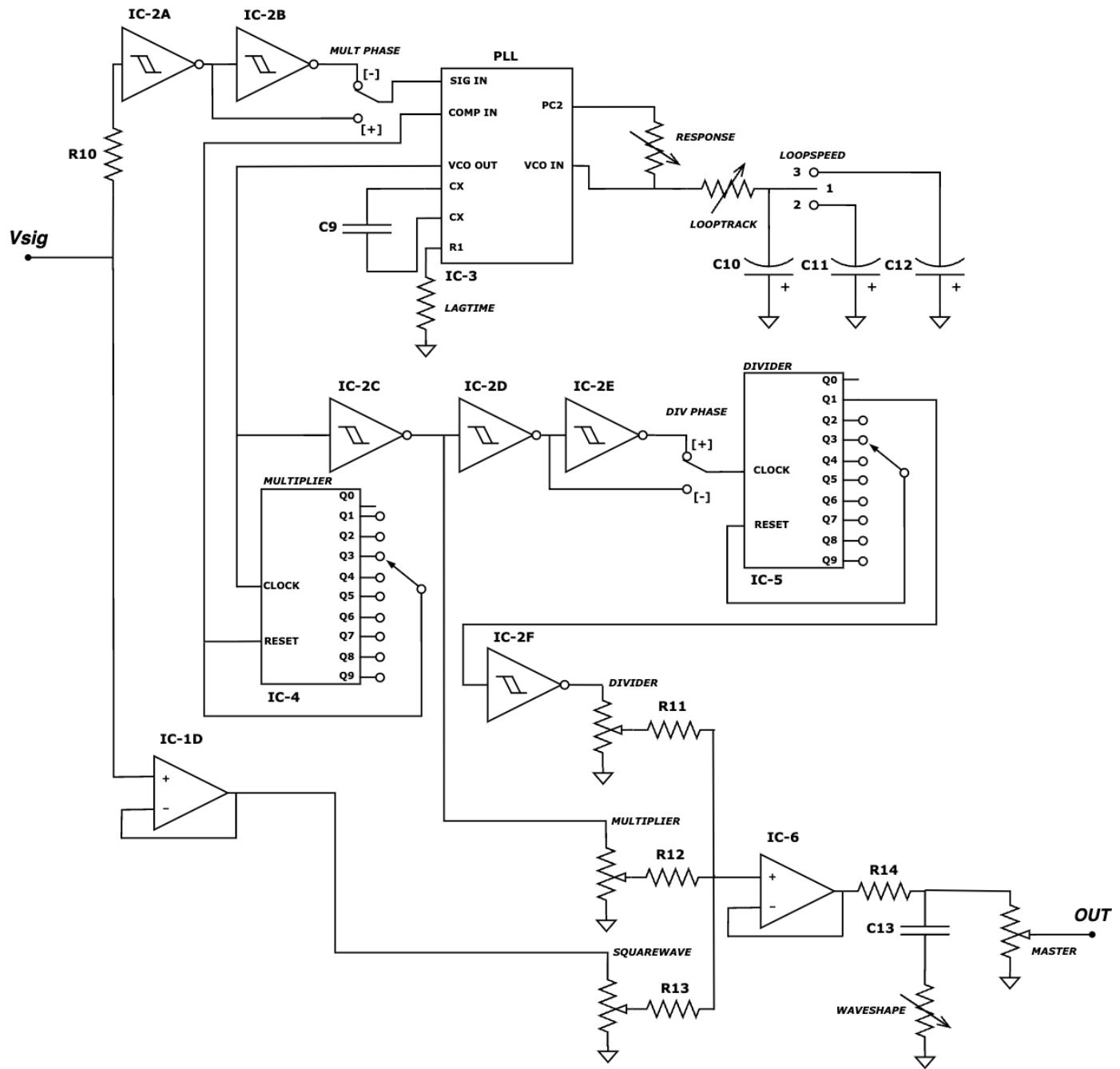


Figure B.2: Digital stage and analog output schematic [2]

### B.3 Power Stage

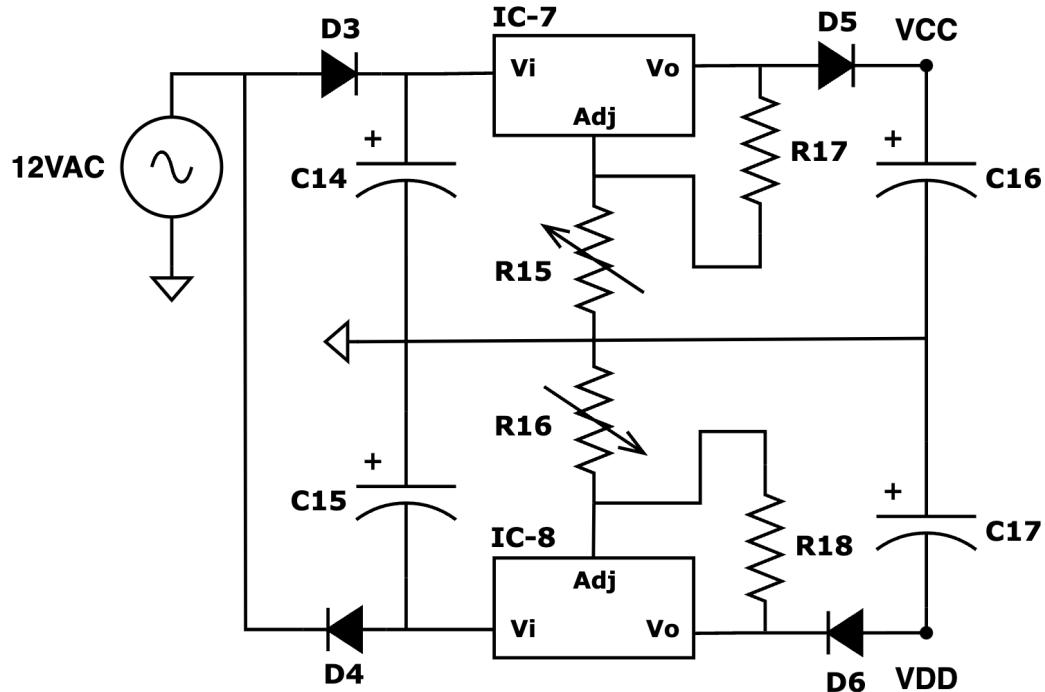


Figure B.3: Power stage schematic [2]

Table B.3: Component values for the power stage B.3

RESISTORS	CAPACITORS
R15 : B10kΩ R16 : B10kΩ R17 : 240Ω R18 : 120Ω	C14 : 470μF C15 : 470μF C16 : 10μF C17 : 10μF
INTEGRATED CIRCUITS	DIODES
IC-7 : 317T IC-8 : 337T	D3 : 1N4001 D4 : 1N4001 D5 : 1N4001 D6 : 1N4001



## Appendix C

# Final Project Proposal

### C.1 Background

The Schumann PLL (Phase Locked Loop) is an analog harmonizer. The pedal generates a square wave from an input signal, and uses decade counters to convert the pitch tracking from the PLL into a fixed pitch above and below the input signal pitch. The input signal can be supplied with any pitched instrument, including guitar or synthesizer, but functions best with monophonic input. This pedal was developed by John Schumann and released in 2003, but had limited production quantities which contribute to its rarity. This was one of the first guitar pedals to use phase locking to track the pitch of a guitar signal, solidifying its importance in guitar effect history and incentivizing digital implementation efforts.

### C.2 Project Aims

For this project I aim to create a functional digital reproduction of the 2003 Schumann PLL guitar effect, ideally suitable for real-time simulation. The digital reconstruction of the circuit topology will most likely consist of a combination of the K-method for simulating nonlinear analog circuits [21] and possibly other computational approaches to simulate the behavior of the more complex integrated circuits. I have identified key stages of the circuit below and through the course of its evaluation I will decide how they will be best implemented in the final algorithm. This approach opens up the possibility for interchangeable implementations and comparison to the analog circuit in later testing. If a robust virtual model of the circuit is able to be implemented, a VST plugin of the effect will be developed alongside the project.

## C.3 Proposed Methodology

The following sections develop important points of consideration in the development of the PLL guitar effect.

### C.3.1 Integrated Circuits

The Schumann PLL utilizes a number of integrated circuits that enable its functionality. The original line of pedals had portions of their primary circuit board covered in black epoxy, known as "gooped" in the pedal building community, which was an effort to protect the intellectual property of the circuit design (another notable gooped pedal is Bill Finnegan's Klon Centaur). Despite this, the PLL has been traced and ICs exposed. The circuit was notably traced in 2013 by user digi2t on diystompboxes.com [22].

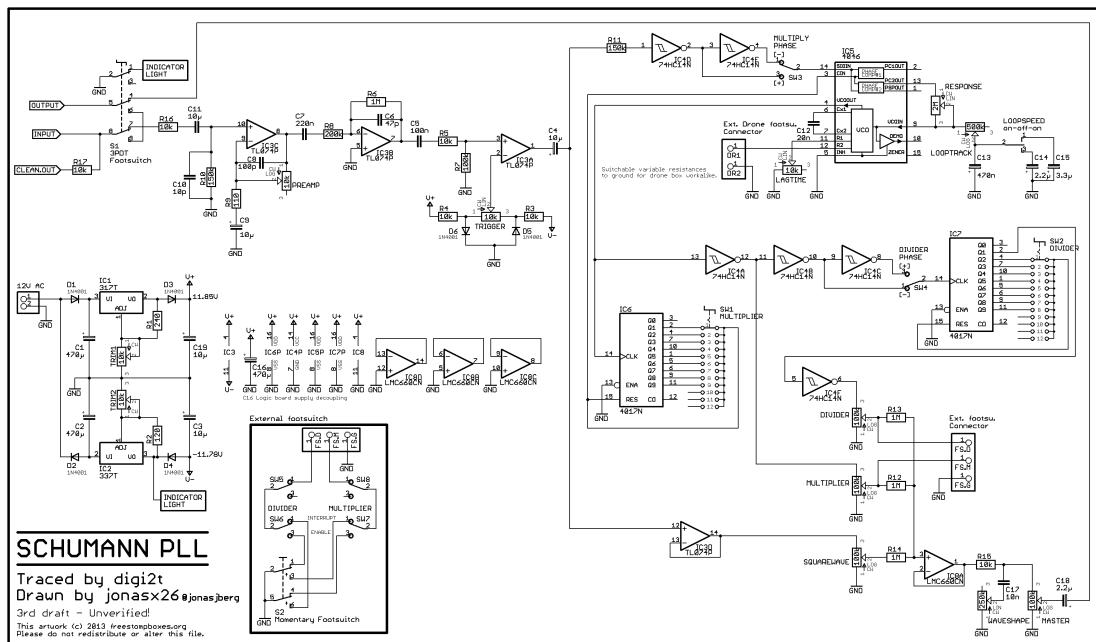


Figure C.1: PLL Schematic by digi2t and jonasx26 [2]

Notable integrated circuits in this design include the following.

1. TL074 quad op-amp [23]
2. 74HC14N hex inverters with Schmitt-trigger inputs [15]
3. 4046 CMOS Phase Lock Loop [3]
4. 4017N Decade Counters/Dividers [7]
5. LM660 quad op-amp [19]

Each of these fulfills a core function of the circuit, but each may be handled differently in the virtual implementation of the pedal, since some of the ICs are possibly too complex to model efficiently (or unnecessary to model at a component level all-together).

### C.3.2 Circuit Topology

The following constitutes a brief breakdown of the effect, analyzing purposes in the pedals topology and possible approaches to simulation.

#### Signal Conditioning

The input section of the circuit utilizes the TL074 op-amp [23] and features input amplification and significant filtering, and feeds into the phase lock loop. This is the stage responsible for generating a square wave from the instrument input. For this stage it seems that K-method virtual analog approaches will be the most appropriate, especially due to the processing on the third op-amp stage.

#### Phase Locking

The second stage of the circuit is phase locking, this takes the square wave from the input signal and outputs a clock signal to be used in the overtone and subharmonic generation. This stage features some user defined variables, but will most likely be implemented with a digital approach to phase locking [24] as opposed to an attempt at a virtual analog model of the CMOS circuit.

#### Schmitt Trigger Inverters

Schmitt-trigger hex inverters [15] are seen throughout the pedal, and are the breadth of the square wave generation in the pedal. They are simply signal inverters that trigger at a designated voltage. The implementation of this part needs further investigation into the stability of the internal circuit and its stability/accuracy in relation to the output of the pedal. A virtual analog approach could be computationally heavy, but a purely logic based approach could degrade the intended sound of the pedal.

#### Secondary Frequency Generation

The overtone and subharmonic are generated from the clock output of the phase locking fed into the 4017N Decade Counter chip [7]. This chip is coupled with a user controlled rotary switch to select the multiplication/division factor of the clock signal from the fundamental, these generated clocks are then passed to the hex inverter for square wave generation.

## **Power Supply**

The power supply section of this pedal is one of the notable elements in its construction, as it needs to convert  $12VAC$  input to  $\pm 12VDC$  rails, but this segment can presumably be ignored in the virtual implementation. If, during further analysis of the circuit, this stage produces notable fluctuation that would cause irregularity in the ICs there may be further worthwhile analysis, but there are no plans at this stage to simulate the power input.

### **C.3.3 Real-time Modelling**

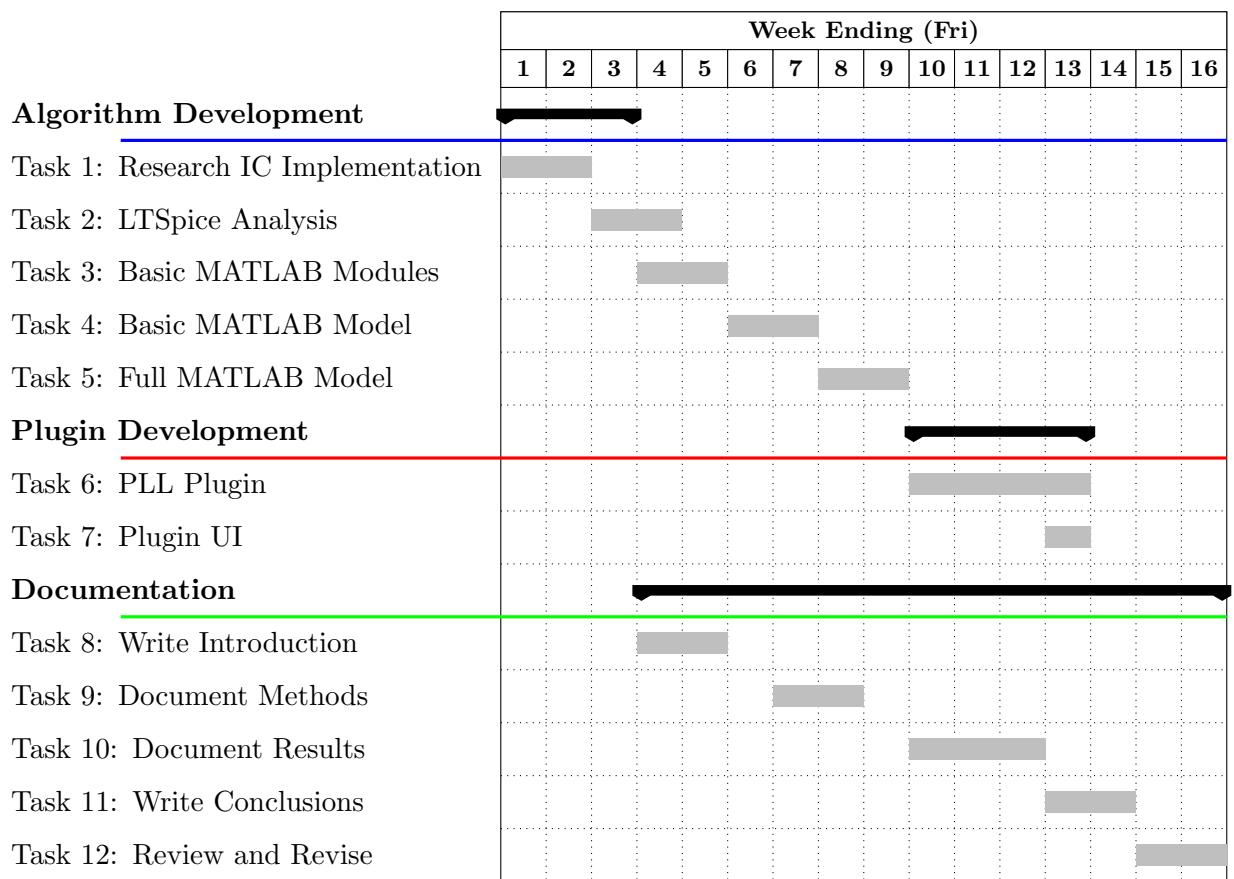
With a robust working model in MATLAB, the final effort is to bring the effect into a VST plugin using the JUCE framework for C++. A user interface will be created with parameters identical to the hardware. The implementation may also include the external foot switches for the PLL developed by Schumann, since these are mostly a matter of signal routing and not new simulation.

## **C.4 Timeline**

### **C.4.1 Milestones**

- Finalized approach/theory for ICs
- Basic MATLAB models for circuit sections
- Basic MATLAB model for full circuit
- Full MATLAB model with functional user inputs and foot switching sections
- First plugin iteration
- Stable plugin with improved UI
- Draft of dissertation
- Final Dissertation

### C.4.2 Gantt Chart





# Bibliography

- [1] [Online]. Available: <https://schumannelectronics.com/pll.html>
- [2] digi2t and jonasx26, *Schumann PLL Schematic*, 2013. [Online]. Available: <https://www.freestompboxes.org/download/file.php?id=21384&mode=view>
- [3] *74VHC4046 CMOS Phase Lock Loop*, Fairchild Semiconductors, 4 1999.
- [4] B. Horowitz and W. Hill, *Art of Electronics*. Cambridge University Press, 1980.
- [5] *CD40106B CMOS Hex Schmitt-Trigger Inverters*, Texas Instruments, 1998.
- [6] W. M. Austin, “Cmos phase-locked-loop applications using the cd54/74hc/hct4046a and cd54/74hc/hct7046a,” 2002.
- [7] *SN74HC4017N Decade Counters/Dividers*, Texas Instruments, 6 1989.
- [8] T. Wilmering, D. Moffat, A. Milo, and M. B. Sandler, “A history of audio effects,” *Applied Sciences*, vol. 10, no. 3, 2020. [Online]. Available: <https://www.mdpi.com/2076-3417/10/3/791>
- [9] C. Anderton, *Electronic Projects For Musicians*. AMSCO Music, 1975.
- [10] K. L. Smith, “Bringing new sounds to rock “n” roll,” Feb 2022. [Online]. Available: <https://www.nysun.com/article/on-the-town-bringing-new-sounds-to-rock-n-roll>
- [11] Jul 2003. [Online]. Available: <https://gearspace.com/board/so-much-gear-so-little-time/5302-radiohead-effect-what.html>
- [12] D. Landes, “John schumann: Behind the gear with schumann electronics,” Sep 2004. [Online]. Available: <https://tapeop.com/interviews/btg/43/john-schumann/>
- [13] [Online]. Available: <https://reverb.com/marketplace?query=Schumann+PLL>
- [14] *CMOS Integrated Circuits Databook*, RCA, 1983.
- [15] *SNx4HC14 Hex Inverters with Schmitt-Trigger Inputs*, Texas Instruments, 2021.
- [16] V. A. Pedroni, *Finite state machines in hardware: Theory and design (with VHDL and SystemVerilog)*. The MIT Press, 2013.
- [17] T. Kailath, *Linear Systems*. Prentice-Hall, 1980.
- [18] J. O. Smith., *Introduction to Physical Signal Models*. Center for Computer Research in Music and Acoustics, 2020.
- [19] *LM660 CMOS Quad Operational Amplifier*, Texas Instruments, 2013.
- [20] R. G. Lyons, *Understanding Digital Signal Processing*. Pearson Education Inc., 2013.
- [21] D. T. Yeh, J. S. Abel, and J. O. Smith, “Automated physical modeling of nonlinear audio circuits for real-time audio effects—part I: Theoretical development,” *IEEE Transactions on Audio, Speech, and Language Processing*, vol. 18, no. 4, p. 728–737, 2010.

## BIBLIOGRAPHY

- [22] digi2t, “Schumann pll,” Mar 2013. [Online]. Available: <https://www.diystompboxes.com/smfforum/index.php?topic=102012.0>
- [23] *Tl074 Low-Noise JFET-Input Operational Amplifier*, Texas Instruments, 12 2012.
- [24] B. Razavi, *Design of Analog CMOS Integrated Circuits*. McGraw-Hill, 2001.