Mo Ijhar

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SUMMARY

Final-year B.Tech student in Electronics and Communication Engineering with strong communication skills, leadership experience, and a passion for technology. Quick learner with a positive attitude and proven ability to work hard and adapt. Volunteer in Deepotsav 2022 and 2023 at Ram ki Paidi, Ayodhya

EDUCATION

B.tech: Dr. Ram Manohar Lohia Avadh University, Ayodhya (Expected 2025).

Intermediate: Passed from U.P. Board, Prayagraj (2020).

High School: Passed from U.P. Board, Prayagraj (2018).

WORK EXPERIENCE

- Developed RTL in Verilog/VHDL for custom IPs, optimized for synthesis and efficient FPGA utilization.
- Performed synthesis, place & route, and bitstream generation in Vivado/ISE/Quartus.
- Documented full FPGA design flow from specs to board testing, ensuring design reusability.

AHA! Solar Ltd - SURYA Gujarat — Intern (Oct. 2022)

SKILLS

Technical Skills	HTML, CSS,JS, Python, .
Soft Skills	Potential to achieve team-goal, Problem Solving, Teamwork, Collaboration.
Software Skills	FPGA System Design, HDL,Verilog, VHDL, FPGA Vendor Toolchains, MATLAB.

PROJECTS

Smart Blind Stick for Visually Impaired.

- Integrated **Ultrasonic Sensor** for obstacle detection (range: up to ~2 meters).
- **Vibration motor** feedback system for tactile alerts.
- Used **ESP32/Arduino UNO** as the main controller.
- Powered by a **rechargeable Li-ion battery** system.
- Optional feature: Added **buzzer or voice alerts** (if you did this, mention it).

Advance Electronic Machine.

- Used Arduino UNO as the main controller to manage vote inputs and display results.
- Connected push buttons for each candidate and interfaced a 16x2 LCD for output.
- Wrote embedded C code to store, count, and display votes securely.
- Assembled the circuit on a breadboard using resistors, buttons, and jumper wires.
  Tested the system by simulating multiple votes and displaying real-time results

Sign Calculator.

- Implemented Sign Calculator in Verilog using basic logic gates to determine sign of operations.
- Simulated AND, OR, NOT, XOR gate logic for fast and accurate sign evaluation.
- Gained hands-on experience in HDL coding, logic synthesis, and FPGA-based digital design flow.