

The schematic diagram illustrates a 16-bit parallel adder implemented using a hierarchical structure of 1-bit full adders. The inputs are two 16-bit numbers, G[0:15] and G[2:17], which are connected to the inputs of the adders. The carry-in is 0, and the carry-out is P[15]. The adders are organized into a tree structure, with 1-bit adders at the bottom, 2-bit adders in the middle, and 4-bit, 8-bit, and 16-bit adders at the top. The final output is the 16-bit sum P[0:15].

[illegible]