

The timing diagram for the 74VHC00 (NAND gate) shows the following signals and their relationships:

- Inputs:**
 - `NET_VCNTR_Dn` (green line)
 - `NET_VCNTR_D` (green line)
 - `NET_VCNTR_X` (green line)
 - `NET_VCNTR_0` (green line)
- Outputs:**
 - `PAD_VSTNC_OUT` (green line)
 - `PAD_VBLANKn_OUT` (green line)
 - `PAD_VBLANK_OUT` (green line)
 - `NET_VBLANK_0` (green line)
 - `NET_VBLANK_1` (green line)
 - `NET_256V` (green line)
 - `NET_256V` (green line)
- Logic Function:** The circuit implements a NAND gate with inputs `NET_VCNTR_Dn` and `NET_VCNTR_D`. The output is `PAD_VSTNC_OUT`.
- Timing Parameters:**
 - `D14`: Delay from `NET_VCNTR_Dn` to `PAD_VSTNC_OUT`.
 - `D13`: Delay from `NET_VCNTR_D` to `PAD_VSTNC_OUT`.
 - `F24`: Delay from `NET_VCNTR_Dn` to `PAD_VBLANKn_OUT`.
 - `G13`: Delay from `NET_VCNTR_D` to `PAD_VBLANKn_OUT`.
 - `G14`: Delay from `NET_VCNTR_Dn` to `PAD_VBLANK_OUT`.
 - `C20`: Delay from `NET_VCNTR_D` to `NET_VBLANK_0`.
 - `D15`: Delay from `NET_VCNTR_D` to `NET_VBLANK_1`.

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The diagram illustrates a 16-bit parallel adder implemented using 74181 ALUs and 74160 counters. The circuit is organized into four stages, each processing a 4-bit segment of the 16-bit operands.

- Inputs:**
 - NET_MCLK** and **PAD_VCNTR.IN** are connected to a 74160 counter (labeled 130) to provide a clock signal (**CLK_VCNTR**) to all 74181 ALUs.
 - PAD_OB1TICK.IN** is connected to a 74160 counter (labeled 231) to provide a clock signal (**CLK_OB1TICK**) to all 74181 ALUs.
 - PAD_DRX.IN** is connected to a 74160 counter (labeled 230) to provide a clock signal (**CLK_OB2TICK**) to all 74181 ALUs.
 - PAD_OB1RST.IN** and **PAD_OB2RST.IN** are connected to the reset inputs of the 74160 counters.
- 74181 ALUs:**
 - There are 16 ALUs in total, arranged in four groups of four.
 - Each ALU has two 4-bit data inputs (**A** and **B**), a 4-bit carry input (**CIN**), and a 4-bit carry output (**COUT**).
 - The ALUs are configured to perform addition using the carry chain.
- 74160 Counters:**
 - There are four 74160 counters, each with a 4-bit data output (**Q0**, **Q1**, **Q2**, **Q3**).
 - The counters are used to generate the carry signals for the ALUs.
 - The carry signals are connected to the **CIN** inputs of the ALUs in a chain.
- Outputs:**
 - The final 16-bit sum is output from the **Q0**, **Q1**, **Q2**, and **Q3** outputs of the 74160 counters.

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Diagram illustrating the internal logic and output connections of the **NET.HCNTNTR** (Network Counter) block, showing two main sections: **NET.HCNTNTR-D0** to **NET.HCNTNTR-D7** and **NET.VCNTNTR-D0** to **NET.VCNTNTR-D7**.

NET.HCNTNTR Section:

- Inputs:** PAD.HF.LP.IN (inverted), PAD.VFLIP.IN (inverted), and PAD.255 (inverted).
- Logic:** The inputs are connected to a series of 8-bit counters (D0-D7) via a bus structure. The outputs of these counters are connected to a series of 8-bit multiplexers (MUX) and 8-bit comparators (CMP).
- Outputs:** The outputs of the MUX and CMP blocks are connected to the following pads:
 - PAD.2H*.OUT
 - PAD.4H*.OUT
 - PAD.8H*.OUT
 - PAD.16H*.OUT
 - PAD.32H*.OUT
 - PAD.64H*.OUT
 - PAD.8H*.OUT
 - PAD.128H*.OUT

NET.VCNTNTR Section:

- Inputs:** PAD.VFLIP.IN (inverted), PAD.A54 (inverted), and PAD.255 (inverted).
- Logic:** The inputs are connected to a series of 8-bit counters (D0-D7) via a bus structure. The outputs of these counters are connected to a series of 8-bit multiplexers (MUX) and 8-bit comparators (CMP).
- Outputs:** The outputs of the MUX and CMP blocks are connected to the following pads:
 - PAD.1V*.OUT
 - PAD.2V*.OUT
 - PAD.4V*.OUT
 - PAD.8V*.OUT
 - PAD.16V*.OUT
 - PAD.32V*.OUT
 - PAD.64V*.OUT
 - PAD.128V*.OUT

The diagram shows the internal logic and output connections of the **NET.HCNTNTR** and **NET.VCNTNTR** blocks, including the input pads, internal logic (counters, multiplexers, comparators), and the output pads.