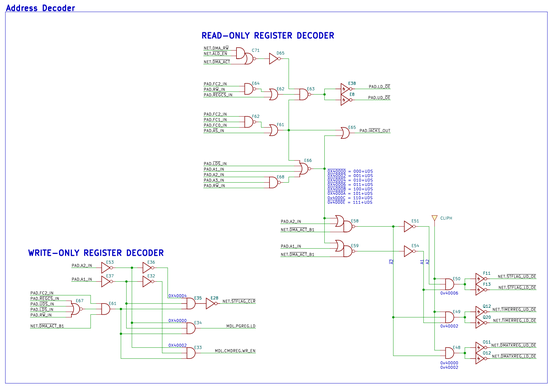
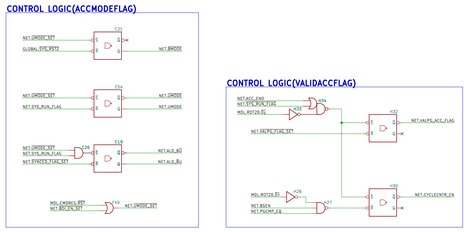
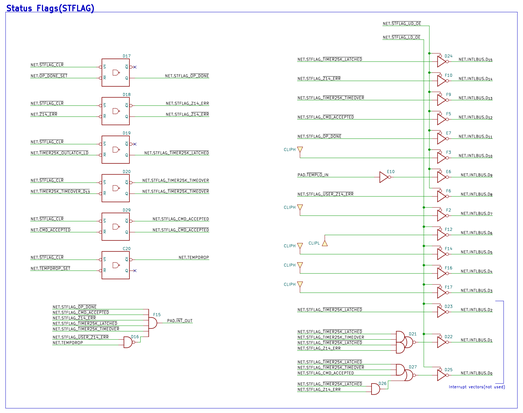
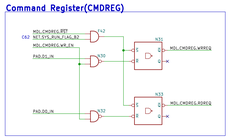
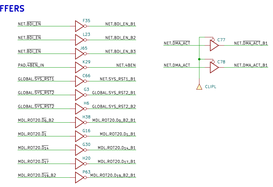


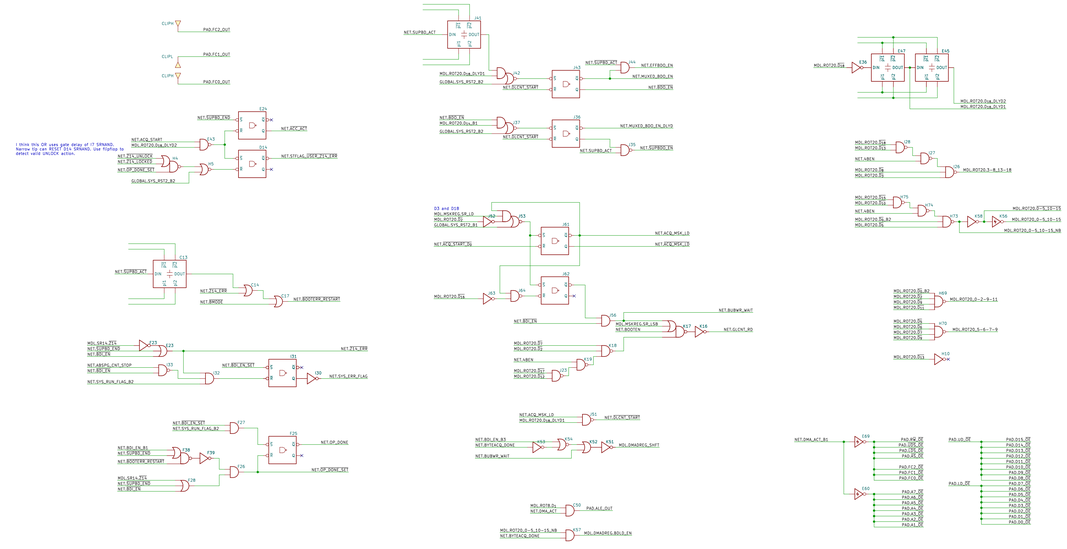






BD_EN = Bubble Data Input Enable
BMOD = Bootloader MODE
CMD_ACT = Command Active
DMA_ACT = DMA Active
STLAG = Status Latch
BDLAG = Bubble Latch Data Enable
ALD_BD = Address Latch Data Bootloader (DAT page
CLCNT = Synchronization Pattern Detector Count)

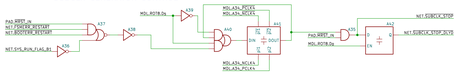




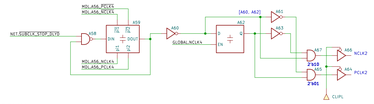
2024 Sehyeon Kim(Raki)
All unnamed clock nodes are 2MHz
Konami 005296/005297 Bubble Memory Controller
IKA Microelectronics Inc.
Sheet 1/1
File: 005297.kicad_sch
Title: 005296/005297
Size: A2 | Date: 2024-11-08 | **Rev: v1.1**
KiCad (3.A. eeschema 7.0.6) | Id: 1/4

Supervisor

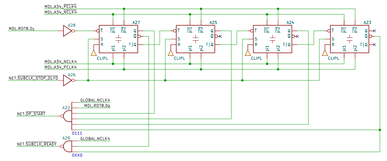
SUBCLK GENERATOR CONTROL



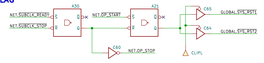
SUBCLK GENERATOR



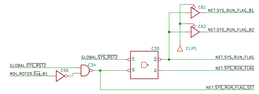
POR DELAY



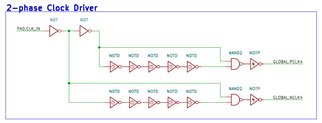
OPERATION START FLAG



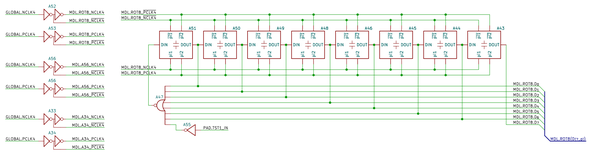
SYSTEM RUN FLAG



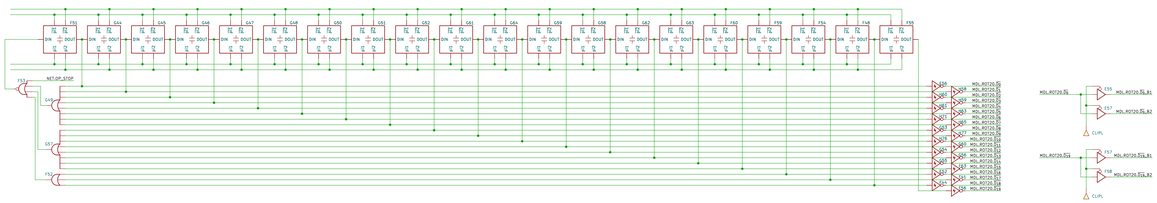
2-phase Clock Driver



8bit Ring Counter(ROT8)



20bit Ring Counter(ROT20)

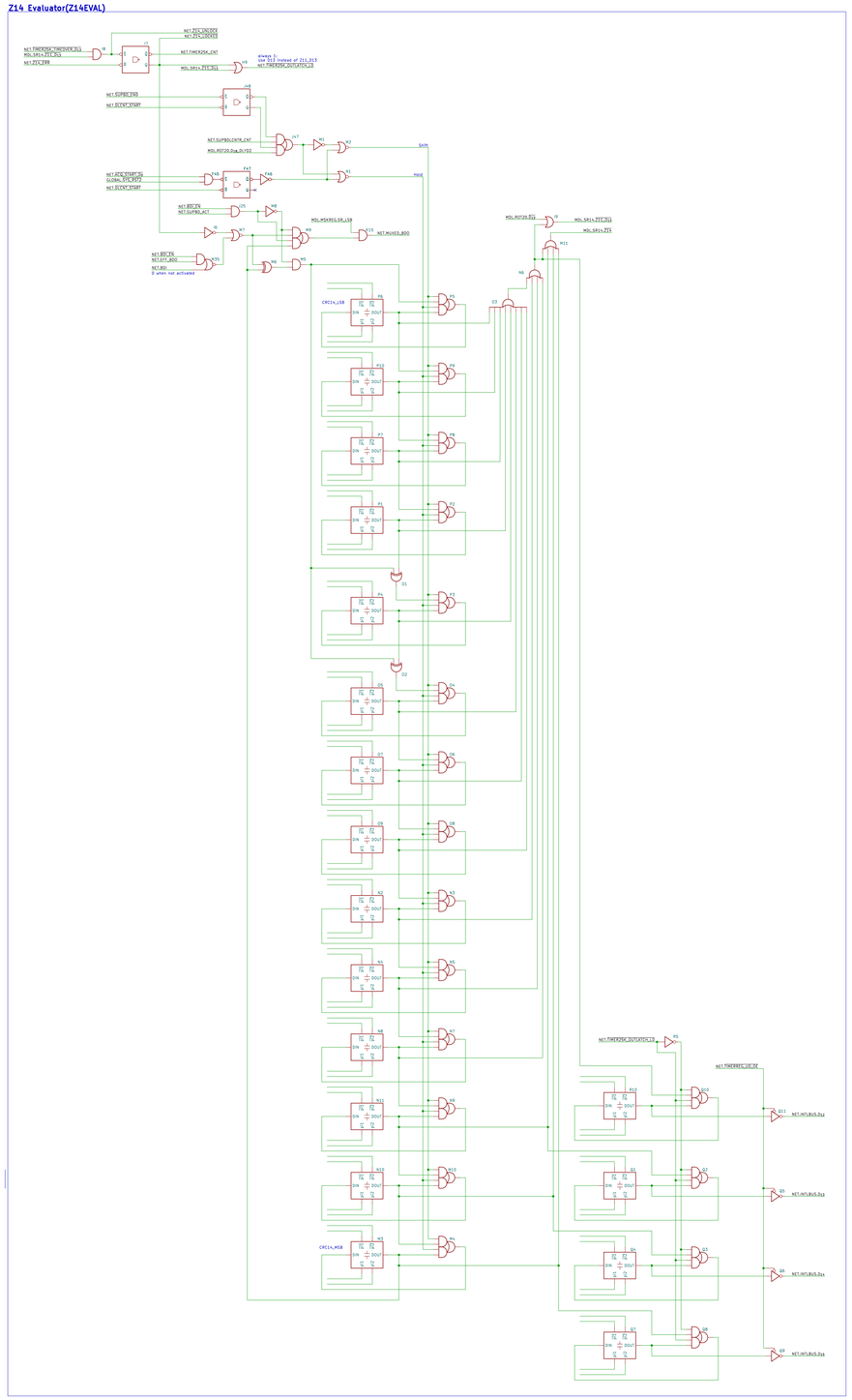


2024 Sahyeon Kim(Ravi)
All unnamed clock nodes are 2MHz
Konami 005298/005297 Bubble Memory Controller
IKA Microelectronics Inc.
Sheet: /K005297_2mhzpa/
File: K005297_2mhzpa.sch

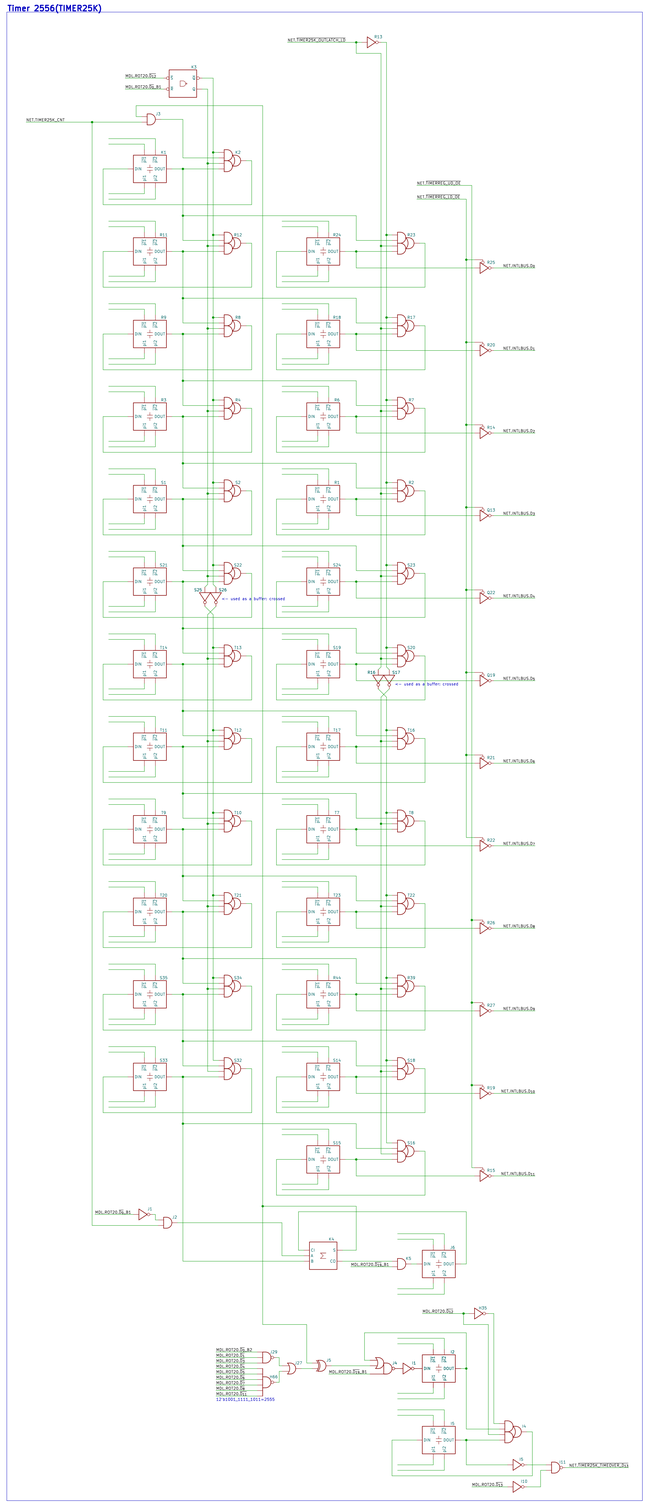
Title: 005296/005297

Size: A0	Date: 2024-11-08	Rev: v1.1
KiCad 8.0.4	eeschema 7.0.0	Id: 2/9

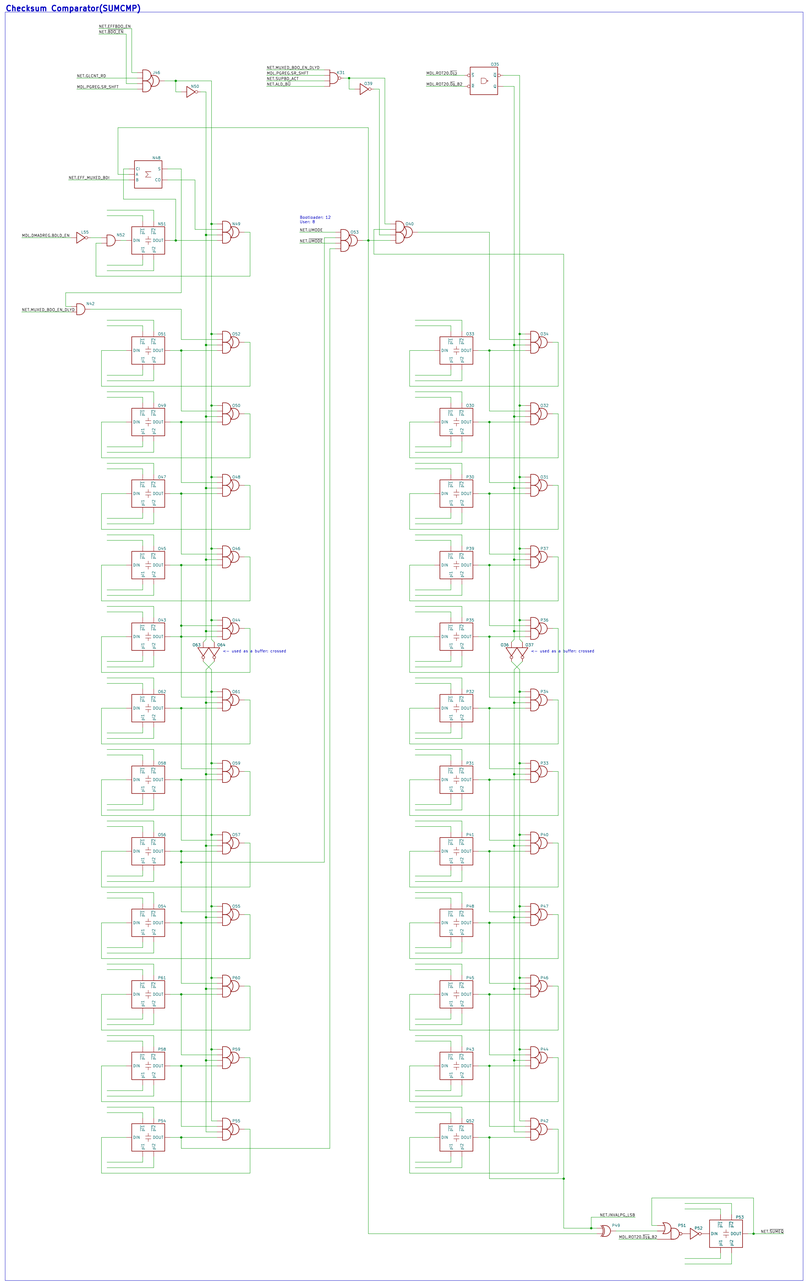
Z14 Evaluator(Z14EVAL)



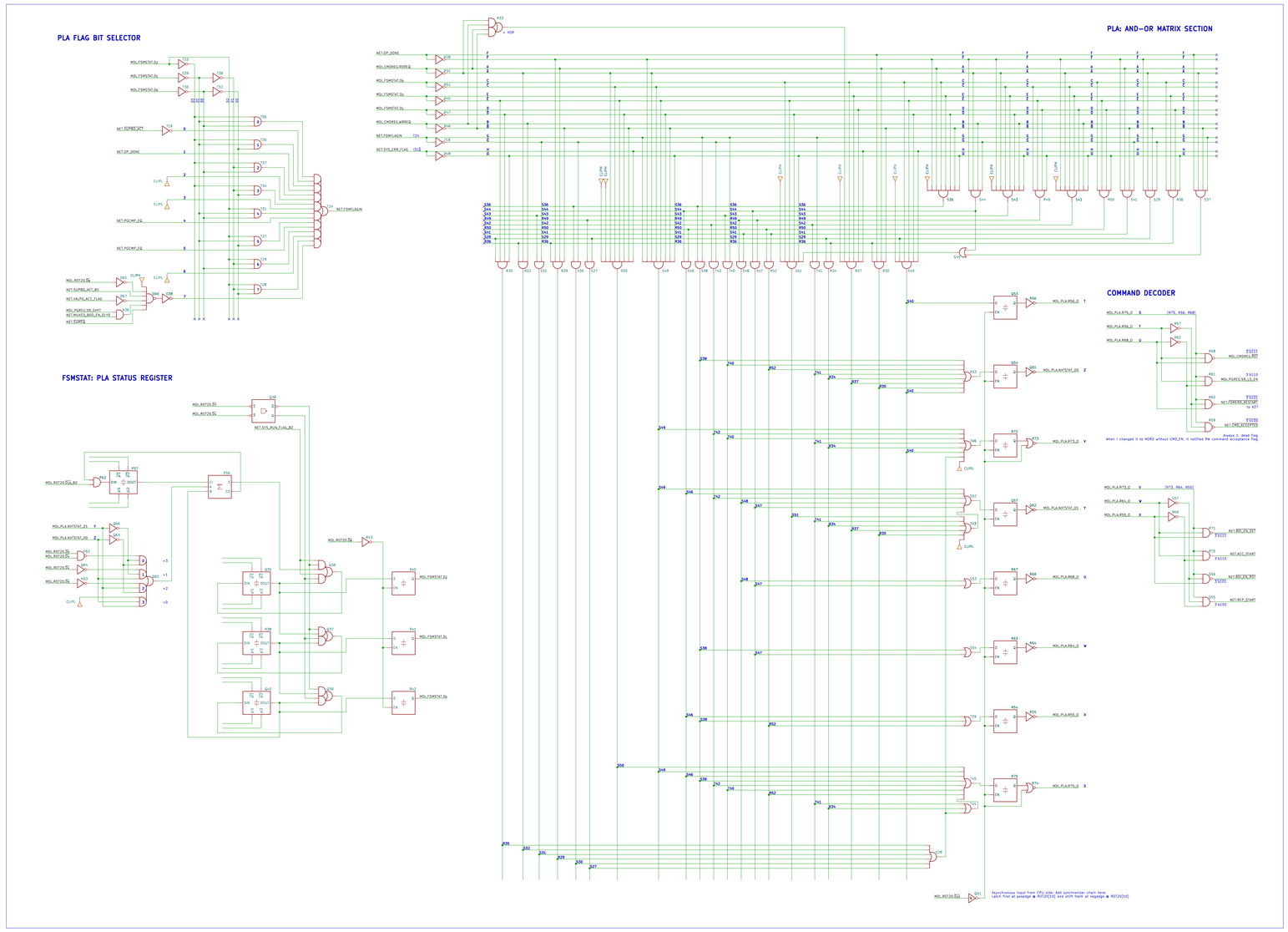
Timer 2556(TIMER25K)



Checksum Comparator(SUMCMP)



2024 Sahyeon Kim(Ra4)
All unnamed clock nodes are 2MHz
Konami 005296/005297 Bubble Memory Controller
IKA Microelectronics Inc.
Sheet: /4005297.security/
File: 4005297.security.kicad_sch
Title: 005296/005297
Size: A2 | Date: 2024-11-08 | Rev: v1.1
KiCad 7.0.A , eeschema 7.0.0 | Id: 5/9

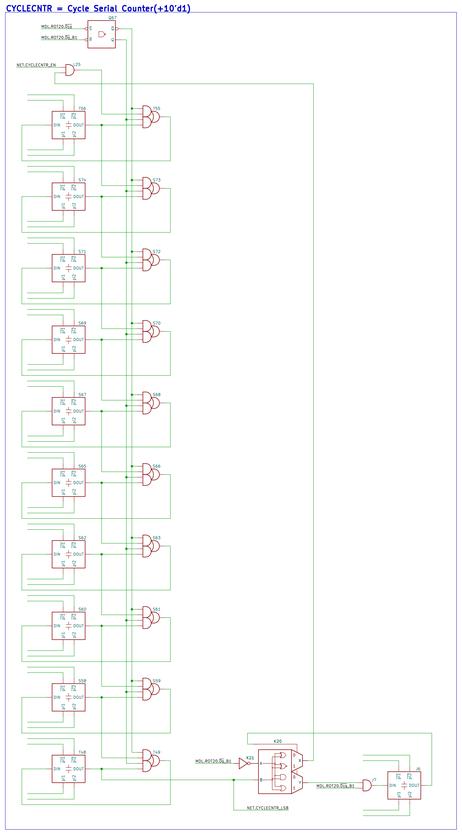


2024 Sehyeon Kim(Raki)
All unnamed clock nodes are 2MHz
Konami 005298/005297 Bubble Memory Controller
IKA Microelectronics Inc.
Sheet: /K005297.pka/
File: K005297.pka.kicad_sch

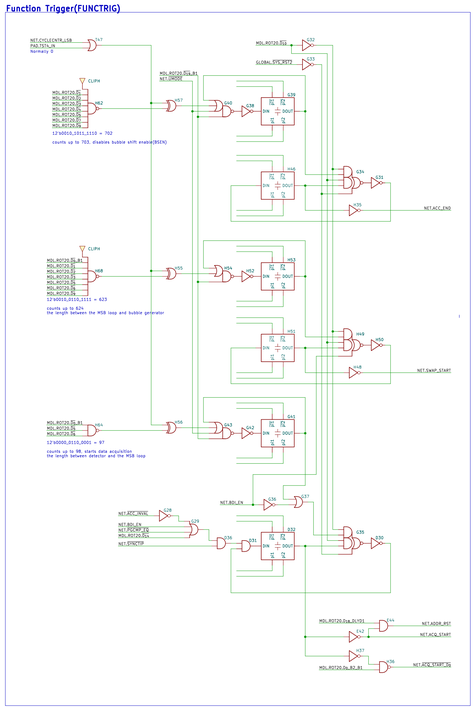
Title: 005298/005297

Size: A3	Date: 2025-11-08	**Rev: v1.1**
KiCad E.D.A. eeschema 7.0.6		Id: 4/8

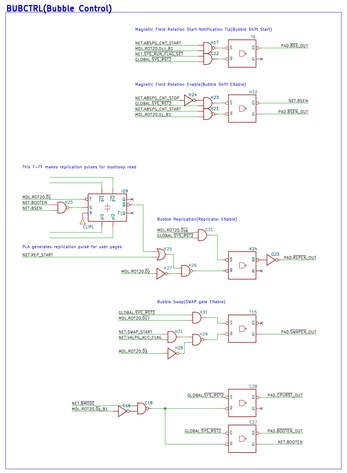
CYCLECNTR = Cycle Serial Counter(+10'd1)



Function Trigger(FUNCTRIG)



BUBCTRL(Bubble Control)



2024 Sehyeon Kim(Raiz)

All unnamed clock nodes are 2MHz

Konami 005298/005297 Bubble Memory Controller

KA Microelectronics Inc.

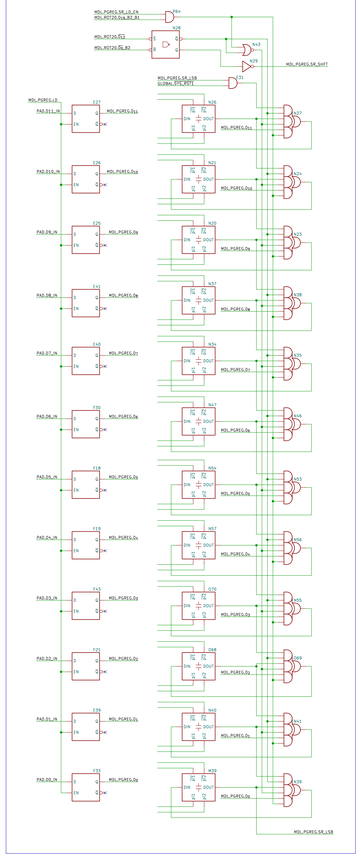
Sheet: /X005297_bubfunc/

File: K005297_bubfunc.kicad_sch

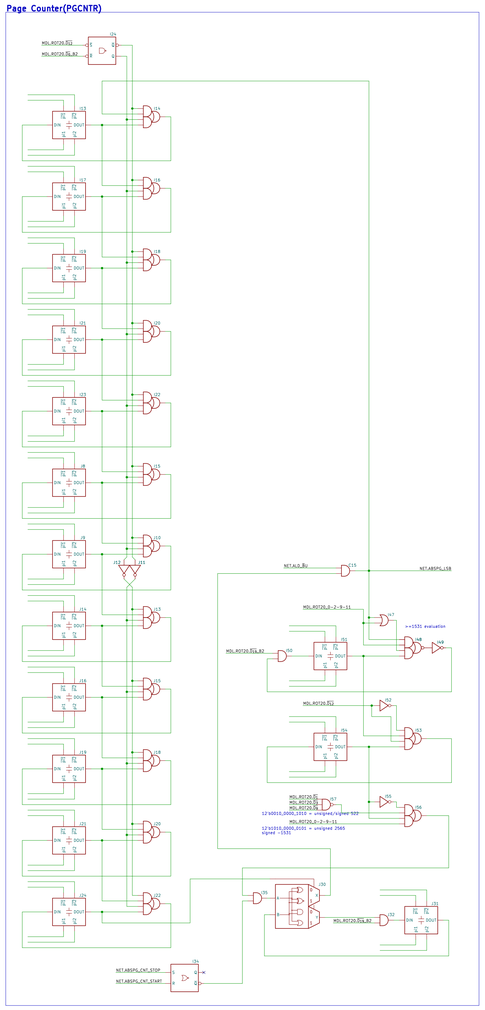
Title: 005296/005297

Size: A0 Date: 2025-11-08	Rev: v1.1
KiCad E.D.A. eeschema 7.0.6	Id: 5/8

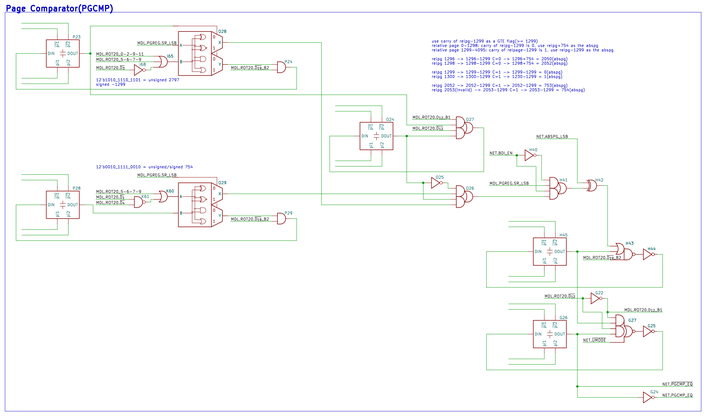
Page Number Register(PGREG)



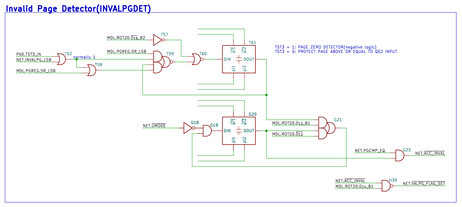
Page Counter(PGCNTR)



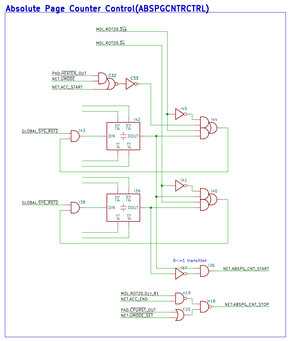
Page Comparator(PGCMP)



Invalid Page Detector(INVALPGDET)



Absolute Page Counter Control(ABSPGCNTRCTRL)



2024 Sahyeon Kim(Ryu)
All unmarked clock nodes are 2MHz
Konami 005296/005297 Bubble Memory Controller

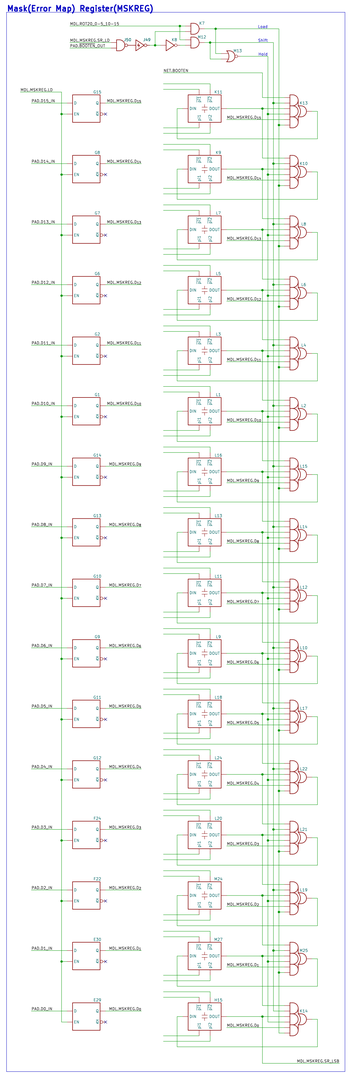
IKA Microelectronics Inc.

Sheet: /4005297.kicad_sch/
File: 4005297.kicad_sch.sch

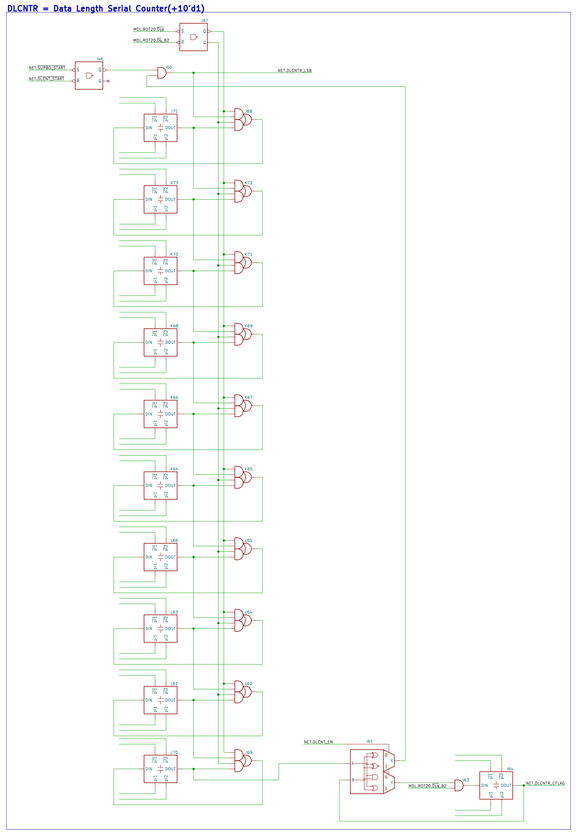
Title: 005296/005297

Size: A2	Date: 2024-11-08	Rev: v1.1
KiCad E.D.A. eeschema 7.0.0		Id: 6/8

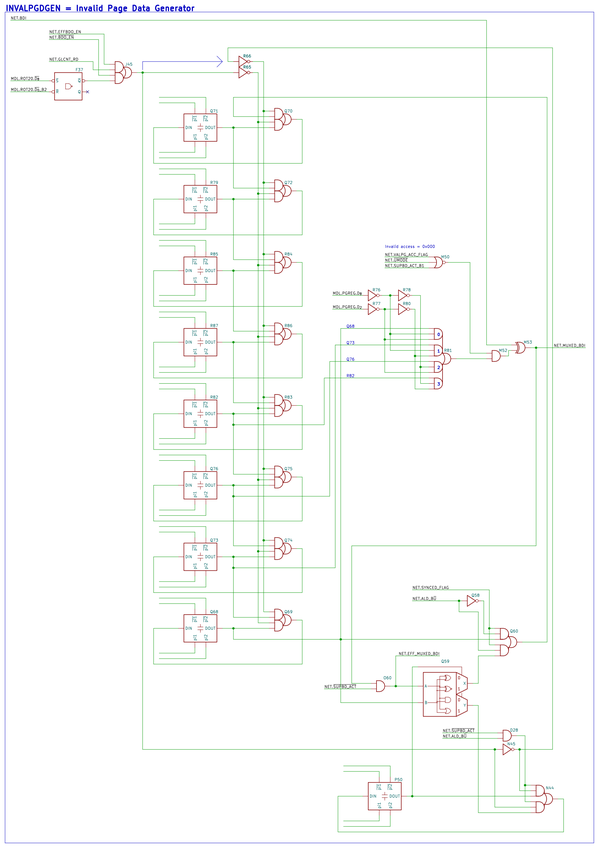
Mask(Error Map) Register(MSKREG)



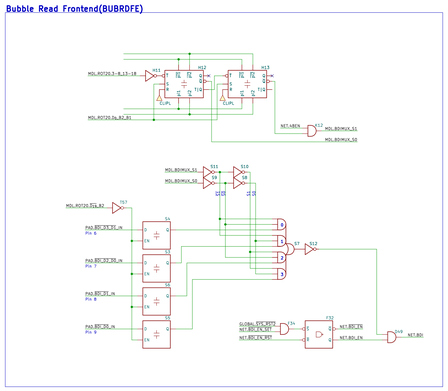
DLCNTR = Data Length Serial Counter(+10'd1)



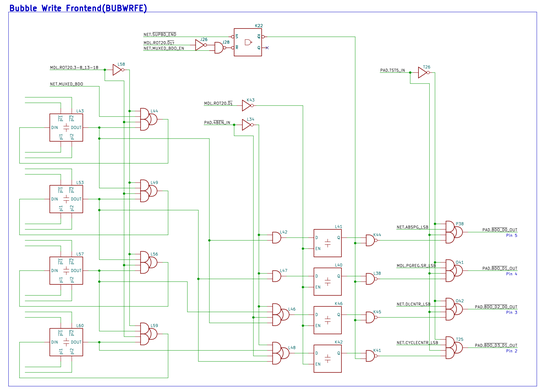
INVALPGDGEN = Invalid Page Data Generator



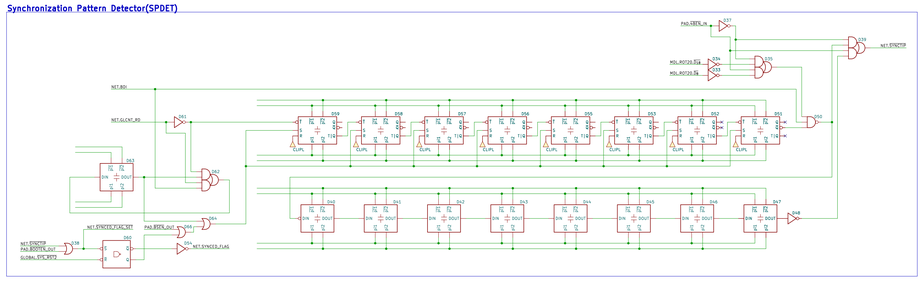
Bubble Read Frontend(BUBRDFE)



Bubble Write Frontend(BUBWRFE)

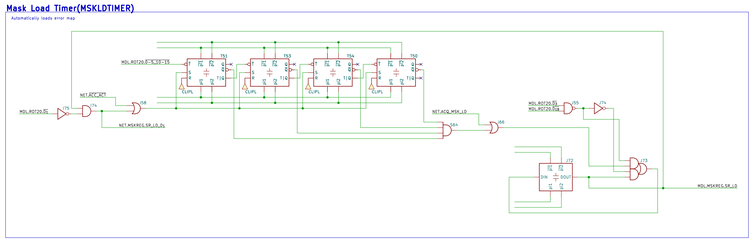


Synchronization Pattern Detector(SPDET)



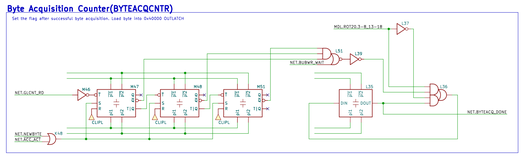
Mask Load Timer(MSKLDTIMER)

Automatically loads error map

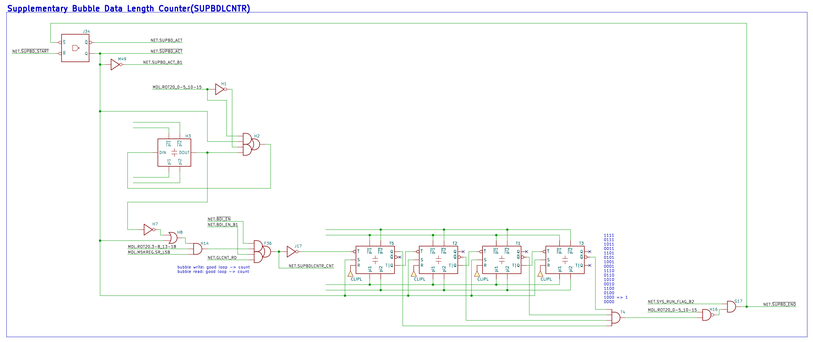


Byte Acquisition Counter(BYTEACQCNTR)

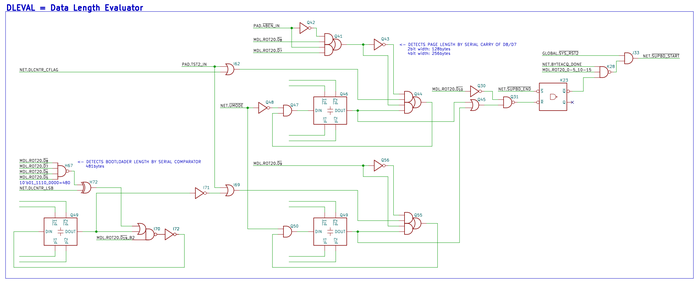
Set the flag after successful byte acquisition. Load byte into 0x00000 OUTLATCH



Supplementary Bubble Data Length Counter(SUPBDLCNTR)



DLEVAL = Data Length Evaluator

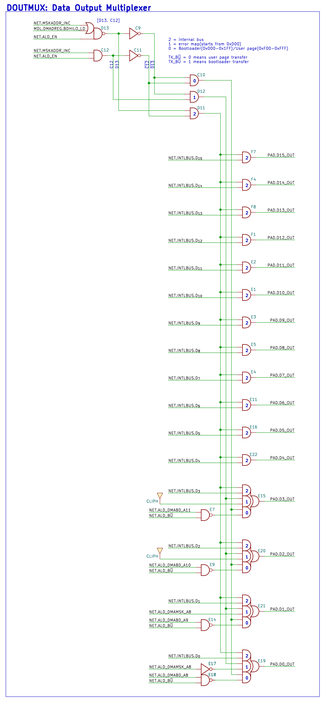


2024 Sehyeon Kim(Raki)
All unnamed clock nodes are 2MHz
Konami 005296/005297 Bubble Memory Controller
IKA Microelectronics Inc.
Sheet: /4005297_bubdata/
File: K005297_bubdata.kicad_sch

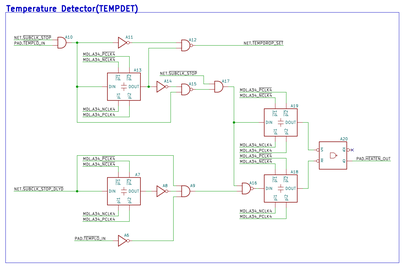
Title: 005296/005297

Size: A3	Date: 2024-11-08	Rev: v1.1
KiCad E.D.A. eeschema 7.0.6		Id: 7/8

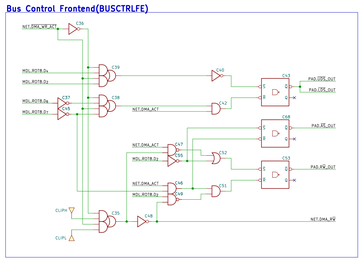
DOUTMUX: Data Output Multiplexer



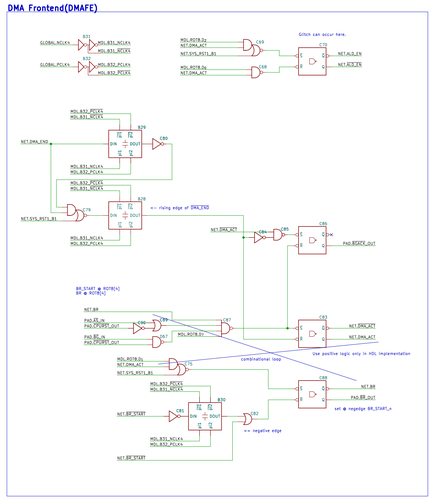
Temperature Detector(TEMPDET)



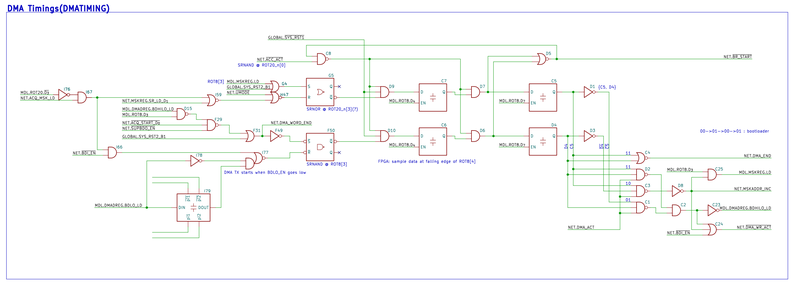
Bus Control Frontend(BUSCTRLFE)



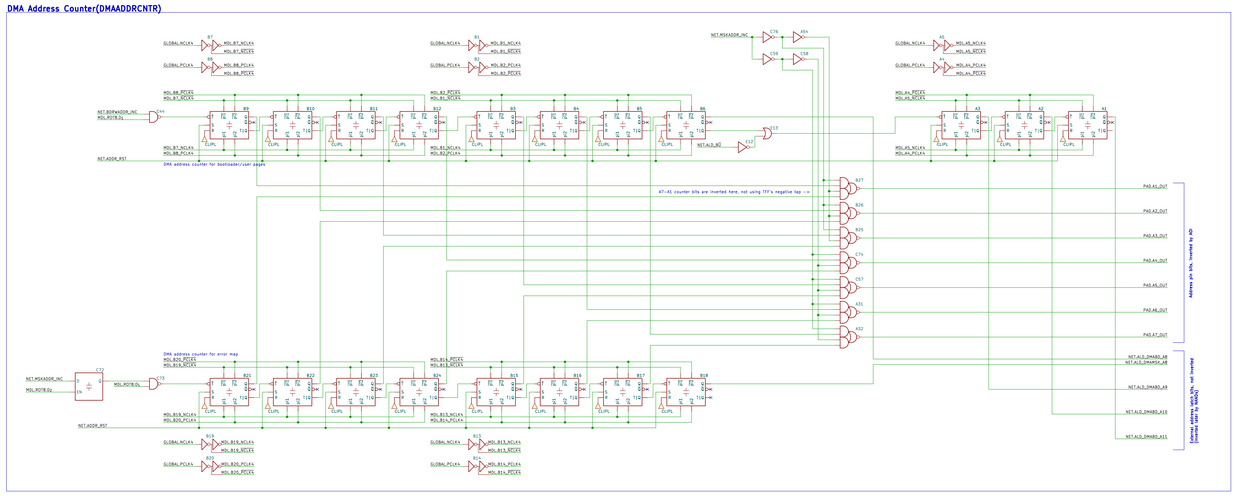
DMA Frontend(DMAFE)



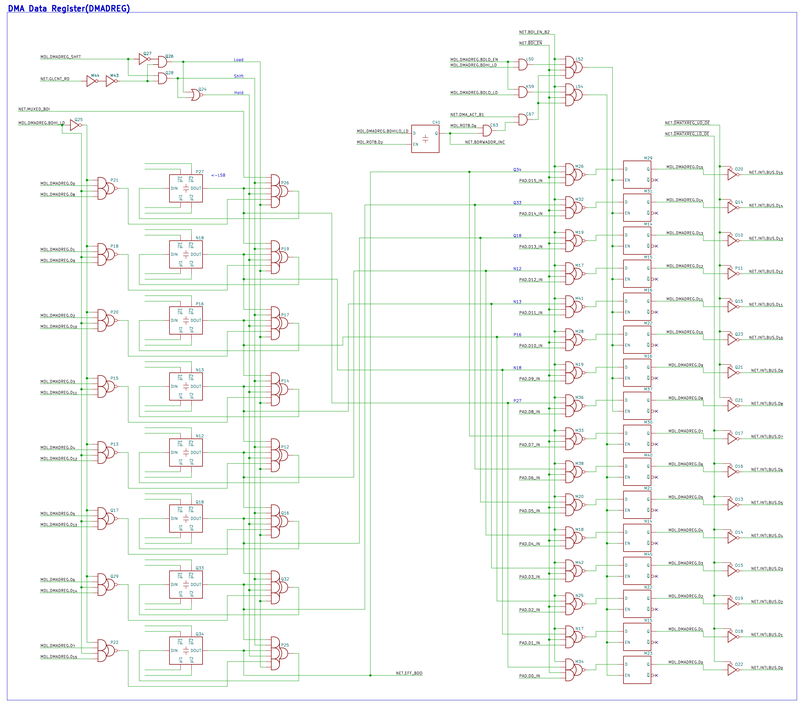
DMA Timings(DMATIMING)



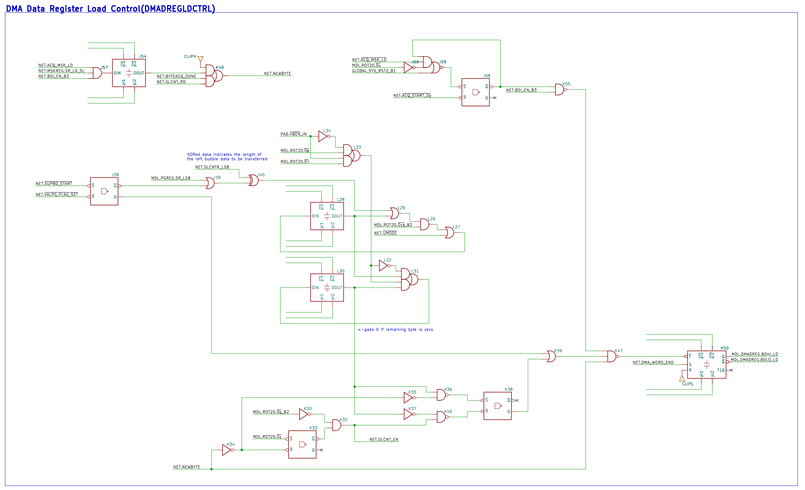
DMA Address Counter(DMAADDRCNTR)



DMA Data Register(DMADREG)



DMA Data Register Load Control(DMADREGLDCTRL)



2024 Sahyeon Kim(Ravi)
All unnamed clock nodes are 2MHz
Kasahi (005296/005297 Bubble Memory Controller
IBM Microelectronics Inc.
Sheet: DMA Frontend
File: K005297_DmaAdad.sch

Title: 005296/005297

Size: A2	Date: 2025-11-08	**Rev: v1.1**
KiCad 7.0.4, eeschema 7.0.6		Id: 6/6