TOSHIBA

ASIC
DESIGN
MANUAL

CMOS ASIC Design Manual

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CMOS ASIC Design Manual

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Preface

This manual is for designers of Toshiba's Application-Specific Integrated Circuits (ASICs). It introduces Toshiba's methodology for designing ASICs. By following this methodology, you can decrease design time, ensure a smooth transition between design phases, and thus create a successful ASIC circuit that works right the first time.

All information in this manual is based on the latest product information available at the time of printing. Toshiba reviewed the accuracy of this manual, but should you find, in this manual, any ambiguities or be in doubt as to any meanings, please direct all queries to your nearest Toshiba ASIC Design Center.

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Manual Organization

This manual is organized as follows:

Chapter 1: Introduction to Toshiba ASICs

Briefly describes Toshiba's ASIC offerings: gate arrays, cell-based ICs, and embedded arrays.

Chapter 2: Choosing a Device and a Package

Describes differentiating characteristics of each of the Toshiba ASIC lines. Also explains the steps to decide on a package.

Chapter 3: Customer Interfacing

Explains the ASIC development flow, the customer interface methodologies for designing Toshiba ASICs, the Toshiba ASIC design environment, the design release package, and various types of prototypes and production parts.

Chapter 4: Circuit Design Techniques

Describes ways to optimize your design and to design reliability and testability into a circuit. Discusses delay calculation, I/O cell considerations, steps to determine a package pinout, CMOS electrical design rules, area optimization, recommendations and rules for design reliability, design techniques for "one-pass" layout success including floorplanning, design-for-testability techniques such as internal scan and JTAG boundary-scan, etc.

Chapter 5: Test Data Development

Provides a complete explanation on the requirements and constraints for various kinds of test data.

Chapter 6: Logic and Fault Simulation

Describes logic and fault simulation procedures. Also presents design acceptance criteria per test data type.

Chapter 7: Power Estimation

Explains how to make power estimation at an early stage of a design cycle as well as detailed power calculation equation.

Appendix A: Initial Specifications Form

Presents a blank form for Toshiba to collect all information needed to carry out rapid assessment of your ASIC requirement and quotation. When your need for an ASIC arises, prepare the Initial Specifications Form based on the planning done at your site, so that we can provide appropriate direction.

Appendix B: Design Release Checklist

Presents a blank form of the Design Release Checklist. It helps you to verify successful completion of various stages of pre-layout specification, and furnishes Toshiba with essential information.

Appendix C: Design Kit Request Forms

Presents blank forms you can use when requesting a Toshiba ASIC design kit or EDA system models for special cells.

Appendix D: Toshiba ASIC Product Lines

Lists Toshiba's ASIC product lines, along with estimated usable gate counts, maximum I/O pad counts, and array designators used in the Toshiba ASIC design kit environment.

Chapter 1

Introduction to Toshiba ASICs

This chapter is organized as follows:

1.1 Introduction

Rules & Tips

- **ASICs are devices where the circuit is dedicated to designer's specific requirements, and the functionality of the circuit is totally controlled by the designer.**

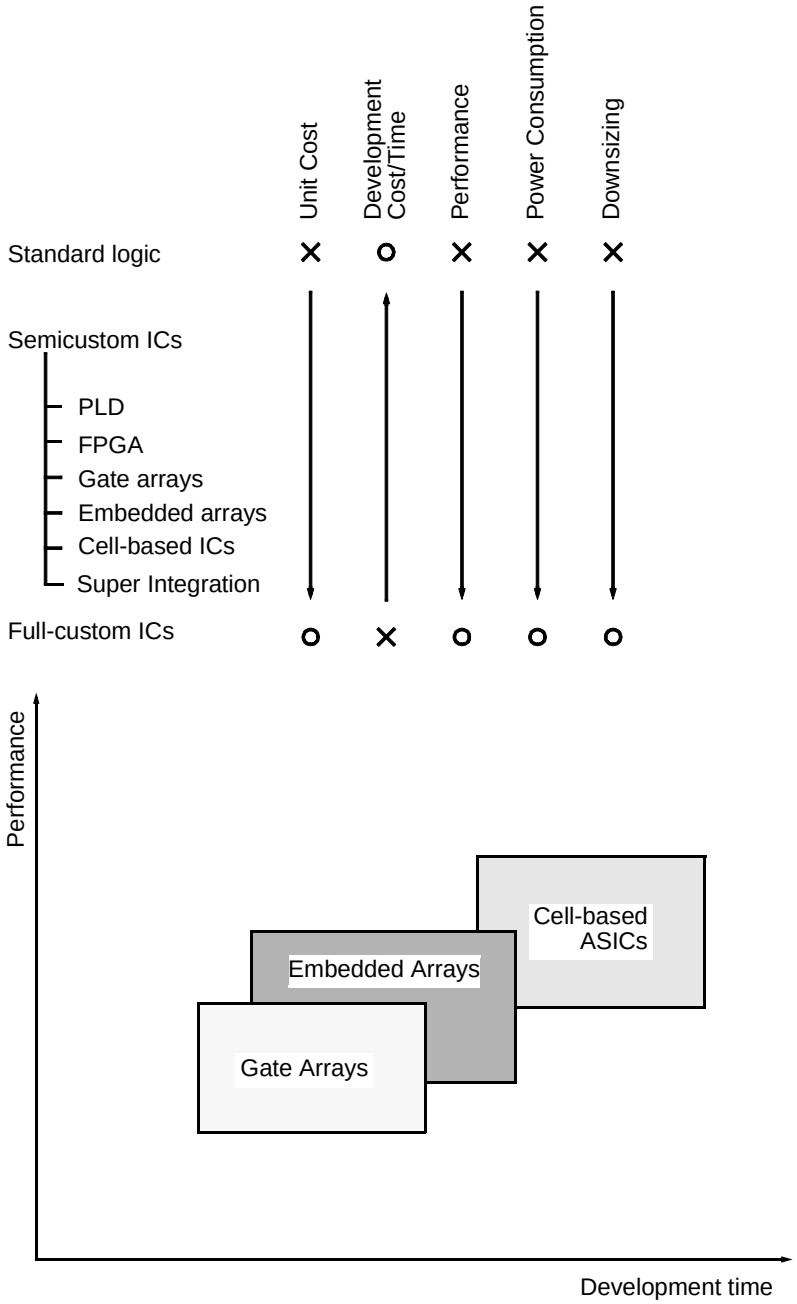
With an ever more rapid development of electronic systems, it is vital that today's engineering groups have access to optimal design solutions. Since the advent of integrated circuits, manufacturers of electronic systems have used each new generation of ICs to improve products by adding features, reducing size, improving performance and steadily reducing product costs. To be competitive in today's marketplace, electronic-based products must remain state-of-the-art. As the scale of semiconductor integration increases and electronic systems become more complex, state-of-the-art often means use of custom LSI circuits.

In this situation, standard, "off-the-shelf" components are often impractical; they offer the quickest, but costly solutions. Compared to standard, off-the-shelf ICs, fully-customized components would give the lowest unit cost as well as represent minimum chip solutions tailored to specific application needs. However, they take a long time — usually one to three years — of tedious development cycles.

Application-specific integrated circuits (ASICs) are devices where the circuit is dedicated to designer's specific requirements, and the functionality of the circuit is totally controlled by the designer. Compared to merchant IC implementations, ASICs offer lower system cost due to significant reductions in component count, board area, and power consumption. Product reliability and equipment maintainability — strong functions of component count — are greatly improved. Compared to full-custom LSI circuits, ASICs offer several advantages: lower development cost, shorter development time, and shorter production lead time. Low development cost means that the LSI implementation of your logic design is cost-justified at much lower volume than a full-custom circuit.

Toshiba prides itself on providing its customers with unique and complete ASIC products and services. Three main techniques of our ASIC products, gate arrays, cell-based ICs, and embedded arrays, form the background to procedures described in this manual.

Figure 1-1 **Benefits and Costs of Digital IC Solutions**



1.2 ASIC Solutions

Rules & Tips

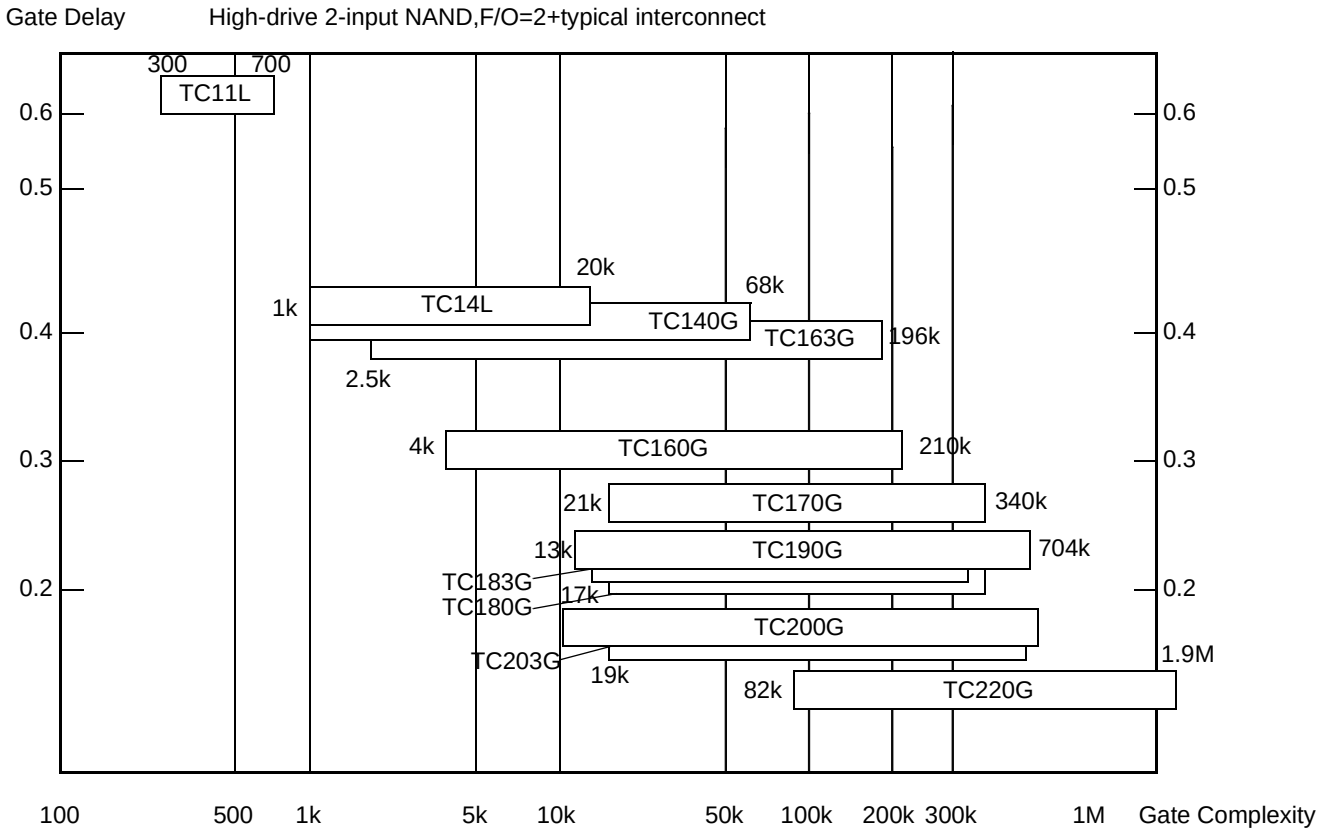
- **Gate arrays, as compared to other ASIC alternatives, can be produced more quickly and less expensively in small quantities.**
- **Cell-based ICs can contain large specialized blocks.**
- **Embedded arrays combine cell-based IC's extensive offerings of high-performance functions with the gate array advantage of quick production turnaround.**

Gate Arrays

When a full-custom LSI is fabricated, many masks must be designed. This takes time and incurs high cost. If a gate array is used, a custom LSI can be developed by only changing metal wiring patterns. The portion below the metal wiring patterns, called masterslice or base array, can be mass-produced in advance and stocked. Custom metal wiring patterns are used on pre-fabricated masterslice to personalize the desired gate array. Therefore, gate arrays can be developed in a short period at a relatively low cost.

All the Toshiba's gate array products employ the sea-of-gates architecture. Masterslices are filled with uncommitted, potentially active transistors. Computer software is used to determine which transistors should be utilized for the circuit design and which transistors should be left unused so the area above can be used for signal routing. This placement and routing flexibility of sea-of-gates makes it possible to integrate large cells such as RAMs, ROMs, and multipliers on the same chip. Toshiba's gate arrays offer single gate array solutions for a wide variety of digital logic applications ranging in size from 300 to 1.9-M gates.

Figure 1-2 Gate Array Product Chart



Cell-Based ICs

Cell-based ICs do not use the masterslice methodology. Instead, all of the masks for the IC design are customized specifically for that design. The density of functions is greater than that achieved by gate arrays and there is little unused silicon area thus giving generally lower unit cost. However, since all of the mask set needs defining, the initial engineering charge is higher for a given gate complexity. This makes cell-based ICs suitable for high-volume products.

Cell-based ICs can contain large specialized megacells such as RAMs, ROMs, FIFOs, register files, and many industry-standard functions including the Z80 microprocessor. Megacells are divided into two groups: hardmacrocells and compilable cells.

The hardmacrocell library includes:

- 16 x 16 multiplier
- 8-, 16-, 24-, and 32-bit adder/subtractors
- 32-bit, 2-operand full adder
- 32-bit, 3-operand full adder
- 16- and 32-bit barrel shifters
- 8-bit ALU
- 8-bit CLA
- CRT controller
- Direct memory access controller (DMA)
- Programmable communications interface (PCI)
- Programmable interval timer (PIT)
- 8-bit programmable peripheral interface (PPI)
- Programmable interrupt controller (PIC)
- 4-bit microprocessor slice
- Carry lookahead generator
- Microprogram controller
- Graphical memory (256 x 24)

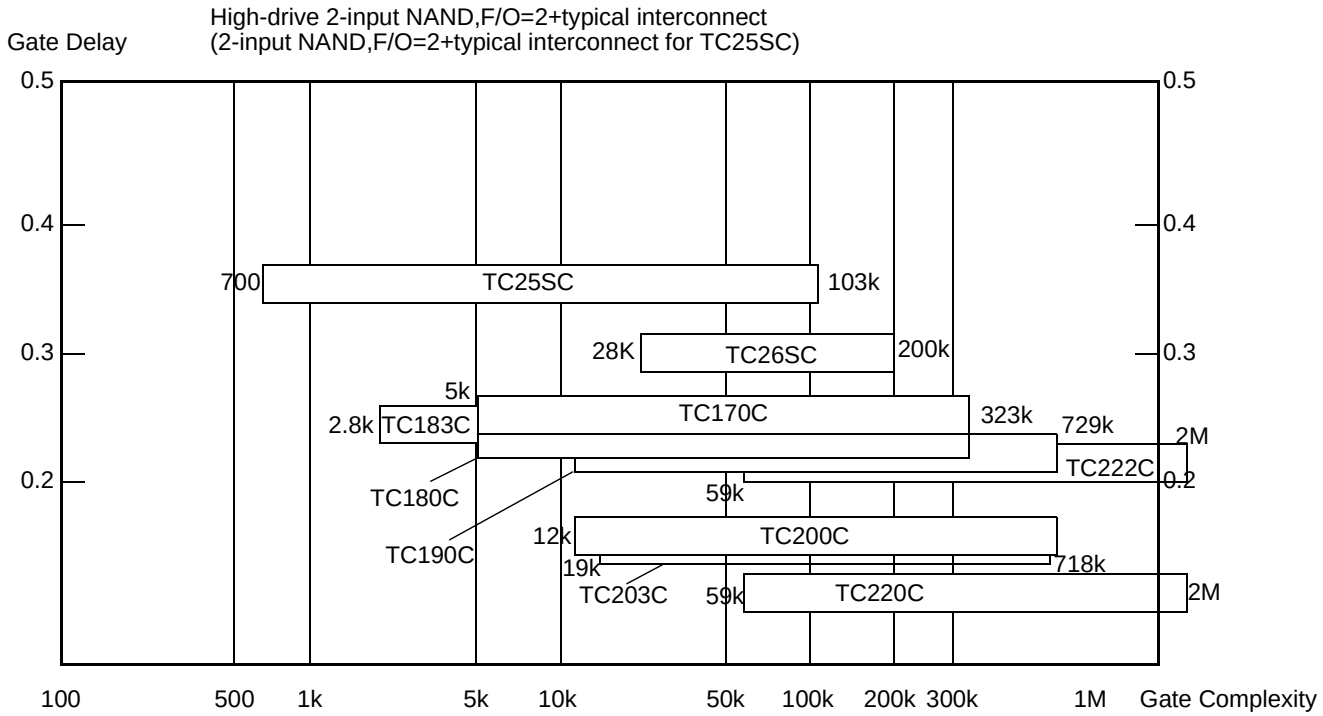
Compilable cell library includes:

- RAM
- ROM

- FIFOs
- Register files
- Multipliers

The Toshiba Universal Megacell Modeling System automatically constructs fully assembled blocks from user-supplied high-level parameters such as word and bit counts. It makes the appropriate engineering decisions and returns complete data base for all specified blocks. For a complete list of megacells available, consult the appropriate data book from Toshiba.

Figure 1-3 Cell-Based IC Product Chart



Embedded Arrays

Embedded arrays provide designers with cell-based integration and performance while incorporating the faster turnaround time associated with gate array. With the embedded array methodology, desired large blocks you select from the cell-based IC library are pre-embedded in the gate array masterslice. Embedded blocks, rather than using gates to build metallized blocks, minimize the silicon area consumed by the blocks. The remaining area above are used for metallization of the logic portion of the design. Figure 1-4 illustrates chip size comparisons between the three ASIC technologies.

Figure 1-5 illustrates the embedded array design flow. Early in the ASIC design cycle, the appropriate area of gates, embedded memory, core functions, and the number of I/Os are agreed upon by you and Toshiba. After the items to be embedded in the customer-specific base array are finalized, the base wafers (formally known as diffused wafers or DW for short) are manufactured concurrently with the completion of your design. Once the design is completed, the layout of the gate array portion of the design is performed on the inventoried customer-specific base wafers. Post-layout simulation is then performed, similar to a standard gate array, confirming that performance requirements are achieved. Manufacturing of prototypes progresses in the same manner as standard gate arrays from this point.

A major advantage using embedded arrays is that changes to the logic design implemented in the gate array section can be easily made. Because only metal mask changes are required for changes in the gate array section, new prototypes are available in a fraction of the time required for cell-based IC technologies.

Figure 1-4 **Chip Size Comparisons between ASIC Technologies**

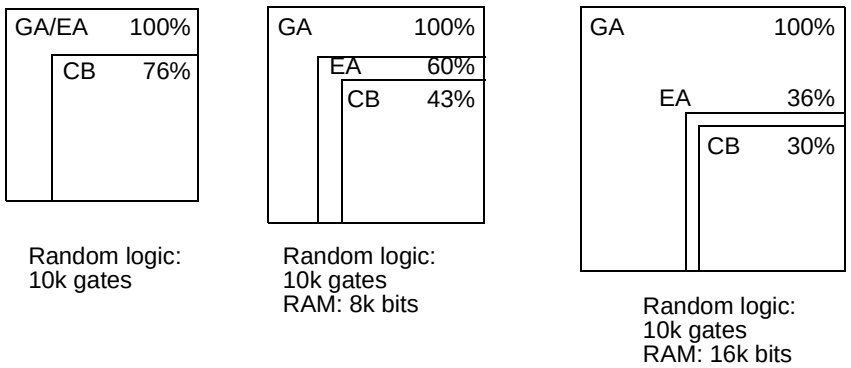


Figure 1-5 **Embedded Array Product Chart**

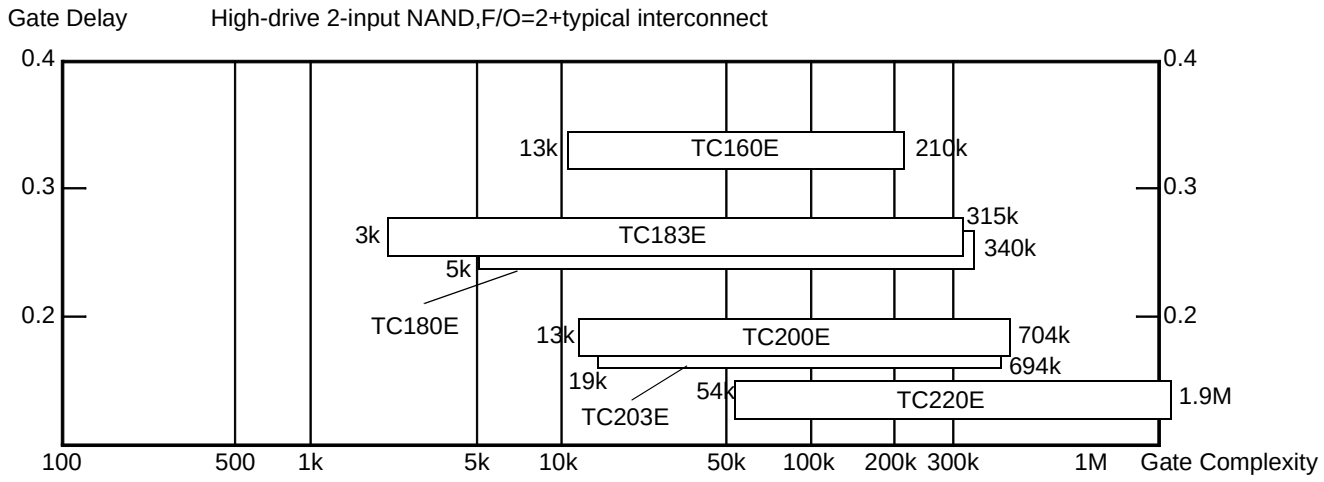
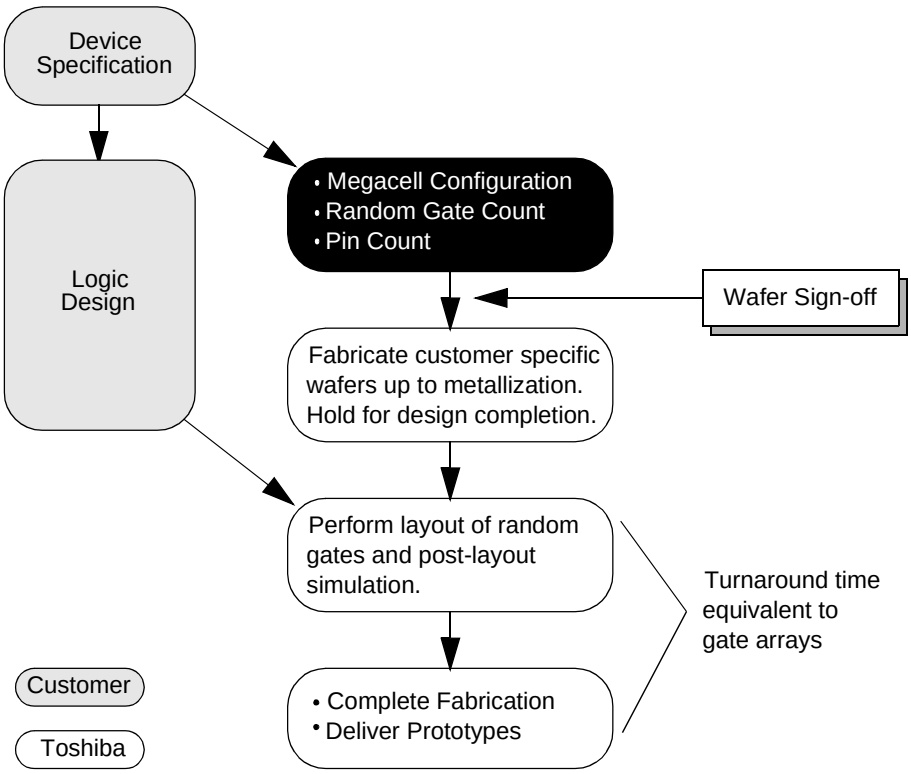


Figure 1-6 **Embedded Array Design Flow**



1.3 Power Supply Alternatives

Rules & Tips

- **Toshiba's ASIC product offerings embrace these lines:**
  1) full 3V operation, 2) full 5V operation, 3) 3V core with mixed 3V/5V I/Os

Table 1-1 charts the Toshiba's ASIC product lines by power supplies and manufacturing processes.

Table 1-1 Toshiba's ASIC Product Lines

	Process (μm)	1.5	1.0	0.8	0.7	0.6	0.5	0.4	0.3
Gate Arrays	5V	11L	14L, 140G	160G	170G	190G			
	3V		14L, 140G	160G			180G	200G	220G
	3V/5V			163G			183G	203G	
Cell-Based ICs	5V			25SC 26SC	170C	190C			
	3V						180C	200C	220C
	3V/5V						183C	203C	
	2V/3V								222C
Embedded Arrays	5V			160E					
	3V						180E	200E	220E
	3V/5V						183E	203E	

* All product names are prefixed by TC, like TC180G.

- ***The 3V core and 3V I/Os can be rated at either 3.0V or 3.3V typical.***
- ***Every I/O of the mixed 3V/5V ASICs can be programmed as either 3V or 5V.***
- ***While the TC180G/C/E and TC200G/C/E series operate with a 3V core and 3V I/Os, they offer 5V-tolerant CMOS- and TTL-level input buffers.***

Dual I/O Options

Toshiba ASIC lines include many product families that operate with a 3V core and offer both 3V and 5V I/Os. The 3V core reduces the power consumption of your design, while the 3V and 5V I/O compatibility offers you flexibility with your system interface design. These ASIC families accomplish this flexibility by using two power rings for I/O circuitry. One ring is set to operate at 3 volts and the other at 5 volts. There are no restrictions on 3V and 5V I/O placement. These ASICs are an ideal vehicle for designing 5V-to-3V and 3V-to-5V bus interface conversion circuitry.

The 3V and 5V I/O capability also gives you a migration path from mixed 3V/5V systems to straight 3V-based systems. Because all popular ICs have not yet been converted from 5V operation to 3V operation, most systems in the near future will be mixed 3V/5V systems. They make an ideal interface ASIC between the 5V and 3V circuitry. In addition, when a design is converted from mixed 3V/5V operation to straight 3V operation, no changes to the ASIC design are needed. The I/Os designed for 5V operation can be used at 3 volts with no changes to the ASIC design, saving you design time and costs.

In addition, the TC222C cell-based ASIC family, the newest addtion to Toshiba’s ASIC portfolio, operates with a 3V core and offer both dual 2V and 3V I/O options, thus allowing a significant reduction in power.

1.4 Absolute Maximum Ratings and Recommended Operating Conditions

Rules & Tips

- **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.**

3V ASICs

Table 1-2 Absolute Maximum Ratings for 3V ASICs (Vss=0V)

Parameter		Symbol	Rating	Unit
DC supply voltage		V_{DD}	-0.3 to +5.0	V
DC input voltage	3V normal type	V_{IN}	-0.3 to V_{DD}+0.3	V
	3V fail-safe type (Power-down protection)		-0.3 to V_{DD}+0.3	
	5V-tolerant type		-0.3 to 7.0	
DC output voltage		V_{OUT}	-0.3 to V_{DD}+0.3	V
DC input current		I_{IN}	±10	mA
Storage temperature		T_{stg}	-40 to +125	°C

Table 1-3 Recommended Operating Conditions for 3V ASICs (Vss=0V)

Parameter		Symbol	Rating	Unit
DC supply voltage		V_{DD}	2.7 to 3.6	V
DC input voltage	3V normal type	V_{IN}	V_{DD} (max.)	V
	3V fail-safe type (Power-down protection)		V_{DD} (max.)	
	5V-tolerant type		5.5 (max.)	
Junction temperature		T_j	-0 to +85	°C

* If you prefer more relaxed conditions, contact your local Toshiba ASIC service group.

5V ASICs

Table 1-4 **Absolute Maximum Ratings for 5V ASICs (Vss=0V)**

Parameter	Symbol	Rating	Unit
DC supply voltage	V_{DD}	-0.3 to +7.0	V
DC input voltage	V_{IN}	-0.3 to V_{DD}+0.3	V
DC output voltage	V_{OUT}	-0.3 to V_{DD}+0.3	V
DC input current	I_{IN}	±10	mA
Storage temperature	T_{stg}	-40 to +125	°C

Table 1-5 **Recommended Operating Conditions for 5V ASICs (Vss=0V)**

Parameter	Symbol	Rating	Unit
DC supply voltage	V_{DD}	4.5 to 5.5	V
Junction temperature	T_j	-0 to +85	°C

Mixed 3V/5V ASICs

Table 1-6 **Absolute Maximum Ratings for Mixed 3V/5V ASICs (Vss=0V)**

Parameter	Symbol	Rating	Unit
DC supply voltage	V_{DDA}	-0.3 to +7.0	V
	V_{DDB}	-0.3 to +5.0*	V
DC input voltage	V_{INA}	-0.3 to V_{DDA}+0.3	V
	V_{INB}	-0.3 to V_{DDB}+0.3	V
DC output voltage	V_{OUTA}	-0.3 to V_{DDA}+0.3	V
	V_{INB}	-0.3 to V_{DDB}+0.3	V
Storage temperature	T_{stg}	-40 to +125	°C

* -0.3 to +7.0 for the TC163G series

Table 1-7 **Recommended Operating Conditions for Mixed 3V/5V ASICs (Vss=0V)**

Parameter	Symbol	Rating	Unit
DC supply voltage	V_{DDA}	4.5 to 5.5	V
	V_{DDB}	3.0 to 3.6 or 2.7 to 3.3	V
Junction temperature	T_j	0 to +85	°C

* If you prefer more relaxed conditions, contact your local Toshiba ASIC service group.

* For the TC222C series, contact your Toshiba Design Center engineer.

1.5 DC Electrical Characteristics

Rules & Tips

- **DC electrical characteristics specify the worst-case dc parametric (i.e., electrical) performance of the I/O buffers that are guaranteed over the specified temperature range.**

3V ASICs

Table 1-8 DC Electrical Characteristics for 3V ASICs (a) (Specified at junction temperature 0 to +85 °C)

Symbol	Parameter		Condition	Case	Value	Unit
V_{IH}	High-level input voltage			Min		V
		LVTTL level			2.0	
		LVTTL level Schmitt trigger			2.0	
		CMOS level			$0.8V_{DD}$	
		CMOS level Schmitt trigger			$0.8V_{DD}$	
V_{IL}	Low-level input voltage			Max		V
		LVTTL level			0.8	
		LVTTL level Schmitt trigger			0.8	
		CMOS level			$0.2V_{DD}$	
		CMOS level Schmitt trigger			$0.2V_{DD}$	
I_{IH}	High-level input current		$V_{IN}=V_{DD}$	Min/Max	-10/10	µA
		Input buffer with pull-down			10/200	
I_{IL}	Low-level input current		$V_{IN}=V_{SS}$	Min/Max	-10/10	µA
		Input buffer with pull-up			-200/10	
I_{OZ}	High-impedance leakage current		$V_{OUT}=V_{DD}$ or V_{SS}	Min/Max	-10/10	µA
V_H	Schmitt trigger hysteresis voltage			Typ		V
		LVTTL level			0.5	
		CMOS level			0.5	
I_{DDS}	Quiescent supply current*		$V_{IN}=V_{DD}$ or V_{SS}	Max		nA/gate
		TC220G/C/E			Data n/a	
		TC200G/C/E			1.8	
		TC180G/C/E			1.8	

*Quiescent supply current is design-dependent, and may exceed the value indicated when a design has input buffers with pull-up or pull-down.

Table 1-9 **DC Electrical Characteristics of 3V ASICs (b)**
(Specified at junction temperature 0 to +85°C)

Symbol	Parameter		Condition		Case	Value	Unit
V_{OH}	High-level output voltage		TC220G/C/E, TC200G/C/E	TC180G/C/E	Min	2.4	V
		Type B1	—	I_{OH}=-1mA			
		Type B2	I_{OH}=-2mA	I_{OH}=-2mA			
		Type B4	I_{OH}=-4mA	I_{OH}=-4mA			
		Type B8	I_{OH}=-8mA	I_{OH}=-8mA			
		Type B16	I_{OH}=-16mA	I_{OH}=-16mA			
		Type B24	I_{OH}=-24mA	I_{OH}=-24mA			
			I_{OH}=-1μA			V_{SS}-0.05	
V_{OL}	Low-level output voltage		TC220G/C/E, TC200G/C/E	TC180G/C/E	Max	0.4	V
		Type B1	—	I_{OL}=1mA			
		Type B2	I_{OL}=2mA	I_{OL}=2mA			
		Type B4	I_{OL}=4mA	I_{OL}=4mA			
		Type B8	I_{OL}=8mA	I_{OL}=8mA			
		Type B16	I_{OL}=16mA	I_{OL}=16mA			
		Type B24	I_{OL}=24mA	I_{OL}=24mA			
			I_{OL}=1μA			V_{SS}+0.05	

*Current out of a pin is given as a negative value.

5V ASICs

Table 1-10 DC Electrical Characteristics of 5V ASICs (a)
(Specified at junction temperature 0 to +85°C)

Symbol	Parameter	Condition	Case	Series	Value	Unit
V_{IH}	High-level input voltage		Min			V
	TTL level			TC11L, TC190C, TC170C, TC160E	2.0	
				TC190G, TC170G, TC160G, TC140G, TC14L, TC26SC, TC25SC	2.2	
	TTL level Schmitt trigger[1]			TC11L, TC190C, TC170C, TC160E	2.0	
				TC190G, TC170G, TC160G, TC140G, TC14L, TC26SC, TC25SC	2.2	
	CMOS level				3.5	
	CMOS level Schmitt trigger				4.0	
V_{IL}	Low-level input voltage		Max			V
	TTL level				0.8	
	TTL level Schmitt trigger				0.8	
	CMOS level				1.5	
	CMOS level Schmitt trigger				1.0	
I_{IH}	High-level input current	$V_{IN}=V_{DD}$	Min/Max		-10/10	µA
	Input buffer with pull-down				10/200	
I_{IL}	Low-level input current	$V_{IN}=V_{SS}$	Min/Max		-10/10	µA
	Input buffer with pull-up				-200/-10	
I_{OZ}	High-impedance leakage current	$V_{OUT}=V_{DD}$ or V_{SS}	Min/Max		-10/10	µA
V_H	Schmitt trigger hysteresis voltage		Typ			V
	TTL level			TC170G/C	0.5	
				TC26SC, TC25SC	0.4	
				TC190G/C, TC160E, TC140G, TC14L, TC11L	0.3	
	CMOS level			TC190G/C, TC170G/C, TC160G	1.5	
				TC26SC, TC25SC	0.6	
				TC160E, TC140G, TC14L, TC11L	1.4	
I_{DDS}	Quiescent supply current[2]	$V_{IN}=V_{DD}$ or V_{SS}	Max	TC190G/C	1	nA/gate
				TC170G, TC160G/E, TC26SC, TC25SC	2	
				TC170C	0.6	
				TC140G, TC14L	3.5	
				TC11L	Data n/a	

1. Not available for the TC11L gate array series.
2. Quiescent supply current is design-dependent, and may exceed the values indicated when the design has input buffers with pull-up or pull-down.

Table 1-11 **DC Electrical Characteristics of 5V ASICs (b)**
(Specified at junction temperature 0 to +85 °C)

Symbol	Parameter	Condition				Case	Value	Unit
V_{OH}	High-level output voltage	TC190G/C	TC170G/C TC160G/E TC26/25SC	TC140G TC14L	TC11L	Min	2.4	V
	Type B1	—	I_{OH}=-1mA	I_{OH}=-1mA	I_{OH}=-1mA			
	Type B2	I_{OH}=-2mA	I_{OH}=-2mA	I_{OH}=-2mA	I_{OH}=-2mA			
	Type B4	I_{OH}=-4mA	I_{OH}=-4mA	I_{OH}=-4mA	I_{OH}=-4mA			
	Type B6	—	—	I_{OH}=-6mA	I_{OH}=-6mA			
	Type B8	I_{OH}=-8mA	I_{OH}=-8mA	I_{OH}=-8mA	I_{OH}=-8mA			
	Type B12	—	—	I_{OH}=-12mA	I_{OH}=-12mA			
	Type B16	I_{OH}=-16mA	I_{OH}=-16mA	—	I_{OH}=-16mA			
	Type B18	—	—	I_{OH}=-18mA	—			
	Type B24	I_{OH}=-24mA	I_{OH}=-24mA	I_{OH}=-24mA	—			
		I_{OH}=-1μA					V_{SS}-0.05	
V_{OL}	Low-level output voltage	TC190G/C	TC170G TC160G/E TC26/25SC	TC140G TC14L	TC11L	Max	0.4	V
	Type B1	—	I_{OL}=1mA	I_{OL}=1mA	I_{OL}=1mA			
	Type B2	I_{OL}=2mA	I_{OL}=2mA	I_{OL}=2mA	I_{OL}=2mA			
	Type B4	I_{OL}=4mA	I_{OL}=4mA	I_{OL}=4mA	I_{OL}=4mA			
	Type B6	—	—	I_{OL}=6mA	I_{OL}=6mA			
	Type B8	I_{OL}=8mA	I_{OL}=8mA	I_{OL}=8mA	I_{OL}=8mA			
	Type B12	—	—	I_{OL}=12mA	I_{OL}=12mA			
	Type B16	I_{OL}=16mA	I_{OL}=16mA	—	I_{OL}=16mA			
	Type B18	—	—	I_{OL}=18mA	—			
	Type B24	I_{OL}=24mA	I_{OL}=24mA	I_{OL}=24mA	—			
		I_{OL}=1μA					V_{SS}+0.05	

*Current out of a pin is given as a negative value.

Mixed 3V/5V ASICs

Table 1-12 DC Electrical Characteristics of 3V/5V ASICs (a) (Specified at junction temperature 0 to +85 °C)

Symbol	Parameter			Condition	Case	Series	Value	Unit
V_{IH}	High-level input voltage				Min			V
		5V input	TTL level			TC203G/C/E, TC183G/C/E	2.0	
						TC163G	2.2	
			TTL level Schmitt trigger			TC203G/C/E, TC183G/C/E	2.0	
						TC163G	2.2	
			CMOS level				3.5	
			CMOS level Schmitt trigger				4.0	
		3V input	LVTTL level[1)]				2.0	
			LVTTL level Schmitt trigger[1)]				2.0	
			CMOS level				0.8V_{DDB}	
			CMOS level Schmitt trigger				0.8V_{DDB}	
V_{IL}	Low-level input voltage				Max			V
		5V input	TTL level				0.8	
			TTL level Schmitt trigger				0.8	
			CMOS level				1.5	
			CMOS level Schmitt trigger				1.0	
		3V input	LVTTL level[1)]				0.8	
			LVTTL level Schmitt trigger[1)]				0.8	
			CMOS level				0.2V_{DDB}	
			CMOS level Schmitt trigger				0.2V_{DDB}	
I_{IH}	High-level input current (5V input)			$V_{INA}=V_{DDA}$	Min/Max		-10/10	µA
			Input buffer with pull-down			TC203G/C/E	25/150	
						TC183G/C/E, TC163G	10/200	
	High-level input current (3V input)			$V_{INB}=V_{DDB}$			-10/10	
			Input buffer with pull-down			TC203G/C/E	50/300	
						TC183G/C/E, TC163G	10/200	
I_{IL}	Low-level input current (5V input)			$V_{INA}=V_{SS}$	Min/Max		-10/10	µA
			Input buffer with pull-up			TC203G/C/E	-150/-25	
						TC183G/C/E, TC163G	-200/-10	
	Low-level input current (3V input)			$V_{INB}=V_{SS}$			-10/10	
			Input buffer with pull-up			TC203G/C/E	-300/-50	
						TC183G/C/E, TC163G	-200/-10	
I_{OZ}	High-impedance leakage current			$V_{OUTA}=V_{DDA}$ or V_{SS} & $V_{OUTB}=V_{DDB}$ or V_{SS}	Min/Max		-10/10	µA

Table 1-12 **DC Electrical Characteristics of 3V/5V ASICs (a) (Specified at junction temperature 0 to +85 °C)** *(Continued)*

Symbol	Parameter			Condition	Case	Series		Value	Unit
V_H	Schmitt trigger hysteresis voltage				Typ				V
		5V Input	TTL level			TC203G/C/E		0.3	
						TC183G/C/E, TC163G		0.5	
			CMOS level			TC203G/C/E		1.25	
						TC183G/C/E, TC163G		1.5	
		3V Input	LVTTL level			TC203G/C/E		0.15	
						TC183G/C/E, TC163G		0.5	
			CMOS level			TC203G/C/E		0.15	
						TC183G/C/E, TC163G		0.5	
I_{DDS}	Quiescent Supply Current [2]			$V_{INA}=V_{DDA}$ or V_{SS} & $V_{INB}=V_{DDB}$ or V_{SS}	Max	TC203G/C/E	Internal	1.8	nA/gate
							I/O	150	
						TC183G/C/E	Internal	1.8	
							I/O	150	
						TC163G	Internal	1.5	
							I/O	n/a	

1. Available only with TC183G
2. Quiescent supply current is design-dependent, and may exceed the values indicated when a design has input buffers with pull-up or pull-down.

Table 1-13 **DC Electrical Characteristics of 3V/5V ASICs (b) (Specified at junction temperature 0 to +85 °C)**

Symbol	Parameter		Condition			Case	Value	Unit
V_{OH}	High-level output voltage		TC203G/C/E	TC183G/C/E	TC163G	Min	2.4	V
	V_{OHA}/ V_{OHB}	Type B1/B1IF	—	I_{OH}=-1mA/-1mA	—			
		Type B2/B2IF	I_{OH}=-2mA/-2mA	I_{OH}=-2mA/-2mA	—			
		Type B4/B4IF	I_{OH}=-4mA/-4mA	I_{OH}=-4mA/-4mA	I_{OH}=-4mA/-2mA			
		Type B8/B8IF	I_{OH}=-8mA/-8mA	I_{OH}=-8mA/-8mA	I_{OH}=-8mA/-4mA			
		Type B16/B16IF	I_{OH}=-16mA/-16mA	I_{OH}=-16mA/-16mA	I_{OH}=-16mA/-8mA			
		Type B24/B24IF	I_{OH}=-24mA/-24mA	I_{OH}=-24mA/-24mA	I_{OH}=-24mA/-12mA			
			I_{OH}=-1μA				V_{DD}-0.05	
V_{OL}	High-level input voltage		TC203G/C/E	TC183G/C/E	TC163G	Max	0.4	V
	V_{OLA}/ V_{OLB}	Type B1/B1IF	—	I_{OL}=1mA/1mA	—			
		Type B2/B2IF	I_{OL}=2mA/2mA	I_{OL}=2mA/2mA	—			
		Type B4/B4IF	I_{OL}=4mA/4mA	I_{OL}=4mA/4mA	I_{OL}=4mA/2mA			
		Type B8/B8IF	I_{OL}=8mA/8mA	I_{OL}=8mA/8mA	I_{OL}=8mA/4mA			
		Type B16/B16IF	I_{OL}=16mA/16mA	I_{OL}=16mA/16mA	I_{OL}=16mA/8mA			
		Type B24/B24IF	I_{OL}=24mA/24mA	I_{OL}=24mA/24mA	I_{OL}=24mA/12mA			
			I_{OL}=1μA				V_{SS}+0.05	

*Current out of a pin is given as a negative value.

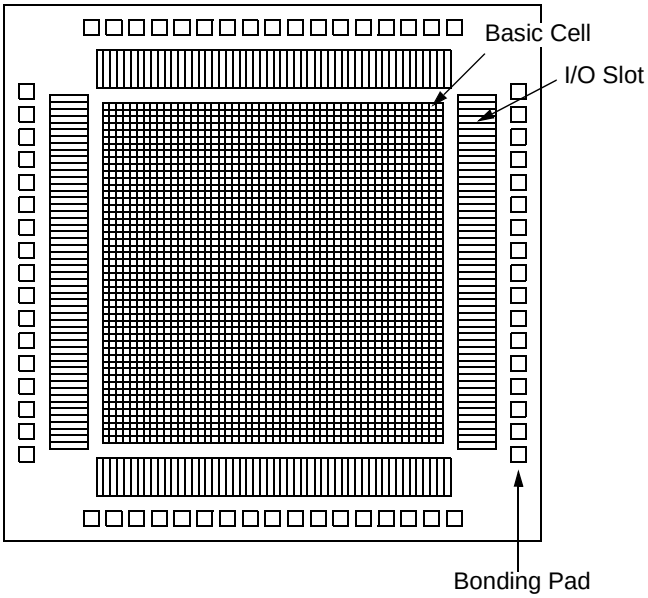
* For the TC222C series, contact your Toshiba Design Center engineer.

1.6 Chip Structure

Rules & Tips

- **One "gate" is equivalent to a two-input NAND (or NOR) gate, or more precisely, two N/P transistor pairs. With cell-based ICs, two grids are equal to one gate.**
- **I/O slots along the four edges of a die are for placing I/O buffers.**
- **Bonding pads are for running wires from the IC pads on the die to chip's body leads.**

Figure 1-7 **Sea-of-Gates Chip**

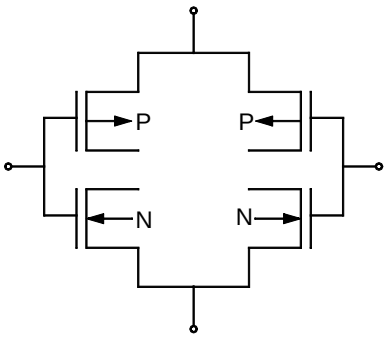


Basic Cells, Gates, and Grids

A block of two contiguous pairs of N- and P-channel transistors is called a basic cell. A basic cell can implement complete basic functions such as a 2-input NAND gate or a 2-input NOR gate.

Gate complexities are measured in terms of the number of basic cells; one gate is equal to one basic cell. For cell-based IC designs, the term "grid" is used instead of "gate" to represent real estate requirements. Two grids are equivalent to one gate.

Figure 1-8 **Basic Cell**



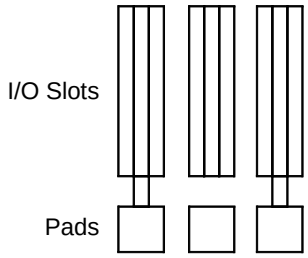
I/O Slots and Bonding Pads

Each masterslice has a fixed number of I/O slots in the peripheral area that are responsible for interfacing internal logic to the outside world. I/O slots consist of an input protection circuit and large geometry transistors for driving heavy off-chip loads.

Two or more I/O slots are dedicated to power supply and ground. Additional I/O slots may be configured as V_{DD}/V_{SS} to suppress system noise. All the other I/O slots can be used for input, output, bidirectional, and 3-state output buffers. If necessary, they can even be used to buffer heavily loaded internal signals.

Bonding pads are for running wires from the IC pads on the die to chip's body leads.

Figure 1-9 **I/O Slot-to-Pad Allotment**



1.7 Logic Functions

Rules & Tips

- **Toshiba offers a variety of logic functions or cells in the form of libraries. The ASIC cell library consists of hundreds of logic functions, ranging from gates, latches, flip-flops, decoders, and shift register to RAMs, ROMs, and many other specialized large cells.**

Macrocells and Primitives Cells

"Macrocell" is a gate array term. "Primitive cell" is a cell-based IC term. A macrocell (primitive cell) is the fixed metal pattern that connects a group of N- and P-transistors to form a logic element. Macrocells vary in complexity from a simple inverter to a complex flip-flop. They are predefined circuits characterized with symbol and model data required for accurate CAD analysis.

I/O Cells

Located along the four edges of a device, I/O cells are responsible for interfacing internal logic to the outside world. Among I/O cells are input buffers, output buffers, bidirectional buffers, 3-state buffers, clock drivers, and oscillators. An extensive flexibility is available in the use of pull-ups/pull-downs, and choice of input voltage levels (CMOS, TTL) and output current drive (1mA, 2mA, 4mA, ... , 24mA).

Macrofunctions and Softmacrocells

"Macrofunction" is a gate array term. "Softmacrocell" is a cell-based IC term. Macrofunctions (softmacrocells) are hierarchically-nested collections of "soft-coded" macrocells. For user convenience, over 70 types of 74-compatible macrofunctions are available in the cell library. The gate array macrofunction library also includes more than 70 types of Toshiba's original functions.

Megacells and Compilable Cells

"Megacell" is a gate array term. "Compilable cell" is a cell-based IC term. Megacells (compilable cells) are large, hard-wired cells such as RAMs and ROMs. The Toshiba megacell modeling software provides thousands of cell types by automatically creating functionally correct cells when a list of desired parameters (such as word/bit configurations) are supplied.

Megafunctions and Hardmacrocells

"Megafunction" is a gate array term. "Hardmacrocell" is a cell-based IC term. While gate array's megafunctions are soft-coded, cell-based IC's hardmacrocells are hard-wired. Megafunction (hardmacrocell) examples include large, complex cells such as multipliers, ALU, barrel shifters, etc. The cell-based IC's hardmacrocell library includes such standard product functions as CRT controller, UART, USART, programmable interrupt controller (PIC), programmable interval timer (PIT), and so on.

Table 1-14 **Logic Function Types**

Gate Array	Cell-Based IC	Cell Examples
Macrocell	Primitive cell	Gates, decoders, flip-flops
I/O cell	I/O cell	Input, output, and bidirectional buffers
Macrofunction	Softmacrocell	74-compatibles
Megacell	Compilable cell	RAM, ROM, FIFO
Megafunction (soft-coded)	Hardmacrocell (hard-wired)	16x16 multipliers, 8-bit ALU, UART, USART, PPI, PTI

* Megacells (compilable cells) and megafunctions (hardmacrocells) are often collectively referred to as megacells, meaning large cells.

Chapter 2

Choosing a Device and a Package

This chapter is organized as follows:

2.1 Choosing an Array Series

Rules & Tips

- **In order to choose the array series that best serves your needs, determine these factors for your circuit: 1) development time scale, 2) chip's power supply, 3) use of memory and other large cells, 4) I/O specifications, 5) speed requirements.**

Initial Specifications Form

When your need for an ASIC arises, contact the nearest Toshiba ASIC service group, and we can help you decide. Please prepare the Initial Specifications Form based on the planning done at your site, so that we can provide appropriate direction. A blank Initial Specifications Form is attached in Appendix A.

The Initial Specifications Form identifies key requirements for your circuit, packaging, customer interface, and development time scales. Because estimates are used, the Initial Specifications Form is considered merely as a guiding document.

Power Supply Alternatives

All the Toshiba's ASIC products — gate arrays, cell-based ICs, and embedded arrays — embrace the following lines:

- Full 3.3V (3.0V) operation
- Full 5V operation
- 3.3V core with mixed 3.3V/5V I/Os (3.0V/5V I/Os)
- 2.0V core with mixed 2.0V/3.0V I/Os

Technology Selection Criteria

Use the following selection criteria checklist to review your circuit requirements.

Table 2-1 **ASIC Type Selection Checklist**

#	Question	ASIC Solutions
1.	If your prototype lead time requirement is within 2 to 3 weeks, then, If 5 to 6 weeks is okay, then,	GA, EA CB
2.	If you wish to integrate high-performance large functions on the same chip, then,	CB, EA
3.	If you wish to integrate large memory, then	CB, EA
4.	If you wish to use analog cells such as A/D and D/A converters on-chip, then	CB
5.	If you have a plan to make changes to the logic section or develop derivatives in the future, then	EA

- Gate arrays offer a restricted library of megacell functions. Please look up the latest catalog for the availability information.
- Not all cell-based IC series can support analog cells.

System Interconnect I/O Cells

Toshiba offers an extensive flexibility in the choice of I/O cells. System interconnect I/O cell examples include:

- Peripheral Component Interconnect (PCI) drivers/receivers
- Gunning Transceiver Logic (GTL) drivers/receivers
- Low-Voltage Differential Signaling (LVDS) drivers/recievers
- Fail-safe inputs with power-down protection

If you are planning to use any of the above cells, ask the Toshiba ASIC service group for the availability information.

Circuit Performance

Your considerations in selecting an array series may include the circuit's speed requirement. Projects of ultra-fast circuits require a check of critical path timing in advance.

Table 2-2 summarizes the features of each of the Toshiba ASIC series that make them stand out from other series.

Table 2-2 Array Characteristics

Series	Quick Turn	Embedded Megacells	3V Operation	Dual I/O Options	Fail-safe I/O	5V-tolerant I/O	Small Design with Many I/Os	Analog Cells	MPU Core	GTL	PCI	DPLL	APLL	LVDS
TC220G	A		A		D	D					D	D		
TC200G	A		A		A	A				D	A	D	D	D
TC180G	A		A		A	A				A	A	A	A	
TC190G	A				D					D	A	D	D	
TC170G	A										A	D	A	
TC160G	A		A								A		D	
TC140G	A		A											
TC14L	A		A				A							
TC11L	A						A							
TC203G	A		A	A	D					D	D	D	D	
TC183G	A		A	A						D	A	A	A	
TC163G	A		A	A							D			
TC220C		A	A		D	D				D	D			D
TC200C		A	A		A	A		D		D	A			
TC180C		A	A		A	A				A	A			
TC190C		A			D				A	D	A			
TC170C		A							A		A			
TC26SC		A						D						
TC25SC		A						A	A					
TC203C		A	A	A	D	D				D	D			
TC183C		A	A	A						D	A			
TC220E	A	A	A		D	D				D	D	D		
TC200E	A	A	A		A	A				D	A	D	D	D
TC180E	A	A	A		A	A				A	A	A	A	
TC160E	A	A						D			A		D	
TC203E	A	A	A	A	D	D				D	D		D	
TC183E	A	A	A	A						D	A		A	

A Available, D In development

- Quick Turn
  Provides rapid turnaround of first prototypes — usually 2 to 3 weeks. Cell-based IC prototyping takes 5 to 6 weeks.
- Embedded Megacells
  Can embed megacells such as large memory. Embedded memories for cell-based ICs and embedded arrays are much more area-efficient than gate array's metallized memories. Gate arrays can integrate up to 18k-bit RAM and up to 16k-bit ROM per block.
- 3V Operation
  Can be rated at either 3.0V or 3.3V (typical).
- Dual I/O Options
  The xx3G/C/E series offers a 3V core and dual 3V/5V I/Os; every I/O can be programmed as either 3V or 5V. The TC222C series offers a 2V core with dual 2V/3V I/Os.
- Fail-safe I/O
  Input buffers with power-down protection, without the clamp diode returned to V_{DD} (see Section 4.2.1, *I/O Protection*, on page 4-18).
- Small Design with Many I/Os
  Supports gate counts from 300 to 20k usable gates with double pad counts.
- Analog Cells
  A/D and D/A converters, comparators, power-on reset, analog phased-locked loop (PLL), etc.
- MPU Core
  Embedded core functionally-compatible with Zilog Z80
- DPLL/APLL
  Analog PLL (APLL) can run faster and provide on-chip frequency synthesis, but it involves use of special analog processes. Digital PLL (DPLL) is an easier vehicle for canceling out chip-to-chip clock skew.
- LVDS
  The LVDS driver/reciever I/O cells fully support the Scalable Coherent Interface (SCI) low-volttage differential standard, IEEE Std 1596-1992.

In the event that you have special requirements for your ASIC project that are not covered in our sales brochures or data books, consult the nearest Toshiba ASIC service group.

2.2 Choosing a Device

Rules & Tips

- **Designs comprised of only hand-crafted logic can be sized, based on the number of gates and I/O pins required.**
- **Designs with megacells require "IC floorplanning" to determine the best device.**

Procedure

Table 2-3 gives the procedure for choosing a device best serving your needs:

Table 2-3 Array Sizing Procedure

Gate array	only hand-crafted logic	Sized, based on the number of gates and I/Os.
	with synthesized logic or megacells	Ask Toshiba for floorplanning.
Cell-based IC		Ask Toshiba for floorplanning.
Embedded array		Ask Toshiba for floorplanning.

Gate Array Sizing

Choosing a device is often called "array sizing." Each device in each array series has a specific number of gates and I/O pads.

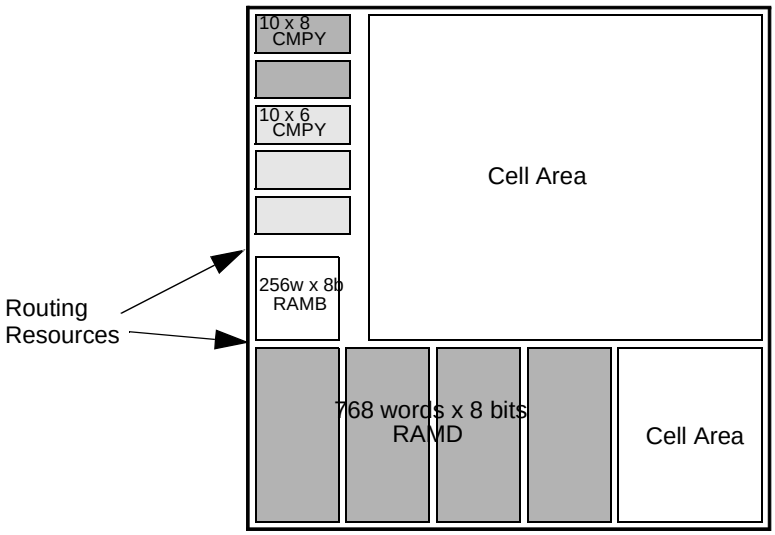
The number of gates fabricated across the chip is called "raw gates." The number of gates available to implement your design is called "usable gates." Actual number of usable gates will depend on the types and numbers of cells used, and may be more or less than indicated in the catalog. For example, designs with a high degree of random logic would present challenges to placement-and-routing.

Several I/O pads may be configured as V_{DD}/V_{SS}, depending on the amount of possible system noise. You must allow for the V_{DD}/V_{SS} pads required at the expense of I/O pads. This will be detailed in Chapter 4, *Circuit Design Techniques*.

Floorplanning

Cell-based ICs and embedded arrays, and often gate arrays, contain megacells such as RAMs and ROMs. Any designs with megacells require floorplanning before the proper device size can be selected. Floorplanner software lets us perform experimentation with various floorplans to achieve optimal gate density and predict chip routability. A floorplan, just like a scale diagram of a room or building, define rectangular regions on the plot of a chip for megacells and cell areas, as depicted below in Figure 2-1.

Figure 2-1 **Floorplan Example**



2.3 Choosing a Package

Rules & Tips

- **Determine the following to select a package: 1) soldering method, 2) package-body size requirement, 3) lead count, 4) compatibility with the chosen masterslice, 5) chip's power dissipation vs. package's thermal performance.**
- **Select a package with adequate thermal performance so that the chip's junction temperature will not exceed 85 degrees C.**

Package Types

Table 2-4 shows various types of packages with their respective range of lead counts.

Table 2-4 Package Availability Chart

Package Style			Lead Count	Features
Through-hole	DIP	DIP	16, 18, 24, 28, 40, 42, 48	
		Shrink DIP	42, 64	
	PGA	Ceramic PGA	64, 69, 85, 101, 121, 145, 181, 225	
		Cavity-down ceramic PGA	115, 223, 299, 391	High dissipation
Surface mount	SOP		24, 28	
	QFP	Plastic	44 to 304	Most inexpensive
		Low-profile plastic (LQFP)	48, 64, 80, 100, 120, 128, 144, 176, 208, 216, 256	1.4 mm thick
		Thin-profile plastic (TQFP)	64, 80, 100, 120, 128, 144, 176	1.0 mm thick
		TAB	208, 240, 256, 304	High density
		Low thermal impedance plastic	160, 184, 208, 240 , 296	High dissipation, low cost
		Ceramic	100 to 304	High dissipation
		Face-down ceramic	144, 184, 304	High dissipation
		AlN ceramic	160, 208, 240, 304	High dissipation
	QFJ (PLCC)		44, 68, 84	
	QTP (TCP)		120 to 504	Thin, high pin count
	BGA	Plastic	225, 256, 352	High pin count
		Tape	256, 304, 352, 420, 480, 500, 576	Small size, high dissipation, high pin count
		Ceramic	In development	High pin count
	CSP (FBGA)		In development	Small size
Chip	Bare chip		Consult with Toshiba.	
	Flip chip		Consult with Toshiba.	

Use the Package Selector Guide

Use the package leaflet to check the package types with adequate lead counts available for your device. Once you have decided on a package, refer to the Toshiba "*ASIC Packaging*" for detailed information on package outlines, lead pitches, pinouts, dedicated power pin allotments, thermal impedance values, and so on.

Thermal Performance Considerations

The circuit's power dissipation causes chip's junction temperature to rise, increasing its propagation delay. The increase in junction temperature is a direct function of the thermal impedance of the package.

Since the rise in junction temperature also affects the device reliability and device life, you should take the package's thermal performance into consideration; this is especially required for large, fast circuits.

The increase in chip's junction temperature (T_j) can be determined by multiplying the total power dissipation (W) in your circuit by the thermal impedance (θ_{ja}) of the package you have chosen. Hence:

$$Tj = Ta + (\theta ja \times W)$$

where Ta is the ambient temperature.

The maximum allowable junction temperature (Tj) for Toshiba ASICs is 85 degrees C. If there is a possibility of the chip's temperature exeeceding this, please consult with the Toshiba ASIC service group.

For thermal impedance values for packages available from Toshiba, refer to the Toshiba *ASIC Packaging*.

Chapter 3

Customer Interfacing

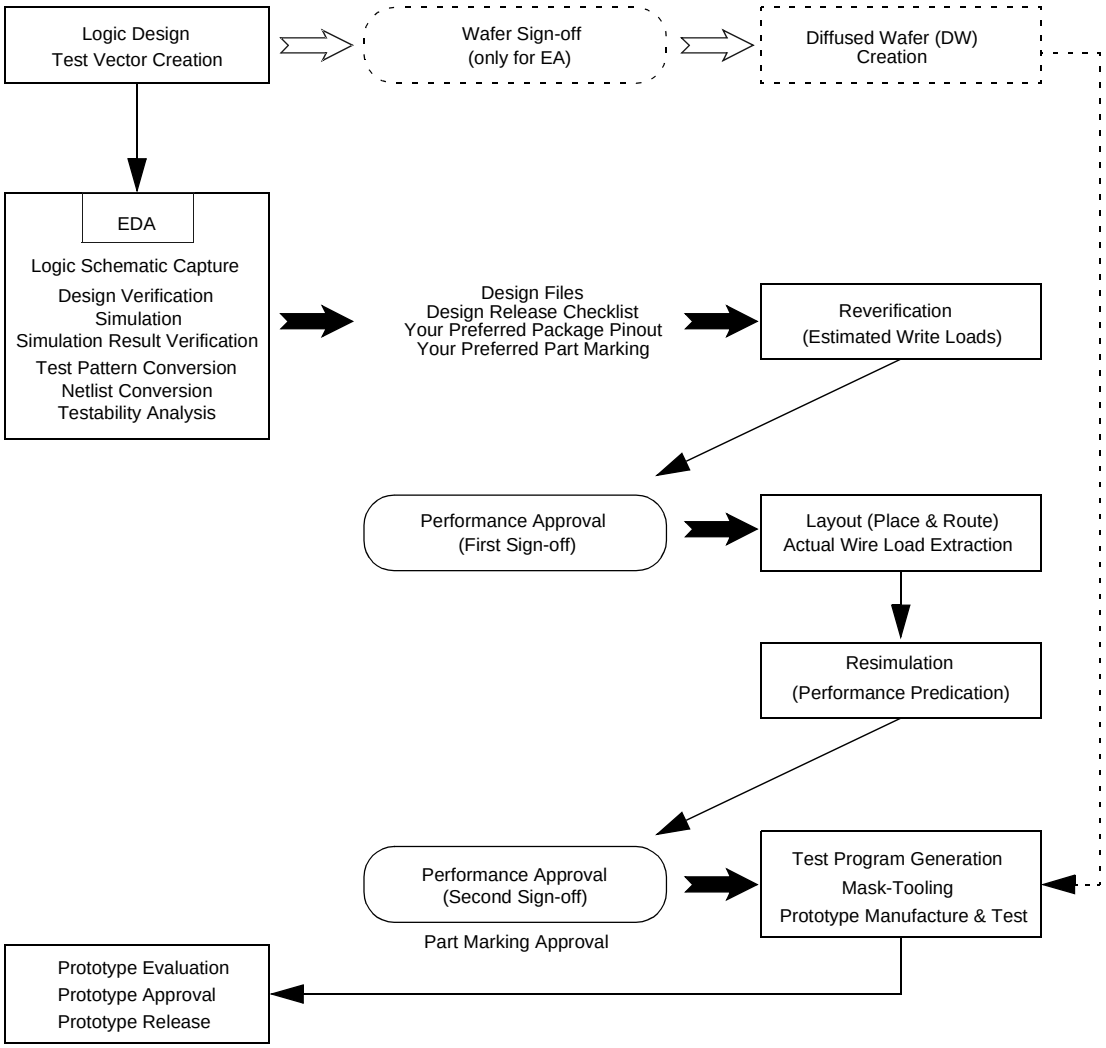
This chapter is organized as follows:

3.1 ASIC Development Flow

Rules & Tips

- **Figure 3-1 illustrates the ASIC development flow and our customer interfacing methodology. The design of an ASIC follows a procedure that includes these steps: 1) design capture, 2) design verification, 3) delay calculation, 4) logic simulation, 5) chip layout, 6) resimulation, 7) prototype manufacture and test.**

Figure 3-1 ASIC Development Flow



The sequence of steps is:

1. *(Embedded arrays only)* With the embedded array methodology, the appropriate area of gates, embedded memory, core functions, and the number of I/Os are agreed upon by you and Toshiba. The Wafer Sign-off Report is completed by you and Toshiba.
2. Your design is captured into a Toshiba-supported EDA system.
3. The captured design is then verified that it fits into the selected array and that it fully complies with the electrical design rules.
4. The rise and fall delays of each cell in the design are calculated using statistically estimated wire loads.
5. Test pattern files are created, and the design is simulated.
6. The First Sign-off Report (Performance Approval) is completed by you and Toshiba.
7. Layout is performed, usually by Toshiba. IC layout is also referred to as place-and-route. It involves *placing* cell overlays on a map or plot of the selected array, and then *routing* interconnect wires between logic cells and to the I/O pads.
8. The final delay values are recalculated based on the actual physical layout, and the design is resimulated.
9. After post-layout simulation, the Second Sign-off Report (Final Performance Approval) is completed by you and Toshiba.
10. Prototype chips, formally known as engineering samples or ES for short, are manufactured by Toshiba and sent to you for evaluation.

3.2 Formal Milestone Documents

Rules & Tips

- **During the design cycle, formal milestone documents requiring signatures are exchanged between you and Toshiba . The signatures (yours and the Toshiba representative's) indicate acceptance of the design at its various stages and authorize Toshiba to proceed with the next step.**

Once you have submitted any of the milestone documents, you can not make changes to the array size or to your design. Any engineering changes will entail additional charges and rescheduling.

Wafer Sign-off Report

When the embedded array methodology is employed, early in the design cycle the appropriate area of gates, embedded memory, core functions, and the number of I/Os are agreed upon by you and Toshiba. Your signature on the Wafer Sign-off Report authorizes commencement of *design-specific* diffused wafer generation.

The Wafer Sign-off must be completed at least four weeks before the schedule for Second Sign-off.

First Sign-off Report

If the results of pre-layout simulation is satisfactory, you and the Toshiba ASIC Department representative sign the First Sign-off Report, releasing the design to layout.

Second Sign-off Report

If the post-layout simulation shows that your design performs correctly, you and the Toshiba ASIC Department representative sign the Second Sign-off Report, authorizing commencement of mask tooling.

Part Marking Form

The part marking includes a logo (TOSHIBA or your company's), product code, production lot number, and the country of origin. If you wish a custom part marking, you can specify your company logo or part number or both, depending on the package type and size. As a rule, custom part marking is printed on only production devices.

A diagram of your preferred part marking should be submitted to Toshiba by the time of First Sign-off.

Figure 3-2 **Part Marking Example**

The Toshiba *ASIC Packaging* details part marking specifications.

3.3 Customer Interface Levels

Rules & Tips

- **The degree of customer involvement in the sequence of ASIC development is called "customer interface." You can involve with us as early or as late on the process as you choose, at a wide variety of levels from design capture through physical layout.**

Toshiba offers a number of levels of customer interface levels, providing a flexible ratio of cost to customer involvement. While our many interface levels are well defined, our interaction with you can be tailored in any way to fit your unique needs.

For example, our interaction flexibility includes acceptance of timing specifications instead of completed test pattern files, and a design netlist file implemented using various library cells other than Toshiba's (e.g., FPGA netlists, RTL HDL codes). If you have special requests, consult with the Toshiba ASIC service group.

- Level 1

  You provide logic schematic diagrams and unsimulated test patterns. Toshiba captures the schematic, and performs the rest of the development work.

- Level 2

  This level is now in disuse.

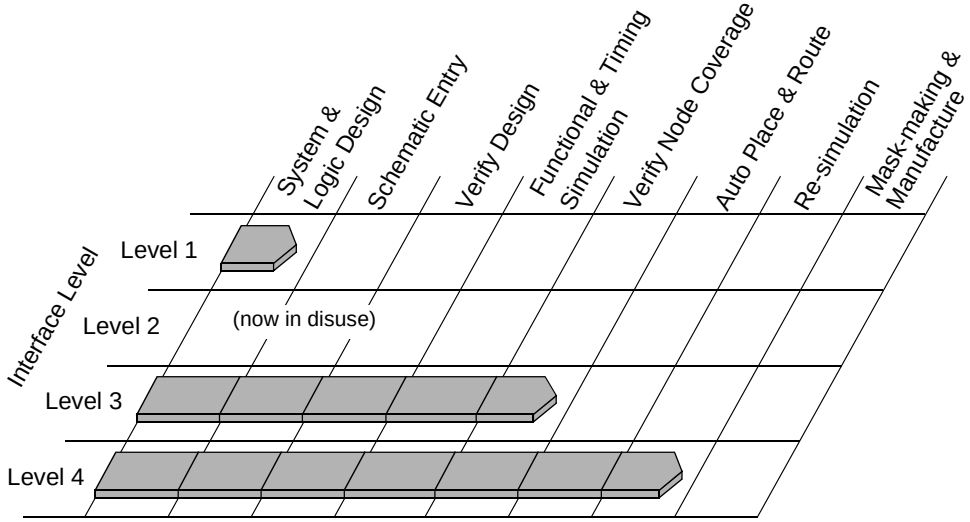
- Level 3

  The Level 3 Interfacing is preferred by Toshiba. In Level 3, you perform design capture and pre-layout simulation using your own EDA tools. Toshiba supplies an ASIC design kit and cell library software. After verifying the circuit's function, you send simulated design files over to Toshiba. Then, Toshiba reverifies your design with a sign-off simulator and carries out the development steps from layout to completion.

- Level 4

  You perform all development work through to mask data generation. The only thing Toshiba is to do is manufacture actual devices.

Figure 3-3 **Customer Interface Levels**



3.4 ASIC Design Environment

Rules & Tips

- **When you choose the Level 3 Interfacing, third-party EDA systems are used as an integral part of the Toshiba design environment. Full implementation is achieved using an EDA system we support and the tools contained in the Toshiba ASIC design kit.**

For each EDA system supported, Toshiba provides a design kit which contains applications and interface software as well as component and technology libraries. Versions exist for Mentor Graphics IDEA Series, Viewlogic Systems Powerview and Workview Office, Cadence Composer and Verilog-XL, and many others.

Figure 3-4 shows the position of third-party EDA systems within the Toshiba design environment.

Designs are entered through a schematic capture tool. The Toshiba design kit contains the schematic symbol libraries.VHDL-based designs using Synopsys Design Compiler, Mentor Graphics AutoLogic, etc. are also supported.

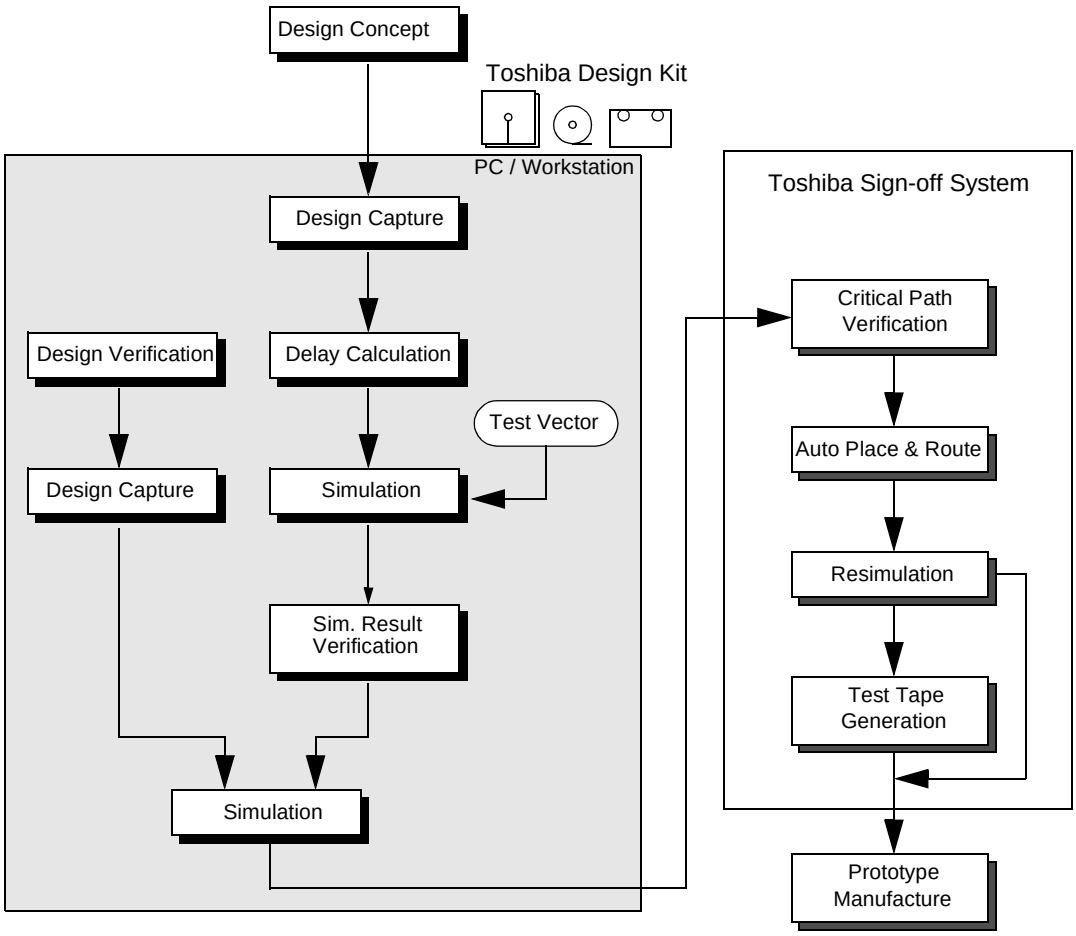
Certified libraries produced and provided by Toshiba allow accurate functional and timing simulations of your ASICs. The delay calculations use estimated wire loads based on Toshiba algorithms. The simulation results verifier program allows you to automatically compare the expected output values with the results of simulation. Additionally, relevant ASIC design rule compliance can be confirmed by the design verifier program included in the design kit.

The test patterns required by Toshiba to complete and test your design include both the input and expected output of your ASIC. The results of simulation from EDA systems can be used as the expected output patterns or you can develop them along with input patterns.

The netlister program converts the verified design information into a compatible file (called TDL) for transferring to our sign-off simulator.

For detailed information and assistance, contact the Toshiba ASIC service group.

Figure 3-4 **EDA Systems and the Toshiba Design Environment**



3.5 Requesting ASIC Design Kits

Rules & Tips

- **When you choose Level 3, ask the Toshiba ASIC service group for an appropriate design kit compatible with your hardware platform. If your design has such cells as megacells, oscillator cells, scan flip-flops, or JTAG cells, also request delay/simulation model files for them.**

EDA Support

Table 3-1 gives the support availability for Toshiba ASIC design kits. Contact the Toshiba ASIC service group for the latest information about which hardware platforms and array series are supported.

Table 3-1 Supported EDA Systems (as of August, 1996)

Category	Vendor	EDA Tool
Sign-off tools	Toshiba	VLCAD
	Toshiba / Cadence	Verilog-XLSign-off System (VSO)
	Toshiba / Viewlogic	VCS Sign-off System (VCSSO)
	Toshiba / IKOS	Voyager Sign-off System
	Toshiba / Cadence	Vital Sign-off System (Leapfrog)
	Toshiba / Mentor	Vital Sign-off System (QuickHDL)
	Toshiba / Model Techlonogy	Vital Sign-off Sign-off System (V-system)
	Toshiba / Synopsys	VSS Sign-off System (VSSSO)
Schematic capture tools	Mentor	IDEA Series
	Viewlogic	Powerview, Workview PLUS, Workview Office, FusionVCS
	Cadence	Concept, Composer
Simulators	Cadence	Verilog-XL
	Zycad	Paradigm XP
	Synopsys	VSS
	IKOS	2800/2900, Voyager
Timing analyzers	Synopsys	DesignTime
	Viewlogic	MOTIVE
Logic synthesis tools	Synopsys	Design Compiler
	Mentor	AutoLogic II

Category	Vendor	EDA Tool
Design-for-test tools	Synopsys	Test Compiler
	Viewlogic	TestGen
	Mentor	DFTAdvisor, FastScan

Design Kit Request

The ASIC design kit is comprised of two software packages: a program package and a library package. The program package is common to all array series. There are different library packages for different array series.

In order to obtain a correct design kit for your hardware platform and EDA tool, please take a few moments and prepare the Design Kit Request. A blank form is attached in Appendix C.

Special Cell Request

The library package contains only commonly-used macrocells (primitive cells) and macrofunctions (softmacrocells). It does not contain megacells and megafunctions (compilable cells and hardmacrocells) since such cells as RAMs and ROMs give thousands of types by different word/bit configurations. Also, oscillator cells, scan flip-flops, and JTAG cells are not stored in the standard library package.

If you are planning to use any of these cells, please prepare the Design Kit Request. A blank form is attached in Appendix C.

Compilable cells for cell-based ICs and embedded arrays offer several aspect-ratio-type options. Which aspect-ratio type is appropriate depends on its ac performance and IC floorplan. Consult with the Toshiba ASIC service group for selection of a proper type.

When non-standard delay multipliers are agreed upon by you and Toshiba for best- and worst-case simulations, the ASIC design kits for certain (but not all) EDA systems need to be customized according to your specifications.

3.6 Design Release

Rules & Tips

- **When you have completed all the pre-defined jobs, you will turn your design over to Toshiba for reverification and formal acceptance. Table 3-2 lists required files.**

Please make sure that you have prepared all the required design files and documents to be handed over to Toshiba. Bear in mind that should any one of them be missing, smooth transitions between design phases may not be ensured.

Design Release Package

The transfer of design data (netlist, test patterns, etc.) to Toshiba for resimulation and chip layout is referred to as "design release." Table 3-2 gives soft copies of your design data files and documents to be submitted to Toshiba.

Table 3-2 Design Release Package List

Design Data	Level 1 Interface	Level 3 Interface
Initial Specifications (Appendix A)	Required	Required
Design Release Checklist (Appendix B)	1. Sections I, III, VII, and VIII (wherever possible). 2. Special Layout Request 3. Pinout Plan	Fill in all pages.
Schematics (hardcopy)	Any format	When requested
Test data	Any format	TSTL2 format
Design netlist	n/r	Toshiba TDL or gate-level Verilog-HDL or VHDL
ROM data	Any format	Toshiba format
Execution listings generated by Design Verifier and Sim. Results Verifier programs	n/r	Required
Part marking diagram	Required	Required

Medium

Store design files in one of the magnetic media listed in Table 3-3 below.

Table 3-3 Design Release Package Media

MS-DOS (3.5” floppy disk)		2DD (720kB)
		2DD (1.44kB)
		2HD (1.44kB)
Sun (SunOS 4.1.x)	3.5” floppy disk	2DD (720kB)
		2HD (1.44kB)
	Tape	1/4” tape cartridge
		8mm tape cartridge
HP (HP-UX 9.0x)		DAT

- Attach a label to each floppy disk or tape cartridge, identifying its content, the operating system used, and the commands used to archive the files and to be used to extract them.
- Divide a file too large to be contained in one floppy disk into two or more disks.
- Prepare two sets of the package in case of I/O errors.
- If you wish the floppy disks or tape cartridge to be returned, please indicate so.

If you want to use a medium not listed in Table 3-3, consult the Toshiba ASIC service group.

You can create your preferred pinout specification as a disk file. The file can be an ASCII text file, or a word processor or spreadsheet software file.

3.7 Special Layout Specifications

Rules & Tips

- **You can include two kinds of layout specifications in the Design Release Checklist, critical paths and soft cell groups, to assure the timing and speed requirements of your design. Layout software lets us take a number of strategies to meet these goals.**

Critical Path Specifications

You can indicate how critical certain nets or paths are in terms of their speed requirements by specifying the minimum and/or maximum propagation delays to be met. Critical path specifications influence the placement of cells to ensure that all the cells on the path are placed close together.

You can define a path with a head and a tail pin. A head pin can be an external input pin or a clock input of a flip-flop. A tail pin can be an external output pin or a data input of a flip-flop.

The maximum delay specifications should be under the worst-case simulation condition; the minimum delay specifications should be under the best-case simulation condition.

Soft Cell Grouping

During placement, cells can be grouped together according to specified constraints. Soft cell groups cluster specified cells inside a rectangular region of specified dimensions. The cells in a soft group are not fixed in relative placement, but all cells in a soft group are placed in proximity.

Grouping closely-coupled logic functions together (and keeping functions with little connectivity in separate areas of the chip) enables the layout tool to perform the best job. In addition, small blocks will have small errors in wire lengths estimations and therefore more accurate wire delay estimates.

On the other hand, cell grouping could cause interconnection paths between groups to get longer than expected or the chip routability to be lowered.

Figure 3-5 Special Layout Specifications

Special Layout Specifications

I. Critical Paths

Source Pin	Destination Pin	Maximum Delay (at worst-case)	Minimum Delay (at best-case)
e.g. External input DATA	External output OUT	20.0 ns	10.0 ns
e.g. F/F input I001/I0014(CP)	F/F input I010/I002(D)	10.0 ns	—

.....

II. Preferred Soft Cell Grouping

Group internal cells of the following instances of module SUB1.

I001/I0014

I001/I0015

I001/I0016

3.8 Prototype and Production Parts

Rules & Tips

- **Toshiba provides a considerable flexibility in the supply of prototype parts, as shown in Table 3-4. Order additional prototype parts by the time of Second Sign-off.**

Prototype Parts

The paragraphs that follow describe different types of ASIC parts available from Toshiba.

- KS

  Upon receipt of the Second Sign-off Report, Toshiba begins mask creation, and manufactures prototypes formally known as KS. The KS parts (normally 10 pieces) are furnished as a part of the base NRE fee.

- ES

  Any additional parts are to be ordered at extra cost if desired. These parts are identified by ES. The ES is normally furnished in ceramic, and is limited to 50 parts. ES parts are functionally tested only (no dc, temperature, parametric, package quality or environmental tests).

- HS

  Samples are available which have been packaged in the final production package AND which have received full production testing. These parts are identified by HS. As such, they can be used for qualification and/or used in pilot or initial production designs. The customer is at risk for these parts, however. HS parts are available in quantities ranging from 50 to 500.

ES and HS parts must be ordered in writing by the time of First Sign-off.

Initial Production

Production parts, known as CS, are standard, fully-tested parts delivered as a part of the normal manufacturing cycle. Lead time is the time from placement of the purchase order with Toshiba to the first shipment of parts against that purchase order. Lead time is counted only from approval of ES and receipt of

the production purchase order. Fulfillment of initial production quantities takes longer than prototypes. Normally, lead times to gate array production are approximately two months. Lead times to cell-based ASICs are approximately three months.

- Risk parts

  These are parts which are started before the customer has given ES approval, and can be part of the initial production parts (CS). Since the parts are started before verification of ES, all parts of this type are ordered at customer "risk" — total liability for payment, even in the event of design error (i.e., except that the malfunction is obviously attributed to production process). For risk start (or flying start), there must be specific, confirmed approval from Toshiba, written, non-cancellable purchase order from the customer, and a customer-signed waiver stating customer liability for these parts.

Table 3-4 Prototype Availability

Type	Packaging	Quantity	Part Marking	Screening
KS	Ceramic	10 pcs	Makeshift Toshiba marking	Function only
ES	Ceramic	Up to 50 pcs	Makeshift Toshiba marking	Function only
HS	Plastic	50 to 500 pcs	Toshiba standard marking[2)]	Function only
CS	Plastic	100 or more pcs	Customer-specified marking	Function, dc and ac

* The customer-specified marking can be optionally used.

Prototype quantities and marking can be tailored to customer's needs. If you have special requests, contact your Toshiba design center engineer.

3.9 Documentation

Rules & Tips

- **Ask the Toshiba ASIC service group for the current versions of ASIC documents whenever you begin a new design. Note that newer versions supersede older versions. For example, cell specifications may change.**

Catalogs

- Toshiba CMOS ASIC
- Toshiba ASIC Packages
- ASIC EDA

Data Books

- Gate Arrays
  - TCxxxG Series Macrocells
  - Gate Array/Embedded Array Macrofunctions
  - TCxxxG Series Megacells/Megafunctions
- Cell-based ICs
  - TCxxxC Series Primitive Cells / I/O Cells
  - TCxxxC Series Softmacrocells
  - TCxxxC Series Hardmacrocells/Compilable Cells/Analog Cells
- Embedded Arrays

  Embedded array designs can include all types of gate array cells (macrocells, macrofunctions, megacells/megafunctions), and cell-based IC's hardmacrocells and compilable cells (but not analog cells).

EDA Operation Manuals

- Powerview/Workview PLUS Design Capture
- Powerview/Workview PLUS User's Reference Manual
- Powerview/Workview Office
- Verilog-XL/VCS Sign-Off System
- Verilog-XL (non-sign-off version)
- VOYAGER Sign-Off System User's Manual

- Mentor System (V8)
- VLCAD System
- VLCAD/DFT User’s Manual

Others

- CMOS ASIC Design Manual
- TDL, TSTL2, ROM Data
- ASIC Packaging
- Design-for-Test (DFT) Handbook

Chapter 4

Circuit Design Techniques

This chapter is organized as follows:

4.1 Delay Calculation

Rules & Tips

- **Bear in mind that a number of factors affect the macrocell's propagation delay — RC-tree effects of interconnect, power supply voltage, die temperature, process deviations, chip's power dissipation, packaging, cooling method, etc.**
- **Delay calculation and simulation are performed twice: once before layout and once after layout.**

Causes of Propagation Delays

When you have completed your gate-level design, you run the delay calculation program prior to simulation to obtain propagation delays for each macrocell in your design. The macrocell's propagation delay is the sum of its intrinsic delay and load-dependent delay. In addition, as the semiconductor process advanced to deep-submicron, RC-tree delays of interconnect wires have increasingly greater impact on the total wire delays.

The circuit's propagation delays are also affected by the variations in the power supply voltage, die temperature, and manufacturing process.

Furthermore, chip's power dissipation — strong functions of circuit's operating frequency, gate complexity, and output loading — causes the die temperature to rise, increasing a circuit's propagation delay. Thermal impedance of the package the chip will be put into as well as the cooling method used (active cooling, free air, heat spreader, etc.) have an impact on the rise in die temperature, thus propagation delay.

Estimated vs. Actual Delays

Prior to layout, the delay calculator estimates the probable wire loads, using the size of the chip and the number of driven inputs. Because it makes use of estimated wire loads, the delay calculation is of necessity approximate; but they are based on a considerable statistical history.

After layout, the delay calculator reads in an actual wire length file, and back-annotates the actual (versus estimated) wire loads into the simulator for post-layout verification. RC analysis is added to this wire length file, along with the normal wire lengths appropriately for each net.

The subsections that follow will discuss the delay calculation equations and the tools available to improve wiring estimation.

4.1 Delay Calculation

4.1.1 Internal Propagation Delays

Rules & Tips

- **Propagation delay times are dependent on the loads that cell outputs drive. However, wire can not be determined until a layout is generated for the circuit. So, before layout, statistically estimated wire loads are used for delay calculation.**

The propagation delay of a macrocell is the sum of its intrinsic delay (Tup/Tdn) and the loading delay associated with the macrocell output. The equations for calculating a macrocell's low-to-high (TpLH) and high-to-low (TpHL) propagation delay are:

$$TpLH = Tup + Kup\ (F.O. + EWL)$$
$$TpHL = Tdn + Kdn\ (F.O. + EWL)$$

where:

Tup/Tdn	Intrinsic macrocell delays from low-to-high and high-to-low transitions
Kup/Kdn	Low-to-high and high-to-low loading delays caused by one equivalent loading unit (LU). A standard loading unit of 1 is defined as the sum of a P- and an N-channel MOSFET gate capacitance. The load consists of the following two elements.
F.O.	Fanout load. A macrocell's fanout is equal to the number of "input loads" it drives. An "input loading factor" is assigned to the inputs of each macrocell and is used to indicate how large a capacitive load is associated with each input.
EWL	Estimated wire load. Prior to layout, probable wire loads are statistically estimated, using the size of the chip and the number of driven inputs as a basis for estimation.

Figure 4-1 **Macrocell Model Data Sheet**

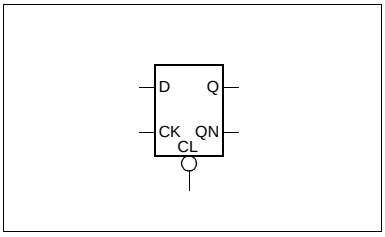
TC180G00 SERIES

MACROCELL DATA SHEET

FD2x | FD2x

SELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD2	D-TYPE FLIP FLOP with CLEAR	8	0	V_{DD}=3.3V, Ta=25°C, Typ.
FD2P		9	0	

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT	
CD	D	CP	Q_{n+1}	QN_{n+1}
L	x	x	L	H
H	L	↓	L	H
H	H	↓	H	L
H	x	↓	Q_n	QN_n

TDL DESCRIPTION

Name (Q, QN) = FD2x (D, CP, CD);

INPUT LOAD (LU)

CELL \ PIN	D,CP	CD
FD2	2.0	2.0
FD2P	2.0	2.0

OUTPUT DRIVE (LU)

CELL \ PIN	Q,QN
FD2	33
FD2P	68

AC CHARACTERISTICS

CELL	PATH	TpLH		TpHL	
		Tup	Kup	Tup	Kup
FD2	CP→Q	0.46	0.048	0.68	0.026
	CD→Q	-	-	0.39	0.026
	CP→QN	0.60	0.048	0.74	0.026
	CD→QN	0.30	0.048	-	-
FD2P	CP→Q	0.50	0.023	0.72	0.014
	CD→Q	-	-	0.43	0.014
	CP→QN	0.67	0.023	0.81	0.014
	CD→QN	0.32	0.023	-	-
UNIT		ns	ns/LU	ns	ns/LU

SCHEMATIC

Figure 4-2 **An EWL Table**

Double-Layer Metal	
Part Number	EWL(LU)
TC180GJ4	2.359 x WAY + 1.180
TC180GF1	2.255 x WAY + 1.128
TC180GB3	2.142 x WAY + 1.071
TC180G84	2.031 x WAY + 1.016
TC180G70	1.961 x WAY + 0.981
TC180G45	1.813 x WAY + 0.906

4.1 Delay Calculation

4.1.2 External Input/Output Buffer Delays

Rules & Tips

- **Separate input buffers are used for TTL and CMOS interface.**
- **The same output buffer can directly drive both TTL and CMOS components. Output buffer propagation delay is dependent on the type of the component being driven, however.**

External Input Buffers

For how to determine the propagation delays from outside parts to the ASIC input buffers (or the input portions of bidirectional buffers), refer to the parts catalog from the vendor of the driving part. The input capacitance values of ASIC input buffers are shown in the “INPUT CAPACITANCE” section in the Toshiba data book.

External Output Buffers

Output buffer propagation delay is a function of buffer type, capacitive load, and type of device being driven. The equation for calculating the propagation delays of external output buffers (or the output portions of bidirectional buffers) are:

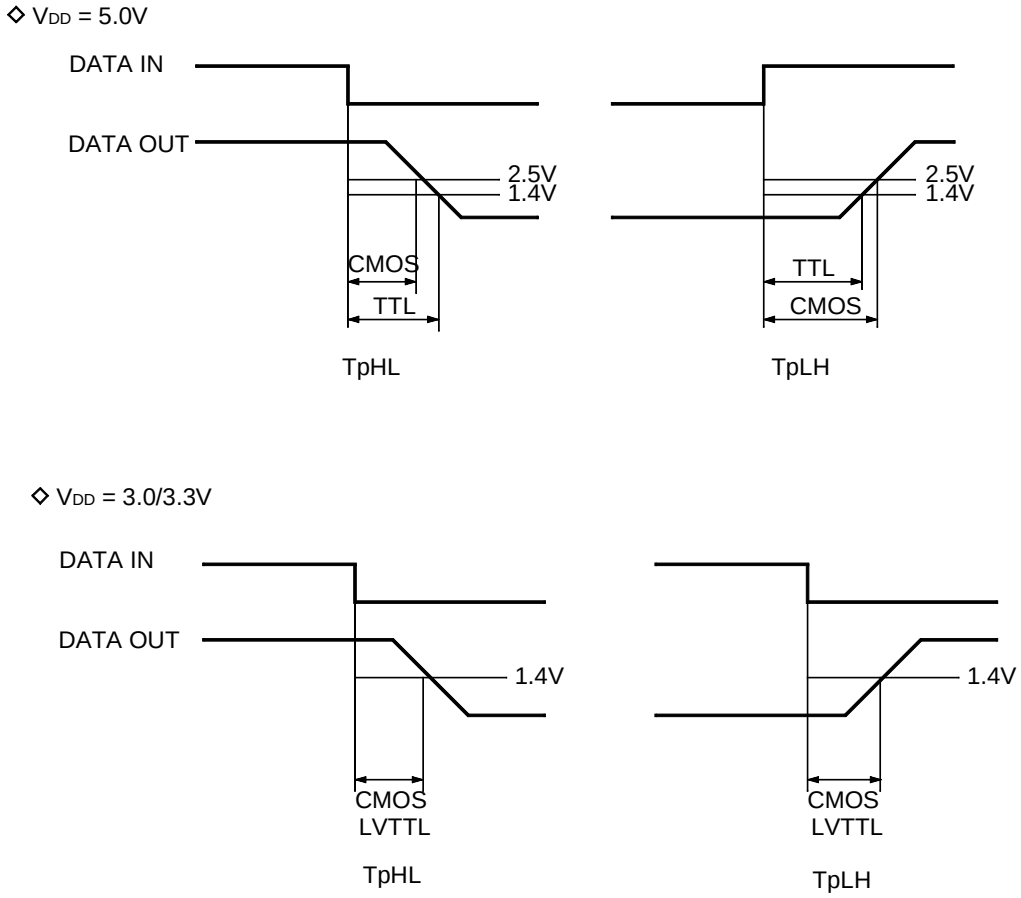
$$TpLH = Tup + Kup \times C_L$$
$$TpHL = Tdn + Kdn \times C_L$$

where C_L is the driven capacitive load in pF outside the ASIC. Note that Kup and Kdn factors differ, depending on the technology type of the driven device (CMOS or TTL/LVTTL).

When driving 5V CMOS chips, output buffer propagation delays are measured from their inception to the time at which the signal achieves the CMOS threshold of 2.5 volts. When driving 5V TTL chips, the delays are measured from their inception to the time at which the signal achieves the TTL threshold of 1.4 volts.

When driving 3V chips regardless of their types, output buffer propagation delays are measured from their inception to the time at which the signal reaches 1.4 volts.

Figure 4-3 **Propagation Delays of Output Buffers**



4.1 Delay Calculation

4.1.3 Variations of Propagation Delays

Rules & Tips

- **All macrocell propagation delays are sensitive to power supply voltage, die temperature, and manufacturing process deviations. The circuit's power dissipation — a function of the operating frequency, and the number of gates and I/Os — causes temperature to rise, increasing propagation delays.**

Supply Voltage, Temperature, and Process Factors

Macrocell propagation delays are sensitive to the supply voltage, temperature, and process variations. The Toshiba data books show delay parameters under the nominal (typical) conditions — a 3.3- or 5-volt power supply, 25°C temperature, and nominal process model. Process variation could increase or decrease delays by up to 50%. Thus, a multiplier factor called K_p is used to estimate the effect of best- and worst-case processing. The K_p varies slightly by silicon technology. Die's junction temperature (K_t) and supply voltage variation (K_v) also affect the delays. Multipliers for K_t and K_v are shown in Figure 4-4 and Figure 4-5, respectively. The formula for calculating delay multipliers (known as K-factors or K_f) is:

$$K_f = K_p \times K_t \times K_v$$

Figure 4-4 **Propagation Delay as a Function of Temperature**

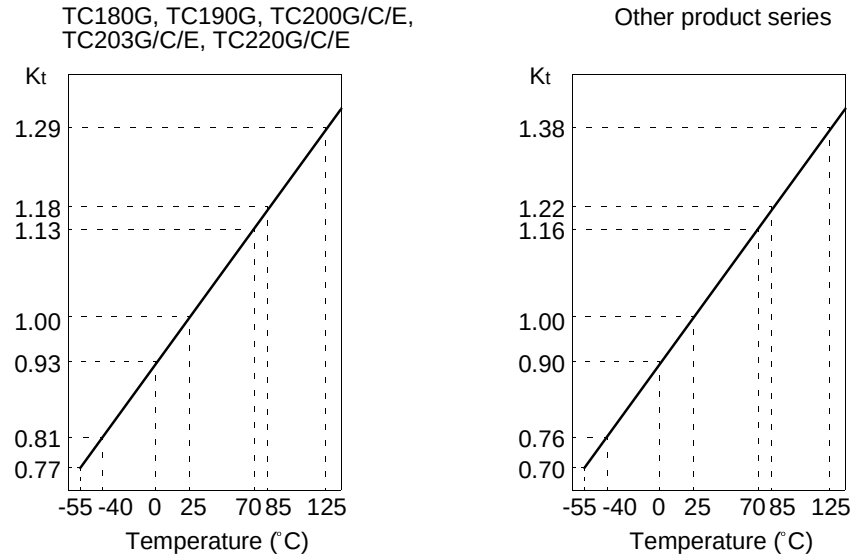
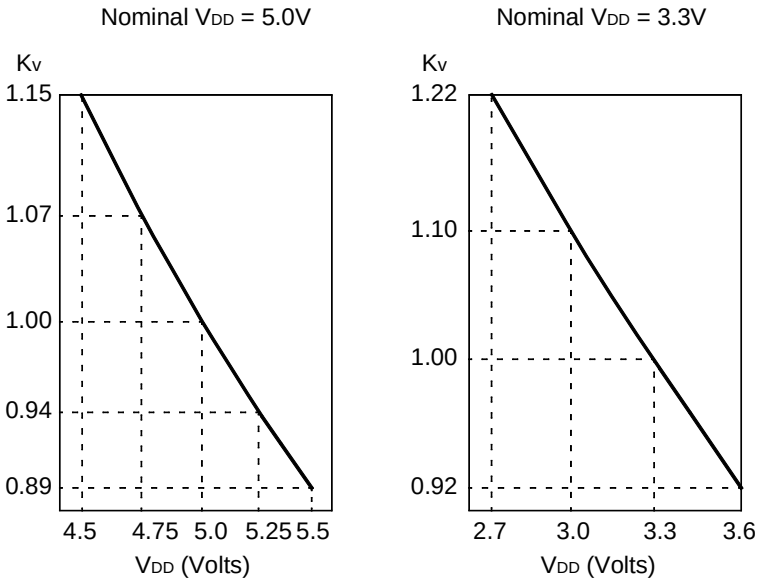


Figure 4-5 **Propagation Delay as a Function of Supply Voltage**



Power Dissipation Factor

Power dissipation causes die temperature to rise, increasing a circuit's propagation delay. The increase in die's junction (T_j) temperature can be determined by multiplying the total power dissipation (W) in your circuit by the thermal impedance (θ_{ja}) of the package you have chosen. Hence:

$$Tj = Ta + (\theta ja \times W)$$

where Ta is the ambient temperature.

For thermal impedance values for packages available from Toshiba, refer to the Toshiba *ASIC Packaging*.

4.1 Delay Calculation

4.1.4 Wiring Estimation Issues

Rules & Tips

- **As levels of integration and circuit's speed increase, accurate timing estimation at an early stage of the design becomes increasingly important. Heavily-loaded clock nets as well as the nets from I/O cells and large megacells tend to have a disparity in wire load estimates.**

In the deep-submicron ASIC realm, wire delay becomes dominant over the interior gate delay. That is a condition with which traditional logic design tools have not been equipped well to deal. If you looked at the wiring a few years ago, it was only 20 percent of total delay. At deep-submicron, wiring could account for more like 50 percent of the total.

Both timing errors and layout iterations can increase as feature size drops. Consequently, post-layout identification of wiring problems can result in costly iterations and time-to-market delays.

The most critical nets that affect the overall timing are:

- clock nets
- nets from I/O cells and megacells

Clock Nets

Smaller geometries mean narrower metal lines having higher resistance per length of wire. For deep-submicron processes, the wiring must be modeled as an RC tree network of distributed resistors and capacitors. This model allows more accurate calculation of the delay introduced by the wire and takes into account that the driven gates receive the signal transition at different times. A signal takes much longer to reach a gate all the way across the chip than it does to reach a gate close to the gate driving the wire.

RC-delay approaches are especially important for clock nets that are timing critical and are usually associated with a heavy load (which means clock nets are prone to large skew). However, RC-delay approaches work only after the information about physical aspects of the design is made available.

It is important to reduce the impact of deep-submicron on wiring estimation and ensure a “one-pass” design cycle without iterations in order to minimize the time-to-market. Toshiba uses its proprietary Toshiba Clock Tree Synthesizer (TCTS) to deskew clock nets. The TCTS will be detailed in Section 4.6.2, *Toshiba Clock Tree Synthesizer (TCTS)*, on page 4-70.

I/O Cells and Megacells

Prior to layout, macrocell delays are estimated, using the size of the chip and the number of driven macrocell inputs as a basis. This estimation is derived, based on a assumption that macrocells will have homogenous distribution across the die as a result of auto-placement.

However, placements of I/O cells and large megacells are very much constrained relative to other macrocells. So, the nets from I/O cells and megacells tend to have a poor correlation in wire lengths beforehand after layout. For logic designers to be able to have access to accurate estimates of wiring for a quick convergence on timing, Toshiba supports third-party floorplanners along with its own design kits. Floorplanners will be described in Section 4.8.2, *Floorplanning Tools*, on page 4-98.

4.2 I/O Cell Considerations

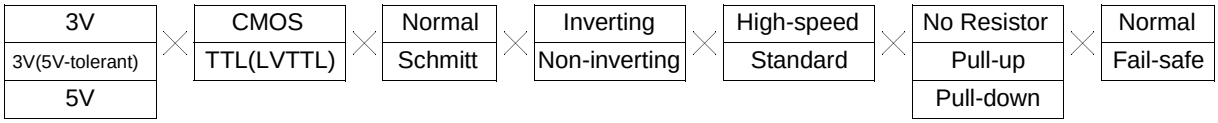
Rules & Tips

- **The Toshiba ASIC cell library contains such I/O cells as input buffers, output buffers, bidirectional buffers, 3-state output buffers, clock drivers, and oscillator cells. System interconnect I/O cells like GTL I/Os, PCI I/Os, and digital PLLs are also included in the library. An extensive flexibility is available in the use of pull-ups/pull-downs, and choice of input voltage levels and output current drive.**

Input Buffers

The various input buffer configurations include CMOS, TTL, inverting/non-inverting, Schmitt trigger, and high-drive clock buffers. Figure 4-6 gives the various types of input buffers available.

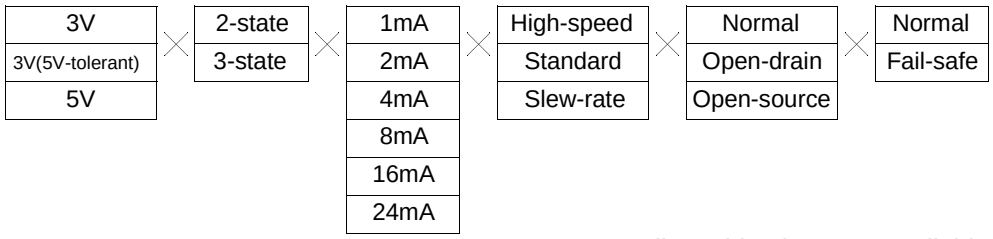
Figure 4-6 Input Buffer Lines (Non-JTAG)



Output Buffers

The various output buffer configurations include slew-rate-control, open-drain, open-source, and 3-state buffers. Output drive strengths of 1, 2, 4, 8, 16, and 24 mA are available. Figure 4-7 gives the various types of output buffers available.

Figure 4-7 Output Buffer Lines (Non-JTAG)



* Not all combinations are available.

Bidirectional Buffers

Bidirectional buffers are configured using a 3-state output buffer and an input buffer, and are available from the library. The diversity in the types of 3-state output buffers and input buffers give a total of three to four hundred bidirectional buffer types.

System Interconnect Buffers

For high-speed inter-chip communications, the Toshiba ASIC series provide these data interface I/Os: Peripheral Component Interconnect (PCI), Gunning Transceiver Logic (GTL), Low-Voltage Differential Signalling (LVDS), and Digital Phase-Locked Loop (DPLL).

4.2 I/O Cell Considerations

4.2.1 I/O Protection

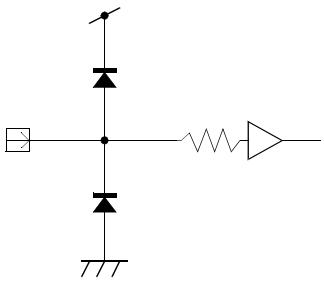
Rules & Tips

- **Do not tie any ASIC package pin to a voltage level above the maximum rated supply voltage of the ASIC, or the device may be permanently damaged.**
- **If power to the ASIC may be removed on the fly, use fail-safe type I/O buffers.**

Input Protection Circuit

CMOS devices have an insulated gate oxide that is subject to voltage breakdown. So, all input, output, and bidirectional buffers have an input protection circuit against voltage surges. An input protection circuit consists of a series resistor with diodes returned to V_{DD} and V_{SS}, as shown below in Figure 4-8.

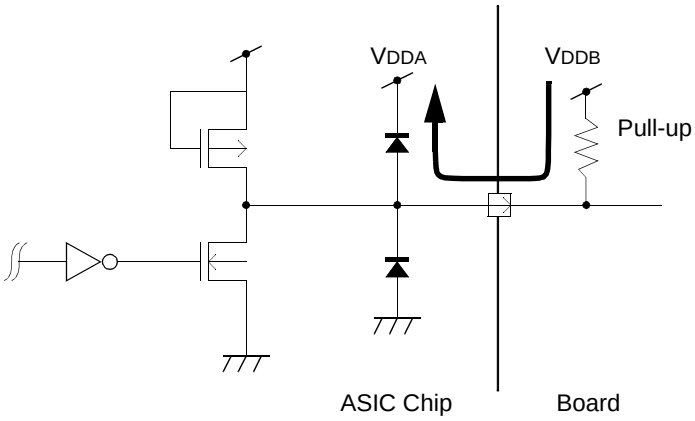
Figure 4-8 Input Protection Circuit



Diodes, while in the recommended operating range ($V_{SS} < V_{in} < V_{DD}$), can be modeled as resistors, representing the reverse bias impedance of the diodes. When a voltage outside the recommended operating range of the ASIC is applied to the input, the diode conducts, causing excessive current drain, as illustrated in Figure 4-9.

When you connect an ASIC's 3-state output or bidirectional pin to a system power bus via an external pull resistor, the system power supply range must be within the recommended operating range of the ASIC. Any ASIC pin may never be tied to a voltage level outside the maximum rated supply voltage of the ASIC; any voltage above this may destroy the device.

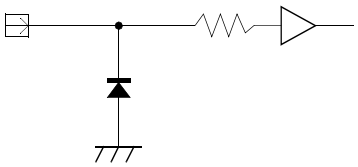
Figure 4-9 **Current Drain**



Fail-safe I/O Buffers

Fail-safe I/O buffers are provided for bus applications that will not load the active bus when power is removed. These I/O buffers does not have a diode returned to V_{DD}. They enable “hot plug” operation where a card is inserted while the system is running. This produces a state where the driven device is being powered while power is removed from the ASIC. (In this state, the V_{DDA} potential becomes equal to the ground level in Figure 4-9 above.)

Figure 4-10 **Fail-Safe Input Buffer**



4.2 I/O Cell Considerations

4.2.2 Input Buffers

Rules & Tips

- **Use standard-drive, not high-speed, input buffers to drive timing non-critical paths.**
- **Use a Schmitt trigger input buffer for slowly changing or noisy input signals.**
- **Never use an input buffer with pull-up or pull-down as a substitute for an external pull resistor attached to a system bus.**

Standard and High-Speed Input Buffers

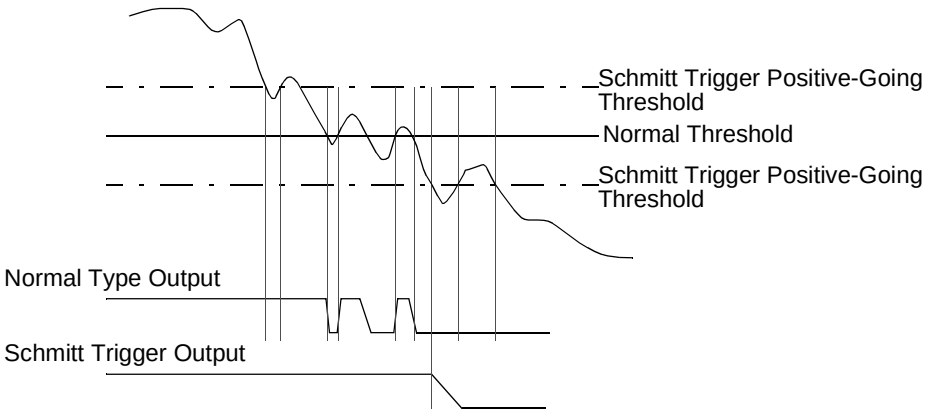
Input buffers are available in standard and high-speed versions. Standard versions help to keep down system noise, and should be used to drive all inputs that are not timing-critical.

Schmitt-Trigger Input Buffers

Schmitt-trigger input buffers exhibit the effect of hysteresis. Hysteresis prevents the element from reacting to noise by the inclusion of two different switching threshold levels for positive- and negative-going input transitions. In addition, Schmitt-trigger input buffers provide excellent noise immunity and the ability to square up slowly changing signals.

Be sure to use a Schmitt-trigger input buffer when the input transition time is on the order of tens of nanoseconds and that input is applied to an edge-sensitive element.

Figure 4-11 A Schmitt-Trigger Input Buffer Offers Maximum Noise Immunity



Input Buffers with Pull-up/Pull-down

Internal pull-up and pull-down resistor options are available with input buffers. Pull resistors can be used to prevent input buffers from floating to an indeterminate state when they are not being driven by an external source. Internal pull resistors of input buffers have a resistance in the range of tens to hundreds of ohms.

Pull resistors are not meant to replace external pull-up or pull-down resistors on the PCB which are attached to 3-state open-drain buses.

5-V-Tolerant I/O Buffers

The 3-V ASIC families offer extended-voltage-range I/O cells to provide flexible solutions for designers of 3-V ASICs implementing them in mixed 3/5-V systems. The 5-V-tolerant input buffers are designed to tolerate the reception of the larger voltage swing of 5-V signals, while being powered by 3.3 V. The 5-V-tolerant output buffers are in open-drain configurations to prevent floating on-chip drivers from being driven by a system 5-V power bus.

The 5-V-tolerant input buffers have a pull-up resistor after the level shifter. These input buffers are therefore maintain the V_{DD} level (3.3 V) when their input pads are left open, not being driven by a signal. However, in actuality, a voltage drop occurs at the pad due to the level shifter, thereby lowering the voltage at the pad below the V_{DD} level.

4.2 I/O Cell Considerations

4.2.3 Output Buffers

Rules & Tips

- **Output-buffer's current capabilities are rated with V_{OL}=0.4V and V_{OH}=2.4V.**
- **Output buffers with slew rate control help to minimize unwanted current noise.**
- **Choosing output buffers entails a careful consideration on the interface to and configuration of the PCB board. Ringing and signal reflections are two major concerns.**

Output Buffer DC Characteristics

The high- and low-level output currents (I_{OH}/I_{OL}) of the output buffers are measured with input conditions applied that will put the voltage at an output at V_{OH}=2.4 volts and V_{OL}=0.4 volts, respectively. For output current characteristics, see an appropriate data book from Toshiba.

Slew Rate Control Output Buffers

All the Toshiba ASIC series has the option to configure outputs (with 4mA or greater drive) with slew rate control to slow down the output edge rates of signals going off-chip. This feature helps to reduce system noise and overshoot and undershoot of the output signals caused by fast rise and fall times. Output buffers with the suffix "R" offer slew rate control. Example:

- B8 Normal type (8mA output buffer)
- B8R B8 with slew rate control

Ringing

The output buffer's "slew rate," or the time it takes for a signal to switch from logical 0 to logical 1 or vice versa, interacts with parasitic package and bonding wire inductance, causing current spike (known as "abrupt transient current"). This phenomenon is referred to as "ringing."

The ringing or the noise voltage increases as the package/bonding-wire inductance and the switching speed of the output signal increase. Conversely, the ringing is filtered by output load capacitance.

Care should be exercised so that a "backswing" of the noise due to ringing does not cause the next-stage component on the PCB to misread input voltage (and therefore logical) levels. Table 4-1 shows the recommended ranges of output capacitance to avoid ringing problems.

In the event that you have any questions or concerns about the ringing effect, contact the Toshiba ASIC service group.

Table 4-1 **Recommended Output Capacitance Ranges**

(The numbers in the table should be considered merely as a rough guide.)

Normal Type	Capacitance	Slew Rate Type	Capacitance
B1	0-90 pF[1)]	B1R	0-90 pF[1)]
B2	0-160 pF[1)]	B2R	0-160 pF[1)]
B4	10-200 pF[2)]	B4R	0-200 pF[2)]
B8	15-200pF[2)]	B8R	0-200pF[2)]
B16	60-200pF[2)]	B16R	0-200pF[2)]
B24	120-350pF[2)]	B24R	0-350pF[2)]

1. The upper limits are based on Tpd<20ns (typ.)
2. The upper limits are based on a consideration of electromigration resistance at 16MHz.

Reflections

Faster output buffers require a closer look at transmission line effects. Signal reflections occur when the current is delivered to a load whose impedance is not matched to the source. When a wave in one medium is incident upon a discontinuity or a different medium, the reflected wave results in the first medium in addition to the incident wave.

The impedance of the line and the propagation delay down the line are the major concerns in considering signal reflections. The loading of the line decreases the effective impedance of the line and increases the propagation delay. Loads that are between the driving output buffers and the end of the line will receive a two-step waveform. The first wave will be the incident wave. The amplitude depends on the output impedance of the driver and the impedance of the line. It will be one-half the voltage swing (V_{DD}) if the output impedance of the driver is equal to the line impedance. The second step of the wave is the reflection from the end of the line, and will have an amplitude equal to that of the first step. Such signal reflections can cause mischief to I/O circuitry. Since it takes two times the line delay for all receivers to see a valid voltage, the output buffers with edge rates no greater than that pose no reflection problems. Table 4-2 shows the maximum line lengths for different types of output buffers, based on this fact.

In the event that you have any questions or concerns about signal reflections, contact the Toshiba ASIC service group.

Table 4-2 **Maximum Line Lengths for Avoiding Reflection Problems**

(The numbers in the table should be considered merely as a rough guide.)

Case 1: Output Load=15pF		Case 2: Output Load=50pF	
Output Buffer	**Line Length**	**Output Buffer**	**Line Length**
B1	~35 cm	B1	~120 cm
B2	~20 cm	B2	~70 cm
B4	~10 cm	B4	~30 cm
B8	~8 cm	B8	~18 cm
B16	~5cm	B16	~12 cm
B24	~4cm	B24	~ 8 cm

4.2 I/O Cell Considerations

4.2.4 Bidirectional Buffers

Rules & Tips

- **A great care should be taken when a bidirectional buffer is used in a design to drive an internal element since the noise generated by the switching of external heavy loads can propagate into the ASIC and the bidirectional-buffer propagation delays are dependent on a huge external load.**

Cautionary notes about bidirectional buffers follow:

- Avoid using the input portion of a bidirectional buffer to drive an internal clock or clear line that is susceptible to noise. Otherwise, any noise produced by the switching of bidirectional buffer modes can propagate to the clock or clear input of internal flip-flops, causing them to latch wrong data or reset.
- When you use a bidirectional output to drive an internal element, be aware of its propagation delays. Output buffer propagation delays greatly vary, depending on the external loads which are typically five to six orders of magnitude larger than internal loads. Note that the typical tester load is 85pF, TTL.

4.2 I/O Cell Considerations

4.2.5 System Interconnect I/O

Rules & Tips

- **For high-speed inter-chip communications, the Toshiba ASIC series provide three types of data interface I/Os: Peripheral Component Interconnect (PCI), Gunning Transceiver Logic (GTL), Digital Phase-Locked Loop (DPLL), and Low-Voltage Differential Signaling (LVDS).**

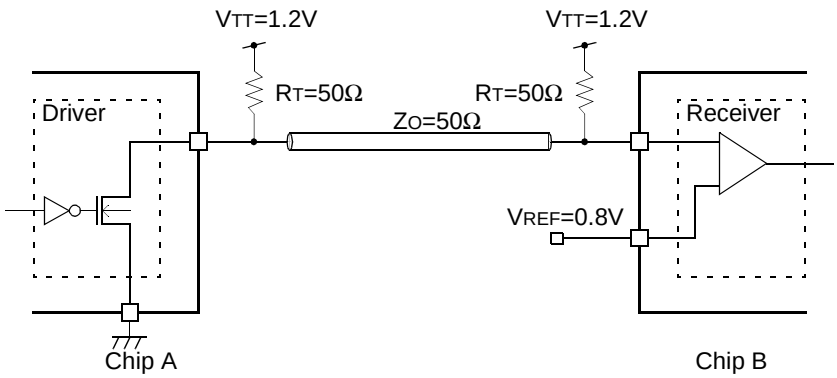
PCI (Peripheral Component Interconnect)

The PCI is a high-speed standard expansion bus that provides a common I/O component interface between the processor/memory subsystems and peripheral I/O. The PCI is intended to meet the local bus requirements of the high-end PCs and workstations. The Toshiba's ASIC cell library includes the universal PCI input, output, 3-state output, and bidirectional buffers.

GTL (Gunning Transceiver Logic)

The GTL driver is an open-drain N-channel device, and the GTL receiver is a high gain differential comparator, with one input connected to a reference voltage of 0.8 volts. The GTL driver is used to drive a 50-ohm transmission line with a 50-ohm resistor connected at each end of the transmission line between the 1.2V V_{TT} supply and the signal line. GTL I/Os use a reduced voltage signal swing (rated at 0.8 volts). GTL I/Os minimize signal reflections that cause overshoot and undershoot in fast switching circuitry, allowing highly reliable high frequency chip-to-chip communication to be achieved.

Figure 4-12 GTL Interface



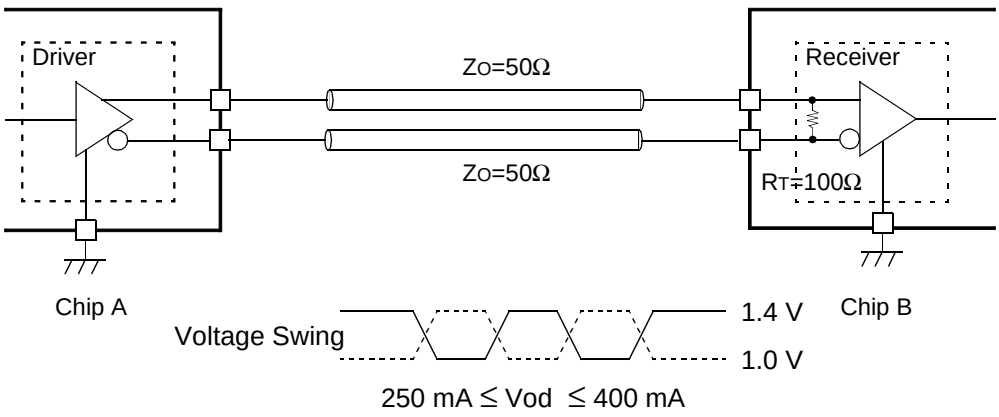
DPLL (Digital Phase-Locked Loop)

The ability to synchronize chips in high frequency systems is one of the limiting factors on system performance. Accurately synchronizing different chips in a multi-chip high performance design is critical to ensure that it functions correctly at the highest clock frequency possible. Inter-chip clock skew makes inter-chip synchronization difficult. The DPLL offers you the ability to minimize the effects of clock skew between chips, reducing the percentage of the clock cycle that must be used as a guard band. The DPLL is part of the Toshiba's extensive library of megacells available to make ASIC design faster and easier.

LVDS (Low-Voltage Differential Signaling)

The LVDS driver/receiver I/O cells fully support the Scalable Coherent Interface (SCI) low-voltage differential signal standard. This standard requires the driver to dirve a 2.5-mA signal into a 100-ohm termination, resulting in significant power savings. The LVDS data-transmission swing is 250 to 400 mA. The use of low-swing differential-mode drivers can significantly reduce electromagnetic interference (EMI). The LVDS I/Os deliver a high data transfer rate. Toshiba's LVDS drivers and receivers are self-contained I/Os with a built-in output-resistor controller and a termination resistor, respectively.

Figure 4-13 **LVDS Driver/Receiver**



4.2 I/O Cell Considerations

4.2.6 Chip-to-Chip Interface

Rules & Tips

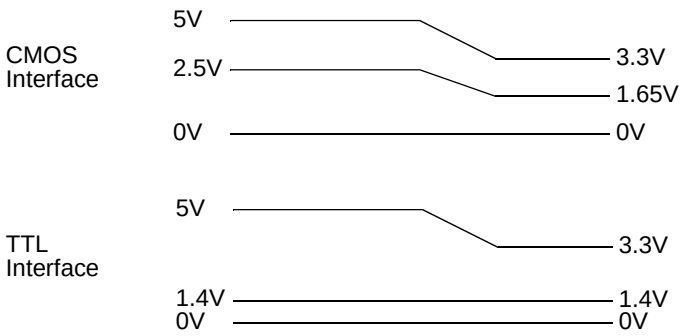
- **TC200G/C/E and TC180G/C/E offer 5V-tolerant I/O buffers in addition to normal 3V I/Os. (They are in development for TC220G/C/E, as of April, 1996.)**
- **TC203/G/C/E and TC183G/C/E offer both 3V and 5V I/O buffers.**

For the ASIC user, the rewards for designing in lower power chips are obvious — they extend battery life, generate less noise, and dissipate less heat, thus saving on packaging costs. Although many components such as microprocessors, memories, ASICs, and standard logic have standardized at 3.3V±0.3V, there remain some types of peripheral components for which 3V-operational versions are not available yet. Therefore, many electronics manufacturers still want to be able to mix 3.3 volts and 5.0 volts.

3V ASIC with 5V-Tolerant Inputs

The TC220G/C/E, TC200G/C/E, and TC180G/C/E series operate with the 3.3-volt system and core voltages; yet at the same time these product series offer input buffers and open-drain output buffers (as of July, 1996) that are 5.0V tolerant for both CMOS and TTL interface. The 5V-tolerant input buffers provide voltage translator from 5.0V to 3.3V for internal logic operations.

Figure 4-14 **Voltage Translation by 5V-Tolerant Input Buffers**



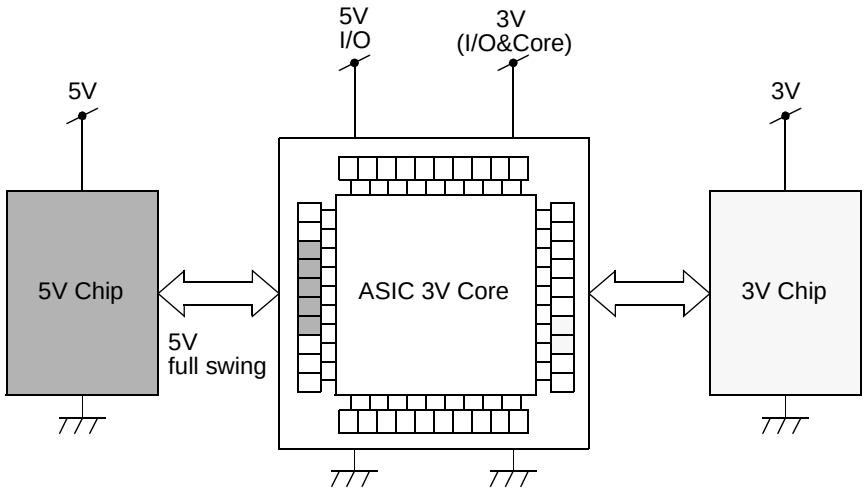
Dual I/O Options

The TC203G/C/E, TC183G/C/E, and TC163G series operate with a 3V core and offer both 3V and 5V I/Os. The 3V core reduces the power consumption of your design, while the 3V and 5V I/O compatibility offers you flexibility with your system interface design. These series accomplish this flexibility by using two power rings for I/O circuitry. One ring is set to operate at 3 volts and the other at 5 volts. There are no restrictions on 3V and 5V I/O placement.

The 3V and 5V I/O capability gives you a migration path from mixed 3V/5V systems to straight 3V-based systems. Furthermore, when a design is converted from mixed 3V/5V operation to straight 3V operation, no changes to the ASIC design are needed. The I/Os designed for 5V operation can be used at 3 volts with no changes to the ASIC design, saving you design time and costs.

In addition, the TC222C cell-based ASIC family, the newest addtion to Toshiba's ASIC portfolio, operates with a 3V core and offer both dual 2V and 3V I/O options, thus allowing a significant reduction in power.

Figure 4-15 **3V-to-5V Interface**



Chip-to-Chip Interface

Table 4-3 to Table 4-6 shows the viability of chip-to-chip interface, depending on the voltage levels of ASIC I/O cell types and the device connected to it.

Table 4-3 Connecting a 3V ASIC I/O Cell with a 5V Device

ASIC I/O Cell (3.3 V)		Power Removal	Interface		Viability	Remark
Direction	Cell Type		Type	Voltage		
Input	Normal	No	—	5 V	No	
	5-V-tolerant				Yes	Use a 5-V-tolerant type to receive a 5-V signal.
	Fail-safe				No	
Output	Normal	No	CMOS	5 V	No	
	5-V-tolerant				Yes	Requires a 5-V pull-up resistor. 1)
	Fail-safe				No	
	Normal	No	TTL	5 V	No	Permitted to drive an external device; Should not be stressed with 5 V. 2)
	5-V-tolerant				Yes	
	Fail-safe				No	Permitted to drive an external device; Should not be stressed with 5 V. 2)
Input	Normal	Yes	—	5 V	No	
	5-V-tolerant				No	
	Fail-safe				No	
Output	Normal	Yes	CMOS	5 V	No	
	5-V-tolerant				No	
	Fail-safe				No	
	Normal	Yes	TTL	5 V	No	Permitted to drive a 5-V device; Should not be stressed with a voltage. 3)
	5-V-tolerant				No	Permitted to drive a 5-V device; Should not be stressed with a voltage. 3)
	Fail-safe				No	Permitted to drive a 5-V device; Should not be stressed with 5 V. 2)

- "Power Removal" indicates a state where the device connected to the ASIC is being powered while power to the ASIC is removed.
- Fail-safe output buffers are available only in open-drain configurations. Fail-safe bidirectional buffers are available in push-pull configurations. (As of May, 1997)
- Fail-safe I/O buffers are available with the TC200 and later series.
- 5-V-tolerant I/O buffers are available with the TC200 and later series.

1. Since ASIC output buffers provide a voltage swing of only 3.3 V, an external 5-V pull-up resistor is needed to drive a 5-V device.

2. Since ASIC output buffers provide a voltage swing of 3.3 V, they can drive a TTL input of an external device. Care should be exercised, however, so that normal and fail-safe output buffers will not be stressed with 5 V from an external device.

3. Since ASIC output buffers provide a voltage swing of 3.3 V, they can drive a TTL input of an external device. Care should be exercised, however, so that output buffers will not be stressed with a voltage since it causes excessive current drain when the power to the ASIC is removed. A pull-up should not be connected to ASIC output buffers for the same reason.

Table 4-4 Connecting a 3V ASIC I/O Cell with a 3V Device

ASIC I/O Cell (3.3 V)		Power Removal	Interface		Viability	Remark
Direction	Cell Type		Type	Voltage		
Input	Normal	No	—	3.3 V	Yes	
	5-V-tolerant				Yes	
	Fail-safe				Yes	
Output	Normal	No	CMOS LVTTL	3.3 V	Yes	
	5-V-tolerant				Yes	
	Fail-safe				Yes	
Input	Normal	Yes	—	3.3 V	No	
	5-V-tolerant				No	
	Fail-safe				Yes	Use a fail-safe type when power can be removed from the ASIC.
Output	Normal	Yes	CMOS LVTTL	3.3 V	No	Should not be stressed with a voltage or connected with an external pull-up resistor. 1)
	5-V-tolerant				No	Should not be stressed with a voltage or connected with an external pull-up resistor. 1)
	Fail-safe				Yes	Use a fail-safe type when power can be removed from the ASIC.

- "Power Removal" indicates a state where the device connected to the ASIC is being powered while power to the ASIC is removed.
- Fail-safe output buffers are available only in open-drain configurations. Fail-safe bidirectional buffers are available in push-pull configurations. (As of May, 1997)
- Fail-safe I/O buffers are available with the TC200 and later series.
- 5-V-tolerant I/O buffers are available with the TC200 and later series.

1. Care should be exercised so that normal and 5-V-tolerant output buffers will not be stressed with a voltage since it causes excessive current drain when the power to the ASIC is removed. A pull-up should not be connected to these ASIC buffers for the same reason.

Table 4-5 Connecting a 5V ASIC I/O Cell with a 5V Device

ASIC I/O Cell (5 V)		Power Removal	Interface		Viability	Remark
Direction	Cell Type		Type	Voltage		
Input	Normal	No	—	5 V	Yes	
	Fail-safe				Yes	
Output	Normal	No	CMOS TTL	5 V	Yes	
	Fail-safe				Yes	
Input	Normal	Yes	—	5 V	No	
	Fail-safe				Yes	Use a fail-safe type when power can be removed from the ASIC.
Output	Normal	Yes	CMOS TTL	5 V	No	Should not be stressed with a voltage or connected with an external pull-up resistor. 1)
	Fail-safe				Yes	Use a fail-safe type when power can be removed from the ASIC.

- "Power Removal" indicates a state where the device connected to the ASIC is being powered while power to the ASIC is removed.
- Fail-safe output buffers are available only in open-drain configurations. Fail-safe bidirectional buffers are available in push-pull configurations. (As of May, 1997)
- Fail-safe I/O buffers are available with the TC200 and later series.

1. Care should be exercised so that normal output buffers will not be stressed with a voltage since it causes excessive current drain when the power to the ASIC is removed. A pull-up should not be connected to these ASIC buffers for the same reason.

Table 4-6 Connecting a 5V ASIC I/O Cell with a 3V Device

ASIC I/O Cell (5 V)		Power Removal	Interface		Viability	Remark
Direction	Cell Type		Type	Voltage		
Input	Normal	No	—	3.3 V	Yes	Use TTL interface. 2)
	Fail-safe				Yes	Use TTL interface. 2)
Output	Normal	No	CMOS TTL	3.3 V	No	Depends on whether the input of the driven device can be stressed with 3.3 V.
	Fail-safe				No	Depends on whether the input of the driven device can be stressed with 3.3 V.
Input	Normal	Yes	—	3.3 V	No	
	Fail-safe				Yes	Use TTL interface. 2)
Output	Normal	Yes	CMOS TTL	3.3 V	No	Should not be stressed with a voltage or connected with an external pull-up resistor. 1) Check whether the input of the driven device can be stressed with 3.3 V.
	Fail-safe				No	Depends on whether the input of the driven device can be stressed with 3.3 V.

- "Power Removal" indicates a state where the device connected to the ASIC is being powered while power to the ASIC is removed.
- Fail-safe output buffers are available only in open-drain configurations. Fail-safe bidirectional buffers are available in push-pull configurations. (As of May, 1997)
- Fail-safe I/O buffers are available with the TC200 and later series.

1. Care should be exercised so that normal output buffers will not be stressed with a voltage since it causes excessive current drain when the power to the ASIC is removed. A pull-up should not be connected to these ASIC buffers for the same reason.

2. The 3.3-V ASIC output buffers should be interfaced to a TTL device.

4.3 Determining a Preferred Package Pinout

Rules & Tips

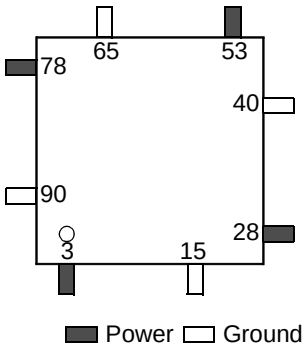
- **Your preferred package pinout plan must be included with your design release package when you hand off your design to Toshiba for layout. Bear in mind that although most designs can be implemented with your preferred pinout, Toshiba cannot guarantee an exact pinout until its mechanical and electrical feasibility is verified.**

The steps below show a typical sequence used to determine a pinout.

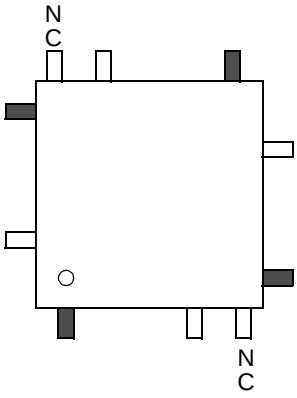
1. Look up the dedicated power and ground pin locations in the Toshiba *ASIC Packaging*.
2. Contact Toshiba to find if your array/package combination has any pinout constraints.
3. Contact Toshiba to find if special I/O cells (e.g., cornered oscillator cells, analog cells) used in your design have any pinout constraints.
4. Calculate the number of power and ground pins required by your circuit. Use dedicated power and ground pins first. Evenly space power and ground pins.
5. Place input and output buffers, considering the floorplan of your circuit.
6. Prepare the Pinout Plan, and transfer it to Toshiba for checking for electrical and mechanical connections (see Appendix B, *Design Release Checklist*).

Figure 4-16 Preparing a Pinout

1. Look up dedicated power and ground pins (section 4.3.1).



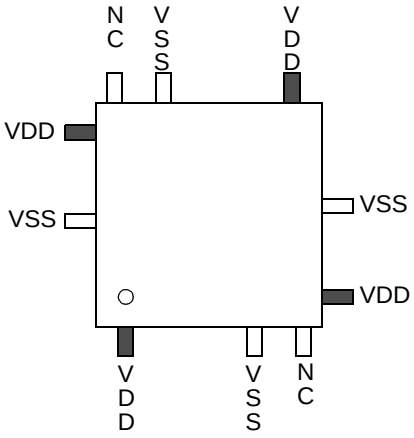
2. Ask Toshiba for any array/package constraints.



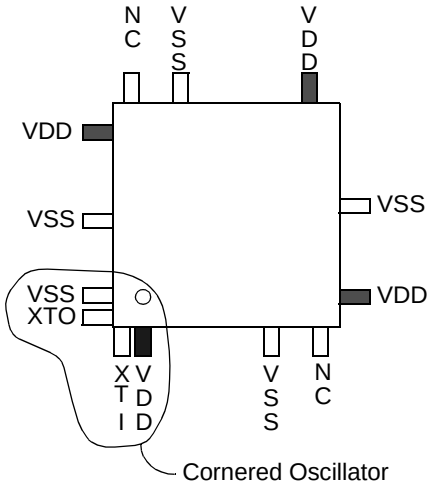
3. Calculate the number of required power/ground pins.

VDD — 5
VDD3 — 1
VSS — 8
VSS2 — 2
VSS3 — 1

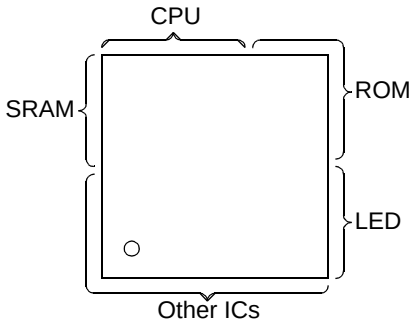
4. Use the dedicated power/ground pins first.



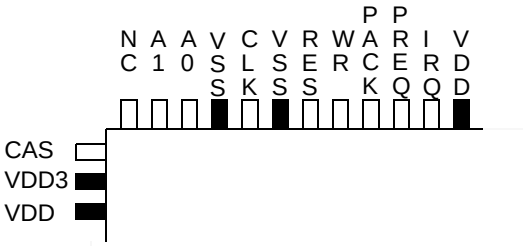
5. Ask Toshiba for any constraints due to special I/Os.



6. Partition pins into functional groups.



7. Place input and output pins. Also place the remaining power/ground pins.



- Position input pins susceptible to noise (e.g., clocks, enables, resets) between VSS pins.
- Evenly space power/ground pins.

4.3 Determining a Preferred Package Pinout

4.3.1 Power and Ground Pins

Rules & Tips

- **Each of the packages has several dedicated power and ground pins preassigned.**
- **All devices must be provided with two or three types power pins (VDD, VDD3, VDDS) and three types of ground pins (VSS, VSS2, and VSS3).**
- **Several array/package combinations have power/ground pin constraints.**

Dedicated Power and Ground Pins

Several dedicated power and ground pins are preassigned for each package. You can use these pins as power/ground pins only. Depending on the design, additional power and ground pins are required at the expense of signal I/O pins. Consult the Toshiba *ASIC Packaging* for the dedicated power/ground pin assignment.

Power and Ground Buses

All ASIC series that operate on a single 3V or 5V power supply (designated TCxx**0**G/C/E) have two power (VDD, VDD3) and three ground (VSS, VSS2, VSS3) buses. All ASIC series with mixed 3V/5V I/O (designated TCxx**3**G/C/E) have an additional power bus (VDDS).

Table 4-7 Power and Ground Bus Types

Power/Ground Bus	Nominal Voltage		Use
	xx0G/C/E	xx3G/C/E	
VDD	3V or 5V	3V	Core and output buffer power
VDD3	3V or 5V	3V	Input buffer power
VDDS	n/a	5V	5V input and output buffer power (in mixed 3V/5V series arrays)
VSS	0V	0V	Output buffer ground
VSS2	0V	0V	Core ground
VSS3	0V	0V	Input buffer ground

The VDD pins shown in the Package Selector Guide can be used as either VDD or VDD3 (but not as VDDS). The VSS pins shown in the ASIC Packaging can be used as VSS, VSS2, or VSS3, whichever is appropriate for your circuit.

Figure 4-17 **Power and Ground Buses (TCxx0G/C/E)**

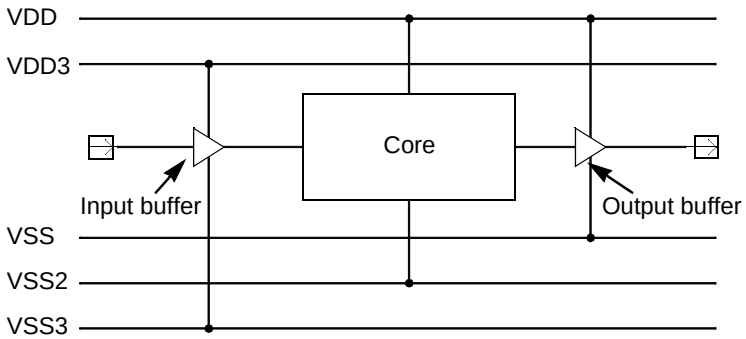
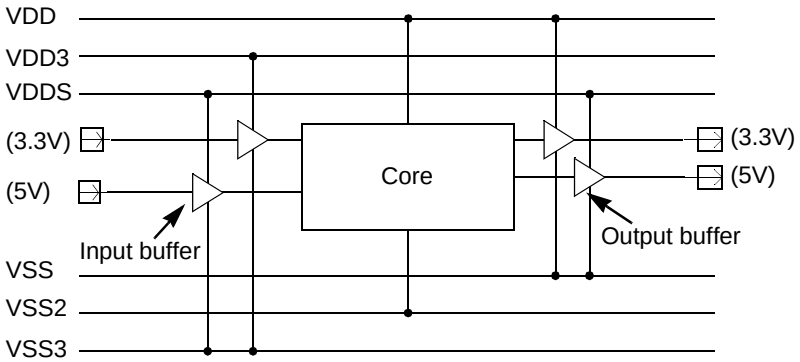


Figure 4-18 **Power and Ground Buses (TCxx3G/C/E)**



Array/Package Combinations

Several array/package combinations have constraints regarding power and ground pin assignment. Contact the Toshiba ASIC service group for this information. Be sure to consult the latest catalog.

4.3 Determining a Preferred Package Pinout

4.3.2 Simultaneously Switching I/Os

Rules & Tips

- **As the number of simultaneously switching inputs (SSIs) and outputs (SSOs) increase, so does the severity of the power bus noise. There are several ways to minimize SSI and SSO problems.**

SSIs and SSOs

Simultaneously switching inputs (SSIs) and outputs (SSOs) are defined as inputs and outputs that switch within the same time window of 5 nanoseconds.

The input/output buffers' slew rate, or the time it takes for a signal to switch from logical 0 to logical 1 or vice versa, causes a current spike. The SSI and SSO buffers can disrupt operation of a circuit by causing noise on adjacent signals, noise at internal core cells, and ground bounce. The severity of the noise voltage (V_n) on the SSI and SSO signals is a function of the number and the switching speeds of SSIs and SSOs, as well as package and bonding wire inductance:

$$Vn = -\left(N \times L \times \frac{di}{dt}\right)$$

where:

N:	Number of SSIs and SSOs
L:	Package and bonding wire inductance
di/dt:	Switching speed of I/O buffers

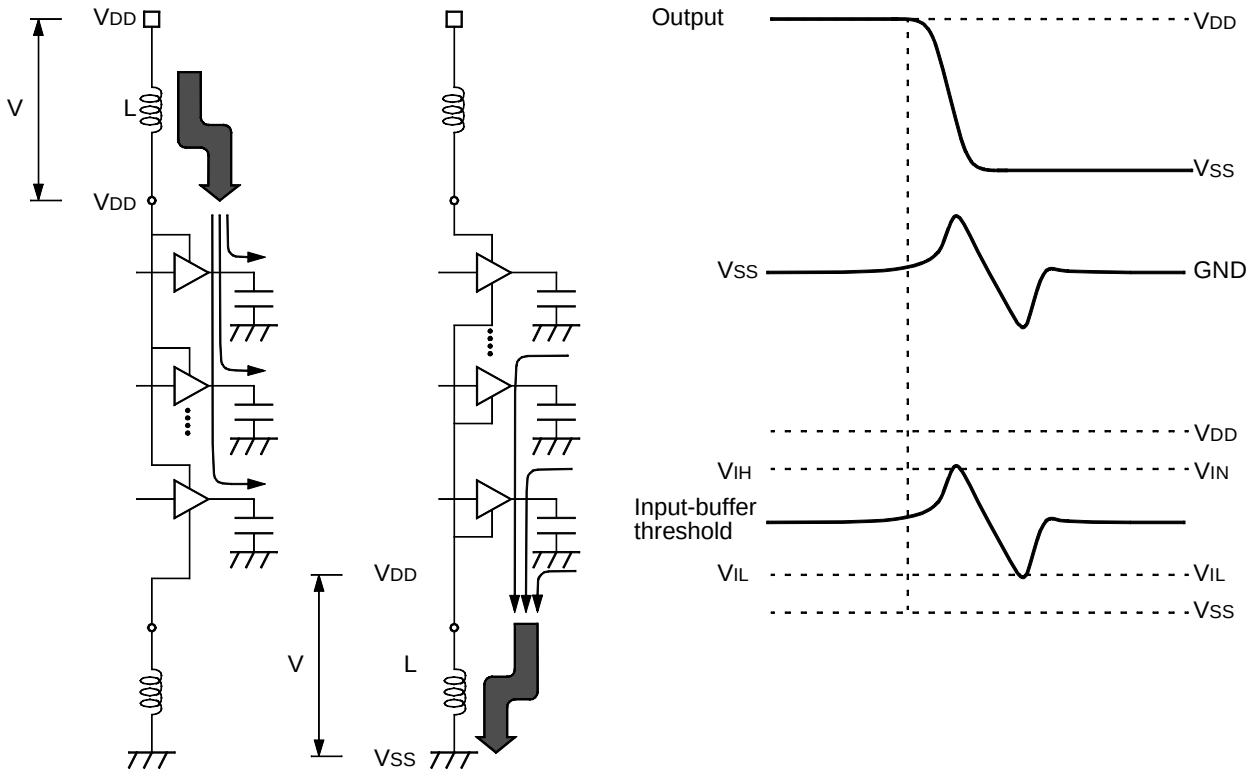
Ways to Control SSI and SSO Noise

There are several ways to minimize SSI and SSO problems:

- Use output buffers with a current capability consistent with your need.
- Use slew rate control output buffers.

- Position SSOs near or between a power/ground pin pair. The most effective types of power/ground pins are determined by Toshiba.
- Position input signal pins susceptible to current noise (such as clocks, enables, and clears) near or between a power/ground pin pair. The most effective types of power/ground pins are determined by Toshiba.

Figure 4-19 **A Model of the I/O Ground Structure**



4.3 Determining a Preferred Package Pinout

4.3.3 Required Power and Ground Pins

Rules & Tips

- **SSIs, SSOs, output-drive specifications, switching power dissipation in internal gates and output buffers, and the package type determine the number of required power and ground pins.**

This section presents equations for determining the total (not additional) number of power and ground pins.

Round off the results of each of the following equations to the nearest number. At least one pin is required for each of the power/ground buses, however, even when the result is less than 0.5.

VDD (Core and Output Buffer Power)

The number of required VDD pins is determined as the larger of the results of Equations (4.1) and (4.2).

$$X_{VDD} = \max [N1, N2]$$

where:

N1: Number of VDD pins required to damp out SSO noise
N2: Number of VDD pins required to accommodate the switching of internal gates and output buffers

The equation for calculating N1 is:

$$N1 = \Sigma NR \div K_{vol} \quad (4.1)$$

where:

NR: Noise rating for an output or bidirectional buffer
K_{vol}: 16 for 5V series;
12 for 3V series.

N1 is applicable to 5V output buffers for 5V series and 3V output buffers for 3V and mixed 3V/5V series.

The equation for calculating N2 is:

$$N2 = (I_{internal} + I_{IOac} + \Sigma I_{OH}) \div K_{pkg} \quad (4.2)$$

where:

$I_{internal}$: Switching power dissipation in internal gates (mA). This is equal to (I_{logic}+I_{memory}) in the early power estimation equation or (I_{clogic}+I_{slogic}+I_{clock}+I_{memory}) in the detailed power calculation equation. See Chapter 7, *Power Estimation*, for a discussion on power estimation. Note that current is obtained by dividing power by voltage.

I_{IOac}: Switching power dissipation in output buffers (mA)

ΣI_{OH}: Total amount of high-level output drive currents (mA)

K_{pkg}: 50 for TCP and PQFP[TAB]
90 for other packages

VDD3 (Input Buffer Power)

The VDD3 pins are for damping out SSI noises. The equation for calculating the number of required VDD3 pins is:

$$X_{VDD3} = (\#\_of\_SSIs) \div 16 \quad (4.3)$$

where (#_of_SSIs) is the largest (i.e., worst-case) number of simultaneously-switching inputs and input-mode bidirectional buffers.

VDDS (5V I/O Power)

The number of required VDDS pins is determined as the larger of the results of Equations (4.4) and (4.5).

$$X_{VDDS} = \max [N3, N4]$$

where:

N3: Number of VDDS pins required to damp out SSI and SSO noises

N4: Number of VDDS pins required to accommodate the switching of output buffers

The following equations are applicable only to 5V I/O buffers used in mixed 3V/5V series arrays.

The equation for calculating N3 is:

$$N3 = (\Sigma NR \div 16) + (\#\_of\_SSIs \div 32) \quad (4.4)$$

where NR is the noise rating for an output or bidirectional buffer.

The equation for calculating N4 is:

$$N4 = (I_{IOac} + \Sigma I_{OH}) \div K_{pkg} \quad (4.5)$$

where:

I_{IOac}: Switching power dissipation in output buffers (mA)
ΣI_{OH}: Total amount of high-level output drive currents (mA)
K_{pkg}: 50 for TCP and PQFP[TAB]
100 for other packages

VSS (Output Buffer Ground)

The number of required VSS pins is determined as the larger of the results of Equations (4.6) and (4.7).

$$X_{VSS} = \max [N5, N6]$$

where:

N5: Number of VSS pins required to damp out SSO noise
N6: Number of VSS pins required to accommodate the switching of output buffers

The equation for calculating N5 is:

$$N5 = \Sigma NR \div 8 \quad (4.6)$$

where:

NR: Noise rating for an output or bidirectional buffer

The equation for calculating N6 is:

$$N6 = (I_{IOac} + \Sigma I_{OH}) \div K_{pkg} \quad (4.7)$$

where:

I_{IOac}: Same as that used in Equation (4.2)
ΣI_{OH}: Same as that used in Equation (4.2)
K_{pkg}: 90 for TCP and PQFP[TAB]
130 for other packages

VSS2 (Core Ground)

The VSS2 pins are for servicing the switching of internal gates. The equation for calculating the number of required VSS2 pins is:

$$X_{VSS2} = I_{internal} \div K_{pkg} \quad (4.8)$$

where:

$I_{internal}$: Same as that used in Equation (4.2)
K_{pkg}: 50 for TCP and PQFP[TAB]
90 for other packages

VSS3 (Input Buffer Ground)

The VSS3 pins are for damping out SSI noise. The equation for calculating the number of required VSS3 pins is:

$$X_{VSS3} = (\#\_of\_SSIs) \div 16 \quad (4.9)$$

Output Buffer Noise Ratings

Noise ratings (NR) for the various types of output and bidirectional buffers are given in Table 4-8 and Table 4-9. NR values are used in calculating the additional power/ground pins required to service SSOs.

Table 4-8 Output Buffer Noise Ratings

(NR values are arbitrarily defined to characterize SSO noise.)

Series	Suffix	B1x B1Tx BD1x	B2 B2Tx BD2x	B4 B4Tx BD4x	B8 B8Tx BD8x	B16 B16Tx BD16x	B24 B24Tx BD24x
TC25SC	R	n/a	n/a	0.75	0.75	1.25	1.75
	—	0.75	0.75	1.00	1.75	3.50	3.50
	H	n/a	n/a	3.50	6.25	9.50	10.75
TC26SC	R	n/a	n/a	0.75	0.75	1.25	1.75
	—	0.75	0.75	1.00	1.75	3.50	3.50
	H	n/a	n/a	3.50	6.25	9.50	10.75
TC160G	R	n/a	n/a	0.25	0.25	0.50	0.75
	—	0.75	1.00	1.00	1.00	2.00	3.00
	H	n/a	n/a	2.00	2.00	3.50	4.00
TC163G	R	n/a	n/a	n/a	n/a	n/a	n/a
	—	n/a	n/a	0.50	0.50	1.00	1.50
	H	n/a	n/a	1.00	1.00	2.00	2.00
TC170G/C	R	n/a	n/a	0.25	0.25	0.50	0.75
	—	0.75	1.00	1.00	1.00	2.00	3.00
	H	n/a	n/a	2.00	2.00	3.50	4.00
TC180G/C/E	R	n/a	n/a	0.40	0.40	0.70	1.00
	—	0.60	0.75	1.00	1.00	1.50	1.50
	H	n/a	n/a	1.50	1.50	2.20	2.20
TC183G/C/E	R	n/a	n/a	0.35	0.35	0.50	0.75
	—	0.75	0.75	1.00	1.00	1.50	1.75
	H	n/a	n/a	1.25	1.50	2.00	2.00
TC190G/C	R	n/a	n/a	0.50	0.50	1.00	1.00
	—	n/a	0.50	1.00	1.00	2.00	2.00
	H	n/a	n/a	1.50	2.00	2.50	3.00
TC200G/C/E	R	n/a	n/a	0.50	0.50	1.00	1.00
	—	n/a	1.00	1.00	1.00	1.50	2.00
	H	n/a	n/a	1.50	2.00	2.50	3.00
TC203G/C/E	R	n/a	n/a	0.50	0.50	1.00	1.25
	—	n/a	0.75	1.00	1.25	1.50	2.00
	H	n/a	n/a	1.25	1.50	n/a	2.25

Suffix: R: Slew rate control (low-drive) No letter: Standard-drive H: High-drive

Table 4-9 **5V Output Buffer Noise Ratings for Mixed 3V/5V Series**

(NR factors are arbitrarily defined to characterize SSO noise.)

Series	Suffix	B1IF	B2IF	B4IF	B8IF	B16IF	B24IF
TC163G	R	n/a	n/a	0.25	0.25	0.50	0.75
	—	n/a	n/a	1.00	1.00	2.00	2.00
	H	n/a	n/a	n/a	n/a	n/a	n/a
TC183G/C/E	R	n/a	n/a	0.35	0.35	0.35	0.50
	—	0.75	1.00	1.00	1.00	1.50	1.50
	H	n/a	n/a	1.75	1.75	1.75	1.75
TC203G/C/E	R	n/a	n/a	0.75	0.75	0.75	1.00
	—	n/a	1.00	1.50	1.50	3.00	2.75
	H	n/a	n/a	2.25	2.25	3.50	4.00

Suffix: R: Slew rate control (low-drive) No letter: Standard-drive H: High-drive

Calculation Example

The following example demonstrates how to calculate the minimum power/ground pin requirement for a hypothetical design. The assumptions are:

- TC180G series (power supply: single 3.3V); QFP package
- Output buffers: 34 B4 outputs, 4 B8 outputs, 8 BD2RC bidirects
- Worst-case SSIs: 8
- Worst-case SSOs: 24 B4 outputs or 4 B8 outputs
- Switching current (see Chapter 7, *Power Estimation*.)
  Current is obtained by dividing power by voltage.
  Output buffers: 12.1 mA, Core: 124.6 mA

1. VDD

The VDD requirement provided by:

$$X_{VDD} = \max [\ N1, N2\ ]$$

Using Eq. (4.1), N1 is calculated as:

$$N1 = \Sigma NR \div K_{vol}$$

Referring to Table 4-8 in the previous section, the noise ratings for output buffers B4 and B8 are both 1.0, respectively. So,

Case 1: $N1 = (24 \times 1.0) \div 16 = 2$
Case 2: $N1 = (8 \times 1.0) \div 16 = 1$

Using Eq. (4.2), N2 is calculated as:

$$N2 = (I_{internal} + I_{IOac} + \Sigma I_{OH}) \div K_{pkg}$$
$$= \{\ 124.6\ mA + 12.1\ mA + (4\ mA \times 34 + 8\ mA \times 4 + 2\ mA \times 8)\ \} \div 90$$
$$= 4$$

$$\mathbf{X_{VDD} = max\ [\ N1, N2\ ] = 4}$$

2. VDD3

The VDD3 requirement using Eq. (4.3) is:

$$\mathbf{X_{VDD3}} = (\#\_of\_SSIs) \div 16$$

$$\mathbf{X_{VDD3} = 8 \div 16 = 1}$$

3. VSS

The VSS requirement is provided by:

$$X_{VSS} = \max [N5, N6]$$

Using Eq. (4.5), N5 is calculated as:

$$N5 = \sum NR \div 8$$
$$= 1.0 \times 24 \div 8 = 3$$

Using Eq. (4.6), N6 is calculated as:

$$N6 = (I_{IOac} + \sum I_{OH}) \div K_{pkg}$$
$$= (12.1 + 184) \div 130 = 2$$

$X_{(VSS)} = \max [N5, N6] = 3$

4. VSS2

The VSS2 requirement using Eq. (4.8) is:

$$X_{VSS2} = I_{internal} \div K_{pkg}$$

$X_{VSS2} = 124.6 \div 90 = 1$

5. VSS3

The VSS3 requirement using Eq. (4.9) is:

$$X_{VSS3} = (\#\_of\_SSIs) \div 16$$

$X_{VSS3} = 8 \div 16 = 1$

To recap:

VDD — 4
VDD3 — 1
VSS — 3
VSS2 — 1
VSS3 — 1

4.4 Basic CMOS Electrical Design Rules

Rules & Tips

- **All ASIC inputs and outputs must enter or exit through I/O buffers.**
- **Connect unused macrocell input pins either to power supply or ground.**
- **Leave unused macrocell output pins open.**
- **Do not use 3-state buses, except for preventing 3-statable RAM/ROM outputs from floating.**

Electrical design rules in this section are inherent with CMOS characteristics. The Toshiba Design Verifier program checks your design for design rule violations. Remember that should your design has any single violation, it may not be implemented as a real device.

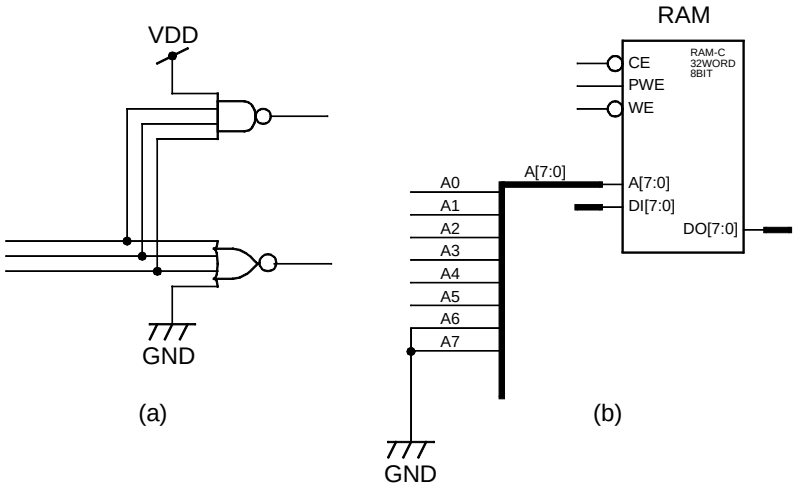
I/O Buffers

All ASIC input signals must enter the array through I/O buffers. Your input buffer choices depend on whether your circuit will be interfacing with CMOS or TTL voltage levels. All ASIC output signals must exit through I/O buffers. I/O buffers are exclusively responsible for chip interface, and may not be used in the internal circuit.

Unused Macrocell Input Pins

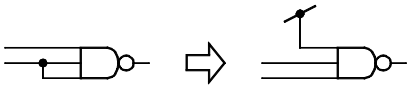
Do not leave a macrocell input pin unconnected (i.e., floating). Unused macrocell input pins must be connected either to power supply or to ground.

Figure 4-20 **Unused Macrocell Input Pins**



Do not connect more than one logically equivalent inputs of a macrocell to the same net.

Figure 4-21 **Logically Equivalent Inputs**

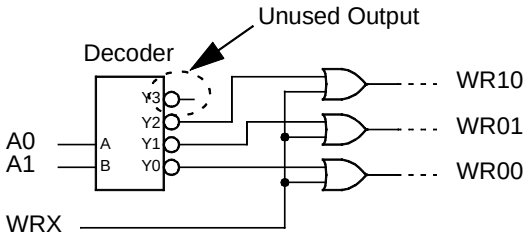


Not This

Unused Macrocell Output Pins

Leave unused macrocell output pins open without connecting a net. All macrocells all of whose outputs are unconnected will be automatically removed by the gate-eating feature of the Toshiba ASIC sign-off system (unless otherwise specified).

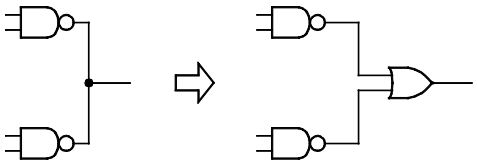
Figure 4-22 Unused Macrocell Output Pins



Wired Connections

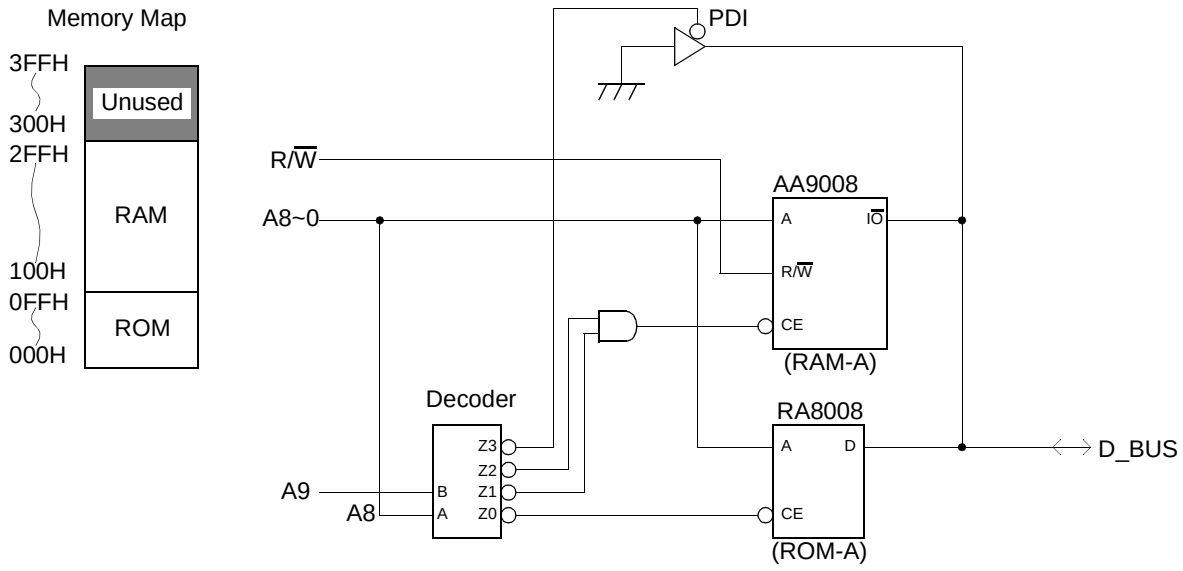
Do not connect more than one macrocell output to the same net. The sole exception is 3-state output drivers. 3-state buses should be avoided, however, but for preventing 3-statable RAM/ROM outputs from going into the floating state.

Figure 4-23 Do Not Wire-OR Multiple Macrocell Outputs



Not This

Figure 4-24 **3-state Driver for Preventing RAM/ROM Outputs from Floating**



3-state Buses

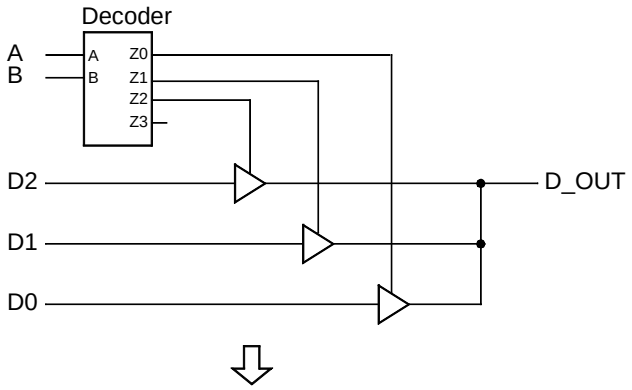
Avoid using 3-state buses since they tend to cause signal conflicts and floats.

A bus conflict occurs when two or more 3-state drivers connected to the same bus are enabled simultaneously. A bus float occurs when all 3-state drivers connected to the same bus are disabled simultaneously. Signal conflicts and floats cause extra static current to flow on a driven gate, making the I_{DDS} measurement unreliable. In addition, signal conflicts may be detrimental because they can cause the driven gates to overheat and be permanently damaged in a very short period of time.

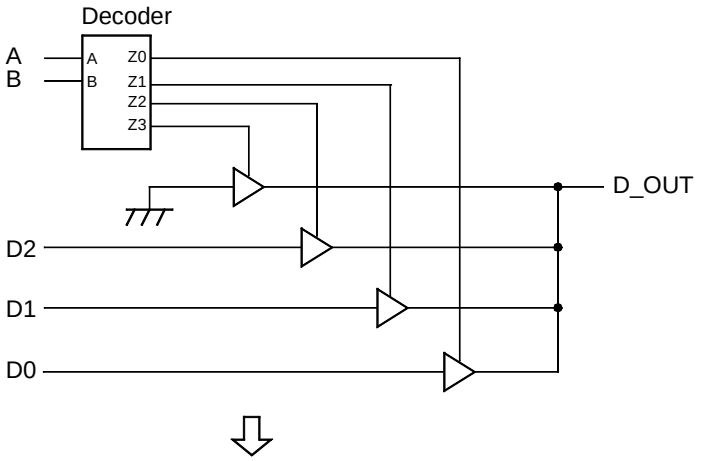
Figure 4-25 and Figure 4-26 show the recommended techniques for avoiding 3-state bus conflicts and floats.

Figure 4-25 **A Recommended Technique for Avoiding 3-state Bus Conflicts and Floats (a)**

(a) A 3-state bus can cause floating node.



(b) “D_OUT” can go into the floating state briefly



(c) Floating-free

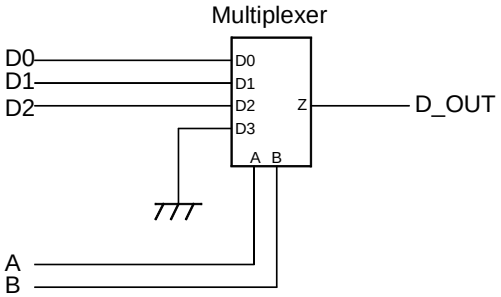
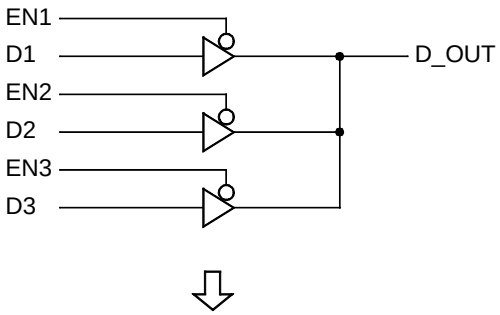
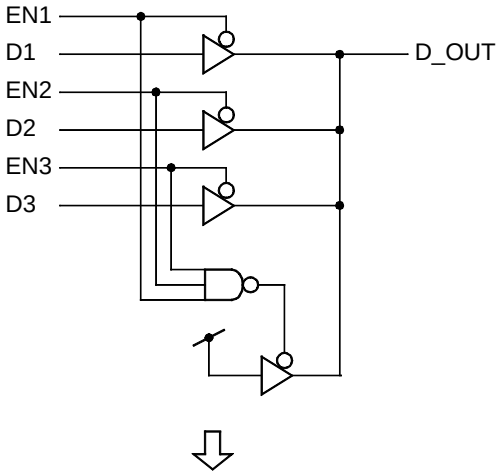


Figure 4-26 **A Recommended Technique for Avoiding 3-state Bus Conflicts and Floats (b)**

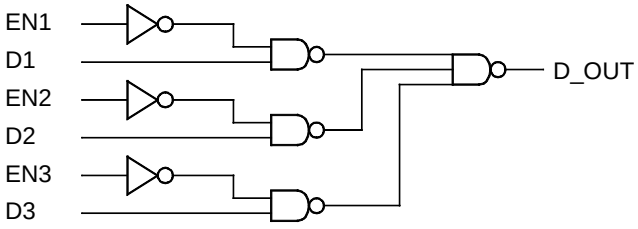
◇ A 3-state bus can cause a floating node.



◇ A 3-state bus goes into the floating state while the enable lines are switching.



◇ Floating-Free



4.5 Choosing Macrocells

Rules & Tips

- **Minimize AND and OR gates to reduce required chip area.**
- **Minimize NOR gates to improve speed.**

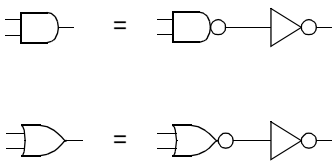
The basic units of ASIC designs are macrocells (or primitive cells). You must be familiar with the Toshiba macrocell lineup before you can learn ways to optimize your design. The macrocell data book presents all information necessary for designing: gate counts, truth tables, ac performance, logical schematics, and so on.

NAND/NOR Gates vs. AND/OR Gates

The CMOS technology favors NAND and NOR gates in terms of gate count. You should use as few AND and OR gates as possible. AND and OR gates are actually implemented with NAND and NOR gates followed by an inverter respectively, as shown in Figure 4-27.

For example, a 2-input NAND and a 2-input NOR require only one gate, whereas a 2-input AND and a 2-input OR require two gates.

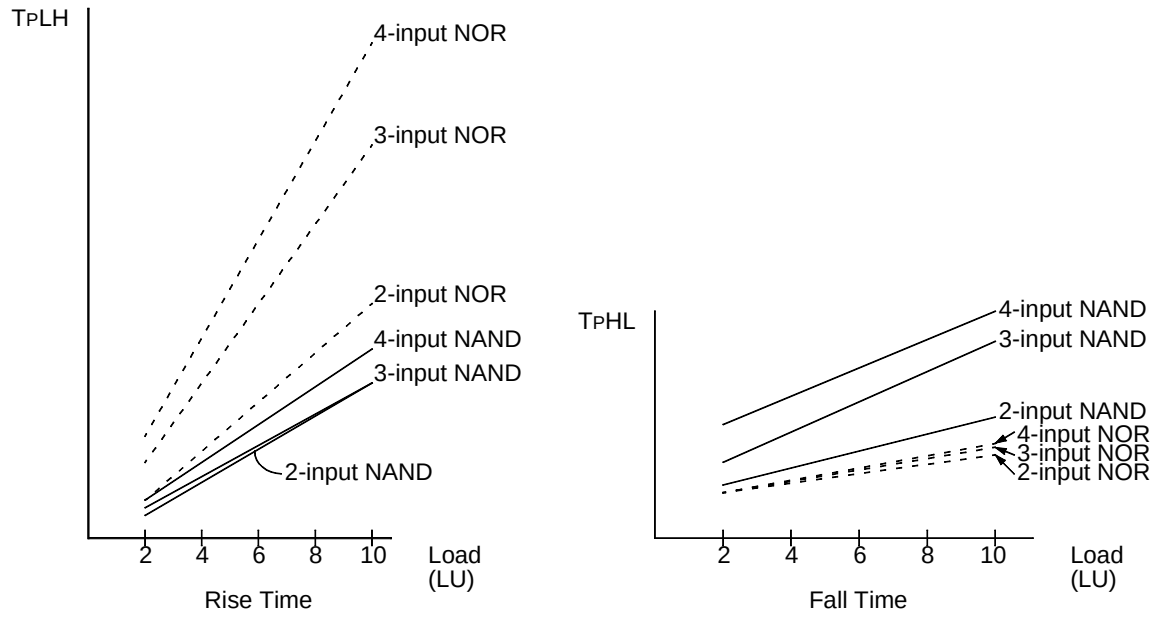
Figure 4-27 CMOS AND and OR Gates



Propagation Delays as a Function of Loadings

NAND gates are preferred over NOR gates in terms of speed. Figure 4-28 shows the propagation delays of various NAND and NOR gates as a function of output loadings. The slopes for NOR gates, especially those with three or more inputs, are noticeably steeper than for NAND gates. Notice that NAND gates have fairly symmetrical rise and fall times. For NOR gates, the rise time can be 2 to 6 times greater than the fall time.

Figure 4-28 **Propagation Delays vs. Output Loadings**



4.5 Choosing Macrocells

4.5.1 Reducing Gate Count

Rules & Tips

- **Optimize a design for area so that it can be built more economically. Reduced gate counts will invariably increase chip routability.**

This section discusses ways to reduce gate count. You may want to refer to the data book as you consider the techniques presented in this section. Keep your Toshiba macrocell data book at your hand and refer to it as needed.

Figure 4-29 and Figure 4-30 are examples of correct gate macrocell choices. The designs at the right of the arrows are more favorable in terms of gate counts than the ones at left.

Figure 4-29 **A 3-Input AND Gate**

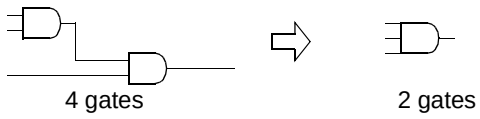
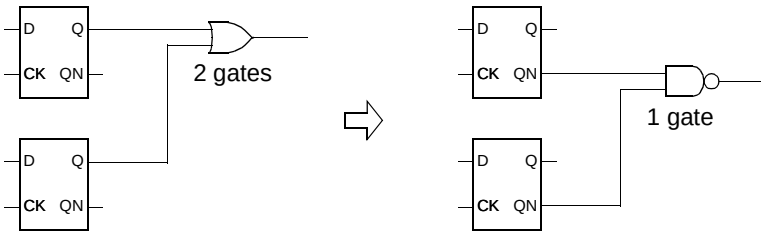


Figure 4-30 **Manipulate the Logic to Accept Inverted Outputs**



Do not choose a macrocell having an unnecessary input function. Figure 4-31 shows a D flip-flop with Clear and Preset, with Clear input tied to VDD. In this case, use the version of the flip-flop with Preset only.

Figure 4-31 **Do Not Use a Macrocell Having an Unnecessary Input Function**

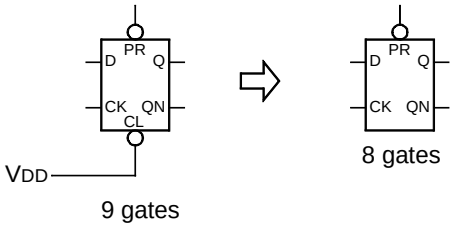
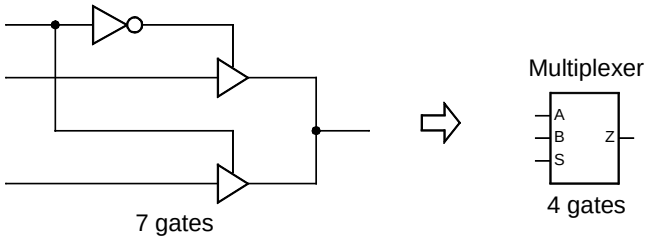


Figure 4-32 shows an example of a selector circuit optimization.

Figure 4-32 **A 2-To-1 Multiplexer**



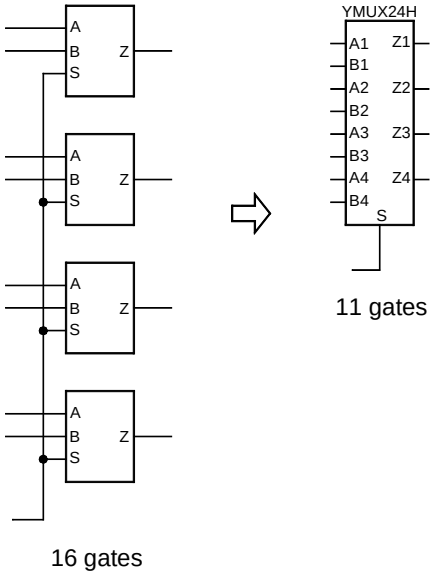
When you need a 4-bit transparent latch with common enable, use the YLD14B or YLD24B cell if you are designing with a gate array. These cells require less gate area than a design implemented using four occurrences of a 1-bit latch.

Likewise, when you need a quad 4-to-1 multiplexer with common control, use the YMUX24H or YMUX24L cell instead of using four occurrences of a 2-to-1 multiplexer.

The softmacrocell library of the cell-based IC series includes a number of generic functions such as multiplexers, encoders, decoders, shift registers, and counters. Examples:

- Quad D flip-flop (Clear and Preset options are available.)
- Octal D flip-flop (Clear and Preset options are available.)
- Quad D latch (Low and high enable versions are available.)
- Octal D latch (Low and high enable versions are available.)
- Dual 2-to-1 multiplexer
- Quad 2-to-1 multiplexer
- Octal 2-to-1 multiplexer

Figure 4-33 **A Quad 2-to-1 Multiplexer with Common Control**



4.5 Choosing Macrocells

4.5.2 User-Defined Macros

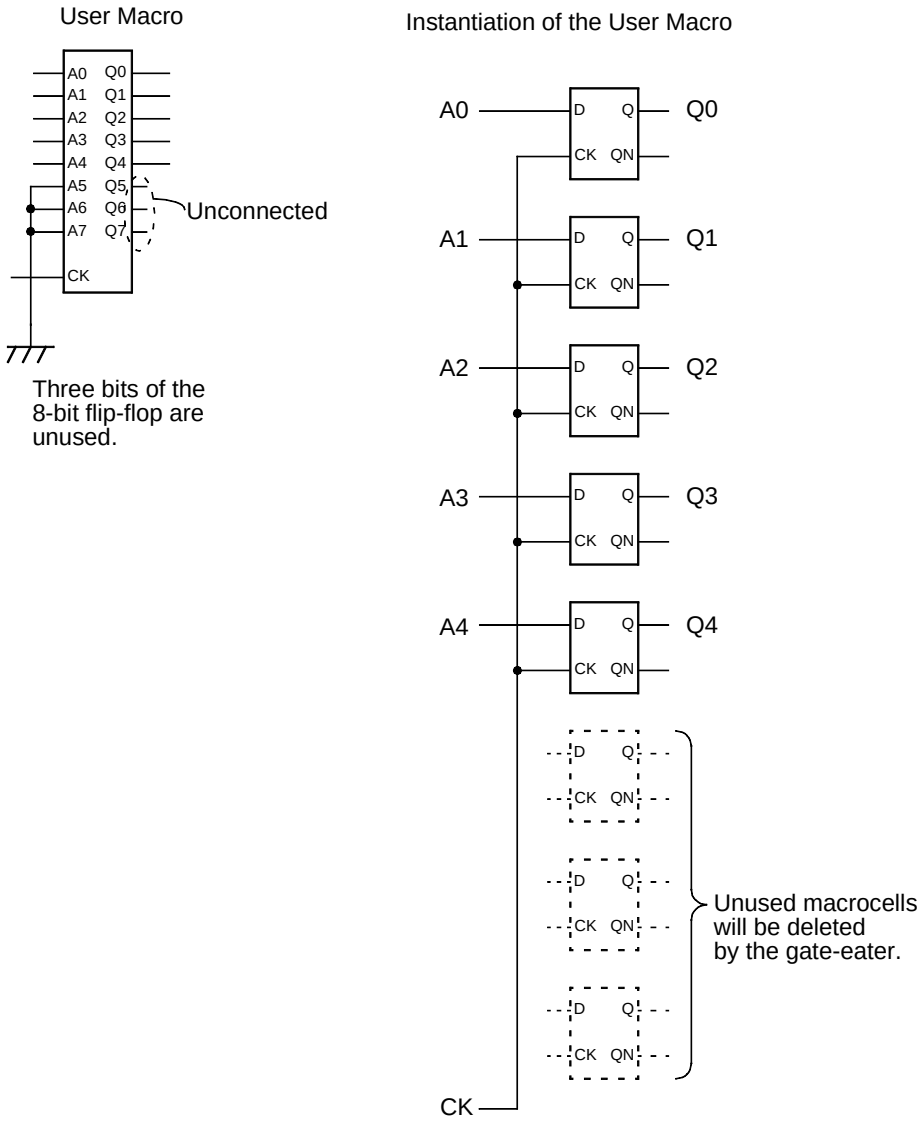
Rules & Tips

- **Understanding the gate-eating feature will enable you to simplify logic entry.**

All macrocells all of whose outputs are unconnected can be automatically deleted with the gate-eating feature of the Toshiba ASIC sign-off system. This feature is especially convenient in situations when, for example, you need multiple flip-flop macros of different bit widths, say, 8-bit and 5-bit long. In this case, you need to create only a 8-bit flip-flop as a user macro, as shown in Figure 4-34. You can then reuse it as a 5-bit flip-flop just by leaving three output bits unconnected.

Many types of counters such as binary counters have a feedback line from flip-flops; so unused counter bits will not always result in gate-eating.

Figure 4-34 **Gate-Eating**



4.5 Choosing Macrocells

4.5.3 FD- and YFD-Type Macrocells

Rules & Tips

Gate array libraries offer FD- and YFD-type flip-flops.

- **Use FD-type flip-flops when you wish to ensure the propagation delays and maximum operating frequency.**
- **Use YFD-type flip-flops when you wish to save on gate areas.**

Gate array libraries include two types of D flip-flops: FD-type and YFD type. FD1 (D-type flip-flop), FD2 (D-type flip-flop with Clear), FD3 (D-type flip-flip with Clear and Preset), and FD4 (D-type flip-flop with Preset) are available in YFD versions, designated as YFD1, YFD2, YFD3, and YFD4 respectively. Figure 4-35 and Figure 4-36 show the electrical schematics of FD1 and YFD1.

Notice that unlike the FD1 flip-flop, the Q and QN outputs of the YFD1 are not driven by separate output buffers. Therefore, the YFD1 requires less gate area than the FD1.

In the YFD1 flip-flop shown in Figure 4-36, while the CP pin is low, the signal from the data pin propagates through G1, G2, and G3, and is set up on the G4 input. The CP signal must remain low during this period so that the master can latch in the correct data. Since the master drives no external loads, the minimum negative pulse width is independent of the loading on the Q and QN outputs.

However, while the clock is high, data is transferred from master to slave. The data signal propagates through G5, G6, and G7, and is set up on the G8 input. The minimum positive clock pulse width is:

$$tw(H) = TpdG5 + TpdG6 + TpdG7$$

Unlike the master, the slave drives external loads; i.e., G6 drives the Q output, and G7 drives the QN output. If Q drives a high fanout line, then the propagation delay of G6 increases. This, in turn, increases the minimum positive clock pulse width requirement.

In addition, since the QN output changes after the Q output via inverter G7, the load on the Q output also affects the propagation delays to the QN output.

Figure 4-35 **FD1 Flip-Flop**

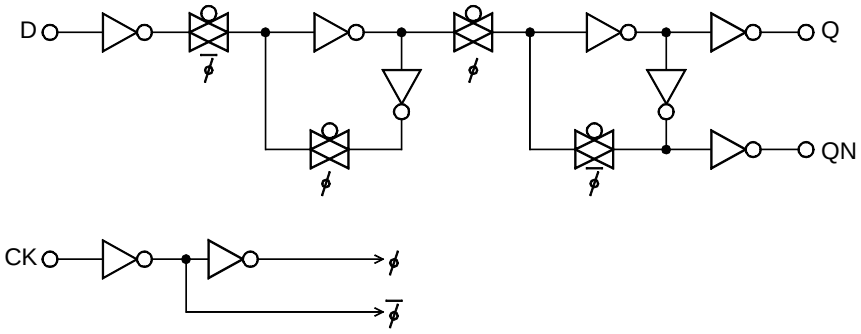
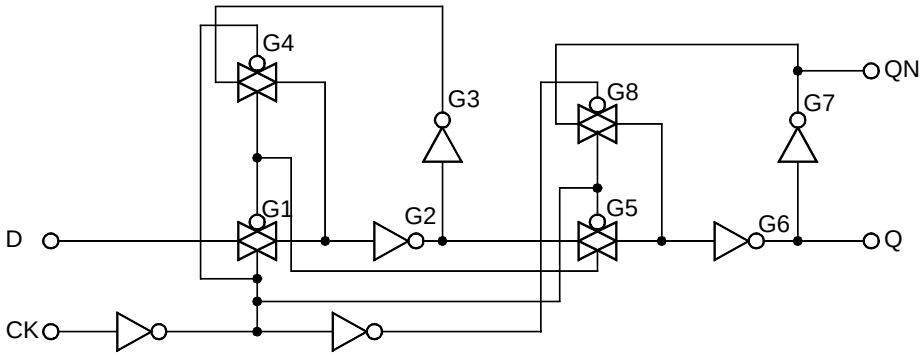


Figure 4-36 **YFD1 Flip-Flop**



YFD-type flip-flops are subject to constraints in connecting to other macrocells. See 4.12 , *Miscellaneous Design Considerations* ***for this.***

4.5 Choosing Macrocells

4.5.4 Flip-Flops without Inverted (QN) Output

Rules & Tips

- **Cell-based IC libraries offer D flip-flops without inverted (QN) output. Use these flip-flops when you do not need the QN output.**

Cell-based IC libraries provide D-type flip-flops in versions without an inverted (QN) output. These flip-flops use the “Q” suffix (e.g., FD1Q, FD2Q, etc.). Figure 4-37 and Figure 4-38 show the electrical schematics of FD1 and FD1Q.

Notice that the FD1 has an extra inverter, G2, in addition to the FD1Q; so the FD1 requires more grid area than the FD1Q. In the FD1, G1 is loaded with both G2 and G3, reducing the speed. Therefore, when you do not need an inverted output from a D flip-flop, the FD1Q is more favorable than the FD1.

Figure 4-37 **FD1 Flip-Flop**

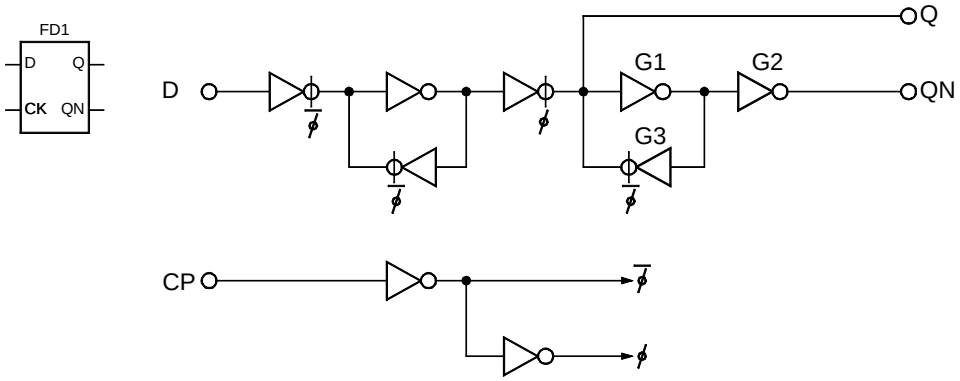
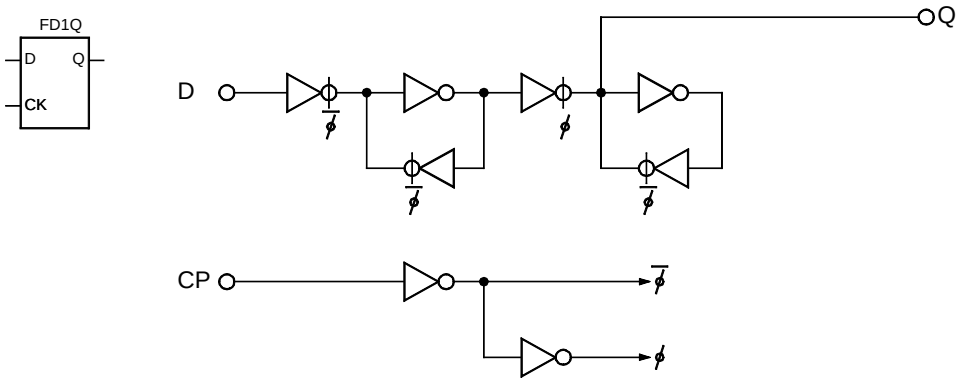


Figure 4-38 **FD1Q Flip-Flop**



4.6 Design-for-Reliability Recommendations

Rules & Tips

- **This section presents ways to design reliability into a circuit. It gives recommendations, or preferred practices for designs, for developing logic that lends itself to simulation and smooth transitions between design phases.**

A summary of what you will learn in this section follows:

- Fanout limits

  Abiding by fanout limits is important for two reasons. One reason is to ensure accurate delay estimates. The other is to protect a circuit against degradation over the guaranteed period of product reliability.

- Toshiba Clock Tree Synthesizer (TCTS)

  The Toshiba Clock Tree Synthesizer (TCTS) enables you to achieve near-zero clock skew while at the same time cut clock delays by approximately 20 percent. TCTS minimizes the post-layout identification of timing errors and layout iterations.

- Clock signals

  Use a single high-drive buffer to drive a system clock so that a clock tree can be automatically generated using the Toshiba Clock Tree Synthesizer (TCTS). The design most sensitive to clock skew is shift registers. Add one or more levels of gates between flip-flops. If in no way can you modify your design to make it comply with the TCTS's requirement, be sure to insert tight safeguards against clock skewing.

- Buffer cell considerations

  Toshiba's ASIC cell libraries include inverting, non-inverting, and inverting/noninverting internal buffers. The number of places a buffer cell fans out should be limited to 64. Use a buffer with a fan-out capability consistent with your need.

- External asynchronous signals

  If an asynchronous data signal comes from the external environment, then use a separate flip-flop to synchronize the incoming signal with the system clock.

- Avoiding race conditions

  A circuit subject to race conditions is bound to be unreliable. If the order of the input signals to the same cell is important for its correct operation, be sure to allow for adequate timing margins.

- Critical path timing

  It is necessary to identify critical paths in order to determine speed requirements. The critical path is typically the slowest signal path between two sets of registers running on the same clock.

4.6 Design-for-Reliability Recommendations

4.6.1 Fanout Limits

Rules & Tips

- **Keep macrocell's output load to within the "OUTPUT DRIVE" values indicated in data books.**
- **For wires switching ultra fast (over 60 to 90 MHz, depending on the ASIC technology used), the maximum allowable load is reduced to minimize electromigration.**

Delay Considerations

A gate connecting to many places has a high fanout and drive a heavy load. In a CMOS circuit, there is no "theoretical" limit to how heavy a load a gate can drive. Nonetheless, for practical purposes, the load should be limited to no more than the numbers indicated in the "OUTPUT DRIVE" section of the data book.

The "OUTPUT DRIVE" numbers represent the number of maximum loading units (LU) a macrocell can drive, in a certain time, into a determinate logical level. No matter how many places a gate fans out, it will eventually reach its final state even if it takes some time to do so. However, the ramp rate of a signal becomes shallow as the load increases. As the ramp rate becomes shallower, the delay prediction becomes less accurate due to the very nature of the digital logic simulator. Moreover, the driven macrocells spend more time in switching, where both N- and P-channel transistors are on, thus consuming excessive power due to overlap currents as a result. This, in turn, causes electromagnetic interference (EMI) to increase.

The Toshiba Design Verifier software contained in ASIC design kits allows you to automatically check all macrocell outputs for loading limits.

Electromigration Considerations

As the metal lines in integrated circuits get thinner, a phenomenon called electromigration (EM/EMG) gets to be a problem because shorts and opens are possible. Electromigration is the self-diffusion of metal along interconnect wires, induced by the passage of a direct current through the metal.

With regard to electromigration, the main impact of submicron to deep-submicron integration is the current capability requirements of interconnect wires. Electromigration occurs over time and may not show up

until a device has had many hours of operation. Assuming that the die temperature and supply voltage are constant for the purpose of discussion, time to failure is a function of current density; that is, switching frequency times load for a given technology.

To avoid potential EMG problems, the “OUTPUT DRIVE” values have been determined, using the maximum operating frequencies shown in Table 4-10 as a basis. This is a safeguard to guarantee an interrupted (i.e., around-the-clock) circuit operation over ten years.

Table 4-10 Switching Frequency Assumptions for EMG Loading Limits

Product Series	Frequency
TC160G/E, TC163G, TC26SC	60 MHz
TC170G/E/C	60 MHz
TC180G/E/C, TC183G/E/C	80 MHz
TC190G/E/C	70 MHz
TC200G/E/C, TC203G/E/C	90 MHz

In the event that any interconnect (e.g., clock) in your design operates faster, the maximum load it can drive must be reduced accordingly. Suppose, for example, the “OUTPUT LOAD” limit of a given TC180G macrocell is 183 LU and it switches at 100 MHz. Then the EMG-based loading limit is calculated as:

$$183 \times \frac{80}{100} = 146.4 \ (\mathrm{LU})$$

Toshiba is now preparing to upgrade the Design Verifier software toward automated checks for EMG loading limits. For software availability, ask the Toshiba ASIC service group.

4.6 Design-for-Reliability Recommendations

4.6.2 Toshiba Clock Tree Synthesizer (TCTS)

Rules & Tips

- **The Toshiba Clock Tree Synthesizer (TCTS) minimizes post-layout identification of timing errors and layout iterations. TCTS enables you to achieve near-zero (no more than 0.1 ns) clock skew while at the same time cut clock delays by approximately 20 percent.**

An ideal clock incurs no delay through the clock network. However, in real world, registers such as flip-flops clocked by a propagated clock have edge times skewed by the path delay from the clock source to the register clock pin. A signal takes much longer to reach an clock element all the way across the chip than it does to reach an element close to the gate driving the wire.

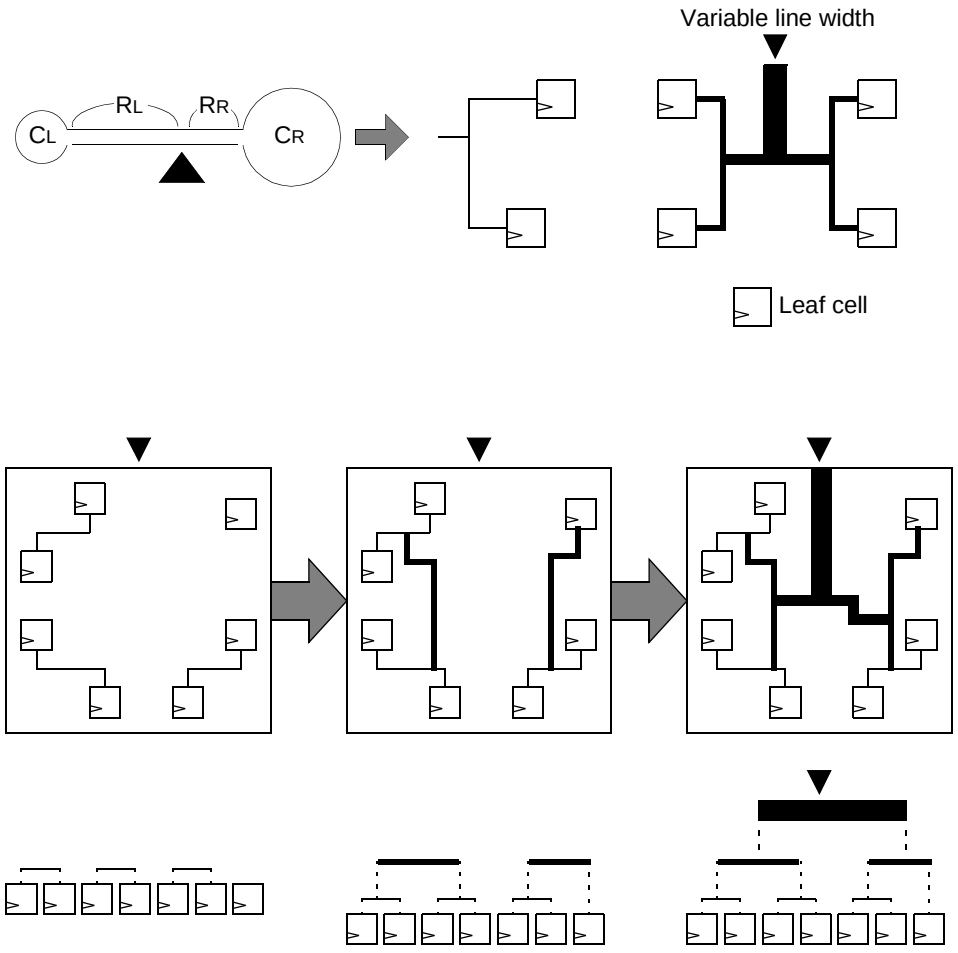
Pre-layout wire load estimates are based on the assumption that all cells are distributed fairly homogeneously across the chip. When a driving gate fans out to many places, wiring estimates tend to be rather wide of the mark. In addition, RC-tree effects of interconnect wires will have a significant impact on the total delay, causing clock skew to increase.

To minimize the risk of post-layout identification of wiring problems and costly layout iterations, Toshiba employs TCTS to deskew heavily-loaded clock signals.

TCTS first creates clusters of the flip-flops so the capacitive load on each piece of the clock net will be balanced. Then it creates a clock distribution system known as a clock tree. During this step, one or more levels of drivers are added, clock nets are partitioned, and added clock nets are connected. Finally, physical connection points and optimal line widths are determined, bottom up, using a method called RC-delay balanced routing. Driver locations are fine-tuned as needed.

Experiences show that TCTS can achieve near-zero clock skew (less than 0.2 ns or one-tenth without TCTS) with approximately 20 percent less delays. Further, the electromigration-based loading limits are abided by during this process.

Figure 4-39 **Clock Tree Synthesis**



4.6 Design-for-Reliability Recommendations

4.6.3 Clock Signals

Rules & Tips

Requirements for Using TCTS:

- **Use a single high-drive buffer designated IDRVx to drive a system clock signal.**
- **As for shift registers, add one or more levels of gates between flip-flops (e.g., IVDA for gate arrays, NIV for cell-based ICs).**

If you can not make your design compliant with the TCTS requirement:

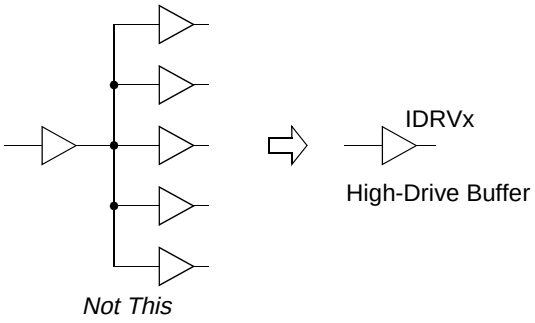
- **Activate every other flip-flop using the opposite polarity of the clock, or**
- **Partition flip-flop strings by bits rather than words, and keep each of the flip-flop strings to within 32 stages.**

System Clock Signals

TCTS requires that you use a single high-drive buffer (IDRVx) in a pre-layout design to drive a large fanout net, rather than splitting the fanout using a tree structure. After pre-layout verification is completed, TCTS takes the design and automatically generates a clock tree. During this process, it automatically replaces the IDRV cell with an appropriate “root driver.”

The maximum number of nets that TCTS can handle varies, depending on the chip size, gate utilization, and circuit configuration; it is typically 4 to 8.

Figure 4-40 Use a High-Drive Buffer Rather Than Splitting the Fanout



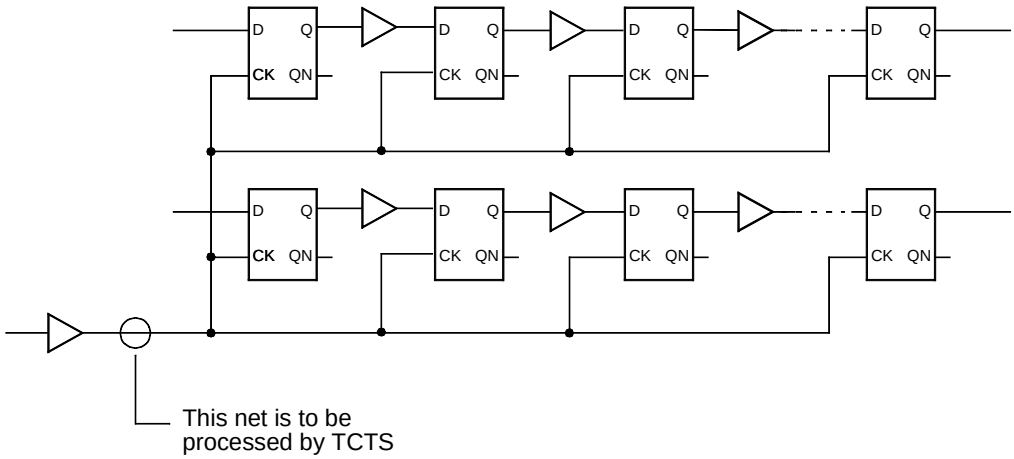
Shift Register Clocks

Shift registers are very sensitive to hold time. Clock lines for wide shift registers tend to have very high fanout whose loads must be balanced properly. The subsections that follow present ways to minimize clock skew on shift registers. They apply not only to a design specifically intended as a shift register but to a design that performs data shift.

Requirement for Using TCTS

Clock skew problems occur when the clock arrives early to one flip-flop causing its output to change before the clock arrives at the next flip-flop. This can result in hold time violations and the wrong data being latched. To avoid this situation, insert one or more levels of gates (e.g., IVDA for gate arrays and embedded arrays; NIV for cell-based ICs) between the flip-flops, as shown in Figure 4-41. Use an IDRVx cell as the root driver. In this case, there is no limit, in the pre-layout design, to the number of flip-flops driven by the IDRV cell since the load on the clock line will be split by TCTS.

Figure 4-41 **Clock Signals To Be Processed with TCTS**

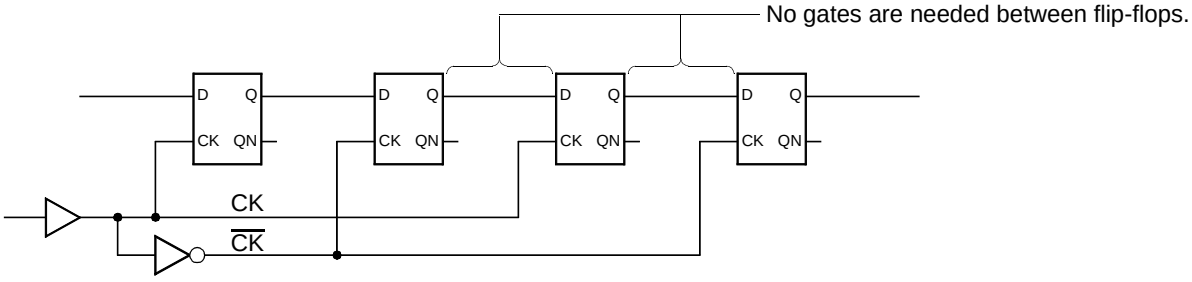


Clock Signals Not To Be Processed with TCTS

Shift registers clocked by a clock signal that will not be processed with TCTS require a careful consideration about clock skew. Two ways to avoid clock skew problems are shown below.

- Activate every other flip-flop using the opposite polarity of the clock, as shown in Figure 4-42. This design does not suffer from clock skew problems because a given flip-flop is clocked on the rising edge of the clock while the next flip-flop is clocked on the falling edge, such that input data to each flip-flop always changes on the inactive edge of the clock to that flip-flop. Therefore, no gates are necessary between flip-flops. Be sure to balance the loads on both edges of the clock.

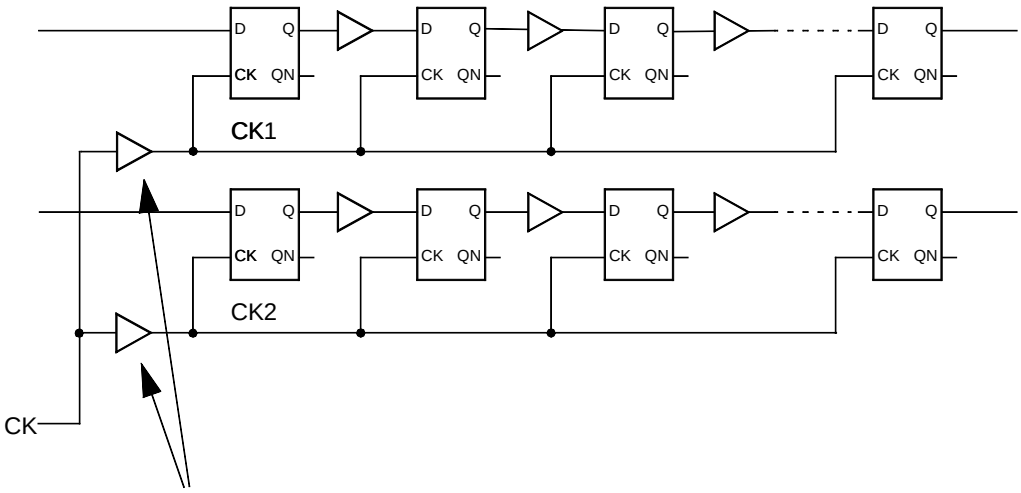
Figure 4-42 Activate Every Other Flip-Flop Using the Opposite Polarity of Clock



■ The “OUTPUT DRIVE” limit must be abided by.
■ Be sure to balance the load on CK and $\overline{CK}$.

- Partitioning flip-flop strings by bits rather than words will invariably reduce clock skew. Insert one or more levels of gates between flip-flops. Add a sub-driver at the head of each of the bit rows. In this case, shift registers should be limited to no more than 32 bits wide as a rule.

Figure 4-43 **Partition Flip-Flop Strings by Row Rather Than by Words**



4.6 Design-for-Reliability Recommendations

4.6.4 Buffer Cell Considerations

Rules & Tips

- **Use a buffer with an adequate drive capability.**
- **Drive data signals with a buffer tree. Keep the fan-out of a buffer to within 64 places.**
- **Use a separate buffer to drive nets from I/O cells and megacells.**

Toshiba's ASIC cell libraries contain inverting, non-inverting, and inverting/noninverting internal buffers. Table 4-11 shows internal buffer cells available for gate array, embedded array, and cell-based IC designs.

Table 4-11 Internal Buffer Cells
(Drive values are for the TC180G/E/C series.)

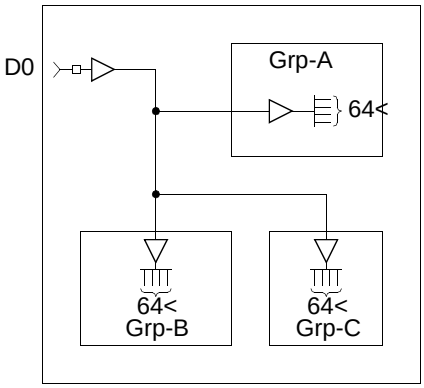
	Gate Array / Embedded Array		Cell-Based IC		Output Stage
	Cell Name	Drive (LU)	Cell Name	Drive (LU)	
Inverting	IV	33	IV	16	Inverter
	IVA	60	IVS	22	Inverter, 2x P-ch in parallel
	IVP	68	IVM	31	2-inverters in parallel
	B5I	98	IVML	47	3- inverters in parallel
	IVAP	111	n/a		2-inverters in parallel, 2x P-ch in parallel
	B4I	130	IVH	61	4-inverters in parallel
	B5IP	195	n/a		6-inverters in parallel
	B4IP	260	IVU	122	8-inverters in parallel
Non-inverting	n/a		NIV	16	1x drive buffer
	n/a		NIVM	32	2x drive buffer
	n/a		NIVH	64	4x drive buffer
	n/a		NIVU	126	8x drive buffer
Inverting / Non-Inverting	IVDA	33, 33	n/a		Inverter/buffer
	IVDAP	68, 68	IVDM	30, 32	2x drive inverter/buffer
	B3I	68, 68	n/a		2x drive inverter/buffer
	B2I	33, 98	IVDM1	17, 47	1x drive inverter/3x drive buffer
	B3IP	130, 130	n/a		4x drive inverter/buffer
	B2IP	68, 195	n/a		2x drive inverter/6x drive buffer

Rules of thumb for using buffer cells follow:

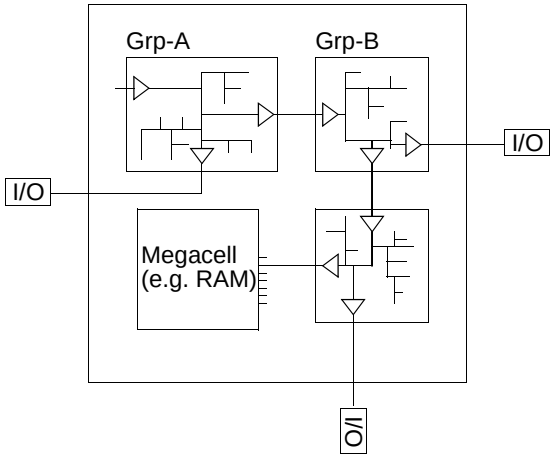
- Avoid the IDRV cell with low fanout.
- Use a buffer cell with a drive capability consistent with your need.
- Build a buffer tree for data signals. A buffer should not fan out to more than 64 places as a rule.
- The nets from I/O cells and large megacells tend to become longer than expected. To reduce the impact of this, use a separate buffer to drive them.

Figure 4-44 **Using Buffer Cells**

■ Build a buffer tree for data signals.



■ Use a separate buffer for inter-block nets and nets to I/O.



4.6 Design-for-Reliability Recommendations

4.6.5 External Asynchronous Signals

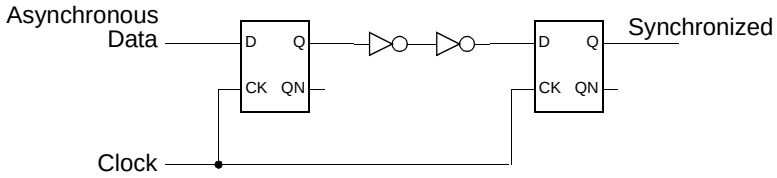
Rules & Tips

- **Use a separate flip-flop to synchronize the incoming signal with the system clock.**

When an asynchronous data signal comes from the external environment, it is not guaranteed that the data signal will meet the setup/hold requirements on the first flip-flop. As a result, the asynchronous signal fed into a flip-flop would cause random spurious failures. If the asynchronous incoming data does not meet the setup time requirement for the flip-flop, there exists a window of time where the incoming signal may cause the flip-flop to develop an unknown, or metastable, logic condition. There is no predicting which logic level the Q output will finally assume.

If the data signal is asynchronous, then guaranteeing the correct operation is only possible by synchronizing it. Run the asynchronous data input to a separate flip-flop, as shown in Figure 4-45.

Figure 4-45 Synchronizing an External Asynchronous Signal



In this circuit, if the metastable state does not last longer than one full cycle, the Q output coming from the second flip-flop will have a determinate logic state. Obviously, the setup/hold time requirements on the first flip-flop must be met during simulation. Allow for the tester head skew (±5ns for a design with no more than 100 pins, ±2 ns for a design with over 100 pins) when defining the input timing. See Section 5.3.5, *Tester Head Skew*, on page 5-16 for this.

4.6 Design-for-Reliability Recommendations

4.6.6 Avoiding Race Conditions

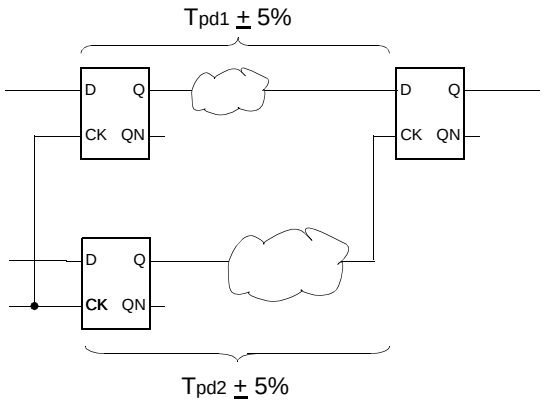
Rules & Tips

- **A circuit subject to race conditions is bound to be unreliable. If the order of the input signals to the same cell is important for its correct operation, be sure to allow for adequate timing margins.**

Correct functioning of sequential circuits depends on the order in which inputs are applied. Race conditions occur when the same signal follows two or more paths having different delays to the same cell. Figure 4-46 is a design susceptible to race conditions.

The interval between signal changes is difficult to predict, since delays vary widely due to variations in processing, power supply, temperature, and chip layout. As a consequence, a circuit subject to race conditions is bound to be unreliable. You should avoid designs whose correct functioning depends on a predictable interval between signals traversing different delay paths. Or otherwise, to reduce the risk of possible race conditions, allow for 5% timing margins for the data path and the clock path each.

Figure 4-46 Avoiding Race Conditions



4.6 Design-for-Reliability Recommendations

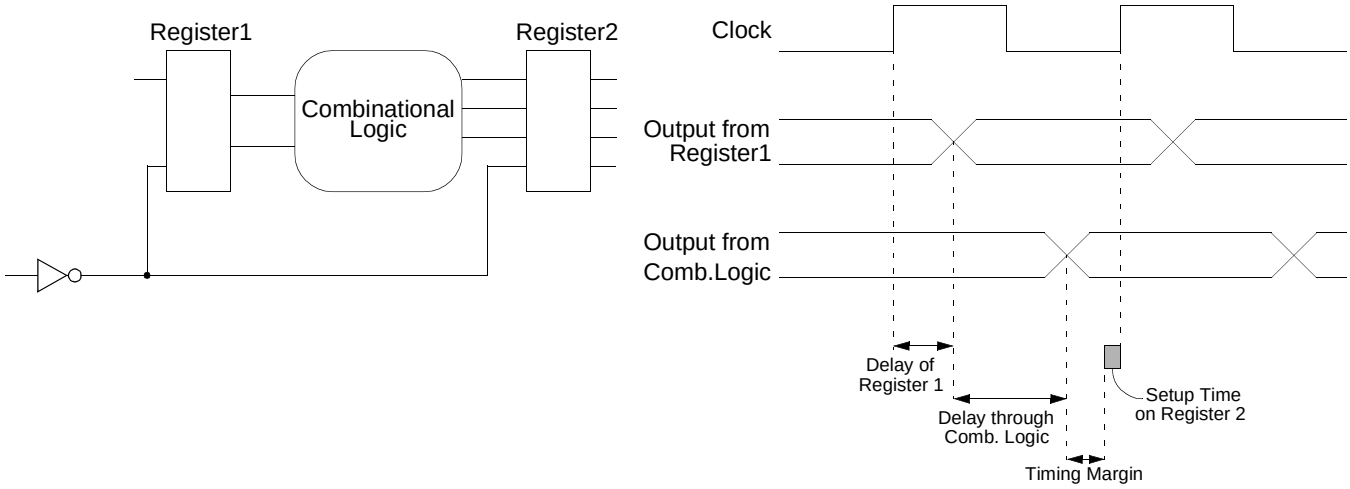
4.6.7 Critical Path Timing

Rules & Tips

- **It is necessary to identify critical paths in order to determine speed requirements. The critical path is typically the slowest signal path between two sets of registers running on the same clock.**

It is necessary to identify the potentially critical path(s) in order to determine speed requirements. Typically, the critical path is the longest signal path between two sets of registers having the same clock.

Figure 4-47 Critical Path



In Figure 4-47, the correct operation of the circuit depends on the relative timing between the data and clock arrival times on Register 2. The timing diagram indicates that for optimum performance it is required that the clock period be as short as possible, but it must not be shorter than the sum of the delay of Register 1, the delay through the combinational logic block, and the setup time for Register 2, regardless of variations in delay times. Hence, this equation must be satisfied:

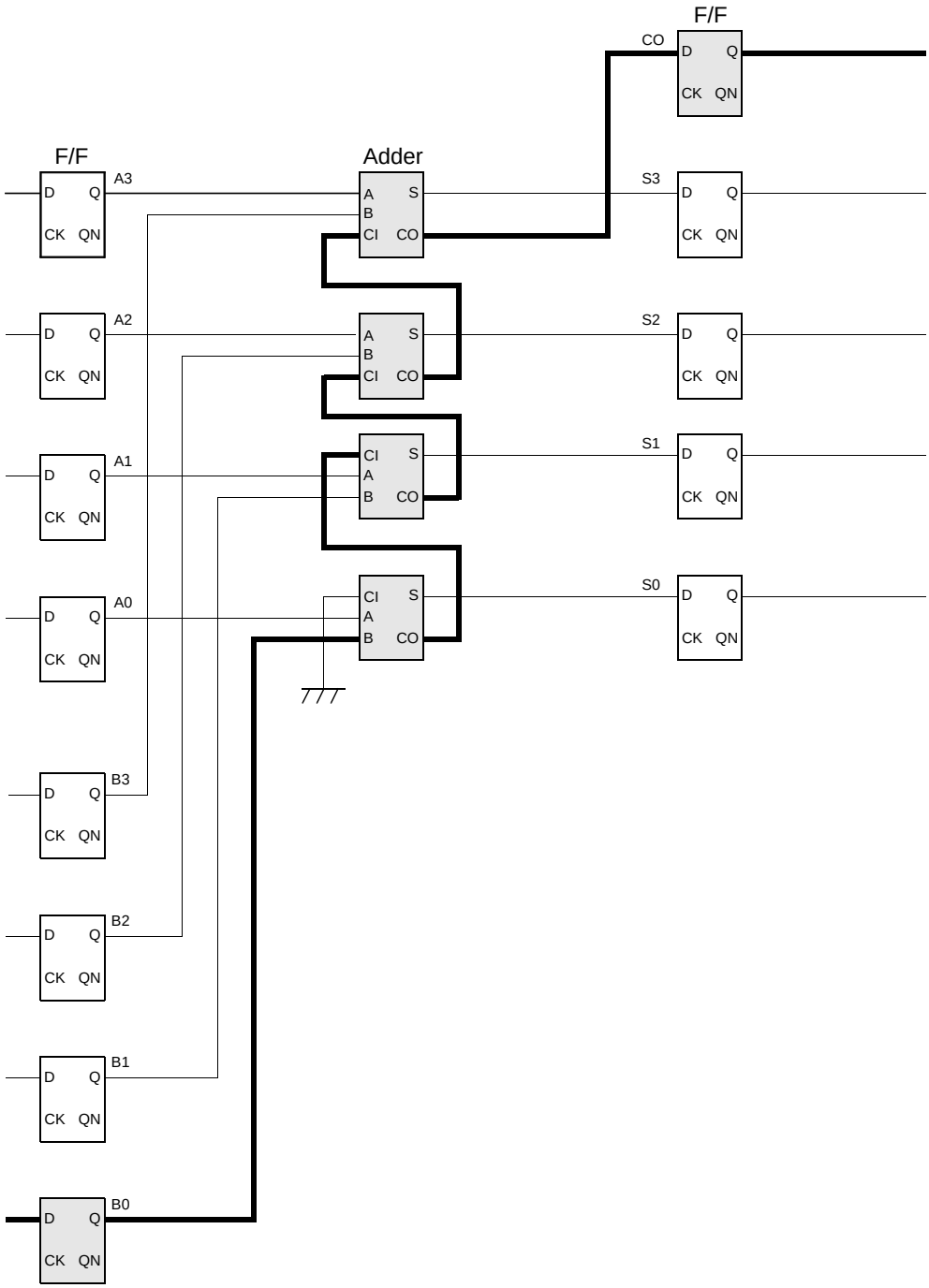
$$T_{R1} + T_{crt} + T_{set} < \text{clock\_period}$$

where:

T_{R1}: Delay of Register 1
T_{crt}: Critical path delay in the combinational logic block
T_{set}: Setup time requirement for Register 2

Figure 4-48 highlights a critical path example in a 4-bit buffered adder.

Figure 4-48 A Critical Path Example in a 4-Bit Buffered Adder



4.7 Design-for-Reliability “Never” Rules

Rules & Tips

- **This section describes design practices that MUST NOT be introduced into an ASIC since they will nearly always cause mischief or problems to simulation, testing, and/or reliability of a circuit.**

A summary of what you will learn in this section follows:

- Asynchronous pulse generators

  Never use such asynchronous pulse generators as ring oscillators, one-shot circuits, and chopper circuits, since the pulse width is bound to be unpredictable. Use a synchronous pulse generator instead.

- Hazard circuits

  Never use a potential hazard generator to drive a clock, clear, or preset line because hazards can cause a false clock signal or clear subsequent registers. Never use gated clocks since gated clocks are also highly susceptible to hazards.

- R-S flip-flop

  Never use cross-coupled flip-flops implemented with NAND or NOR gates. They are prone to conflicting Set and Reset signals, latching in an erroneous data.

4.7 Design-for-Reliability “Never” Rules

4.7.1 Asynchronous Pulse Generators

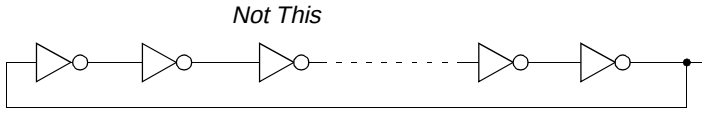
Rules & Tips

- **Never use such asynchronous pulse generators as ring oscillators, one-shot circuits, and chopper circuits, since the pulse width is bound to be unpredictable.**

Ring Oscillators

Rings of an odd number of inverters have no stable condition and will oscillate with a period that is some odd submultiple of the propagation delay twice around the ring. Since propagation delays are affected by the processing, supply voltage, temperature, and the chip layout, the resulting pulse width is bound to be unpredictable. Since internal nodes are inaccessible during device testing, the speed of the ring oscillator and the generated clock signal can not be measured with a tester.

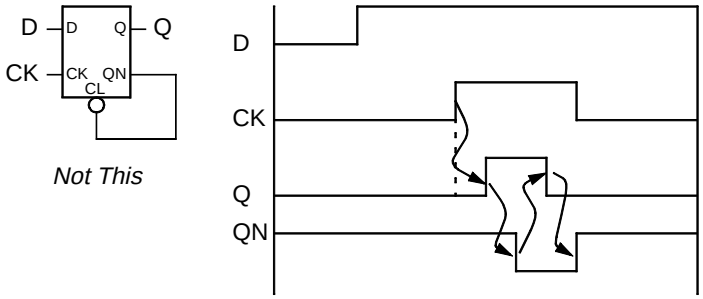
Figure 4-49 Do Not Use a Ring Oscillator



One-Shot Circuits

A one-shot circuit example is shown in Figure 4-50. In this circuit, when the Q output goes high, the QN output goes low and clears the flip-flop, creating a narrow positive pulse on the Q output. The width of the pulse is equal to the high-to-low delay from CL to Q. However, delay times are affected by the processing, supply voltage, temperature, and the chip layout. Since the CL-Q delay determines the pulse width, the loading condition on the Q output also has an influence on it. For these reasons, the one-shot-generated pulse is bound to be unreliable.

Figure 4-50 **One-Shot Circuit**

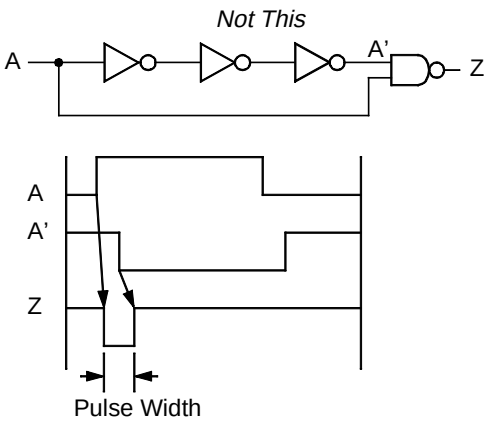


Chopper Circuits

Figure 4-51 shows a chopper circuit. The timing diagram beneath the circuit shows that the width of the pulse generated by this circuit is equal to the difference in propagation delays through the inverter chain and the wire beneath it.

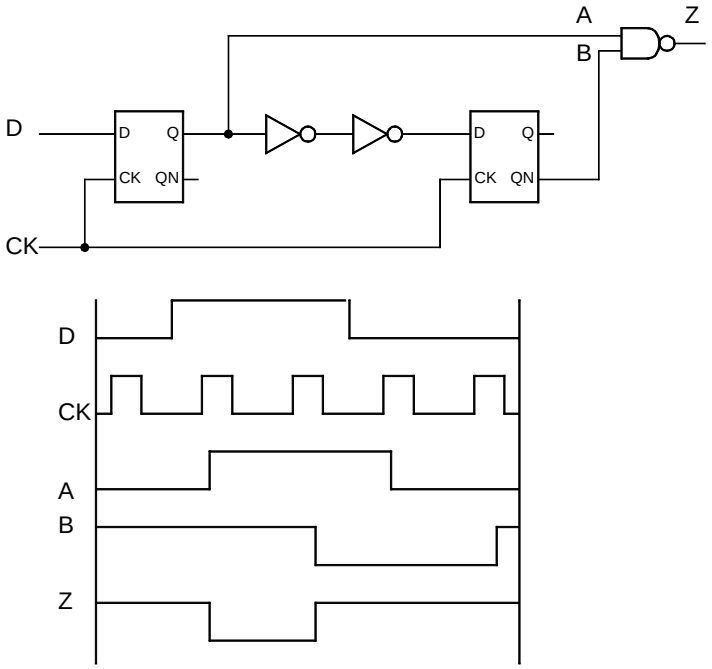
However, higher voltage supply, lower temperature and process variation will decrease the propagation delay of the inverter chain while affecting the wire delay only slightly. As a result, wire delay can approach that of the inverter chain. If the wire delay finally equal that of the inverter chain, no output pulse will be generated, and the circuitry will fail. Also, a narrow pulse is bound to be subject to edge rounding. Under heavy loading, the pulse may fail to reach a valid logic level, or it may disappear altogether.

Figure 4-51 **Chopper Circuit**



Use a synchronous pulse generator in place of an asynchronous one, as shown in Figure 4-52. Replace the inverter chain with two D flip-flops, and allow signal A to feed the data input of the first flip-flop.

Figure 4-52 **Use a Synchronous Pulse Generator**



In the synchronous pulse generator, the Z output is equal to the NAND of the Q of the first flip-flop and the QN of the second flip-flop. Its pulse width is equal to one full cycle of the incoming clock. You can generate longer pulses by using more flip-flops.

4.7 Design-for-Reliability “Never” Rules

4.7.2 Hazard Circuits

Rules & Tips

- **Never use a potential hazard generator to drive a clock, clear, or preset line because hazards can cause a false clock signal or clear subsequent registers.**
- **Never use gated clocks since gated clocks are also highly susceptible to hazards.**

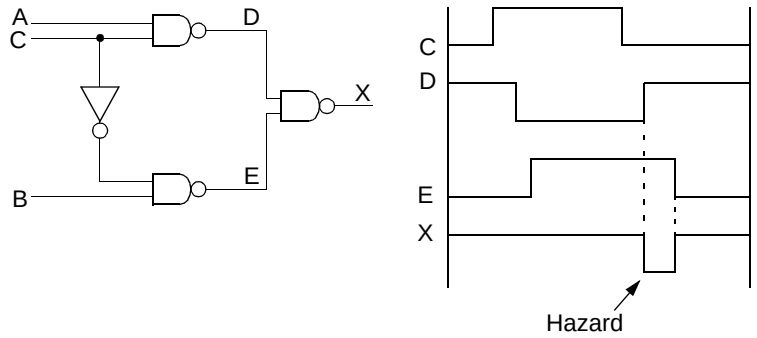
What is a Hazard?

A hazard is an abrupt signal transition from one logic state to another and then back again. Be aware of hazard behavior and how it might affect subsequent circuit’s operation.

Figure 4-53 below shows a circuit that invariably causes hazards. To understand how a hazard is generated, assume that A, B, and C are initially high. Therefore, output X is high. If C makes a high-to-low transition, D goes high, and E goes low. Note that, however, C propagates through two levels of gates — an inverter and a NAND gate — and most likely will reach the last NAND gate later than the low-to-high transition occurs at D. During this brief time, the output from the last NAND gate (X) glitches low regardless of the logic states of A and B.

Figure 4-53 A Potentially Hazard Generator

◇ A Potential Hazard Generator



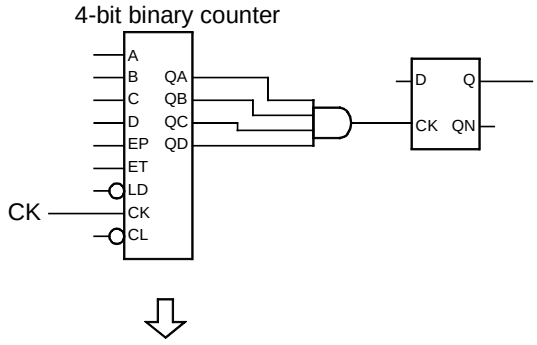
Using a Separate Flip-Flop for Decoded Signal

It is not probably risky to use the output of a potential hazard generator to drive the data input of a synchronous circuit if that output reaches a steady state before the active clock edge is applied. However, it is risky to use such a circuit to drive a clock, clear, or preset line because the potential hazard can cause a false clock signal or clear subsequent registers.

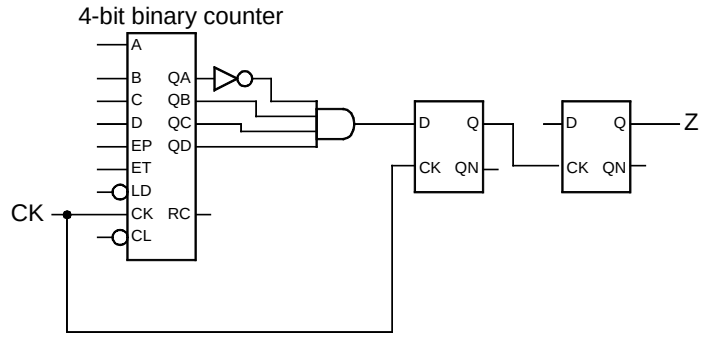
In Figure 4-54(a), the terminal count of the binary counter is detected with an AND gate. The decode signal is then used to drive a clock line. However, the loading on each of the Q outputs varies, and their propagation delays also vary. Therefore, the inputs to the AND gate do not stabilize at the same time. The output of the AND gate changes between a high and a low state, creating false clock signals, until it finally stabilizes to a steady state. To avoid hazard problems, decode the outputs of a binary counter by decoding one count before the terminal count and running the decoded signal into a separate flip-flop.

Figure 4-54 **Run a Decoded Signal into a Separate Flip-Flop (a)**

(a) The Carry Output Clocks a Flip-Flop

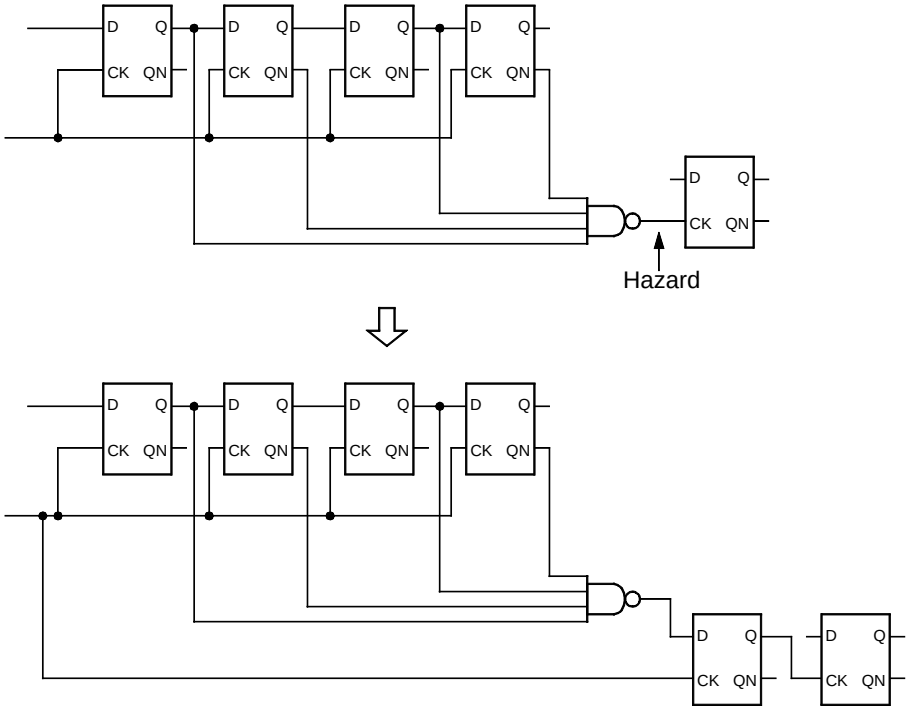


(b) Run a Decoded Signal into a Separate Flip-Flop



Another design example using the same technique is shown in Figure 4-55. In the modification of this design, the clock signal coming from the last flip-flop output will have a clean waveform.

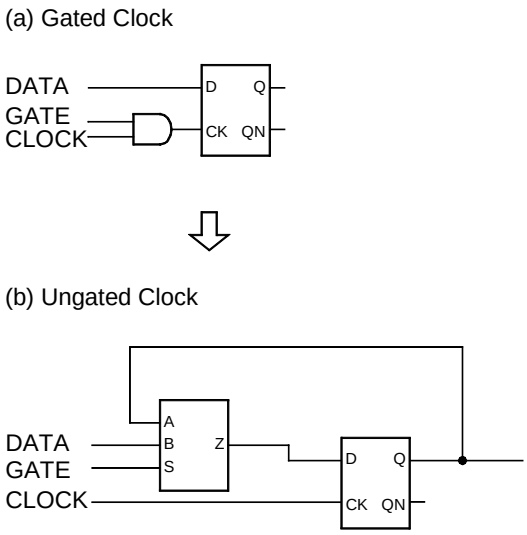
Figure 4-55 **Run a Decoded Signal into a Separate Flip-Flop (b)**



Gated Clock

Do not use a gated clock since instability in the gated signal can generate a hazard, causing the flip-flop to latch wrong data. The circuit of Figure 4-56(a) has a gated clock signal. A gated clock can not be modified by TCTS. The alternate design of Figure 4-56(b) is a better implementation of the same logic function. It uses the signal that would be used to gate the clock to control a multiplexer instead. However, a gated clock may be used in situations where a skew (or a time difference) as long as a few nanoseconds will not cause a timing problem.

Figure 4-56 **Do Not Use a Gated Clock**



4.7 Design-for-Reliability “Never” Rules

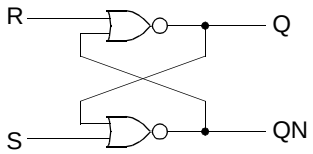
4.7.3 Cross-Coupled R-S Flip-Flops

Rules & Tips

- **Never use cross-coupled flip-flops implemented with NAND or NOR gates since they are prone to conflicting Set and Reset signals, latching in an erroneous data.**

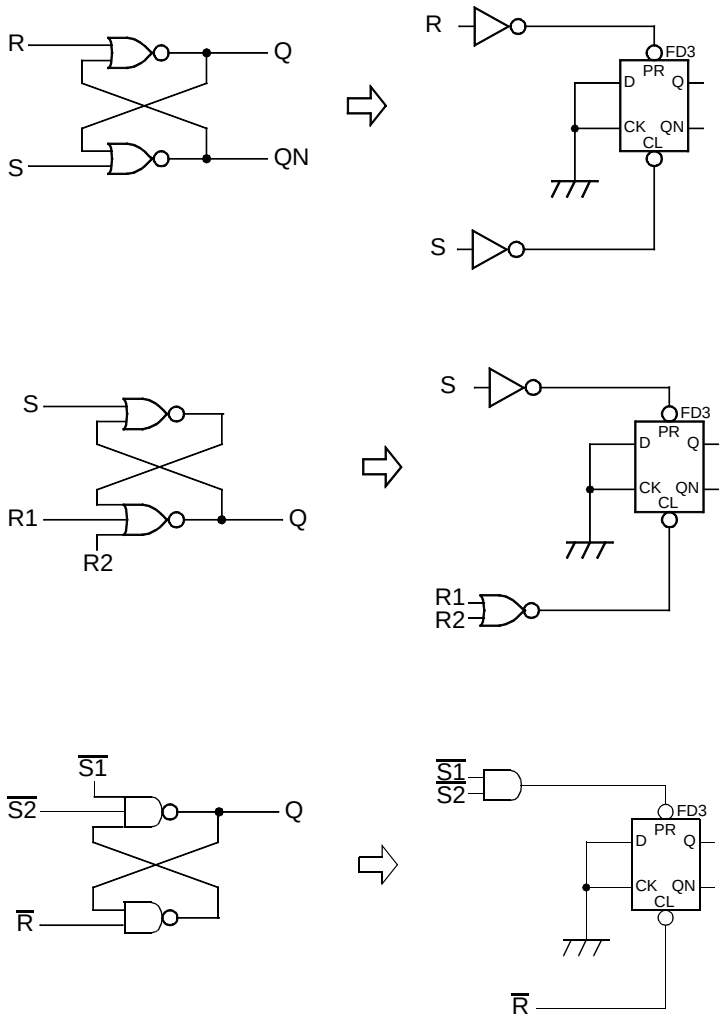
Figure 4-57 shows a cross-coupled R-S flip-flop using NOR gates. Note that if S is 0, Q can be driven to 0 by activating R; but once it is reset to 0, R can change without affecting Q. Q can only change from 0 by activating S. Note also that activating both R and S simultaneously results in an indeterminate output. Whether S or R wins the conflict will be determined by the physical aspect of the circuitry, or more specifically, the wire length of the cross-coupled interconnect nets.

Figure 4-57 Cross-Coupled R-S Flip-Flop



To avoid the conflicting states between R and S, the logic implementations using the FD3 flip-flop (with Clear and Preset) shown in Figure 4-58 are recommended.

Figure 4-58 **Modifications Over Cross-Coupled R-S Flip-Flops**



4.8 Design for Layout Success

Rules & Tips

- **When you are working with large, high-speed ASICs, physical layout can not be done in isolation. A two-way link between logical and physical (i.e., layout) designs is essential to a certain degree. Although logic designers need not have a detailed knowledge about layout steps, they must follow the practices for designs to ease the burden of layout, avoid (or reduce) layout iterations, and ensure the first-time success of post-layout simulation.**

A summary of what you will learn in this section follows:

- Block-level manual floorplanning

  Follow the guidelines for block-level floorplanning to ease the layout, improve gate utilization, reduce system noise, and speed up critical paths.

- Floorplanning tools

  A floorplanner allows you to quickly converge on timing at the front end. It also enables you to reoptimize a synthesized design. Toshiba provides a design kit for users owning a Toshiba-supported floorplanner.

- Clock signals

  Edge-operated clocked elements such as flip-flops are very sensitive to clock skew. To ensure the first-time success of the post-layout simulation, the place-and-route steps entail generation of a clock tree.

- Reset signals

  A heavily-loaded system reset signal is prone to RC-tree delays of more than 10 nanoseconds. Usually, system reset signals are powered by a buffer tree. You can have a system reset signal processed by TCTS, however, to split its load and reduce propagation delays.

- Maximum gate utilization

  Gate utilization is one of the most crucial factors in predicting chip routability. However, many other factors have an impact on as to whether your design is routable.

4.8 Design for Layout Success

4.8.1 Block-Level Manual Floorplanning

Rules & Tips

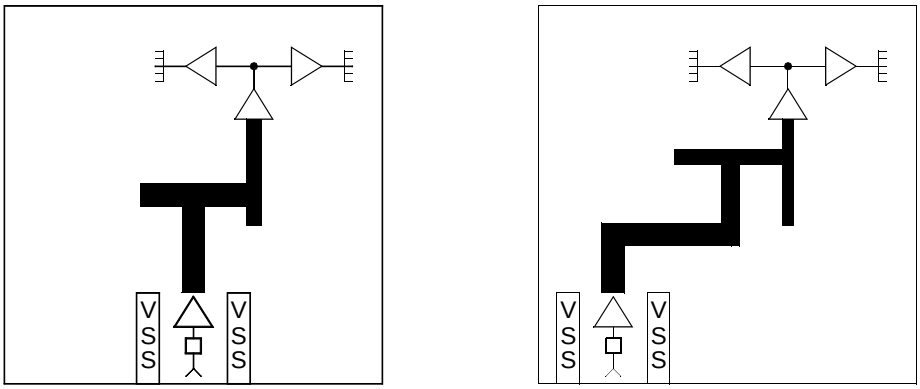
- **Position the noise-sensitive input pins such as clocks and resets between two VSS pins.**
- **Position the clock pin near the midpoint of a side to reduce overall clock delays.**
- **Position critical path pins close together.**
- **Position closely-coupled pins in proximity.**
- **Allow enough routing resources for nets that will route around megacells.**
- **Place megacells in proper locations so that cell areas will be rectangular.**
- **Do not let a megacell be an obstruction for a critical path to be straight.**
- **Use a separate buffer to drive the nets from I/O cells and megacells, as well as inter-block nets.**

I/O Cell Placement

Rules of thumb for placing I/O cells are:

- Sandwich noise-sensitive input pins such as clocks and resets between two VSS pins as a safeguard against noise due to simultaneously-switching outputs. Put the clock pin near the midpoint of a side so that overall clock delays will be reduced. For added safety, it is better, though not mandatory, to place a VDD3 and a VSS3 pin near a clock pin to damp out the ground rise on the VSS bus.
- Position the input and output pins at the head and tail of a speed critical path close together. Do not let megacells block critical paths. Otherwise, part way through the routing process, it is going to be found out that the obvious connection between two points is already taken, and the available route, if there is one, involves wandering halfway across the chip, crossing too many sites of the chip and incurring too many nanoseconds.
- Position all closely-coupled pins in proximity. For example, placing data bus pins in random locations makes timing convergence difficult to achieve.

Figure 4-59 **Position the Clock Pin Between Two VSS Pins**



Not This

Figure 4-60 **Place Critical Path Pins in Proximity**

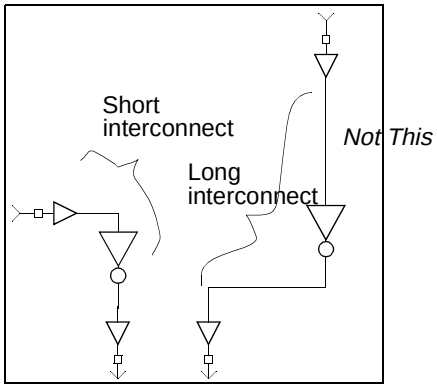
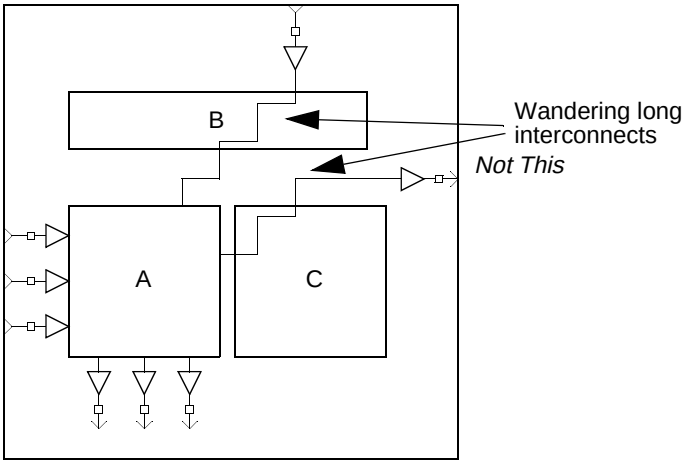


Figure 4-61 **Place Pins Connecting to the Same Block in Proximity**



Megacell Placement

Megacells are given precedence over cell areas in floorplanning since megacell locations have a greater impact on the subsequent floorplan and placement steps. A general assumption is that first- and second-metal wires do not run on a top of megacells. This assumption often makes megacells a limiting factor for routability and final routing quality. Good rules of thumb for placing megacells are:

- Allow enough routing resources for nets that will route around megacells.
- Place megacells so that the remaining cell areas will be rectangular or as nearly rectangular as possible. Avoid creating polygonal or long, narrow cell areas. Otherwise, long interconnections — the sort of nets that run between blocks — would result in wandering almost aimlessly around the chip.
- Do not let a megacell be an obstruction for a critical path to be straight.

Figure 4-62 **Allow Enough Routing Resources Around Megacells**

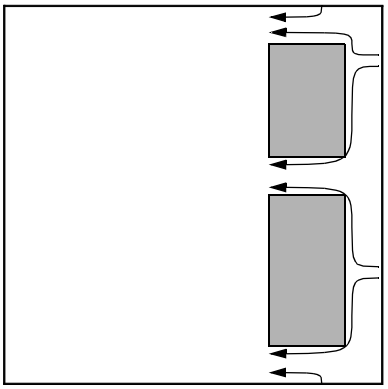


Figure 4-63 **Leave Rectangular Space for Cell Areas**

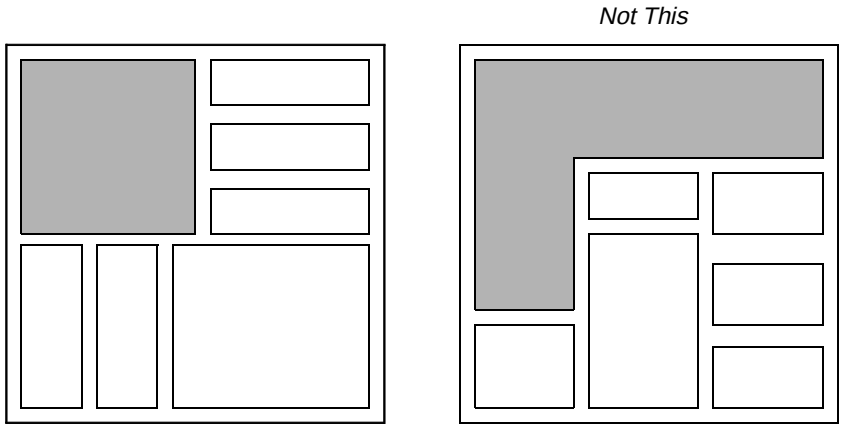
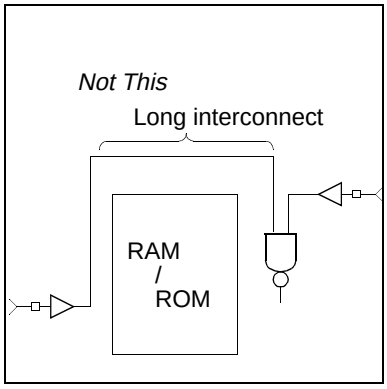


Figure 4-64 **Do Not Let a Megacell Block a Critical Path**



Interconnect Considerations

As discussed in Section 4.6.4, *Buffer Cell Considerations*, on page 4-76, the nets from I/O cells and large megacells tend to become longer than expected. To reduce the impact of this, use a separate buffer for these nets.

4.8 Design for Layout Success

4.8.2 Floorplanning Tools

Rules & Tips

- **A floorplanner allows you to quickly converge on timing at the front end (prior to pre-route simulation and timing analysis). It also enables you to reoptimize a synthesized design.**
- **Toshiba provides a design kit for users owning a Toshiba-supported floorplanner.**

In the deep-submicron ASIC realm, interconnect delay becomes dominant over the interior device delay. If you looked at the interconnect in the 1.0-micron generation, it was only 20 percent of total delay. At half micron and below, interconnect could account for more like 50 percent of the total. Since timing problems do not show up until the physical aspects of the design are completed at the back end, post-layout identification of interconnect problems can result in costly layout iterations. Therefore, closer links between logic and layout are more important below 0.5 micron. Here comes ASIC floorplanning tools.

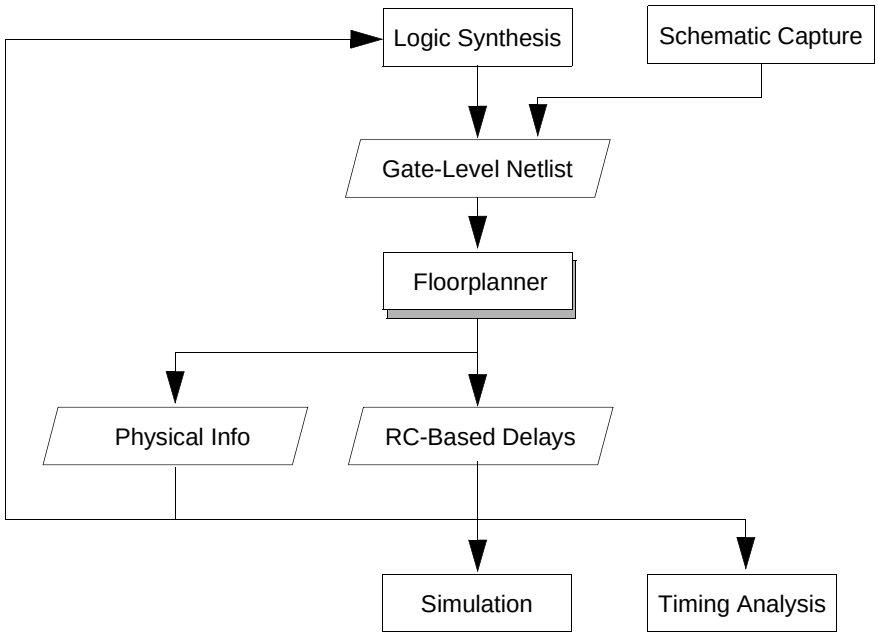
Benefits of Using a Floorplanner

Floorplanners provide accurate timing estimates without requiring logic designers to get involved in a “full” place-and-route. They help designers of deep-submicron ASICs estimate interconnect delays, routability and die size, and move floorplanning/placement from the back end to the person doing the design at the gate or register-transfer level.

Turnaround with accurate timing data is the most important benefit of floorplanning. More specifically, the profits of using a floorplanner are:

- You can back-annotate RC-based delays into a logic synthesis tool, and reoptimize a design, honoring information about a floorplan.
- You can “forward-annotate” RC-based delays to the pre-route simulation and timing analysis. The improved timing accuracy permits circuits that work right the first time up front.
- Since a floorplanner allows you to automatically generate a final-quality placement at the frond end, Toshiba does not have to do placement when your design goes to the layout tool, enabling quick-turn layout.

Figure 4-65 **Where Floorplanners Fit in the General Design Flow**

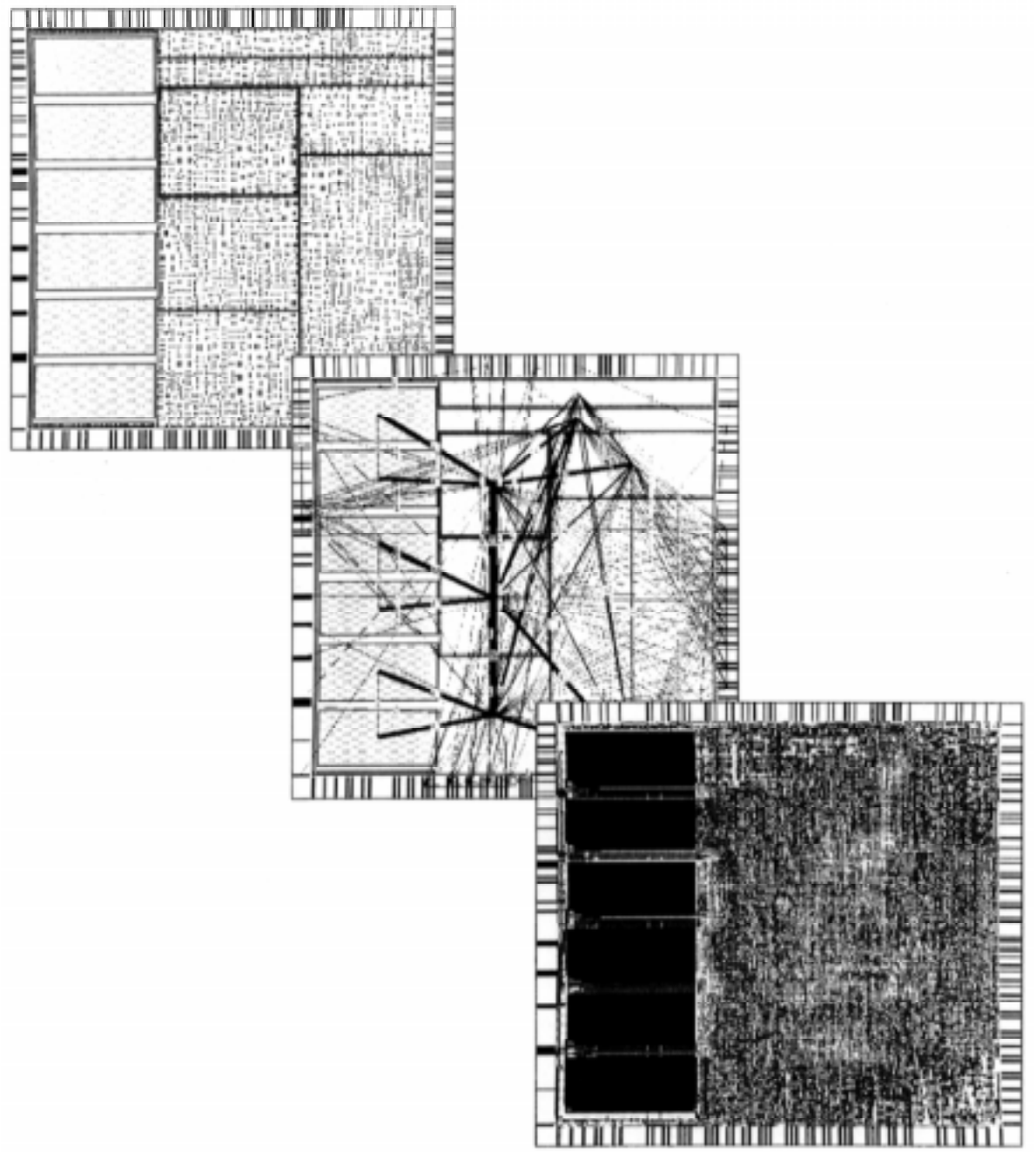


General Features of Floorplanners

Generally, floorplanners take a gate-level netlist as input. You begin your floorplanning session with a state of seed-placed (i.e., preplaced) I/O cells. Next, you simply read your netlist into the floorplanner. The floorplanner automatically creates an initial block placement, in accordance with the logic hierarchy of your design. Since megacells have a critical impact on the final floorplan quality as well as chip routability (and the chip performance), they are your first priority. After you have fixed megacell locations, you determine where to place cells areas, considering how signals broadcast throughout the chip (see the top plot in Figure 4-66). In most cases, you will need to resize and merge cell areas to get an optimal floorplan.

When a floorplan is completed, the automated placement capability of a floorplanner tool allows you to generate a cell placement. The benefits of getting definitive cell locations within the chip are more accurate routability and wire length estimates. At this point, you can get a feedback on the routing in your floorplan. The middle plot in Figure 4-66 displays bundles connecting the centers of areas and I/O pads. The width of each bundle is proportional to the number of nets which interconnect the areas or I/O pads. The bottom plot in Figure 4-66 shows the color map feature indicating the routing congestion in different parts of the chip.

Figure 4-66 **Floorplanner Features**



4.8 Design for Layout Success

4.8.3 Clock Signals

Rules & Tips

- **Following the design-for-reliability guidelines in Section 4.6.3, *Clock Signals*, will also simplify layout and post-layout simulation.**
- **Delay cells are available to adjust the data arrival time with respect to clock's active transition.**

Review of Design-for-Reliability

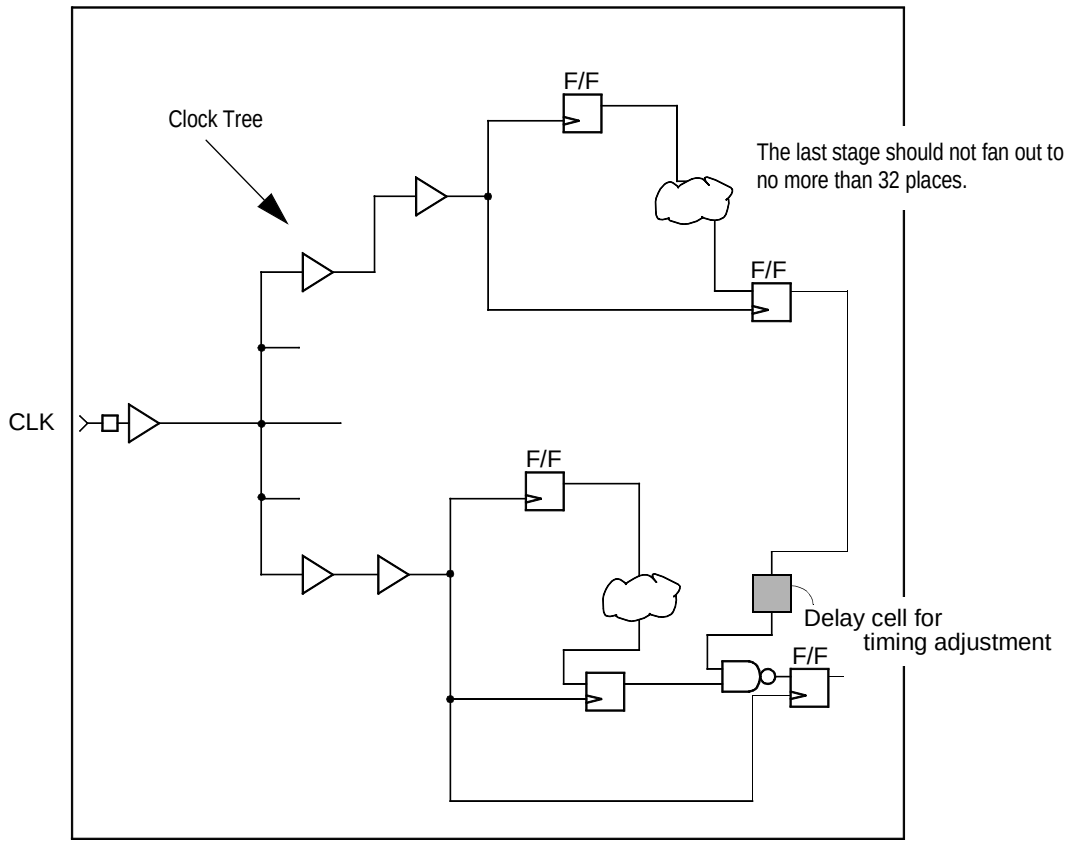
Following the design-for-reliability guidelines presented in Section 4.6.3, *Clock Signals*, on page 4-72 will surely render your design easier to deskew through the use of special layout strategies using TCTS. To recap:

- Use a single high-drive buffer designated IDRVx in a pre-layout design to drive a large fanout clock net, instead of splitting the fanout with a buffer tree. The maximum number of nets that TCTS can handle is typically 4 to 8.
- For clock signals that can not be processed with TCTS, build a buffer tree to split and balance the load. Each of the driver cells should not fan out to more than 32 places.
- For non-edge-operated signal lines (where clock skew problems need not be worried about), build a buffer tree, and limit the number of driven cells to 64 for each buffer.

Delay Cell for Retiming

Figure 4-67 shows a single-clock design where the clock line diverges into two lines, each of which drives different flip-flop strings. The diverged clock signals finally converge elsewhere in the design at a clocked element — one of them goes to the data input. Even when the same edge of the clock is used for both of the flip-flop strings, you need to insert an appropriate delay cell in the data line in order to adjust the data arrival time with respect to a clock's active transition at the converging point. The clocks for each of the flip-flop strings must be driven by an independent clock tree.

Figure 4-67 **Adjusting Data Arrival Time Using a Delay Cell**



4.8 Design for Layout Success

4.8.4 System Reset Signal

Rules & Tips

- **A heavily-loaded system reset signal is prone to RC-tree delays of more than 10 nanoseconds. Usually, power up a system reset signal by means of a buffer tree.**
- **For very-heavily loaded reset signal, you can employ TCTS to split the load.**

Adding a reset signal is the simplest and most effective way to initialize all flip-flops in a design at one time. Reset signals are often on a par with clock signals in terms of the number of driven cells. Remember that whereas the gate capacitance of a clock input is typically around 1 LU, a reset input has nearly or more than double that gate capacitance — 1.6 to 2.1 LU. In addition, longer wires translate into larger RC-tree delays. In a complex design, RC-tree effects alone can cause upwards of 10-nanosecond delays from the system reset I/O pin to the reset pin of the farthest element all the way across the chip.

In most cases, time differences (or skew) in reset signal's arrival times between multiple elements would not inadvertently influence the reset behavior since reset signals are usually level-operated (versus edge-operated). Therefore, to control the timing of the arrival of a reset signal, a system reset signal is powered up by a buffer tree.

In the case of a very-heavily-loaded system reset signal, you can utilize TCTS to split its load. Considering the limit of the number of signals that TCTS can handle (typically 4 to 8), you should not expend TCTS resources on more than one reset signal, however.

4.8 Design for Layout Success

4.8.5 Maximum Gate Utilization

Rules & Tips

- **Gate utilization is one of the most crucial factors in predicting chip routability. However, please bear in mind that many other factors have an impact on as to whether your design can fit into silicon. Ask Toshiba for chip routability estimates after you have completed a gate-level design.**

Gate utilization, or the ratio of the number of gates used by a design to the number of gates available on the chosen masterslice, has the most significant impact on chip routability. However, gate utilization is merely one of many determining factors; no types of front-end tools can give a definitive answer as to whether or not your design is routable. The final place-and-route systems use elaborate steps in getting the design to route, so the final placement and routing step is the only acid test for routability.

For example, chip routability is influenced by the number and types (i.e., topological aspects) of macrocells used, the total number of macrocell input/output pins, the number of interconnect wires, and the shapes of routing resources. Wide macrocells lower the flexibility of routing since routing congestions can easily occur around them. Square or near square cell areas help to ease routing.

A rule-of-thumb for populating a chip is listed in the “Usable Gates” section in the Toshiba CMOS ASIC catalog. Usable gate counts have been extrapolated, based on a design with the most typical chip configuration. Actual usable gates may decrease for a design that uses a large number of small gate macrocells (requiring four or less gates). Usable gates are also reduced for a complicated design where the number of nets exceeds the number of cells.

The Toshiba Design Verifier software produces a network summary containing information that the Toshiba layout engineers reference to estimate the chip routability. When your gate-level design have passed the Design Verifier with no errors, ask your Toshiba design center engineer for your chip routability estimate.

4.9 Design for Testability

Rules & Tips

- **This section presents ways to design testability into a circuit. It gives recommendations for developing logic that lends itself to both simulation and testing.**

Testing of Combinational Logic vs. Sequential Logic

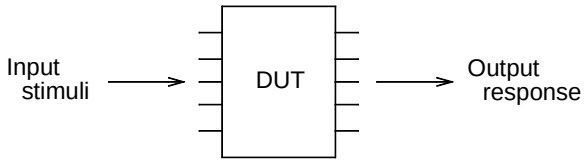
For a small combinational circuit, test patterns are relatively easy to develop. Combinational logic where the output states are a function of only the values applied to the inputs may be exhaustively tested with a test sequence that creates all of the possible input combinations and checks the output response for evaluation. For a combinational logic with n inputs, a total of 2^n test patterns would be required.

However, test generation is usually considerably more complex for sequential logic than for combinational logic because of the very nature of sequential logic; that is, the major difficulty in testing sequential logic is to determine the internal state of the circuit, since the output response of a sequential logic depends not only on the applied input values but also on the internal state of the circuit. If sequential logic has a total of m state variables, the number of test patterns required to fully test it increases to $2^n \times 2^m$. It is obvious that without design-for-testability (DFT) strategies test pattern development and test processes would be uneconomical, and often prohibitively costly, with circuit complexity approaching the VLSI realm.

Testing of an Integrated Circuit

An integrated circuit is tested to determine if it works according to specifications. Figure 4-68 shows a device under test (DUT) to which test stimuli are applied and the resulting output response is monitored. If the correct response is known, then we can determine whether the device is operating as we intended it to or not.

Figure 4-68 **Testing of a Device**



Keep in mind that the response can be observed only at physical output pins of a device. The output response is evaluated by comparing the device response to an expected response which usually comes from a logic simulation process.

Necessity of Design-for-Testability

Since test patterns are used to judge GO/NO-GO of manufactured devices, they must be extensive enough to identify potential faults. However, production testers have their hardware limitations as to pattern memory capacity. In addition, lengthy test patterns require more CPU time to simulate, thus incurring cost and lowering design productivity.

In the sections that follow, we will look at several design practices which cause testability problems and the techniques that can be used to remedy them. The solutions are rather straightforward and there is frequently more than a single solution.

4.9 Design-for-Testability

4.9.1 Circuit Initialization

Rules & Tips

- **Use a reset signal to initialize all elements whose state can not be readily determined by other means.**

When testing starts, the device under test can power up in an arbitrary state. To simulate this fact, all the signals in a circuit are set to undefined values (X) prior to simulation. Therefore, all internal registers such as flip-flops must be initialized to known states before proper simulation can begin. Use the reset signal to initialize all elements whose state can not be readily determined by other means. Although shift registers may be initialized by clocking in known input data, adding reset signals greatly reduces the number of test patterns required.

The designs above the arrows in Figure 4-69 to Figure 4-71 show a piece of untestable sequential logic since the circuit's initial output condition is unknowable. The designs below the arrows are better logic implementations easy to initialize.

Figure 4-69 **Circuit Initialization (a)**

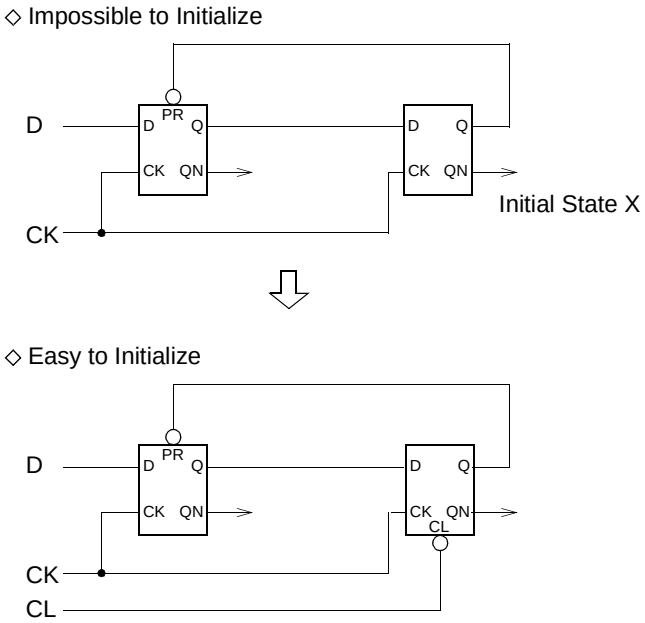
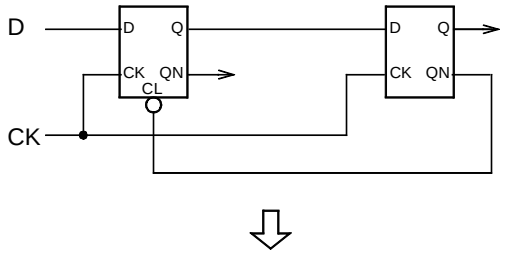


Figure 4-70 **Circuit Initialization (b)**

◇ Impossible to Initialize



◇ Easy to Initialize

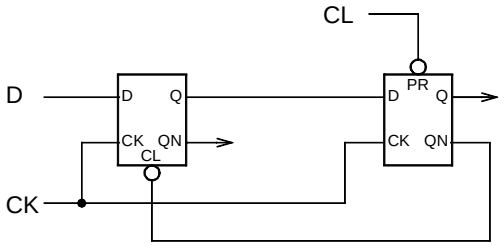
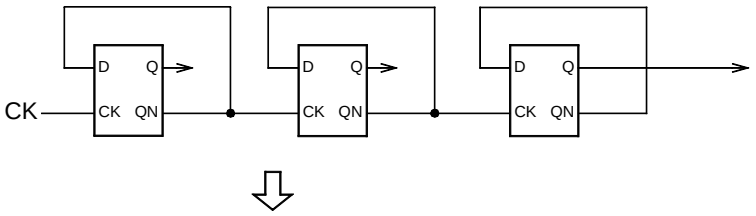
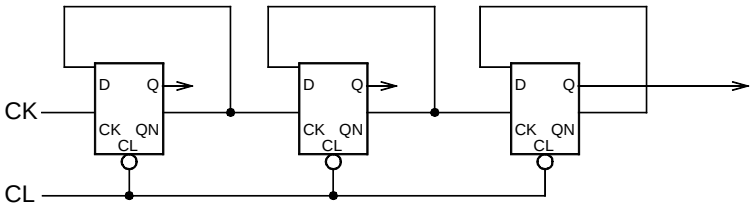


Figure 4-71 **Circuit Initialization (c)**

◇ Impossible to Initialize



◇ Easy to Initialize



4.9 Design-for-Testability

4.9.2 Counters

Rules & Tips

- **Break up a long counter into small chunks by means of a multiplexer.**
- **Add a test line for the internal logic that is kept from instantaneously responding to changes on the input pins.**

Breaking Up Long Counters

Long counters cause testability problems because a counter of several stages requires a prohibitively large number of test patterns to reach a particular state. The design of Figure 4-72(a) is a 16-stage counter, which requires 2 to the power of 16 (65,636) patterns to reach its terminal count. The 16-bit counter can be broken into two 8-stage counters by means of a multiplexer as shown in Figure 4-72(b). Then, any state can be reached with no more than 256 test patterns.

Frequency Dividers

Using a binary counter, high-frequency clock can be easily divided down by powers of two. With a 4-stage counter, the f/16 clock will occur after 2^4 clock cycles. The frequency divider using a binary counter may operate satisfactorily in circuit systems, but it can hinder efficient testing since a number of test patterns are needed for the divided clock signal to appear at the output, and the internal logic is kept from instantaneously responding to changes on the input pins.

Figure 4-73 shows a technique to reduce the number of test patterns required. The multiplexer, with the control line routed to an external I/O pin, allows you to direct either the reference clock signal or the f/16 clock signal to the internal logic. When TEST=1, the multiplexer acts as a buffer, and the divided clock signal appears at the output only after its propagation delay.

Use a multiplexer cell (MUX21H for gate arrays and embedded arrays; MX2 for cell-based ASICs), not an AND-OR gate. A selector circuit implemented as AND-OR is a potential hazard generator and can cause a false clock signal.

Figure 4-72 **Two Short Counters Are Easier to Test**

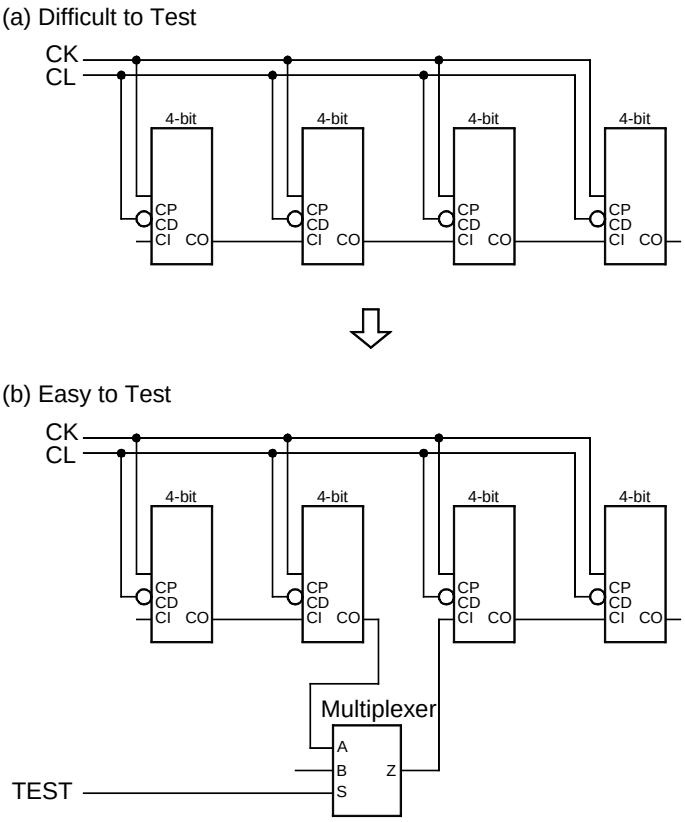
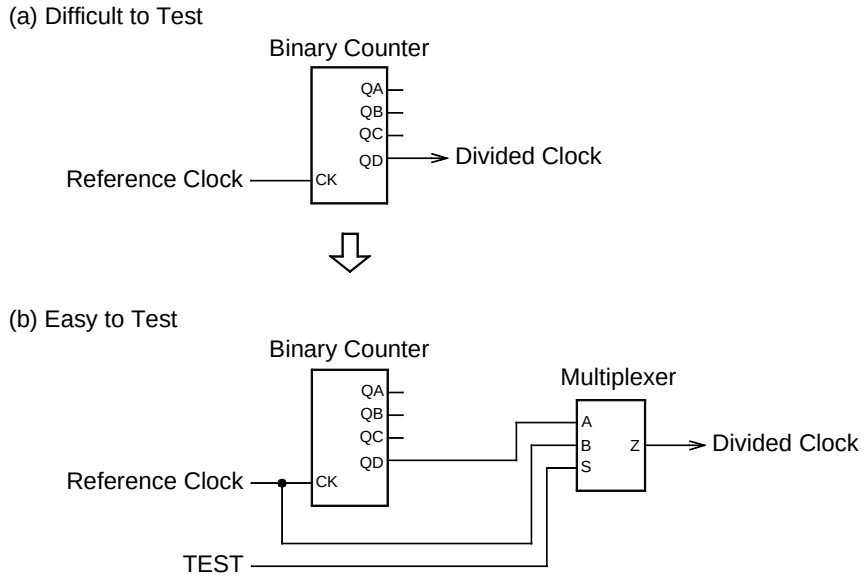


Figure 4-73 **Frequency Divider — Multiplex the Reference and Divided Clock Signals**



4.9 Design-for-Testability

4.9.3 Improving the Controllability and Observability

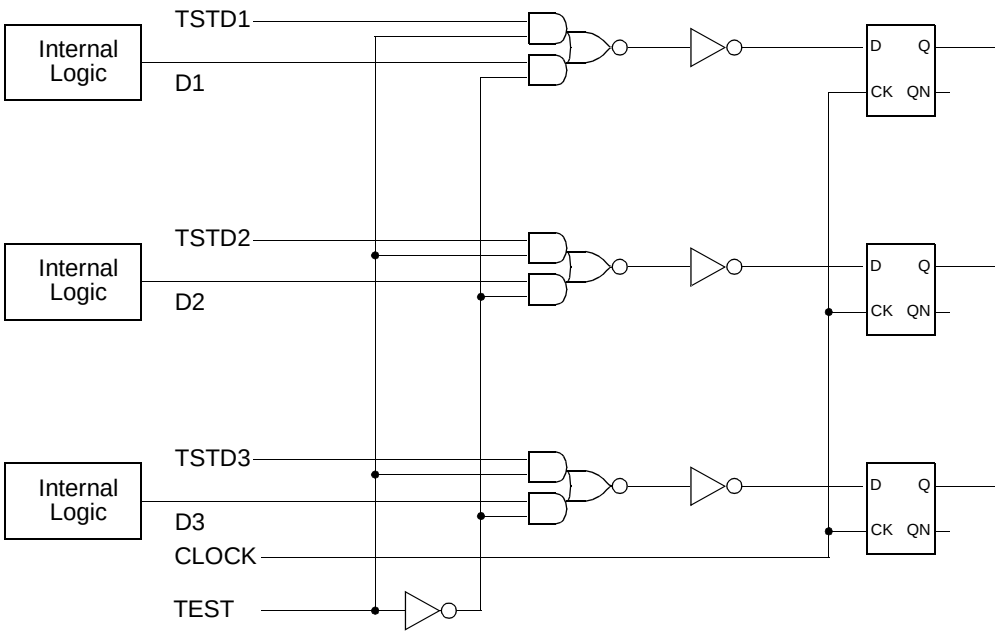
Rules & Tips

- **Make deeply buried states controllable and observable.**

Making Buried States Controllable

Figure 4-74 illustrates a technique for making buried states of internal flip-flops more accessible. When TEST=1, the D inputs of the flip-flops are forced into a logic values equal to TSTD1, TSTD2, and TSTD3. You can then easily control the flip-flops by routing these lines to package input pins.

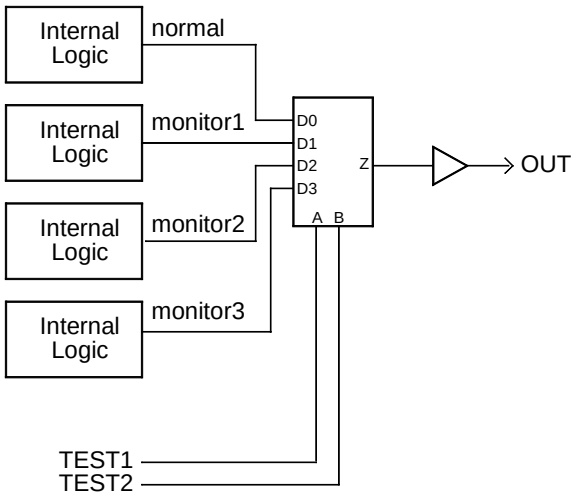
Figure 4-74 **Controlling Deeply Buried Flip-Flops**



Making Buried States Observable

You can make buried internal states more observable by multiplexing them and routing the multiplexer output to a package output pin, as shown in Figure 4-75.

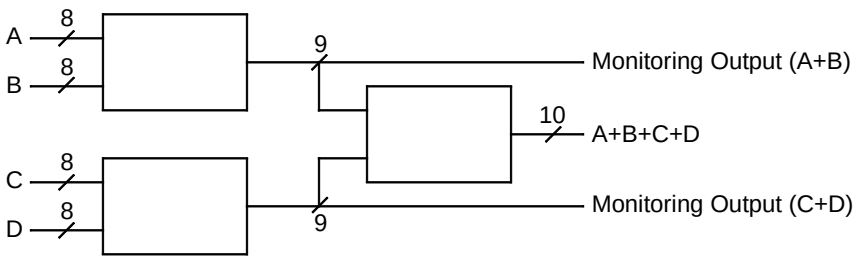
Figure 4-75 Observing Deeply Buried States



TEST1	TEST2	OUT
0	0	normal
1	0	monitor1
0	1	monitor2
1	1	monitor3

A circuit with a high input-to-output-pin ratio is difficult on which to achieve an adequate fault test coverage. Since for a fault to be detected, the effect of the fault must be propagated to a physical output pin where you can observe it, but such a circuit has a very limited number of observation points (see Chapter 6, *Logic and Fault Simulation* for fault test coverage). Improving test coverage on such circuits is only possible by routing appropriate internal nodes directly to package output pins, as shown in Figure 4-76.

Figure 4-76 Monitoring Internal Nodes



4.9 Design-for-Testability

4.9.4 Testing Megacells

Rules & Tips

- **For proper testing of megacells, you should have direct access to their input and output pins.**

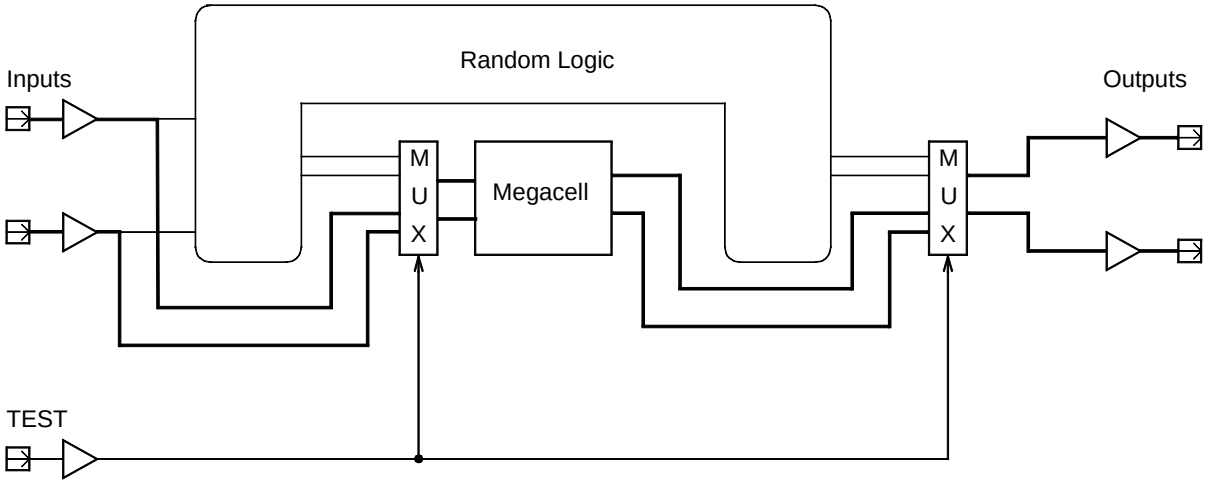
ASIC circuits often contain large megacells such as RAMs and ROMs. These megacells require a large number of test patterns for an adequate test, and without direct access to their inputs and outputs from the package pins, they can be impossible to test.

The simplest and most effective way to test megacells is to add multiplexing logic, as shown in Figure 4-77. You can make the megacell input/output pins directly accessible and observable by connecting multiplexers to package pin test points. The flow of data in test mode is shown by bold paths.

You can reduce the number of additional test pins by having data I/O pins shared between normal and test operation. The multiplexer control pin is separately required, however.

When you have added a test logic that allows direct access to all megacell input/output pins, Toshiba provides you with megacell test patterns.

Figure 4-77 **Isolating a Megacell from the Rest of the Design**



4.9 Design for Testability

4.9.5 Testing Analog Cells

Rules & Tips

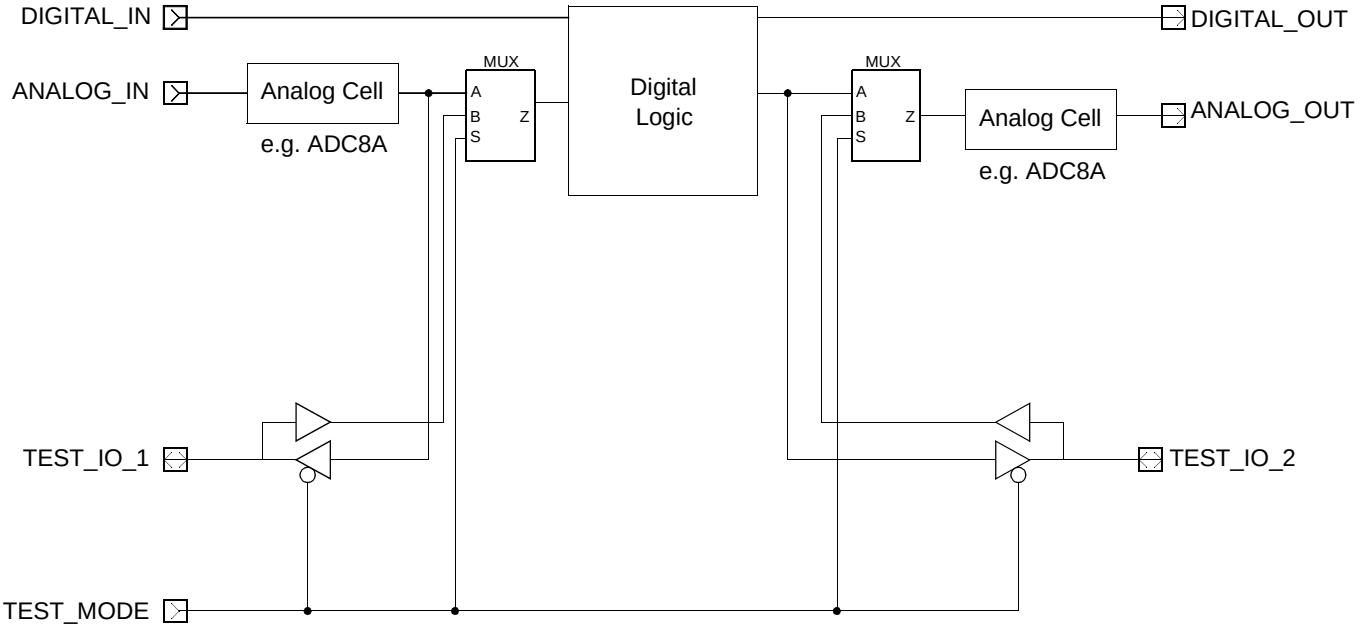
- **Analog cells are parametrically tested in isolation. Add multiplexing logic to separate analog cells from digital portions.**
- **Provide separate analog power/ground (AVDD/AVSS) pins for each analog cell.**
- **Use of analog cells could yield constraints on I/O placement.**

Some of the Toshiba's ASIC product series allow analog cells to be integrated on the same chip. During testing, parametric evaluation will be executed at Toshiba for each of the analog cells separately. For proper testing, analog cells must be partitioned from digital logic portions by means of multiplexing logic in a similar manner as for megacell testing (see Figure 4-78, which follows).

On the tester, customer's test patterns are used to test all of the array except analog cells, which are powered down during this time. That is, analog cells are not used to feed data to the array core. During the testing of analog cells, the rest of the array does not toggle. This procedure is used to eliminate coupling of digital switching noise into the analog cells through the analog power/ground pins.

In the logic design phase, you must prepare test patterns that represent the digital sequence that would be coming from an analog cell. These test patterns are applied directly to the package test input pin. Digital data that would be fed to an analog cell is directly monitored at a package test output pin.

Figure 4-78 Testing of Analog Cells



Separate analog power/ground pins (AVDD and AVSS) are required for each of the analog cells used. Use of analog cells could yield restrictions on I/O placement. Some analog cell pins consume more than one package pin. Consult with Toshiba ASIC service group engineer for analog circuit specifications.

4.9 Design-for-Testability

4.9.6 Fault Test Coverage Considerations

Rules & Tips

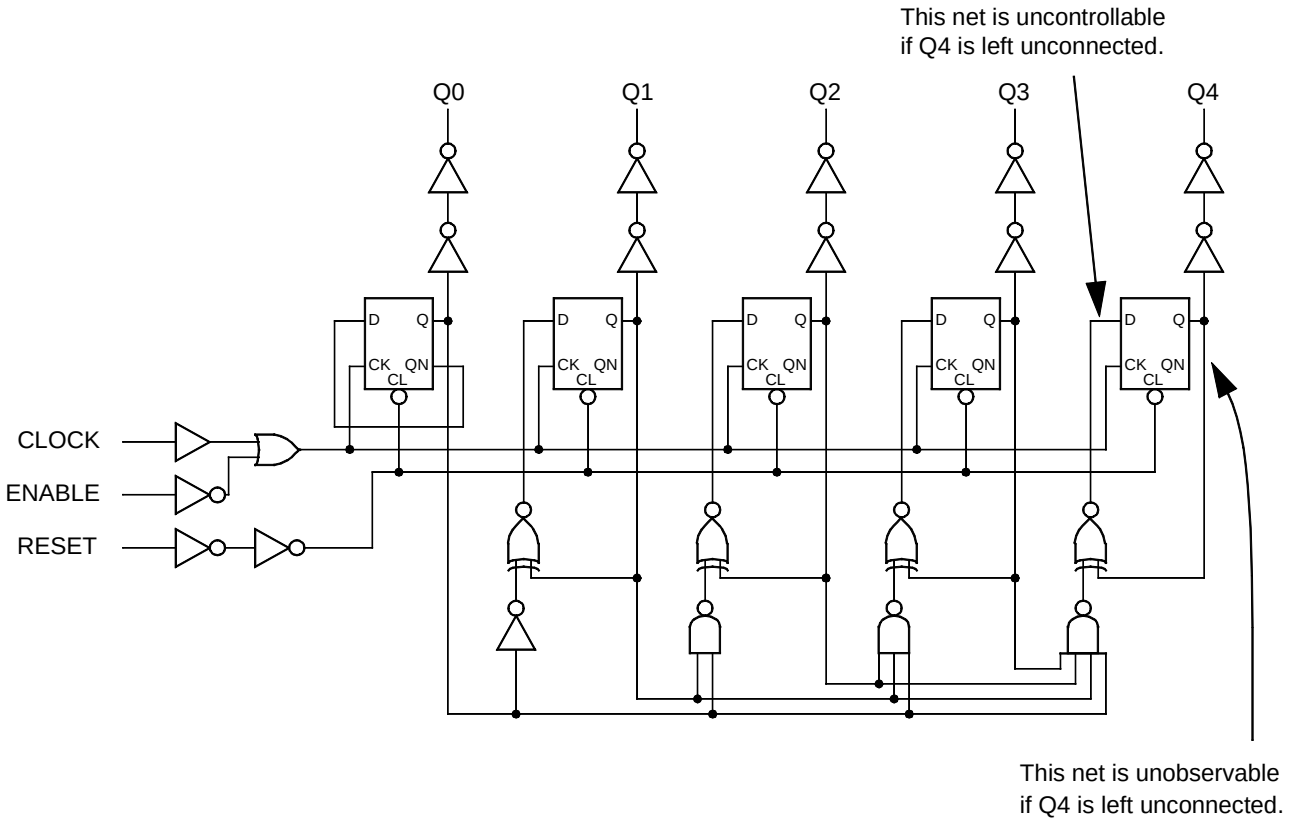
- **Redundant logic and internal nodes tied to a constant logic value will lower the fault test coverage achievable. Be aware of the limitations of the gate-eater.**

Unused Outputs and Gate-Eating

All macrocells all of whose outputs are unconnected will be automatically removed by the gate-eating feature of the Toshiba ASIC sign-off system (unless otherwise specified). A care should be exercised, however, when you consider applying the gate-eating to certain user macros such as counters. Suppose, for example, that you have a pre-designed 5-bit up counter and want to reuse it as a 2-bit up counter. This can be done just by leaving the upper three-bit outputs unconnected. However, many types of counters have an internal feedback line from the flip-flop outputs; so unused counter macro outputs will not result in the uncommitted internal flip-flops being deleted.

Note that the penalty of unused macrocells is that they will cause a loss of fault coverage. A stuck-at fault, a defect introduced during manufacturing, must be both controllable and observable to be detected, but there is no observing the outputs from macrocells with every output unconnected (see Figure 4-79).

Figure 4-79 **Counters Have Feedback Loops from Flip-Flop Outputs**



Inputs Tied to Fixed Logic Values

Cell inputs that are tied to fixed logic values will cause a loss of fault coverage. For example, counters with Count Enable(s) tied to constant logic 1 (V_{DD}) are common design practices. Remember that to detect a stuck-at fault, a test pattern must control the value at a node to the opposite of the faulty value. Hard-wiring a node to a fixed logic level makes it untestable.

4.9 Design-for-Testability

4.9.7 Internal Scan Design

Rules & Tips

- **Where fault test coverage is important, use an internal scan design technique. It provides excellent controllability and observability on sequential logic, and enables you to automatically generate test patterns with very high fault coverage.**

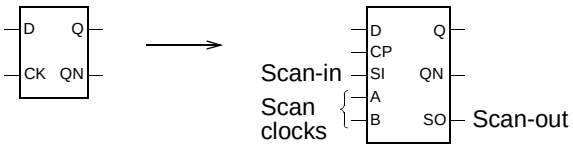
Basic Structure of Internal Scan Design

For a small combinational logic, test patterns with 100% fault coverage are relatively easy to develop. However, testing a large sequential design is more complicated, and may require a complex set of patterns applied in a specific sequence. Internal scan design is one of the most popular design-for-testability (DFT) techniques if you need fault coverage of more than 95% for large designs.

Internal scan provides total or near total controllability and observability on sequential logic. More importantly, it enables the computer software to automatically generate test patterns with very high fault coverage.

In the scan design technique, sequential cells in your design are replaced by logically equivalent elements that also perform a serial shift function. Figure 4-80 shows a non-scan D-type flip-flop and its scannable versions.

Figure 4-80 Standard Flip-Flop and Scannable Flip-Flop (Dual-Clock Type)



The scan flip-flops are chained together to form one or more large shift registers called scan registers, as illustrated in Figure 4-81, which follows. By means of this shift register path, or scan path, the internal states of the circuit can be controlled and observed.

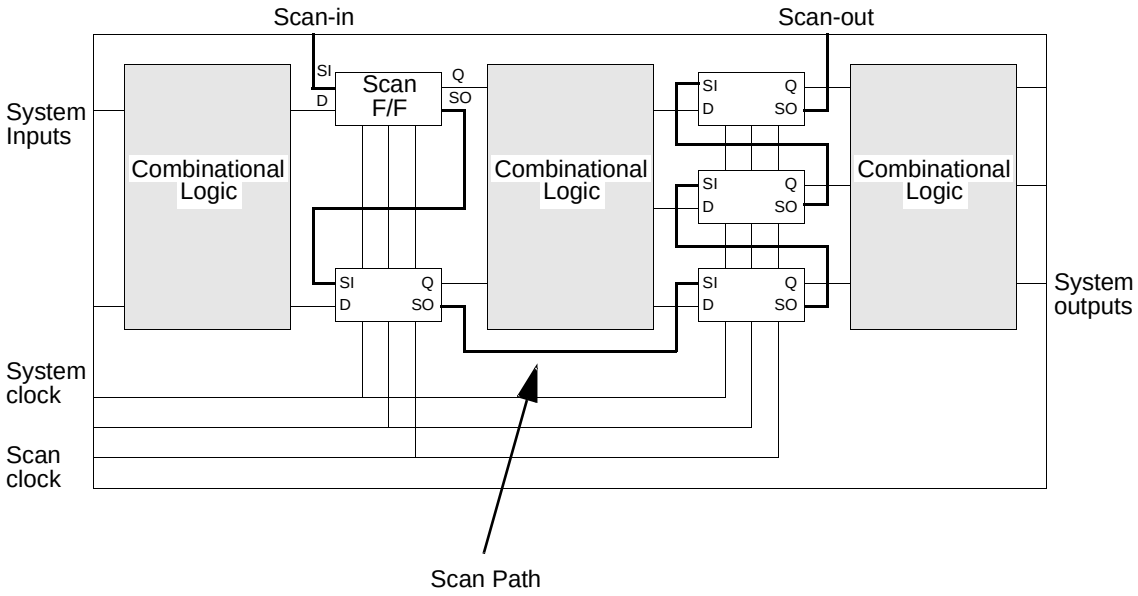
How Internal Scan Design Works

When a circuit is designed with a scan path, scan flip-flops has two operating modes: parallel load mode (system mode) and serial shift mode (scan mode). In parallel load mode, scan flip-flops receive data from the combinational logic block. In serial shift mode, the input to each scan flip-flop comes from the output of the previous scan flip-flop.

In serial shift mode, the scan flip-flops connected in a scan path can be controlled to any logic values by serially shifting in specific logic values. Therefore, the scan path makes the combinational logic islands in your design more controllable, and easier to test. Furthermore, the scan path makes internal combinational nodes easier to observe, since the outputs of the combinational logic islands can be latched into scan flip-flops, then shifted out at external output pins for evaluation.

In effect, flip-flops outputs may be treated as though they were primary inputs, and their inputs can be treated as though they were primary outputs. Thus, in addition to the scan path giving access to the internal states of a circuit, the scan path can also be considered as a means of partitioning a circuit into less complex combinational logic blocks and a long scan path, as depicted in Figure 4-81.

Figure 4-81 **Circuit Partitioned by a Scan Path**



The internal scan test is executed in the following sequence:

1. The mode control line is set to scan (i.e., serial shift) mode.
2. Test patterns are serially shifted into scan flip-flops via the scan path.
3. The mode control line is switched to system (i.e., parallel load) mode.
4. Functional test patterns are applied to the external input pins.
5. The output response from the system logic is evaluated at the external output pins.
6. The system clock is pulsed once to latch all internal states into scan flip-flops.
7. The mode control line is switched back to scan mode.
8. The contents of the scan flip-flops are serially shifted out from the scan path.

Penalties of Internal Scan Design

Despite all the benefits of the scan design technique, the freedom available to designers are bounded by four considerations:

- *Area overhead* — Replacing non-scan cells with more complex scan cells increases sequential logic area. Additional interconnections required for scanning also increase the area overhead. It is critical to hold the area overhead within a certain limit not to have to go to the next die size.
- *Additional package pins* — You must have extra I/O pins that may be allocated for test purposes. You can minimize the number of additional I/O pins by sharing I/O pins between system logic and test signals.
- *Loss in chip performance* — Scan design may reduce circuit performance since higher gate loads or increased logic delays may be involved.
- *Design constraints* — Scan design imposes a very specific set of design constraints on the designer.

For an in-depth discussion on internal scan, consult the Toshiba *Design-For-Test Handbook.* The section that follows describes the styles of internal scan design techniques supported by Toshiba.

4.9 Design-for-Testability

4.9.8 Toshiba Internal Scan Techniques

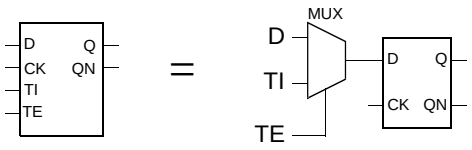
Rules & Tips

- **The single-clock style of scan implementation is more preferable in terms of area overhead.**
- **The dual-clock style is more favorable in terms of speed.**
- **Toshiba DFT environment supports only full-scan (not partial-scan).**

Single-Clock Scan (Multiplexed Flip-Flop)

This scan implementation uses a D flip-flop with a multiplexed data input. Figure 4-82 shows a multiplexed flip-flop with a simple edge-triggered clocking scheme.

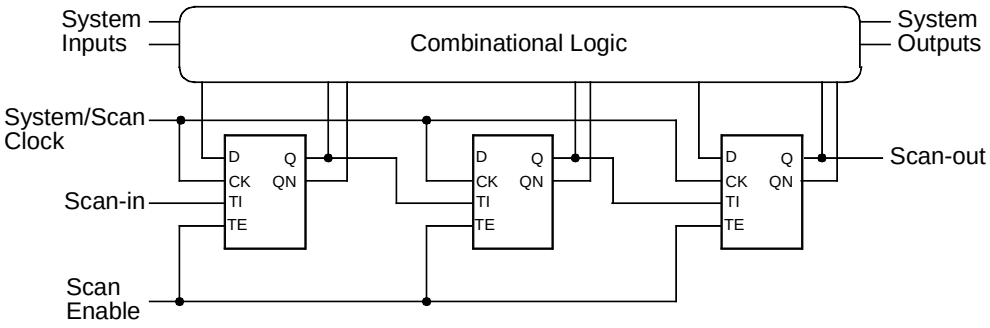
Figure 4-82 Multiplexed Flip-Flop



In normal operation mode, the test enable (TE) signal selects data from the system data input (D). In serial shift mode, the test enable signal selects data from the test input (TI). This input comes from the Q output of the previous flip-flop in the scan path. Note that the CK input is used in both normal and serial shift operation.

Figure 4-83 shows a single-clock scan design using the multiplexed flip-flop implementation.

Figure 4-83 **Single-Clock Scan Design**



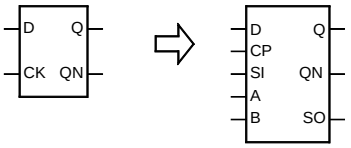
The characteristics of this scan implementation are:

- *Moderate area overhead* — Typically, a multiplxed D flip-flop is only 20-30% larger than a standard D flip-flop. Also, only one global control line is needed for the test enable signal.
- *Some performance impact* — Adding a multiplexer to the data input of a flip-flop can increase the setup time by 20-100%. In addition to this, more gate loads (thus delay overhead) are involved for the flip-flop output.
- Requires careful considerations on the normal and test clock timing.

Dual-Clock Scan

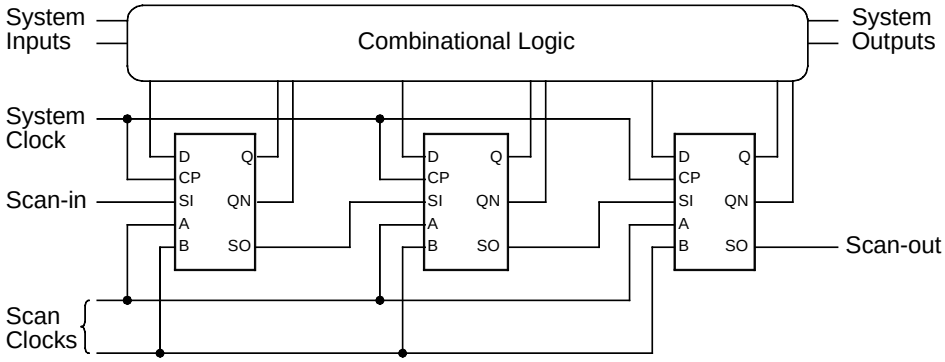
Figure 4-84 shows a D flip-flop before and after it is modified for scan with dual clocks.

Figure 4-84 Standard and Scannable Dual-Clock D-Type Flip-Flops



In normal operation mode, the scan flip-flop functions exactly the same way as the standard flip-flop. In serial shift mode, two non-overlapping test clocks (A and B) are used to shift data from the serial scan input (SI) to the serial scan output (SO). Figure 4-85 shows a dual-clock scan design.

Figure 4-85 Dual-Clock Scan Design



The characteristics of this scan implementation are:

- *Significant area overhead* — The area overhead increases due to the two dedicated test clocks and the dedicated serial scan input and output.
- *No performance impact* — This makes the dual-clock scan technique suitable for integrated circuits for high-speed applications.
- *Relaxed design rules for normal mode clock(s)*— Because the normal mode clock is never used in test mode, there are no rigid rules for clocking schemes.

Full-Scan vs. Partial-Scan

In the full-scan technique, as the name implies, scannable flip-flops substitute for all flip-flops in a design. With a full-scan design, test patterns are easier to generate, and fault coverage upwards of 95% and approaching 100% can be achieved.

The inputs and outputs of scannable elements have direct controllability and observability, similar to primary inputs and primary outputs. Test patterns are easier to generate for a full-scan design because:

- Inputs to all combinational logic blocks are directly controllable;
- Outputs from all combinational logic blocks are directly observable;
- Efficient combinational automatic test pattern generation (ATPG) algorithms can be used, since the design is effectively broken up into smaller combinational blocks by scan paths.

In some cases, however, it may be difficult to convert all flip-flops in a design to scan equivalent type. Timing and chip area constraints commonly limit the number of flip-flops that can be scanned in a design. Designs that contain some scan elements but are not fully converted to scan are known as partial-scan designs.

Partial scan is beneficial if an attempt at a full-scan implementation is defeated by timing or area constraints. The percent of fault coverage achieved for a partial-scan design is related to the ratio of scanned flip-flops. Constraint-driven partial scan offers a trade-off between the achievable fault coverage and the impact on chip size and performance.

To adequately test a partial-scan design, a sequential ATPG algorithms are required to allow propagation of faults through non-scan sequential elements. In general, a partial-scan can not achieve as high a fault coverage as a full-scan design. A partial-scan design needs more test patterns than a full-scan design to detect a given fault. Thus, sequential test generation is slower than combinational test generation and uses more computer resources. In addition, the ATPG can not allow for setup/hold timing margins for non-scan elements that are not connected in a scan path.

For all these reasons, Toshiba supports only full-scan with its DFT tools. Although customers can employ partial-scan, Toshiba recommends the use of full-scan to ensure testability.

Benefits and Penalties of Internal Scan

Table 4-12 gives the benefits of scan. Table 4-13 gives some indications of the implementation costs incurred by each scan implementation style.

Table 4-12 Benefits of Scan

	No Scan	Partial Scan	Full Scan
Control Points	External inputs only	External inputs, Q and QN of scan cells	
Observation Points	External outputs only	External outputs, D inputs of scan cells	
Typically Achievable Fault Coverage	80%	90-95%	Over 95%
Test Pattern Development Time (e.g. 20k-gate design)	1-3 months	0.5-1 month	Less than 1 week

Table 4-13 Penalties of Internal Scan Design

Implementation Costs	Single-Clock	Dual-Clock
Area Overhead	Limited (5-15%)	Significant (10-20%)
Test I/O Pin Requirement	At least 1*	At least 1*
Delay Overhead	Some	None
Clock Skew Consideration	Required	Not required

* At least two I/O pins are required if bidirectional buffers are not controllable externally.

4.9 Design-for-Testability

4.9.9 JTAG Boundary-Scan

Rules & Tips

- **JTAG boundary-scan provides control over I/Os of digital ICs for board-level testing. A full implementation of boundary-scan gives you access to on-chip test features including internal scan.**

The JTAG boundary-scan is a board-level test vehicle that provides control over the input and output pads of digital ICs on a printed circuit board. The I/O circuitry of each IC is modified so as to form a long shift-register chain. Since the first proposal for a boundary-scan standard came from the Joint Test Action Group (JTAG), a group of European companies, often it is simply referred to as JTAG. The JTAG proposal was later approved as the IEEE 1149.1-1990 standard.

The main objectives of boundary-scan are:

- Checking interconnections between ICs for shorts, opens, and solder bridges;
- Checking for misloaded components, including wrong, missing, or dead components.

In addition to its application in testing assembled printed circuit boards, the test logic defined by the IEEE 1149.1 standard provides access to a wide range of DFT features built into the IC, including internal scan.

Figure 4-86 illustrates a simple boundary-scannable board design, with serial test interconnect (boundary-scan path) around the edge of each IC.

Figure 4-86 **Boundary-Scannable Board Design**

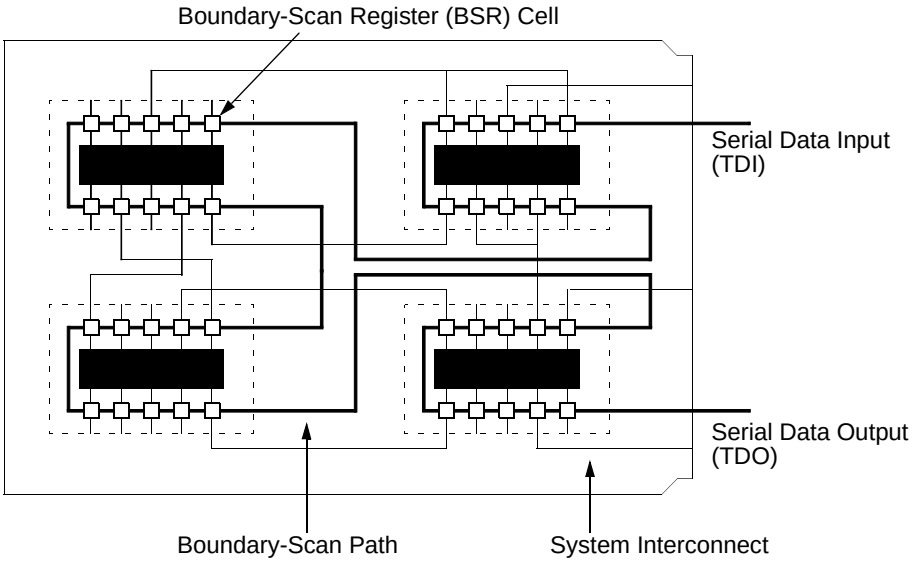
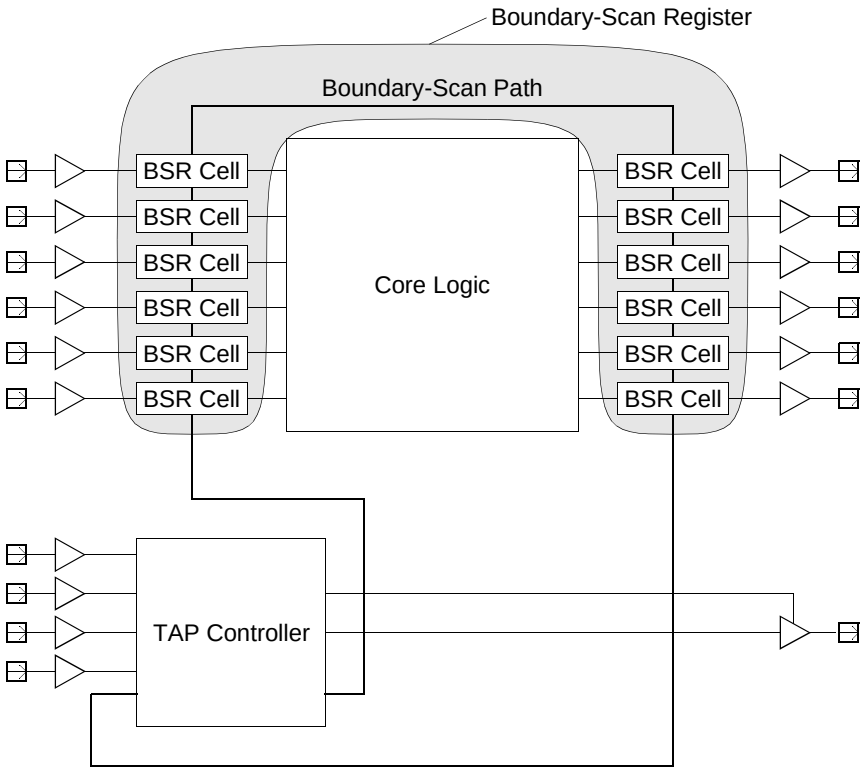


Figure 4-87 shows a general structure of JTAG boundary-scan within an IC.

Figure 4-87 **General Structure of JTAG Boundary-Scan**



4.9 Design-for-Testability

4.9.10 Toshiba JTAG Cell Library Guide

Rules & Tips

- **Toshiba offers four types of JTAG controller cells, supporting 4, 6, 14, and 18 instructions.**
- **JTAG requires at least four dedicated test I/O pins, and incurs gate and I/O delay overhead.**

JTAG Controllers

Toshiba's JTAG library includes four types of JTAG controller cells, which are comprised of the TAP controller, instruction register, instruction decode logic, and other requisite components. Table 4-14 shows the Toshiba JTAG controller offerings:

Table 4-14 Availability of JTAG Controller Cells

Gate Arrays Embedded Arrays	Cell-Based IC	Function
XJTG4A	SJTG4A	Supports four JTAG instructions, including the three mandatory instructions.
XJTG6A	SJTG6A	Supports six JTAG instructions, including the three mandatory instructions.
XJTG14A	SJTG14A	Supports a total of 14 instructions, including five JTAG instructions and Toshiba's private instructions. Usable in conjunction with internal scan.
XJTG18A	SJTG18A	Supports a total of 18 instructions, including six JTAG instructions and Toshiba's private instructions. Usable in conjunction with internal scan.

Table 4-15 lists the instructions supported by the above JTAG controller cells.

Table 4-15 Supported Instructions

Gate Arrays Embedded Arrays	Cell-Based IC	Supported Instructions		
XJTG4A	SJTG4A	JTAG mandatory		EXTEST, SAMPLE/PRELOAD, BYPASS
		JTAG optional		HIGHZ
XJTG6A	SJTG6A	JTAG mandatory		EXTEST, SAMPLE/PRELOAD, BYPASS
		JTAG optional		INTEST, IDCODE, HIGHZ
XJTG14A	SJTG14A	JTAG mandatory		EXTEST, SAMPLE/PRELOAD, BYPASS
		JTAG optional		INTEST, HIGHZ
		Toshiba private	Internal scan	SLSCAN, STESTEL, STESTIL, STESTEM, STESTIM, STESTP, PARSHIFT
			Frequency test	NDSTST
			I_{DDS} test	IDDS
XJTG18A	SJTG18A	JTAG mandatory		EXTEST, SAMPLE/PRELOAD, BYPASS
		JTAG optional		INTEST, IDCODE, HIGHZ
		Toshiba private	Internal scan	SLSCAN, STESTEL, STESTIL, STESTEM STESTIM, STESTP, PARSHIFT
			Burn-in test	SELFBI
			Frequency test	NDSTST
			I_{DDS} test	IDDS
			Observing test control signals	MODSET, MODSCAN

* The term “mandatory instruction” means that the instruction is defined and required by the IEEE 1149.1 standard. The term “private instruction” means a design feature intended for exclusive use by the component manufacturer, or Toshiba, as opposed to “public instructions.”

Boundary-Scan Register (BSR) Cells

Table 4-16 shows the lines of the Toshiba BSR cells to be added between I/O buffers and the system logic.

Table 4-16 BSR Cell Lines

Gate Arrays Embedded Arrays	Cell-Based IC	Function
XBSRI1A	SBSRI1	Boundary scan input register
XBSRIN1	SBSRIN1	Boundary scan input register, inverting output
XBSRI2A	SBSRI2	Boundary scan input register without an update latch
XBSRIN2	SBSRIN2	Boundary scan input register without an update latch, inverting output
XBSRI3A	SBSRI3	Boundary scan input register without an update latch and the INTEST logic
XBSRIN3	SBSRIN3	Boundary scan input register without an update latch and the INTEST logic, inverting output
XBSRC2A	SBSRC2	Boundary scan clock driver register
XBSRCN2	SBSRCN2	Boundary scan clock driver register, inverting output
XBSRO1	SBSRO1	Boundary scan output register
XBSRP1	SBSRP1	Boundary scan output register with the private PARSHIFT logic
XBSRB1A	SBSRB1	Boundary scan bidirectional register
XBSRBN1	SBSRBN1	Boundary scan bidirectional register, with inverting input buffer
XBSRB3A	SBSRB3	Boundary scan bidirectional register without the INTEST logic
XBSRBN3	SBSRBN3	Boundary scan bidirectional register without the INTEST logic, with inverting input buffer
XBSRE1	SBSRE1	Boundary scan enable control register

Boundary-Scan Implementation Costs

Use of a JTAG controller cells necessitates a minimum of four I/O test pins for the Test Access Port (TAP) — TDI, TMS, TCK, and TDO. Making TRST* optional allows the trade-off of having an asynchronous reset for the TAP versus the cost of adding an extra input pin. In addition, the XJTG14A (SJTG14A) and XJTG18A (SJTG18A) can optionally have additional two input pins to achieve control of on-chip megacells through internal scan flip-flops.

Table 4-17 shows the JTAG boundary-scan implementation costs for a gate array.

Table 4-17 JTAG Boundary Scan Implementation Costs for Gate Arrays (TC160G/TC180G)

	XJTG4A	XJTG6A	XJTG14A	XJTG18A
Gate Overhead				
JTAG controller cell	234 gates	454 gates	437 gates	991 gates
Input BSR cells	(10 x pin_count) gates	(21 x pin_count) gates	(21 x pin_count) gates	(21 x pin_count) gates
Output BSR cells	(16 x pin_count) gates	(16 x pin_count) gates	(16 x pin_count) gates	(16 x pin_count) gates
Bidirect BSR cells	(20 x pin_count) gates	(29 x pin_count) gates	(29 x pin_count) gates	(29 x pin_count) gates
I/O Delay Overhead	Limited	High	High	High
Test I/O Pin Requirement	4 or 5	4 or 5	4 or 7	4 to 7

4.9 Design for Testability

4.9.11 Toshiba DFT Environment

Rules & Tips

- **Toshiba supports both internal scan and JTAG boundary-scan with a its proprietary DFT tool and popular third-party DFT tools. Both front- and back-end supports are available.**

Front-End and Back-End DFT Services

Toshiba supports both the front- and back-end development for design-for-testability. For each DFT tool supported, Toshiba provides the libraries, interface software programs, and documentation. The customer checks design rule compliance, adds test logic, and generates test patterns. This is termed front-end services since all design-for-test operations occur prior to design hand-off. If you do not own a DFT tool, Toshiba performs all these tasks after design hand-off. This type of support is called back-end services as opposed to front-end services.

Supported DFT Tools

Table 4-18 shows the support availability of test automation tools:

Table 4-18 Supported DFT Tools

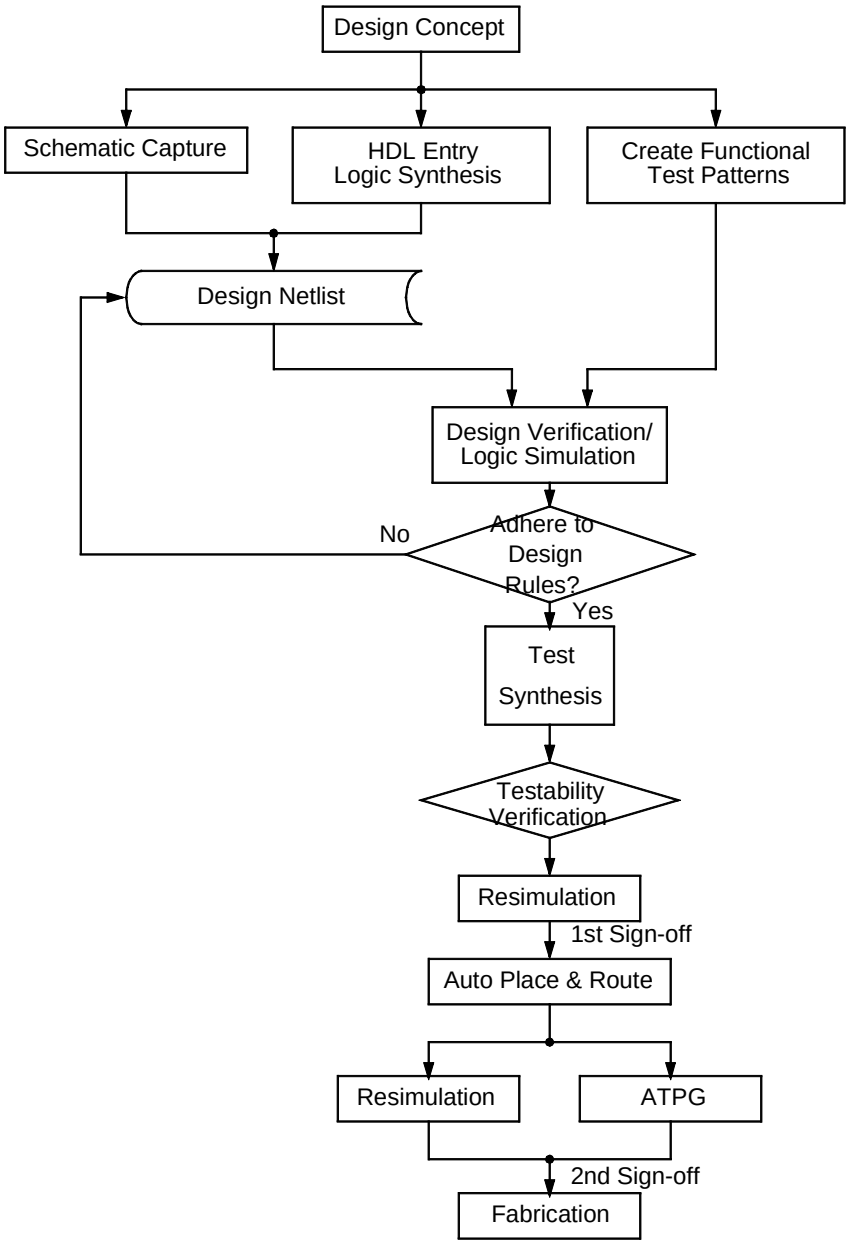
Tool	Single-Clock Scan	Dual-Clock Scan	JTAG
Toshiba VLCAD/DFT	Yes	Yes	Yes
Synopsys Test Compiler	Yes	Yes	Yes** (V3.0 or above)
Synopsys Test Compiler Plus	Yes	Yes	Yes**
Sunrise TestGen	Yes	Yes	Yes
Mentor DFTAdviser FastScan	Yes	Yes	
Mentor BSDArchitect			Yes**

** Can not use Toshiba library cells.

DFT Design Flow

Figure 4-88 illustrates where DFT steps fit in the general ASIC design flow:

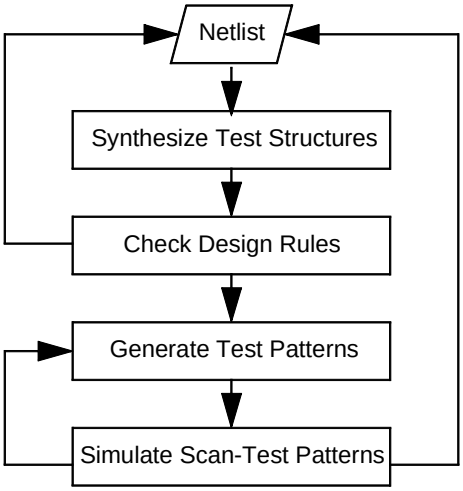
Figure 4-88 DFT Design Flow



General Features of DFT Tools

As a whole, DFT tools place special emphasis on adding test structures (such as scan paths) and generating production test patterns with high fault coverage. Features of DFT tools would fall into four major groups, as shown in Figure 4-89 below.

Figure 4-89 Features of DFT Tools



A list of features of DFT tools follow:

- Synthesizes test structures that inherently make your design testable
  - — Adds internal scan test logic
  - — Adds IEEE 1149.1-compliant boundary-scan logic
  - — Allocates and connects single or multiple scan paths
  - — Provides automatic or manual scan path ordering
  - — Allows you to specify flip-flops that you do not want replaced by their scannable equivalents

- Checks the design rules
  - — Allows you to define logic conditions for a test mode
  - — Allows you to specify design rules to be checked
- Generates test patterns
  - — Allows you to break a large design into manageable chunks
  - — Allows you to control which faults are considered
  - — Allows you to control the level of computing efforts expended in test pattern generation by specifying the target fault coverage, the maximum number of test patterns, etc.
  - — Allows you to generate test patterns in stages, and build on previously generated patterns to generate a new pattern set
  - — Compacts generated test patterns
  - — Reports the fault coverage percentage (and maybe node toggle coverage) achieved
  - — Writes out test patterns in a particular serialized format
- Simulates the generated scan-test patterns
  - — Reduces the long simulation run time inherent with scan designs through the use of broadside (i.e., parallel) loading of scan elements.

4.10 Oscillator Cells

Rules & Tips

- **Oscillator cells require a test logic to be tested in isolation.**
- **Ask Toshiba for an oscillator cell evaluation vehicle.**
- **The I/O assignment for an oscillator cell is constrained.**

Normal and Cornered Oscillator Cells

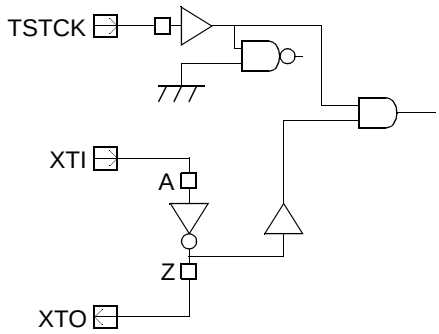
Toshiba's cell libraries include two types of oscillators: normal types and cornered types. Normal types can be placed on any pads whereas "cornered" oscillators are constrained to one of the two specific corners of the chip. Normal type cell names begin with OSC; cornered type names begin with OSCX. Normal types use transistors in I/O slot locations while cornered oscillators use specially-designed transistors on chip's corners to deliver stable oscillation even at a low frequency.

Test Logic and Test Pattern Requirements

All oscillator cells have two pad pins, A and B, and one internal pin, ZI. Those with stop control has one extra internal pin, E or EN, for enabling and disabling oscillation. The output pad, Z, provides the inverted signal feedback to the crystal that is necessary for oscillation. ZI provides the internal clock signal to the array core.

Add a test logic shown in Figure 4-90, which follows, so that the array core can be tested in isolation. If you can not set aside an I/O pin for TSTCK in Figure 4-90, consult with the Toshiba ASIC service group.

Figure 4-90 **Oscillator Cell and Test Logic**



- Input buffer for TSTCK: CMOS type.
- AND gate: YCAN2P for gate arrays and embedded arrays, and AN2P for cell-based ASICs.

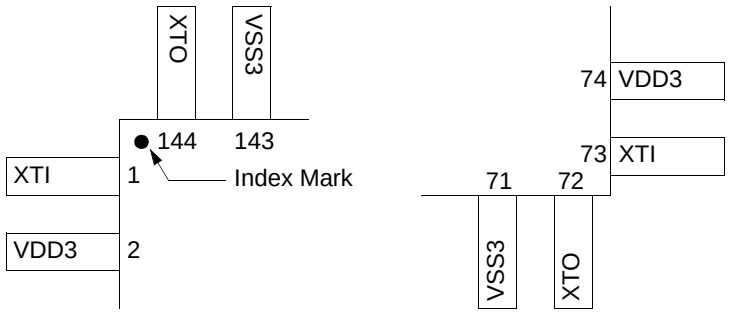
Testing is carried out as follows:

- During functional testing, a clock is applied from test clock pin TSTCK, with XTI being held at a constant logic 0.
- A clock is applied from XTI when testing the integrity of the path from XTI to the internal clock pin.
- When performing dc test on I/O pins except XTO, a clock is applied from TSTCK, with XTI being held at a constant logic 0.
- When performing dc test on XTO, TSTCK is maintained at logic 0 while XTI toggles between logic 0 and logic 1.
- Stop control is parametrically checked during dc test; digital logic simulators can not deal with it.

I/O Pin Assignment Constraints

For normal-type oscillator cells, the A (XTI) input pin must be positioned next to a VDD pin, and the Z (XTO) output next to a VSS pin. For cornered oscillator cells, the A input pin must be placed adjacent to a VDD3 pin, and the Z output pin adjacent to a VSS3 pin.

Figure 4-91 **Pin Assignment Example of a Cornered Oscillator (QFP144)**



Design Considerations

Rules of thumb for an oscillator design follow:

- Use the oscillator cell consistent with your frequency need.
- Ask the Toshiba ASIC service group for an evaluation vehicle, and experiment on oscillation characteristics beforehand.
- Be aware of the instability at oscillation start-up when creating a system design.
- Keep PCB traces and components leads as short as possible to avoid parasitic capacitances and inductances. Also, do not allow the oscillator signals to cross other signals.

Oscillator Application Examples

The oscillator cell contains an inverting amplifier and a driver to the ASIC core. You must supply external components needed to build a working oscillator. A typical implementation of the oscillator cell with no feedback resistor is shown in Figure 4-92. An implementation example using the oscillator cell with a feedback resistor is shown in Figure 4-93. Recommended CR values and typical electrical characteristics are available in the Toshiba macrocell data book.

Figure 4-92 **Application Example of Oscillator Cells with No Feedback Resistor**

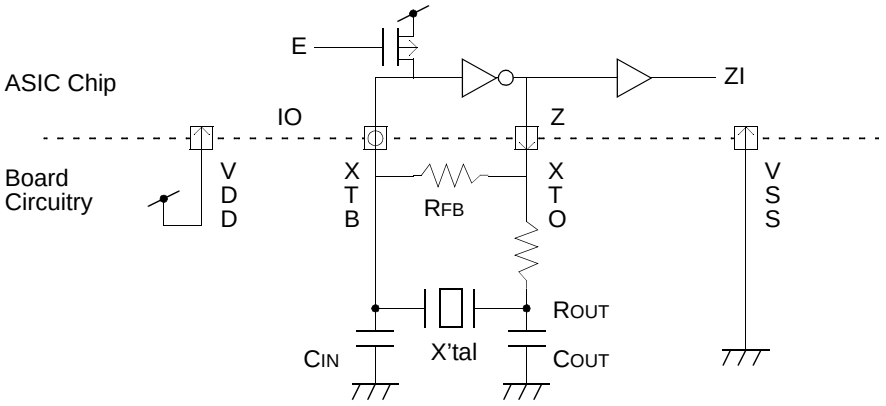
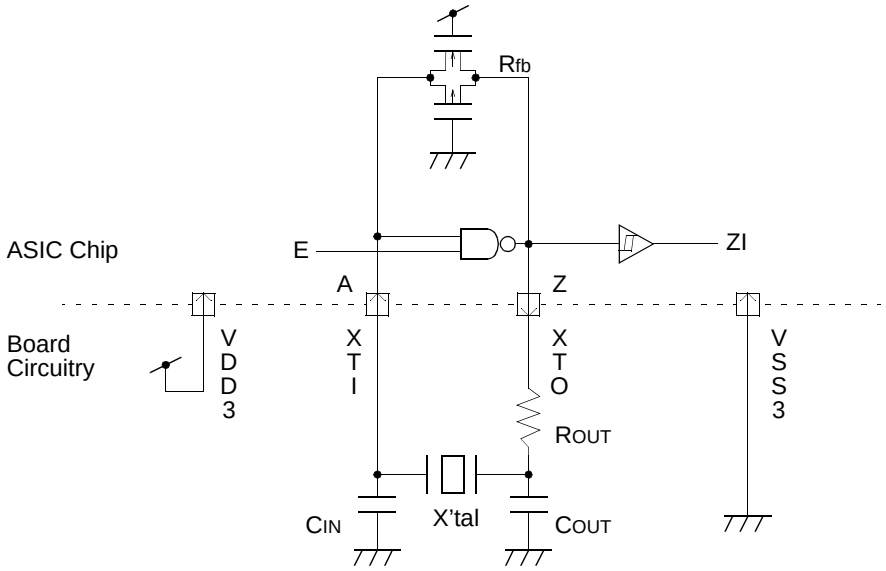


Figure 4-93 **Application Example of Oscillator Cells with Feedback Resistor**



4.11 Digital Phased-Locked Loop (DPLL)

Rules & Tips

- **Toshiba's digital PLL (DPLL) offers you the ability to minimize chip-to-chip clock skew.**

The ability to synchronize chips in high frequency systems is one of the limiting factors on system performance. Accurately synchronizing different chips in a multi-chip high performance design is critical to ensure that it functions correctly at the highest clock frequency possible. Inter-chip clock skew makes inter-chip synchronization difficult. The DPLL minimizes clock skew between chips, reducing the percentage of the clock cycle that must be used as a guard band.

Figure 4-94 Effects of Inter- and Intra-Chip Clock Skew

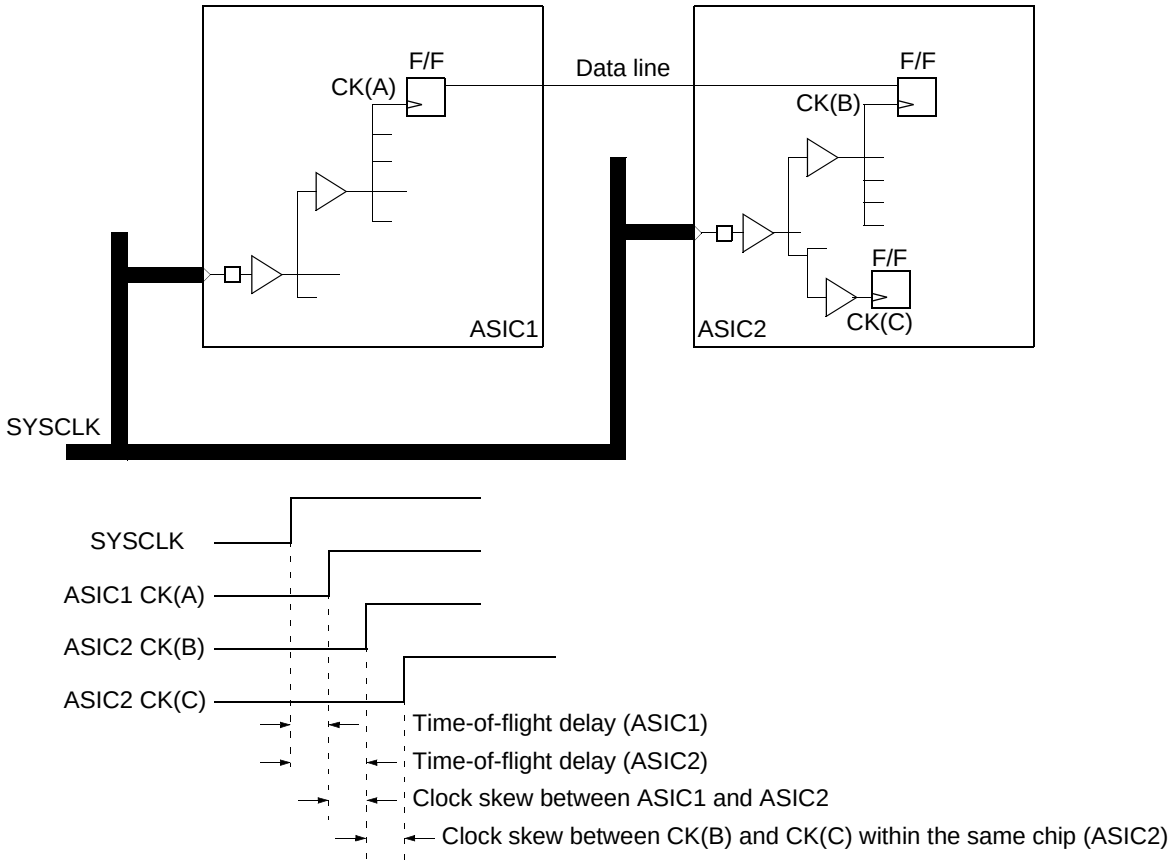
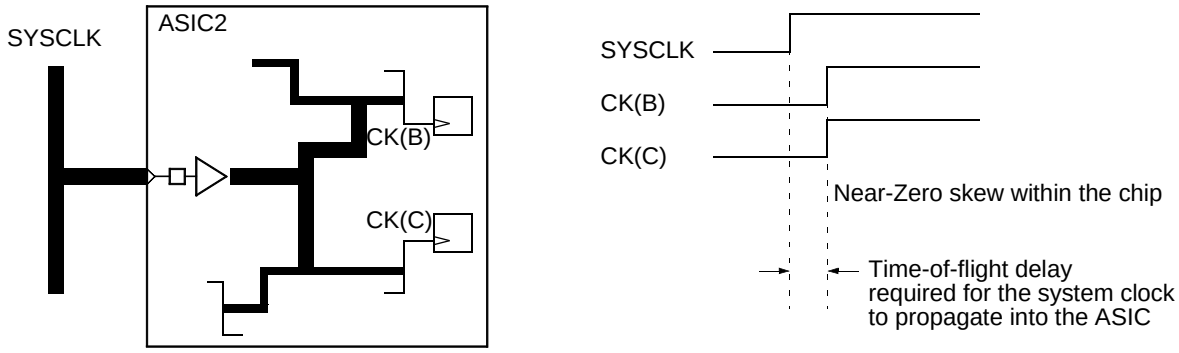
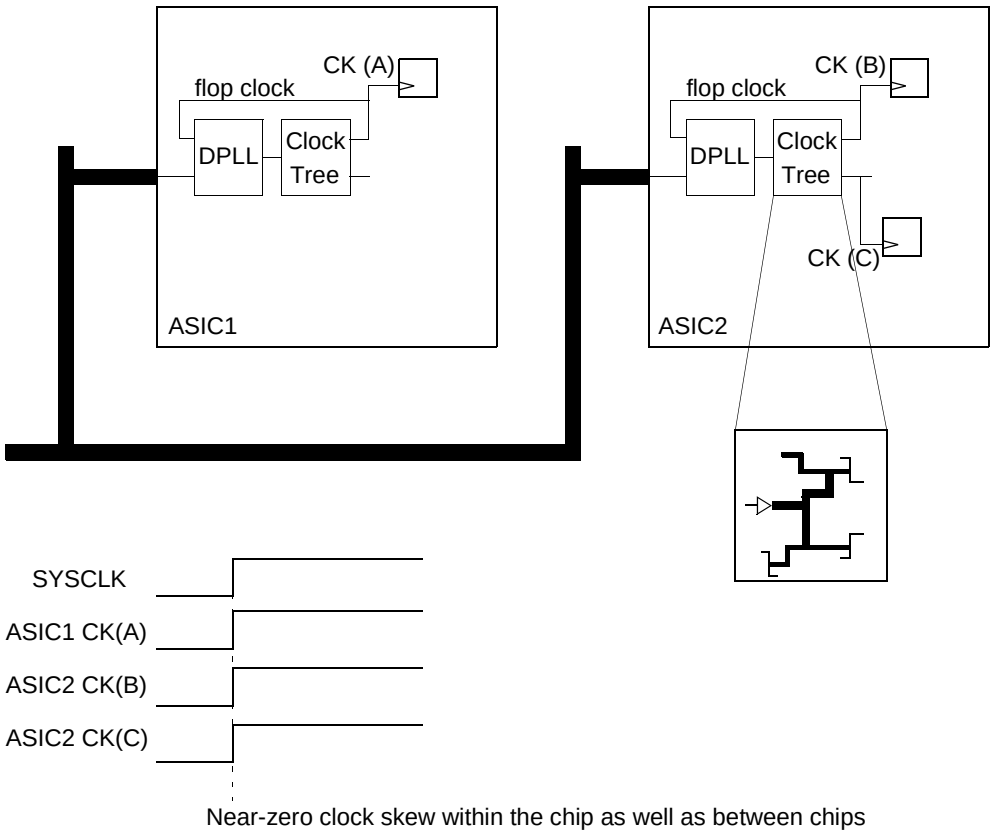


Figure 4-95 TCTS and DPLL Solutions

◇ After running the TCTS



◇ After running the TCTS and using a DPLL



Near-zero clock skew within the chip as well as between chips

4.12 Miscellaneous Design Considerations

Rules & Tips

- **Do not apply the same logic value to the S and SN inputs of the MUX21LA[P] multiplexer cell.**
- **Use IDRVx buffer cells only as a clock driver.**
- **Do not apply input value combinations to RAM/ROM address pins that map to a non-existent memory locations.**
- **Set the Chip Enable (CE) input of ROM-A to logic 1 for I_{DDS} test.**
- **Megacells functionally-compatible with Intel's 82xx family provide only standard functions.**
- **Depending on product series, connecting certain outputs of flip-flops and latches to certain inputs of multiplexers is risky.**
- **Depending on product series, connecting input buffers to certain inputs of multiplexers is risky.**

High-Drive Buffer Cells

Buffer cells designated IDRV followed by a numeric suffix (IDRV4, IDRV8, IDRV16, etc.) provide a high drive at the expense of large-geometry transistors in one or more I/O slot locations. These buffer cells are intended only for use as a clock driver to be processed with TCTS. Do not use them for buffering a normal signal.

Memory Cells with a Non-2^n Word Count

Memory cells such as RAMs and ROMs are available with flexible word/bit configurations. The number of address input pins determines the word count or the range of address locations. For example, memory cells with eight address inputs have an ability to make access to a maximum of 2 to the power of 8 (256) address locations from 0 to 255. So, in a memory cell with fewer than 256-word capacity, addressing problems can occur; that is, address inputs that can occur during system operation can attempt to access non-existent memory locations. Should this occur during simulation, all internal states in the memory will be disrupted. To keep this from happening, add a masking logic to the Chip Enable (CE) line in order to disable any access to non-existent memory locations.

5-V-Tolerant 3.3-V Push-Pull Bidirectional Buffers

The 5-V-tolerant 3.3-V push-pull bidirectional buffers draw current when placed in the 5-V-tolerant state. This current is turned off by setting the STBY pin at a low state. (In this state, the buffers may not be stressed with 5 V.) For the I_{DDS} test to take place, the STBY pin must be set to a low state.

Testing of ROM-A

The ROM-A of a gate array uses a sense amp to differentiate between low- and high-conductance thresholds for the two logic states during read operation. The sense amplifier must be disabled during I_{DDS} test so that it does not contribute static current to the I_{DDS} measurement. In other words, the Chip Enable (CE) input must be set to logic 1 for the I_{DDS} measurement to occur.

82xx-Compatible Functions

Toshiba's cell library offers megacells functionally-compatible with Intel's 82xx microprocessor peripheral family such as DMA, UART, PIT, and PPI. In many cases, 82xx-compatible ICs available on the market have extended functions and hidden operating modes. Megacells for Toshiba ASICs only support the standard functions described in the Toshiba data books.

Multiplexers Using Transmission Gates

In TC160 and later series devices, you should be aware of the connections of multiplexers that use transmission gates in them. A malfunction might occur in flip-flops or latches when

- a certain output of a flip-flop or a latch is connected to a certain multiplexer input, AND
- another certain multiplexer input (shown in Table 4-19) is tied to power supply or ground.

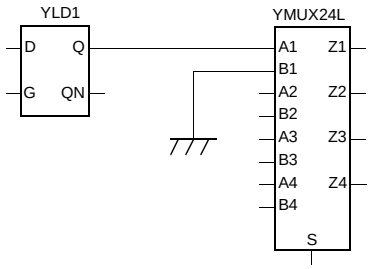
Table 4-19 gives risky interconnections between flip-flops/latches and multiplexers.

Table 4-19 **Risky Interconnections between Flip-Flops/Latches and Multiplexers**

Driving Cell	Output Pins	Driven Multiplexer	Input Pins
YFD1, YFD2, YFD3, YFD4	Q, QN	MUX21L, MUX21LP	(A, B)
YLD1, YLD2	Q, QN	MUX41, MUX41P	(D0, D1), (D2, D3)
YLD14B, YLD24B	QA, QAN, QB, QBN, QC, QCN, QD, QDN	MUX81, MUX81P	(D0, D1), (D2, D3), (D4, D5), (D6, D7)
LSR1, LSR1P, LSR2, LSR2P	Q, QN	YMUX24L, YMUX24LP	(A1, B1), (A2, B2), (A3, B3), (A4, B4)

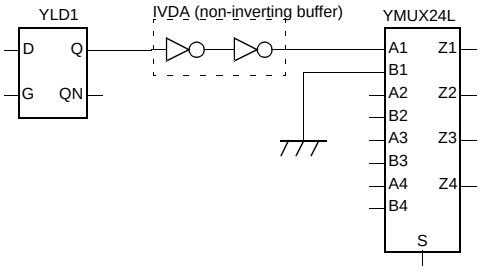
An example of a risky design practice is shown in Table 4-96. In this design, the Q output of YLD1 latch is connected with the A1 input of YMUX24L multiplexer, and the B1 input of that multiplexer is tied to ground.

Figure 4-96 **Example of Risky Interconnection between a Latch and a Multiplexer**



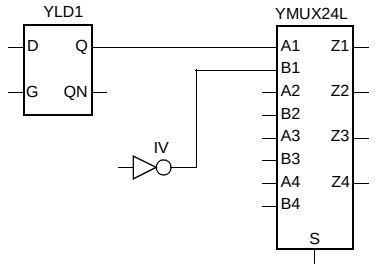
You can remedy this problem by adding an buffer gate between the latch and the multiplexer, as shown in Figure 4-97.

Figure 4-97 **Adding a Buffer Gate between a Latch and a Multiplexer**



You can also remedy the problem by adding a gate macrocell, as per Figure 4-98. This gate macrocell serves the purpose of maintaining the input signal voltage; so any other signal may not be connected to it.

Figure 4-98 **Adding a Gate Macrocell between a Latch and a Multiplexer**



Macrocells Using Transmission Gates

With TC180G/C/E and later ASIC series, connecting macrocells that use transmission gates in them to input (bidirectional) buffers or oscillator cells might cause the device susceptible to latchup. Figure 4-99 shows a risky design example.

Figure 4-99 **Connecting a Bidirectional Buffer to a Multiplexer (Risky)**

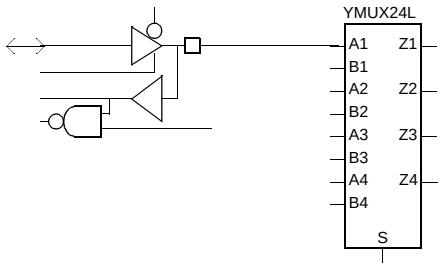


Table 4-20 and Table 4-21 give the macrocells using transmission gates.

Table 4-20 Macrocells Using Transmission Gates (Gate Arrays)

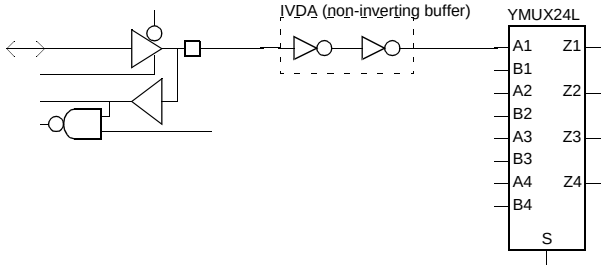
Cell Name	Input Pin
MUX21LX	A, B
MUX41, MUX41P	D0, D1, D2, D3
MUX81, MUX81P	D0, D1, D2, D3, D4, D5, D6, D7
YFD1, YFD3, YFD4	D
YLD1, YLD2	D
YLD14B, YLD24B	DA, DB, DC, DD
YMUX24L, YMUX24LP	A1, B1, A2, B2, A3, B3, A4, B4

Table 4-21 Macrocells Using Transmission Gates (Cell-Based ASICs)

Cell Name	Input Pin
RAM1	D
LDN1, LDN1P, LDN1Q, LDN1QP	D
LDN2, LDN2P, LDN2Q, LDN2QP	D
LDP1, LDP1P, LDP1Q, LDP1QP, LDP1TQN	D
LDP14TQN	D0, D1, D2, D3
LDP2, LDP2P, LDP2Q, LDP2QP	D

You can avoid the latchup problem by adding a buffer or gate macrocell, as per Figure 4-100.

Figure 4-100 **Adding a Buffer or Gate Macrocell**



4.13 Dos and Don’ts for Logic Synthesis

Rules & Tips

- **Gate utilization is merely one of the determining factors for chip routability.**
- **Use a single IDRVx cell to drive clocks and resets to be processed by TCTS.**
- **Do not use scan flip-flops in a pre-scan-insertion design.**
- **Specify maximum and minimum delay targets for critical paths.**
- **Set the operating condition to worst case for logic synthesis.**
- **Be aware of the characteristics of the FD and YFD flip-flops.**
- **Do not use combinational feedback loops.**

Layout Considerations

The maximum allowable area for the design and the clock network definition are the two major concerns for layout of a synthesized logic.

Maximum Area

As discussed in Section 4.8.5, *Maximum Gate Utilization*, on page 4-105, the maximum gate utilization depends on the number and types of macrocells used, the number of interconnect wires, and many other factors. Extensive use of small gate macrocells will lower the flexibility of routing since routing congestions occur around them. A rule-of-thumb for populating a chip is listed in the “Usable Gates” sections in the Toshiba CMOS ASIC catalog. These numbers have been extrapolated, based on a design with the most typical chip configuration.

The Toshiba Design Verifier software produces a network summary containing information that the Toshiba layout engineers reference to estimate the chip routability. When your gate-level design has passed the Design Verifier with no errors, ask your Toshiba design center engineer for your chip routability estimate.

Clock Signals

As discussed in Section 4.8.3, *Clock Signals*, on page 4-102, the clock nets on which you are planning to use TCTS must be driven by a single high-drive buffer (IDRVx). Remember that clock nets serviced in a tree configuration can not be subjected to TCTS. This rule applies to a system reset signal as well (see Section 4.8.4, *System Reset Signal*, on page 4-104).

Scan Flip-Flops

Do not use scan flip-flops in a design before automatic scan insertion. Scan flip-flops are intended exclusively for test synthesis tools to substitute for original non-scannable flip-flops.

In addition, do not use standard flip-flops that can not be replaced by functionally-equivalent scan types. For example, for TC220G/E and TC220C designs, the following flip-flops can be used.

- TC220G/E
  FD1(P), FD2(P), FD3(P), FD4(P)
- TC220C
  FD1(P), FD2(P), FD3L1(P), FD4(P)

You can find scan flip-flop pages in data book by look for “D-flip Flop with (xxxx) SCAN TEST INPUT” in the functional index. For example, the TC220G/E and TC220C series offer the following scan flip-flops.

- TC220G/E
  FD1S(P), FD2S(P), FD3S(P), FD4S(P), FD1SF(P), FD2SF(P), FD3SF(P), FD4SF(P)
- TC220C
  FD1E(P), FD2E(P), FD3L1E(P), FD4E(P), FD1SF(P), FD2SF(P), FD3L1SF(P), FD4SF(P)

Design Implementation

- Array size
  Wiring delays vary for different array sizes. To minimize fanout-limit and timing errors after logic synthesis, be sure to specify a proper area target for a design.

- Operating conditions

  After synthesis, circuit designs are simulated using three delay cases: best-, typical- and worst-cases. Be sure to specify maximum and minimum delay targets for critical paths so that the design will work properly with all of the three delay cases. Note that in a sequential design the critical path is typically the longest combinational path between two sets of registers. So be sure to set the operating condition to worst-case for synthesis. See Section 4.6.7, *Critical Path Timing*, on page 4-80 for more on critical paths.

- FD- and YFD-type flip-flops

  Gate array libraries include two types of D flip-flops: FD types and YFD types. While YFD types require less gate area than FD types, the delay of the YFD types are affected by the load on both Q and QN. Be sure to use right flip-flops at right locations. For in-depth discussion on the YFD-type flip-flops, see Section 4.5.3, *FD- and YFD-Type Macrocells*, on page 4-62.

- Feedback loops

  Do not use combinational feedback loops, since delay estimates for feedback loops could be wide of the mark.

Chapter 5

Test Data Development

This chapter is organized as follows:

5.1 Introduction

Rules & Tips

- **TSTL2 can be used as a single source file both for simulation and testing.**
- **The TSTL2 test data is structured so as to take the most advantage of tester's hardware resources. To produce test data files efficiently, you must understand the limitations of the target tester as well as how testing is performed.**

One Source for Simulation and Testing

TSTL2 can be used in both design and test phases to describe device tests. TSTL2 supports the interface capabilities for:

- input stimuli for various simulators, and
- formatted test programs for various prototype and production testers.

This means that one test data file can serve as a source for both simulation and test purposes.

The Toshiba ASIC design kits contain bidirectional interface programs between the Toshiba TSTL2 and the simulation language for a specific third-party EDA simulator. This allows you to write TSTL2 test data compilable into input stimuli for various simulators, or work solely in a preferred simulation environment, then automatically generate TSTL2 test data from the results of simulation.

TSTL2 allows you to automatically compare the expected output values specified in the TSTL2 test data with the actual simulation outputs.

Test Pattern Compaction

TSTL2 is a fast method of compacting lengthy test patterns efficiently. Features of TSTL2 include such statements and structures as repeat blocks, callable subroutine definition, constant logic value definition, sequence definition, and serialized scan test description. Using these features causes the tester program to map into the data compression mechanism of the tester, resulting in more efficient use of tester's hardware resources.

By reading the sections that follow, you can decide the best way to create test patterns for your circuit that accord with the timing and hardware limitations of the tester. See the Toshiba *TDL, TSTL2, ROM Data* manual for the syntax and semantic rules of TSTL2.

5.2 Various Test Data Files

Rules & Tips

- **Various test data files are required for the testing of an ASIC design:**
  1) **Functional test**
  2) **Megacell test (optional)**
  3) **Scan test (optional)**
  4) **DC/I_{DDS} parametric test**
  5) **High-impedance functional test**
  6) **V_{IL}/V_{IH}/ac test**
  7) **At-speed test (optional)**

Functional Test

The functional test data allows the tester to do the following:

- verify the circuit's logic functionality
- check for internal faults

Since functional test data is used to judge GO/NO-GO of manufactured devices, it should be comprehensive enough to cover every potential fault.

Megacell Test

VLSI circuits often contain large megacells such as RAMs and ROMs. Megacells require many test patterns for an adequate test, and without direct access to their inputs and outputs from the package leads, they can be impossible to test. When you have added Toshiba standard test logic, Toshiba provides you with the megacell test data (see Section 4.9.4, *Testing Megacells*, on page 4-114).

Scan Test

Scan design techniques provide total or near total controllability and observability on sequential logic and enable the computer software to automatically generate test patterns with high fault coverage. Section 4.9, *Design for Testability*, on page 4-106 briefly describes scan design techniques.

DC/IDDS Test

The DC test checks the manufactured devices for conformity with I/O buffers' parametric (i.e., electrical) performance specifications. Specifically, it measures output drive currents (IOH/IOL), output voltages (VOH/VOL), input currents (IIH/IIL), input voltages (VIH/VIL), and disable leakage currents (IDH/IDL) on I/O buffers. The IDDS test measures the quiescent supply current leading from the VDD pin into the circuit. IDDS is measured to determine how much dc leakage current remains in the circuit after all activities in the circuit have ceased.

High-Impedance Functional Test

The high-impedance (high-Z) functional test, also known as 3-state enable test, must put all 3-state and bidirectional lines into the high-impedance state at least once. This test checks to see if the 3-state enable lines work properly.

VIL/VIH/ac Test

The VIL/VIH/ac test allows the tester to do that following:

- measure a circuit for input threshold voltages (VIL/VIH)
- measure the device speed to check for conformity with ac performance specifications

You should include the Toshiba standard test logic in order to simplify the VIL/VIH/ac tests. When you have added the test logic, Toshiba creates this test data.

At-Speed Test

The at-speed test is run on a logic simulator when the circuit's operating frequency exceeds the tester's maximum test rate to check the circuit's function at frequency, with output loading parameters set to the actual conditions.

5.3 Common Tester Restrictions

Rules & Tips

- **All kinds of test data for use by a tester must accord with the timing and hardware resource limitations of the tester.**

During the testing sequences, the tester uses the following test data files which you create during simulation; that is, all kinds of test data but the at-speed test.

- Functional test
- Megacell test
- Scan test
- DC/I_{DDS} test
- High-impedance functional test
- V_{IL}/V_{IH}/ac test

10- and 20-MHz Testers

Restrictions differ, depending on the pin count of your device. Devices with no more than 100 pins will be tested on a low-end 10 MHz tester to save on test costs. Devices whose pin count exceeds 100 pins involve the use of a higher-performance 20 MHz tester. A 20 MHz tester imposes more relaxed restrictions on your test specifications.

Common Restrictions

There are restrictions on the number of patterns you can use, and on how you set them up. Tester restrictions can be grouped as under:

- Basic semantic rules
- Maximum number of test patterns
- Timing resolution
- Tester head skew
- Initial value of DT waveform
- Switching of bidirectional pin modes
- Bidirectional pin conflicts

The sections that follow discuss these restrictions in details.

Should a test data file violate any of the restrictions, that test data file can not be used for incoming inspection.

5.3 Common Tester Restrictions

5.3.1 Basic Semantic Rules

Rules & Tips

- **Toshiba conventions specify the requirements for I/O pin values in the first test cycle.**

- The TSTL2 test data must include all I/O pins used in your design. For I/O pins that are not to be tested by a given test data, the CONST statement provides an easy way to maintain I/O pins at fixed logic values.
- All output and bidirectional pins must be initially masked out (i.e., set to X or a don’t care) in the first pattern.
- Input pins programed as a DT waveform type must start out with a pattern symbol “0”.
- Input pins programed as a PP waveform type must start out with a pattern symbol “0”.
- Input pins programmed as an NP waveform type must start out with a pattern symbol “1”.
- Non-operative blank lines may not be within test patterns.

5.3 Common Tester Restrictions

5.3.2 Maximum Number of Test Patterns

Rules & Tips

- **The maximum number of test patterns and the number of test pattern files are limited so that all test patterns can be executed in a single memory load. Restrictions differ, depending on device's pin count.**

Ideally, the number of test patterns should be measured in a manner compatible with the tester's data compaction algorithms. The degree of pattern compaction varies, however, depending on how the source test data is described. In general, the number of tester patterns would become slightly less than the source.

Table 5-1 **Total Number of Test Patterns**

Devices with ≤100 pins	Devices with ≥101 pins
Up to 51k patterns	Up to 110k patterns

Table 5-2 **Maximum Test Patterns**

Test Data Type		≤ 100 pins	≥ 101 pins
Functional Test	Per file	3.6k	64k
	# of files	16	32
V_{IL}/V_{IH}/ac Test	Per file	3.6k	64k
	# of files	1	1
DC/I_{DDS} Test High-Z Functional Test	Per file	3.6k	3.6k
	# of files	1 for each	1 for each

5.3 Common Tester Restrictions

5.3.3 Timing Resolution

Rules & Tips

- **TSTL2 emulates timing capabilities supported by testers to make it possible to find tester timing problems during logic simulation.**

Figure 5-1 **Input and Output Timing Capabilities**

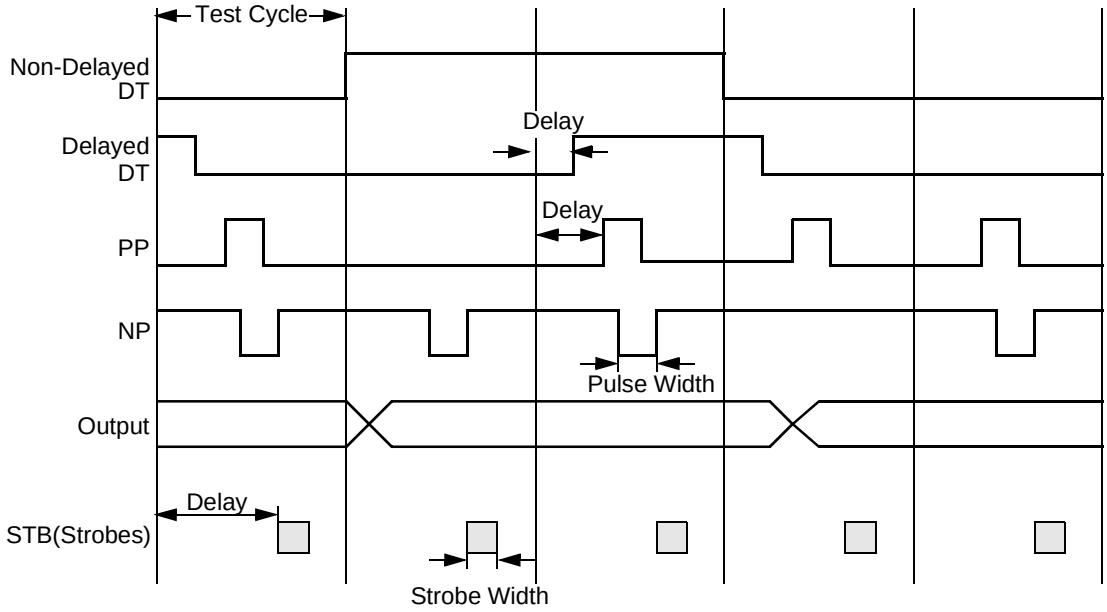


Table 5-3 **Test Cycle Length Restrictions**

Test Data Types	≤ 100 pins	≥101 pins
Functional Test Megacell Test Scan Test	≥100 ns, in 10 ns increments	≥50 ns, in 1 ns increments
DC/IDDS Test High-Z Functional Test	Fixed at 1000 ns	Fixed at 1000 ns

Table 5-4 Input Waveform Timing Restrictions

Waveform	Parameter	≤ 100 pins	≥ 101 pins
Non-delayed DT	Delay	0 ns	0 ns
Delayed DT	Delay (D)	10 ns ≤ D ≤ (test_cycle) - 20 ns	5ns ≤ D ≤ (test_cycle) - 10 ns
	Min. increments	5 ns	1 ns
PP / NP	Delay (Leading edge)	≥ 10 ns	≥ 5ns
	Trailing edge	≤ (test_cycle) - 20 ns	≤ (test_cycle) - 10 ns
	Min. pulse width	≥ 20 ns	≥ 10 ns
	Min. increments	5 ns	1 ns
Number of Input Timesets		5	7

* Timeset 0 is reserved for DT waveform with delay=0.

Table 5-5 Output Strobe Timing Restrictions

Test Data Types	Parameter	≤ 100 pins	≥ 101 pins
Functional Test Megacell Test Scan Test	Delay (D)	10 ns ≤ D ≤ (test_cycle) - 20 ns	5ns ≤ D ≤ (test_cycle) - 10 ns
	Width	Fixed at 10 ns	Fixed at 5ns
	Min. increments	5 ns	1 ns
DC/IDDS Test High-Z Functional Test	Delay	Fixed at 980 ns	Fixed at 980 ns
Number of Output Timesets		2	2

5.3 Common Tester Restrictions

5.3.4 Strobe Margins

Rules & Tips

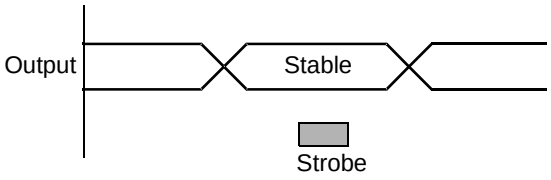
- **All output strobes must be placed with adequate margins relative to the nearest signal transitions so that the outputs are sampled when in a stable level.**

Margin Requirements

Remember that the tester is not as stable or as accurate as the simulator. Even if you specify the output strobes at a certain time, the tester may not be able to apply them at exactly that time, due to the effects of tester head skew.

Figure 5-2 illustrates a situation in which an output strobe is scheduled properly so that a signal is sampled when in a stable level.

Figure 5-2 Stable Region



However, if the strobe is skewed to such an extent that the signal is sampled while changing or in a level opposite to the expected result, the testing is made unreliable. To avoid this situation, all output strobes must be placed with adequate margins relative to the nearest signal transitions. Table 5-6 gives the minimum strobe margins required.

Three Cases of Simulations

Run best-case, worst-case, and typical-case simulations, and ensure that the steady state results of all three cases of simulations match. The calculation of I/O delays must be specified on the basis of output pad loadings of 85 pF, TTL.

Table 5-6 **Minimum Strobe Margins Required**

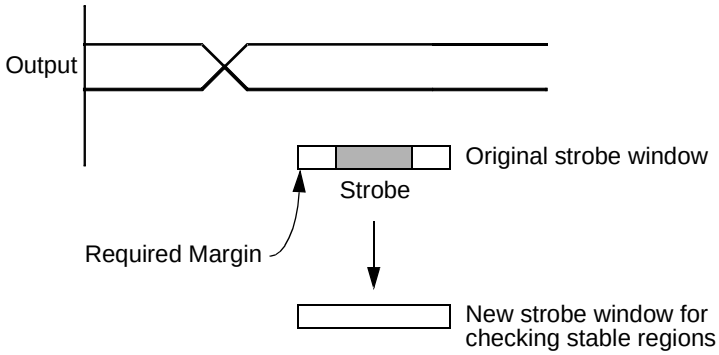
Test Data Type		≤ 100 pins	≥ 101 pins
Functional Test Megacell Test Scan Test DC/IDDS Test	Total width	30 ns	10 ns
	Before strobe	10 ns	5 ns
	After strobe	10 ns	0 ns
High-Z Functional Test	Before strobe	980 ns	980 ns

A Tip on Identifying Strobe Margin Shortages

In the case of lengthy test patterns, it is difficult and time-consuming to identify the cycles in which there are not adequate strobe margins. Here is a special tip on determining the cause of strobe margin lack.

First of all, simulate the original test data file and verify that there are no expected data mismatches. Suppose the tester requires that the region shown in Figure 5-3 be stable. If the Simulation Results Verifier program (contained in the ASIC design kit) shows that you do not have enough strobe margins, specify the entire region that should have been stable as a new strobe window. Then, re-execute simulation. This time, a simulation output comparison will be carried out throughout the new strobe window, and all time points with insufficient strobe margins are indicated as a list of “expected data mismatches.”

Figure 5-3 **Re-positioning Strobes to Identify Strobe Margin Shortages**



5.3 Common Tester Restrictions

5.3.5 Tester Head Skew

Rules & Tips

- **You must account for the possible tester head skew if the sequence of certain input signals is critical.**

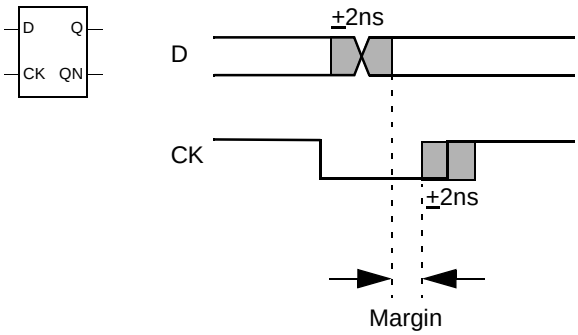
When two or more signals change at the same time, the simulator will accurately predict circuit operation, but it will not analyze the effect of the skew between the input signals. Testers are not that accurate, however. Even if you specify the input signals in the same timeset, the skew between any two input pins can be as follows.

Table 5-7 **Possible Tester Head Skew**

≤ 100 pins	≥ 101 pins
± 5ns (max.)	± 2 ns (max.)

If the sequence of certain input signals is critical, either apply them at different cycles, or place them in different timesets with sufficient delay between them.

Figure 5-4 **Tester Head Skew**



5.3 Common Tester Restrictions

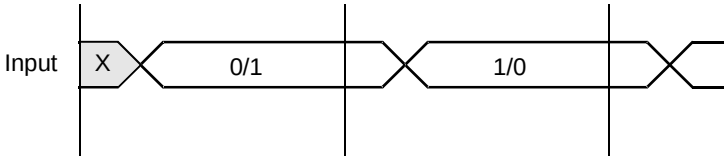
5.3.6 Initial State of DT Waveforms

Rules & Tips

- **The DT waveform always starts out at logic X, regardless of the pattern in the first test cycle.**

Testers have a register that drives test values into the device under test, which powers up in an undefined state. Therefore, TSTL2 specifies that the DT waveform start out at logic X in the first test cycle in accordance with the tester environment.

Figure 5-5 **DT Waveform's Initial State In the First Cycle**



5.3 Common Tester Restrictions

5.3.7 Bidirectional Pin Modes

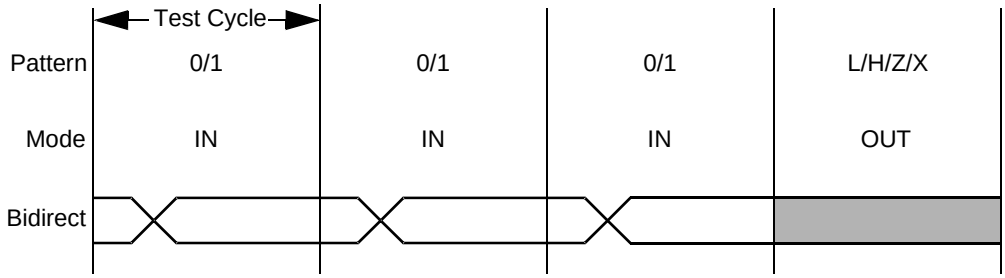
Rules & Tips

- **Bidirectional pins always change directions at cycle boundaries (even if the signal is delayed-DT type).**
- **The DT waveform starts out at different values on testers and simulators when the signal changes from output mode to input mode.**

Changes of Input and Output Modes

Testers do not allow mixed input/output mode of a bidirectional signal to occur in the same cycle. This means when a bidirectional signal changes from input mode to output mode or vice versa, the change will always occur at the cycle boundary even if the signal is delayed-DT type. Figure 5-6 illustrates this.

Figure 5-6 Bidirectional Pin Modes



Initial States of DT Waveforms

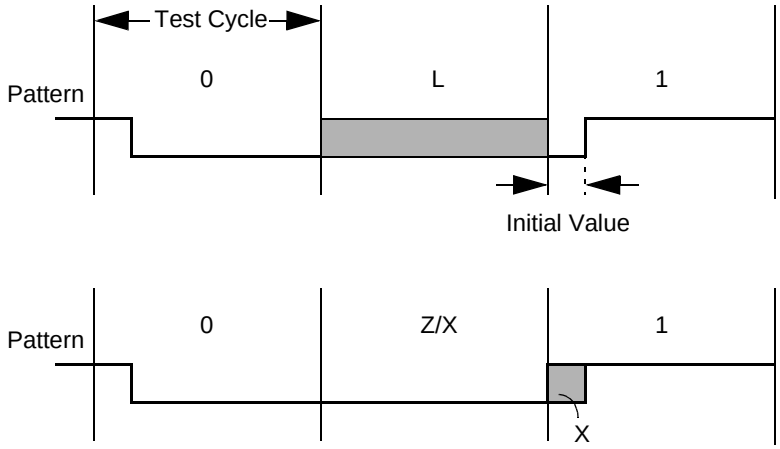
Be aware of the differences between the simulation and test environments when a signal programed as delayed-DT type changes from output mode to input mode. The DT waveform starts out at different values as shown in Table 5-8, depending on the preceding output pattern data (not the actual value).

Table 5-8 **DT Waveforms Initial Values**

Preceding Pattern*	Simulator	Tester
L	0	0
H	1	1
Z	0	X
X	1	X

* Not the actual output value

Figure 5-7 **DT Waveform's Initial State After Mode Changes (Tester)**



5.3 Common Tester Restrictions

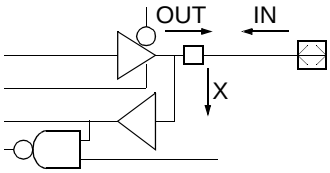
5.3.8 Bidirectional Pin Conflicts

Rules & Tips

- **Bidirectional pin conflicts make the I_{DDS} testing unreliable, and may often be detrimental because they can cause the driven gates to overheat and be permanently damaged in a short time. You must avoid them by inserting a don't care (X) cycle when a bidirectional pin changes modes.**

Bidirectional pin conflicts[1] occur when the output portion of a bidirectional buffer is enabled, and is outputting a logical value that opposes its external input source. The table alongside the drawing in Figure 5-8 shows values for IN and OUT that will result in bidirectional pin conflicts.

Figure 5-8 Bidirectional Pin Conflicts



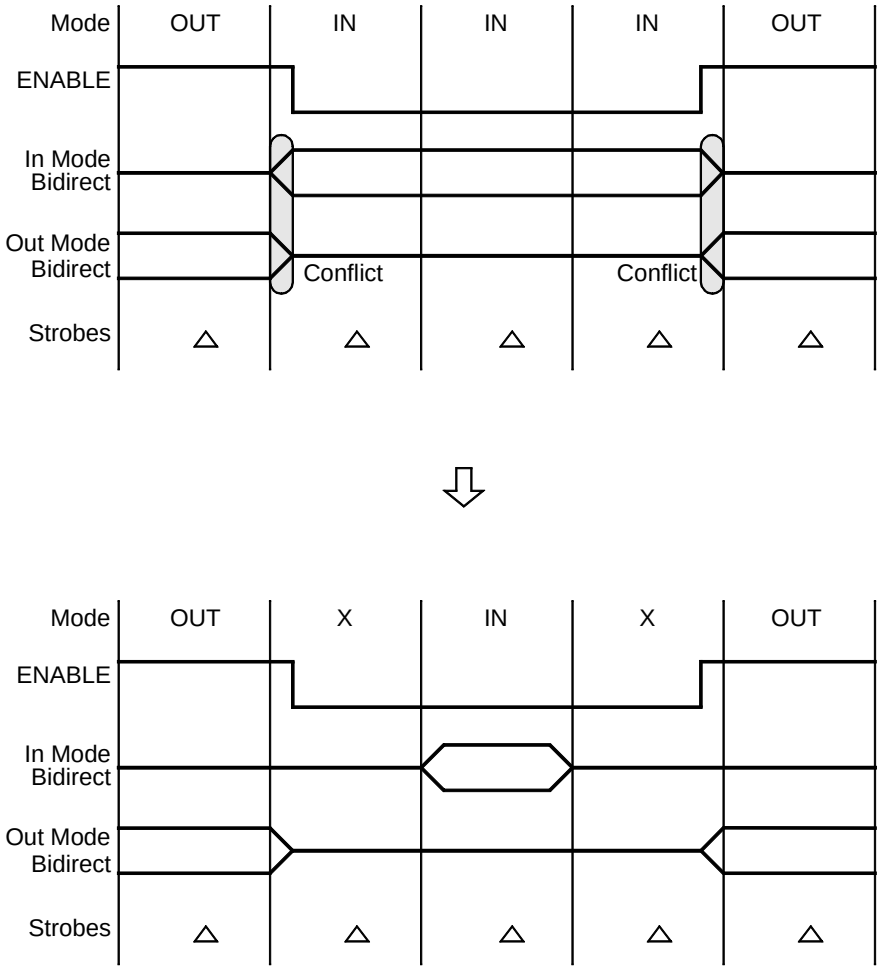
IN	0	1	0	1
OUT	1	0	X	X

Bidirectional pin conflicts introduce noise, which makes IDDS testing unreliable. They may be detrimental because they can cause the driven gates to overheat and be permanently damaged in a very short period of time.

Figure 5-9 shows a way to prevent "turnaround conflict." This is a circumstance where the direction control changes from input to output while the tester is driving the pin, or from output to input while the on-chip bidirectional buffer is outputting a logical value. To avoid bidirectional pin conflicts, insert a don't care (X) cycle between an input and an output mode cycle.

1. Synonyms of bidirectional pin conflicts include I/O conflicts, bidirectional contentions, and bus contentions.

Figure 5-9 **Avoiding Bidirectional Pin Conflicts**



5.4 DC/IDDS Test Requirements

Rules & Tips

- **Since the DC/IDDS test is carried out on a tester, it must follow all the common tester restrictions.**
- **The DC/IDDS must be able to set up the circuit's I/O in all possible states at least once.**
- **Do not write MEASURE statements in your DC/IDDS test data.**

Being executed on a tester, the DC/IDDS test must abide by all the common tester restrictions discussed in Section 5.3.

DC Parametric Test

The DC parametric test checks your circuit for dc parametric (i.e., electrical) performance. The DC test data must allow the tester to measure the following dc data on all I/O pins:

- IOH/IOL, VOH/VOL: High- and low-level output currents and voltages
- IIH/IIL, VIH/VIL: High- and low-level input currents and voltages
- IDH/IDL: High- and low-level disable currents

IDDS Test

The IDDS test measures the quiescent (static) supply current leading from the VDD pin into the circuit. IDDS is measured to determine how much dc leakage current remains in the circuit after all activities in the circuit have ceased. IDDS is the abbreviation of *direct drain static current*. The IDDS test is also referred to as static current test.

MEASURE Statements

TSTL2 provides a statement called MEASURE to specify when and where dc parametric measurements are to take place. You need not place any MEASURE statements in your TSTL2 test data manually.

Toshiba's test system will automatically search the test data for the best suitable timing for dc measurements, and embed the tester program with appropriate MEASURE instructions.

Requirement Overview

The DC/IDDS test must be written in such a way as to use the conditions shown in Table 5-9.

Table 5-9 DC/IDDS Test Conditions

Test Cycle	1000 ns	
Output Strobe Delay	980 ns	
Minimum Strobe Margins	≤ 100 pins	Total: 30 ns, Before: 10 ns, After: 10 ns
	≥ 101 pins	Total: 10 ns, Before: 5 ns, After: 0 ns
Maximum Test Steps	3,600	
Bidirectional Float State	No longer than the two cycle length	

The DC/IDDS test is required to set up the circuit at certain logical conditions (high, low, or high-impedance) appropriate for each type of tests.

Keep the DC/IDDS test as short as possible. To minimize the number of measurements to be performed and thus maximize the test efficiency, the DC/IDDS test should be able to force all or as large a number of the I/O pins as possible to the defined states at one time.

The sections that follow will discuss the specific requirements for the DC/IDDS test.

5.4 DC/I_{DDS} Test Requirements

5.4.1 DC Parametric Tests

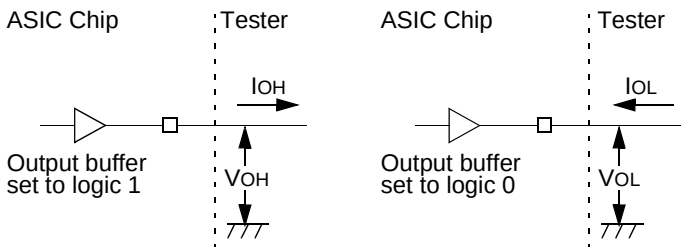
Rules & Tips

- **The DC/I_{DDS} test must be written in such a way that all I/O buffers are placed in all possible states at least once.**

I_{OH} / I_{OL}

The I_{OH}/I_{OL} test checks the drive of output buffers. I_{OH} and I_{OL} are the current into an output with input conditions applied that according to the product specification will establish a high and a low level (i.e., the V_{OH} and V_{OL} voltages) at that output, respectively. The DC/I_{DDS} test must be written in such a way that each of the output and output-mode bidirectional buffers reaches the high and low states at least once.

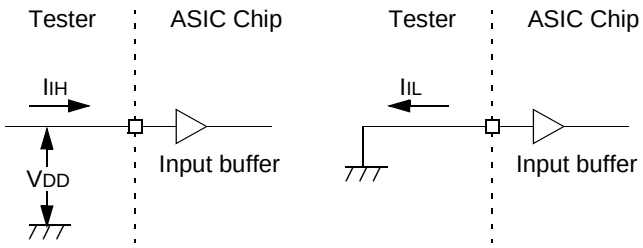
Figure 5-10 The I_{OH}/I_{OL} Test



I_{IH} / I_{IL}

I_{IH} and I_{IL} are the current into an input when a high- and a low-level voltage are applied to that input. For I_{IH}/I_{IL} measurements to take place on bidirectional pins, the DC/I_{DDS} test must be written in such a way that each of the bidirectional buffers is set in input mode at least once.

Figure 5-11 The I_{IH}/I_{IL} Test



IDH / IDL

IDH and IDL are the leakage current into an output of a disabled 3-state output buffer when a high- and a low-level voltage are applied to that output. The DC/IDDS test must be written in such a way that each of the 3-state output buffers reaches the 3-state (i.e., high-impedance) condition at least once.

Making Measurements Reliable

Remember that all DC tests are executed at the cycle end. If the target I/O pin is kept stable for the length of full two cycles, you can ensure a test cycle at the end of which a target I/O pin is in a steady state (Figure 5-12).

Figure 5-12 **I/O Pins Need Be Stable for the Length of Full Two Cycles**

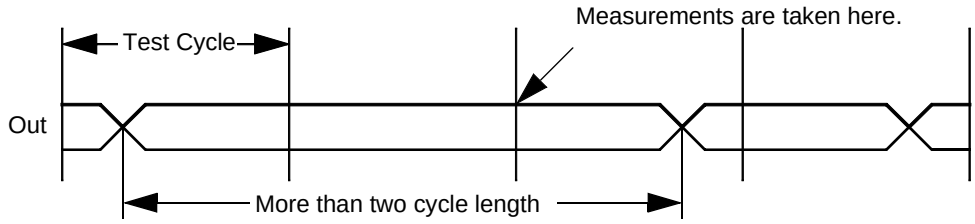


Table 5-10 summarizes the DC test requirements.

Table 5-10 **DC Test Requirements**

Pin Type	Input Conditions	Output Conditions
Input	0, 1	—
Output	—	L, H
Bidirect	0, 1	L, H
3-state output	—	L, H, Z

5.4 DC/I_{DDS} Test Requirements

5.4.2 I_{DDS} Test

Rules & Tips

- **The I_{DDS} test measures power supply leakage current to determine whether excess current flows, implying a fault. Be sure to set up a condition in which all dc current is turned off so that dc leakage can be measured easily.**

Test Requirements

To eliminate all sources of dc current, the circuit must be set up as follows *simultaneously*:

- Set input buffers with pull-up at a high state.
- Set input buffers with pull-down at a low state.
- Set bidirectional buffers with pull-up at a high state in either input or output mode.
- Set bidirectional buffers with pull-down at a high state in either input or output mode.
- Set internal 3-state drivers at a low or high state. Any internal floating nodes must be eliminated.
- Set 3-statable outputs of megacells and megafunctions at a low or high state.
- Set the Chip Enable (CE) input of ROM-A at a high state to disable the internal sense amp.
- Set the STBY input of 5-V tolerant 3.3-V push-pull bidirectional buffers at a low state.
- For memory cells whose word count is a power of two, address input values must be within the existent address ranges. For example, a memory cell with a word count of 224 has eight address pins, which enable you to specify addresses in the range from 0 to 255. However, addresses 244 to 255 may not be accessed. Alao, do not apply an indeterminate state (X) to any address pins.

- For memory cells having the CE pin, set it at an inactive state. Also, do not apply an indeterminate state (X) to the CE pin.

Improving the IDDS Testability

External bidirectional buffers and internal 3-state buses can be a problem in creating IDDS test patterns.

It is recommended that the 3-state enable lines of bidirectional buffers be controlled externally so that in input mode bidirectional buffers can be easily forced into the logical level in accordance with pull resistance type: “1” for pull-up, “0” for pull-down.

Figure 5-13 Controlling a Bidirectional Buffer Externally

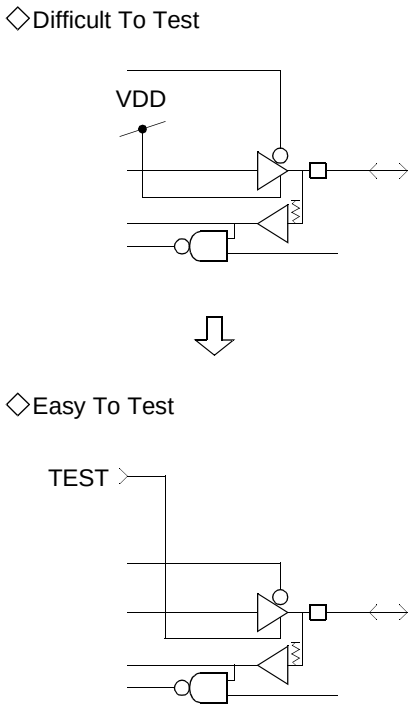
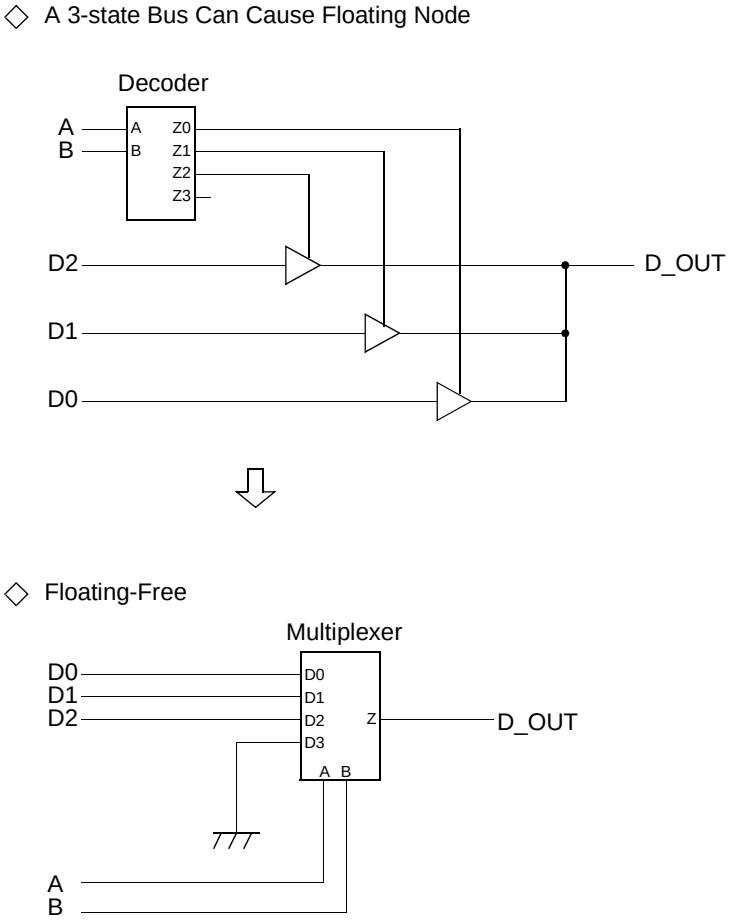


Figure 5-14 shows a design that uses a 3-state bus. A floating node occurs when all of the 3-state buffers driving a bus are disabled. A floating node causes static current to flow on the driven gate, making the IDDS measurement unreliable. A design using a multiplexer is a better implementation of the same logic function since it eliminates a floating node.

Figure 5-14 Avoiding a Floating Node

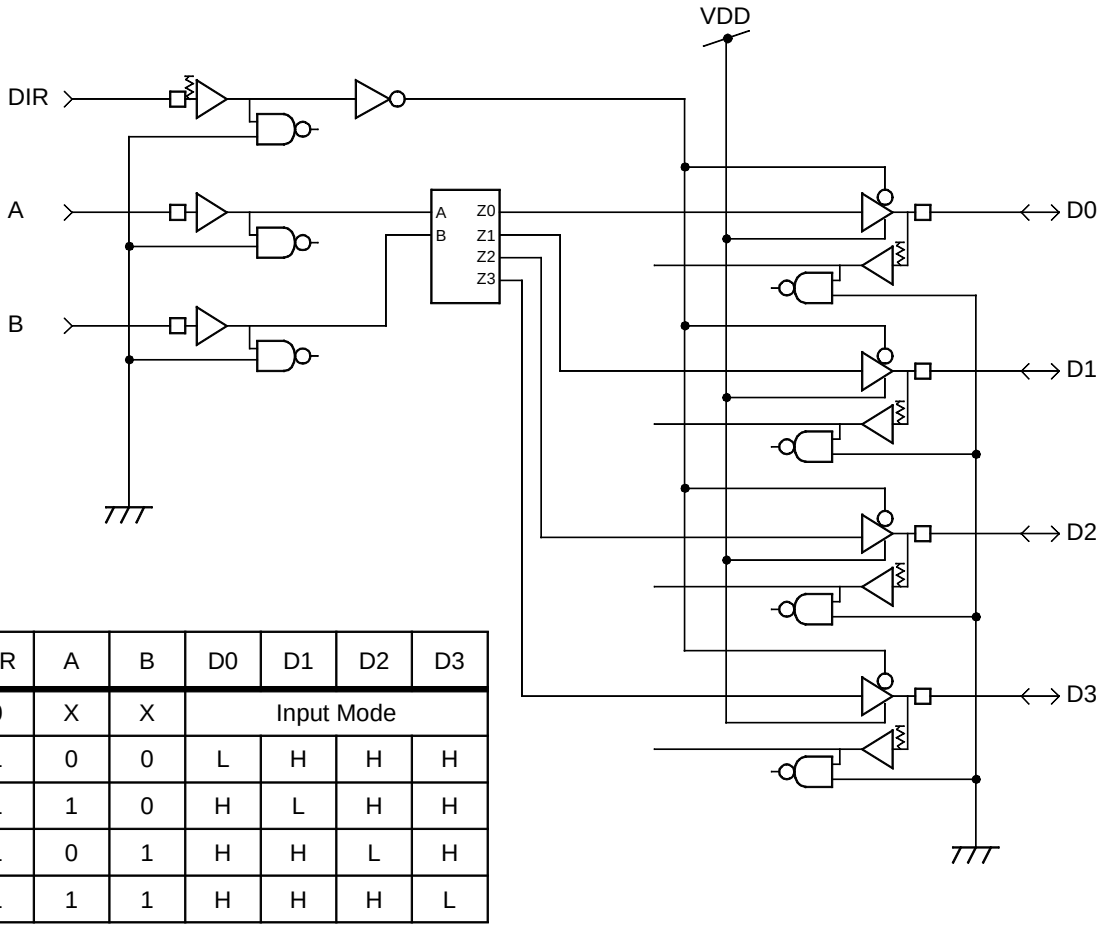


Untestable Design

Figure 5-15 shows a design on which a reliable IDDS test can not be executed. When DIR=1, either one of the bidirectional buffers (D0 to D3) is placed at a low state although they must be put at a high state, matching the pull-resistance level. Conversely, DIR must be low to set all the bidirectional buffers at a high state simultaneously, although it must be at a high state for accurate IDDS measurement. In either case, one pull-up resistor contributes static current to IDDS measurement.

You can remedy this problem by changing DIR to a input buffer without a pull-up resistance.

Figure 5-15 A Design that Makes IDDS Measurement Unreliable



DIR	A	B	D0	D1	D2	D3
0	X	X	Input Mode			
1	0	0	L	H	H	H
1	1	0	H	L	H	H
1	0	1	H	H	L	H
1	1	1	H	H	H	L

5.4 DC/IDDS Test Requirements

5.4.3 DC/IDDS Test Logic

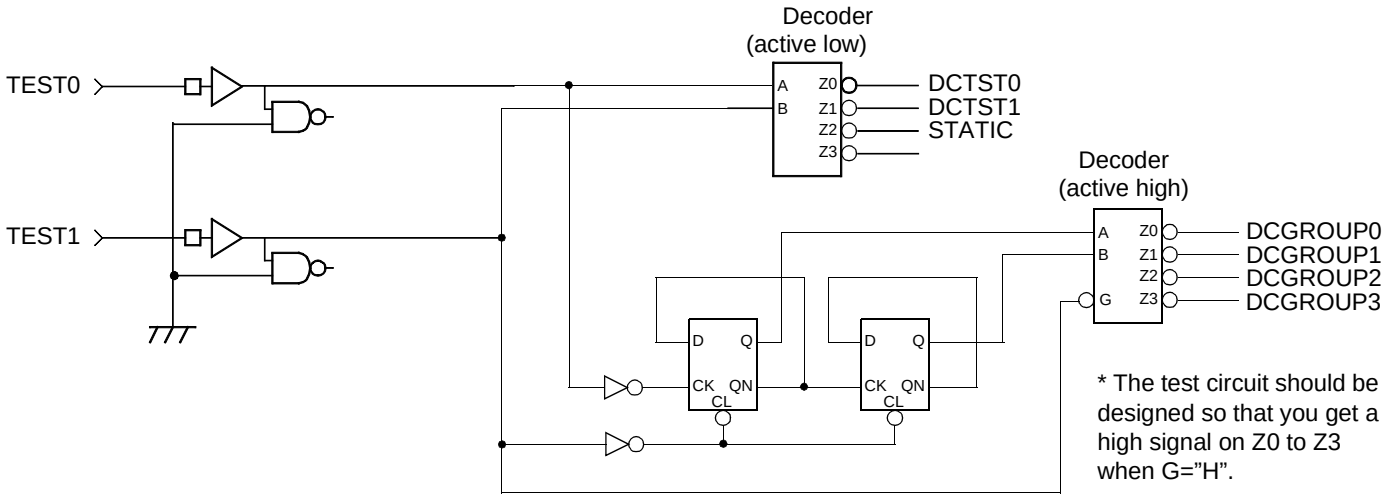
Rules & Tips

- **Add a test logic to keep DC/IDDS patterns short.**

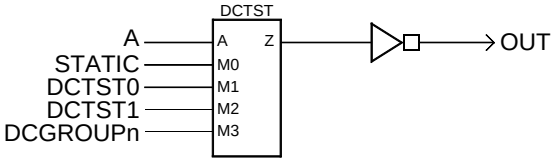
The DC/IDDS test must set all I/O buffers in all possible states using a limited number of patterns. Gate count permitting, it is recommended to add a test logic shown in Figure 5-16 wherever possible to keep patterns as short as possible.

- Classify output and bidirectional buffers into groups each of which does not exceed a total of 64mA output drive currents. Per group, connect the M3 pin on the DCTST block to the DCGROUPn (n=0, 1, 2, 3, ...) on the decoder as illustrated in Figure 5-16, which follows.
- If your design has test circuitry for the VIL/VIH/ac test, connect the input buffers for TEST0 and TEST1 to the NAND tree.
- The input buffer must be the one without pull resistance.
- When mounting the device to a printed circuit board, package pins TMODE0 and TMODE1 must be connected to the VDD line on the printed circuit board so that the device will permanently be in the normal operating mode.

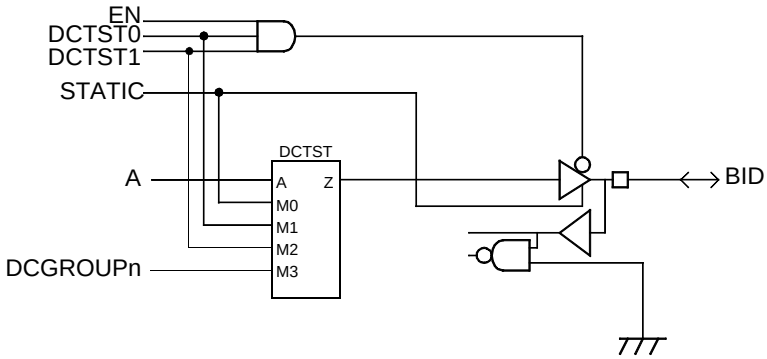
Figure 5-16 **DC/I_{DDS} Test Logic**



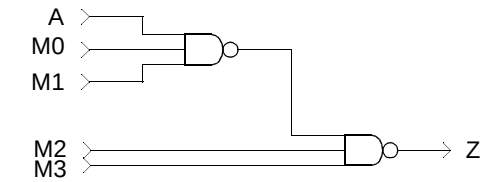
◇ Output Buffer



◇ Bidirectional Buffer



◇ Underlying Circuit of DCTST



TEST0	TEST1	Mode
0	0	Out/Bidirect "L"
1	0	Out/Bidirect "H"
0	1	Bidirect Input Mode
1	1	Normal Output

5.5 VIL/VIH/ac Test Requirements

Rules & Tips

- **Since the VIL/VIH/ac test is carried out on a tester, it must follow all the common tester restrictions. The VIL/VIH/ac test is executed using a special test logic.**

Being executed on a tester, the VIL/VIH and frequency test must abide by all the common tester restrictions discussed in Section 5.3.

The test logic illustrated in Figure 5-17 on page 5-34 allows the tester to do the following:

- measure a circuit for input threshold voltages (VIL/VIH)
- measure the device speed to check for conformity with ac performance specifications

To perform a reliable VIL/VIH test, you must insert additional circuitry. The VIL/VIH test is executed with the input driver levels set at VIL (max) and VIH (min). This leaves no noise margin for the input buffers when output buffers generate large current spikes while switching simultaneously. As a result, input buffers may misread voltage and therefore logical levels.

To avoid this, Toshiba requires that your design include both a NAND tree structure and a TSTOUT pin, as depicted in Figure 5-17. A system data output pin can be used as a TSTOUT pin. No gate overhead is involved in the NAND tree, since all Toshiba input buffers have an internal NAND gate.

If your design has bidirectional buffers, you must add a TESTI pin for test enable, as shown in Figure 5-17. This pin allows you to disable all the output portions of bidirectional buffers. The TESTI pin is also used as one of the select controls of a four-to-one multiplexer.

The VIL/VIH patterns are very specific. The first pattern is all 1s. Zeros are then applied according to the pattern shown in Figure 5-11. Only the TSTOUT pin is monitored during the VIL/VIH test; all other output pins are temporarily masked out.

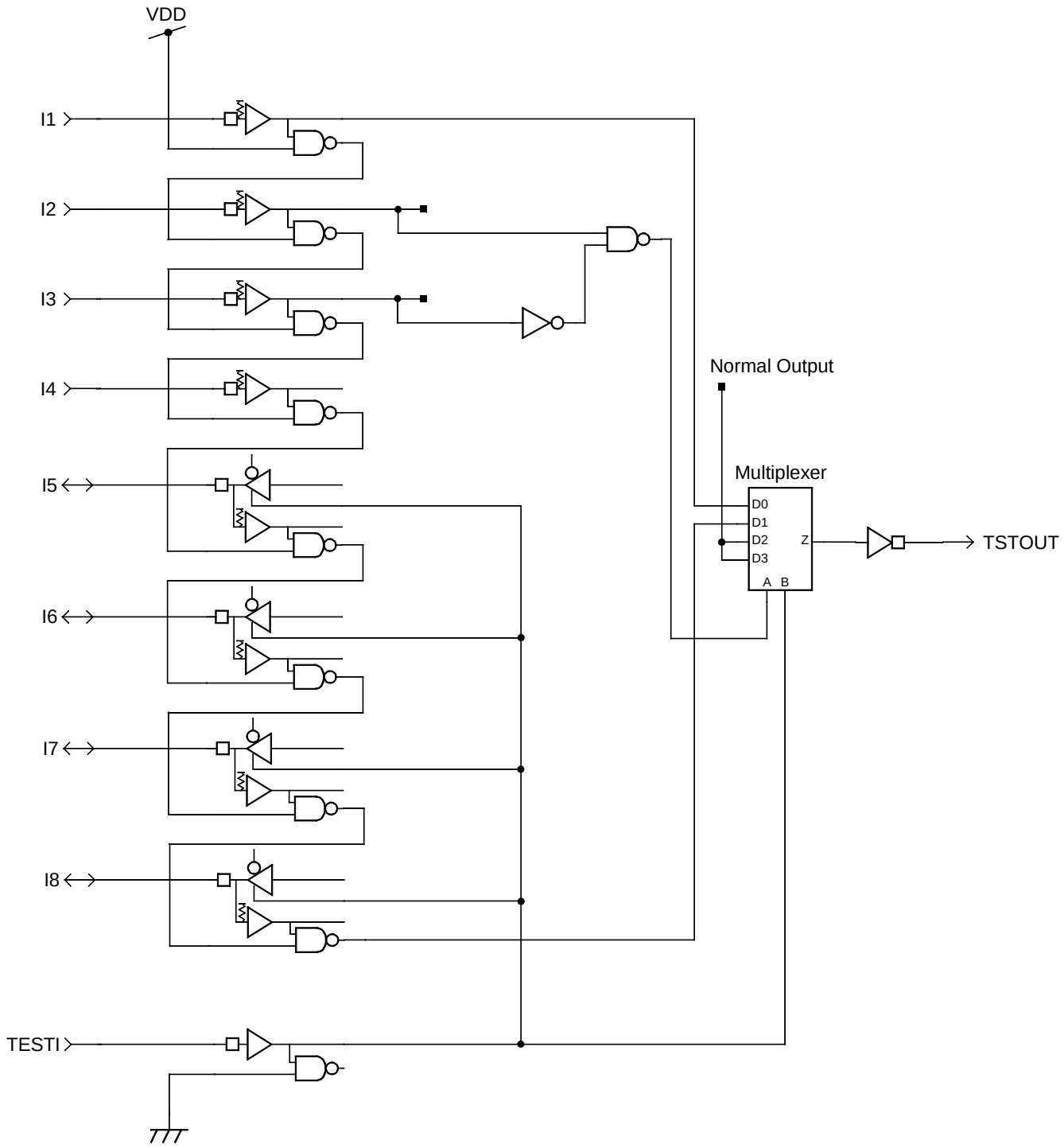
In addition to the NAND tree lending itself to a reliable VIL/VIH measurement, it is used to measure the device speed to check for conformity with ac performance specifications. The device speed is determined by measuring the propagation delay through the NAND tree. Testers are not so stable, however, and as explained in Section 5.3.5, *Tester Head Skew*, on page 5-16, inaccuracy is introduced at physical input pins. To compensate any negative or positive tester error at the head of the NAND tree (I1), the NAND tree delay is determined by:

1. measuring the delay from I1, passing through the string of NAND gates, to TSTOUT,
2. measuring the delay from I1, passing through the multiplexer, to TSTOUT (this is called calibration mode), then
3. subtracting the calibration mode delay from the total delay measured at step 1.

Table 5-11 VIL/VIH/ac Test Logic Behavior (TESTI=0)

Test Item	I1	I2	I3	I4	I5	I6	I7	I8	TSTOUT	Measurement
VIL/VIH Test	1	1	1	1	1	1	1	1	1	VIH on I1
	0	1	1	1	1	1	1	1	0	VIH on I2, VIL on I1
	0	0	1	1	1	1	1	1	1	VIH on I3, VIL on I2
	0	0	0	1	1	1	1	1	0	VIH on I4, VIL on I3
	0	0	0	0	1	1	1	1	1	VIH on I5, VIL on I4
	0	0	0	0	0	1	1	1	0	VIH on I6, VIL on I5
	0	0	0	0	0	0	1	1	1	VIH on I7, VIL on I6
	0	0	0	0	0	0	0	1	0	VIH on I8, VIL on I7
	0	0	0	0	0	0	0	0	1	VIL on I8
ac Test	1	1	1	1	1	1	1	1	1	NAND tree (initial state)
	0	1	1	1	1	1	1	1	0	NAND tree Tpd(H–L)
	1	1	1	1	1	1	1	1	1	NAND tree Tpd(L–H)
	1	1	0	x	x	x	x	x	1	Calibration mode I1–MUX–TSTOUT (initial state)
	0	1	0	x	x	x	x	x	0	I1–MUX–TSTOUT Tpd(H–L)
	1	1	0	x	x	x	x	x	1	I1–MUX–TSTOUT Tpd(L–H)

Figure 5-17 V_{IL}/V_{IH}/ac Test Logic



5.6 High-Impedance Functional Test Requirements

Rules & Tips

- **Since the frequency test is carried out on a tester, it must follow all the common tester restrictions.**

Being executed on a tester, the frequency test must abide by all the common tester restrictions discussed in Section 5.3.

The high-impedance (high-Z) functional test, also known as 3-state enable test, must put each of the 3-state and bidirectional lines into the high-impedance state at least once. This test checks to see if the 3-state enable lines work properly.

The high-impedance functional test must be written in such a way as to use the conditions shown in Table 5-12.

Table 5-12 High-Impedance Functional Test Conditions

Test Cycle	1000 ns
Output Strobe Delay	980 ns
Minimum Strobe Margins	980 ns
Maximum Test Steps	3,600

5.7 At-Speed Test Requirements

Rules & Tips

- **At-speed test is required only when the circuit's frequency exceeds the tester rating. Since the at-speed test is run only on a logic simulator, it need not follow the common tester restrictions.**

The simulator can test your circuit at any frequency, and at a resolution as fine as 0.01 ns. There is no waveform and timing restrictions on the at-speed test data.

However, the number of test patterns and the test data files should be limited to reasonable levels. Simulating dozens of l00k-pattern files will certainly lower the efficiency of verification and sign-off.

The Toshiba ASIC sign-off system has a number of convenient functions. Please consult the Toshiba ASIC service group about the design acceptance criteria.

Chapter 6

Logic and Fault Simulation

This chapter is organized as follows:

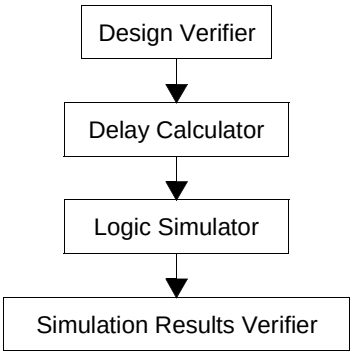
6.1 Overview of Simulation Procedures

Rules & Tips

- **Verify that your design is electrically and physically feasible.**
- **Use an output load specifications file only when simulating an at-speed test.**
- **Run best-case, worst-case, and typical-case simulations on every test pattern file.**

Figure 6-1 below shows the general simulation environment.

Figure 6-1 General Simulation Environment



Design Verification

Before simulating your design, execute the Toshiba Design Verifier program on it. The main purpose of the Design Verifier is to verify the circuit's physical and electrical feasibility for implementation as a real device. Verification means:

- Checking pin-to-pin connections for electrical rules violations;
- Checking if any macrocell output pins are not connected to loads in excess of their drive strengths;
- Checking if the design fits into silicon.

Please remember that if there remains any single violation, your design can never be implemented as a real device.

Delay Calculation

The Toshiba Delay Calculator program calculates propagation delay times for each cell in a design and creates a delay file. The delays reflect temperature, voltage, and process-condition parameters that the user can specify.

Output Load Specifications

When simulating an at-speed test pattern, you should create a text file that specifies:

- capacitance loadings on output and bidirectional pins;
- the types of capacitive load of the driven devices (CMOS or TTL).

The default is 85pF, TTL, which is equal to the typical tester conditions. The Delay Calculator will use the data in the file to compute rise and fall times for the I/O buffers described in it. When simulating other kinds of test pattern files, never supply an output load specification file; that is to say, you must use the default tester conditions for simulation.

Simulation Conditions

As discussed in Section 4.1.3, *Variations of Propagation Delays*, on page 4-12, propagation delays are sensitive to power supply voltage, die temperature, and manufacturing process spreads. Run best-case, worst-case, and typical-case simulations, and ensure that the steady state results of all three cases of simulations match. When simulating an at-speed test, use the actual output load conditions for the calculation of I/O delays. For the other types of test data, use the typical tester conditions (i.e., 85 pF, TTL). Regardless of test data types, estimate the rise in chip temperature, based on its power dissipation (see Chapter 7, *Power Estimation*), and use the chip temperature (instead of ambient temperature) for delay calculation.

Simulation Results Verification

The Toshiba Simulation Results Verifier program allows you to automatically compare expected output values against the actual results of simulation. It also allows you to check if and where signal conflicts and floats occurred during simulation. The sign-off versions of the Simulation Results Verifier program are equipped with many other features that ease your burden of verifying the simulation results of a large, complex design.

6.2 Design Acceptance Criteria

Rules & Tips

- **When you have completed pre-layout simulation, complete the Design Release Checklist for inclusion in the design release package. Design acceptance criteria are given below.**

Table 6-1 shows design acceptance criteria for Toshiba ASICs. Use it to review your progress.

Table 6-1 Design Acceptance Criteria

Item	Case	Functional	Megacell	DC/IDDS	Scan
Expected Data Mismatches	B, N, W	Run best-case, worst-case, and typical-case simulations, and ensure that the steady state results of all three cases of simulations match.			
Strobe Margins	B, N, W	Ensure that there are more margins than stipulated. • ≤100 pins: Before: 10 ns, After: 10 ns, Total: 30 ns • ≥101 pins: Before 5 ns, After: 0 ns, Total: 10 ns			
Signal Conflicts	N	• Ensure that bidirectional pin conflicts do not occur altogether. • Ensure that internal 3-state bus conflicts do not occur except for brief ones that take place while the enable signal is switching.			
Signal Floats	N	• Ensure that internal 3-state bus floats do not occur except for brief ones that take place while the enable signal is switching. • External bidirectional pin floats are not checked for functional, megacell, and scan tests.		Bidirects: < 2 cycle length	
Node Toggle Coverage	N	Checked during logic simulation.		Checked during logic simulation.	Checked during ATPG.
Fault Coverage (Optional)	N	Checked with fault simulation.		Checked with fault simulation.	Checked during ATPG.

Case: B: Best-case, N: Nominal, W: Worst-case

(Continued)

Item	Case	High-Z	VIL/VIH/ac	At-Speed
Expected Data Mismatches	B, N, W	Run best-case, worst-case, and typical-case simulations, and ensure that the steady state results of all three cases of simulations match.		Use specified operating conditions.
Strobe Margins	B, N, W	Before: 980 ns	Not checked	
Signal Conflicts	N	• Ensure that bidirectional pin conflicts do not occur altogether. • Ensure that internal 3-state bus conflicts do not occur except for brief ones that take place while the enable signal is switching.		Not checked
Signal Floats	N	• Ensure that internal 3-state bus floats do not occur except for brief ones that take place while the enable signal is switching. • External bidirectional pin floats are not checked.		Not checked
Node Toggle Coverage	N	Not checked		
Fault Coverage (Optional)	N	Not checked		
Others	N	Check for high-Z test require-ment.	Check for >70 ns pulse width (typ.).	Check for customer-specified criteria.

Toshiba offers fault simulation services at extra cost. The non-sign-off versions of the Simulation Results Verifier do not have the ability to check for internal 3-state conflicts and floats. Some EDA tools offer toggle-checking capability, but many do not.

At the end of the pre-layout phase of the design process, a completed Design Release Checklist must be filed. It helps you to verify successful completion of various stages of pre-layout specification, and furnishes the Toshiba ASIC design group with essential information. A blank form of the Design Release Checklist is provided in Appendix B.

6.3 Fault Simulation

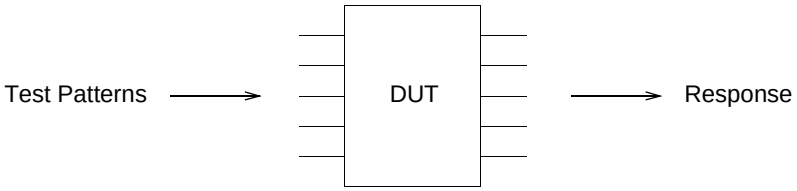
Rules & Tips

- **Fault simulation is growing in importance because of the need for greater confidence in large ASICs.**
- **Toshiba offers fault simulation services as an option.**
- **Toggle-checking is part of the standard verification procedures for Toshiba ASICs.**

Testing of a Digital Device

An integrated circuit is tested to determine if any physical defects were introduced during manufacturing. Figure 6-2 shows a device under test (DUT) to which test patterns are applied and the resulting output response is monitored. If the correct response is known, then we can determine whether the device is operating as we intended it or not.

Figure 6-2 Testing of a Device



The response is observed at physical output pins of a device. The output response is evaluated by comparing the device response to an expected response which usually comes from a logic simulation process.

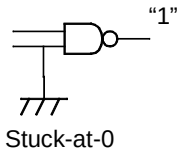
If the response from the DUT differs from the expected response, then an error is said to have occurred. In cases where an error manifested itself as an incorrect logic value, that error is referred to as a mismatch. A fault or faults — physical defects introduced in the manufacturing process — cause an error.

If the DUT responds correctly, we may have confidence that the DUT is fault-free. We can only conclude, however, that the DUT does not include any of the faults for which it was tested. For the above assumption to be reasonable, the test pattern should be able to cover most, if not all, of the faults that are likely to occur. For this very reason, grading the test pattern is very important.

Stuck-At fault Models

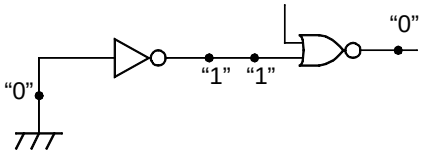
In digital devices, the effect of physical defects is represented by a fault model at the logic level. The fault model which is most commonly used is the stuck-at fault model, where the inputs and the outputs of the logic gate are assumed fixed to a value, either logic 1 or logic 0, irrespective of what value is applied or should be coming out of the network. For example, consider a two-input NAND gate with one input stuck at 0. Regardless of the logic level of the other input, the output is always at 1.

Figure 6-3 **Stuck-At Faults**



To detect a stuck-at fault on a circuit node, you must have both controllability and observability on that node. Controllability is a measure of ease or difficulty of driving a node into a known state. Observability is a measure of the ability to determine the logic value present on a node. Figure 6-4 shows examples of non-controllable and non-observable nodes.

Figure 6-4 **Non-Controllable and Non-Observable Nodes**



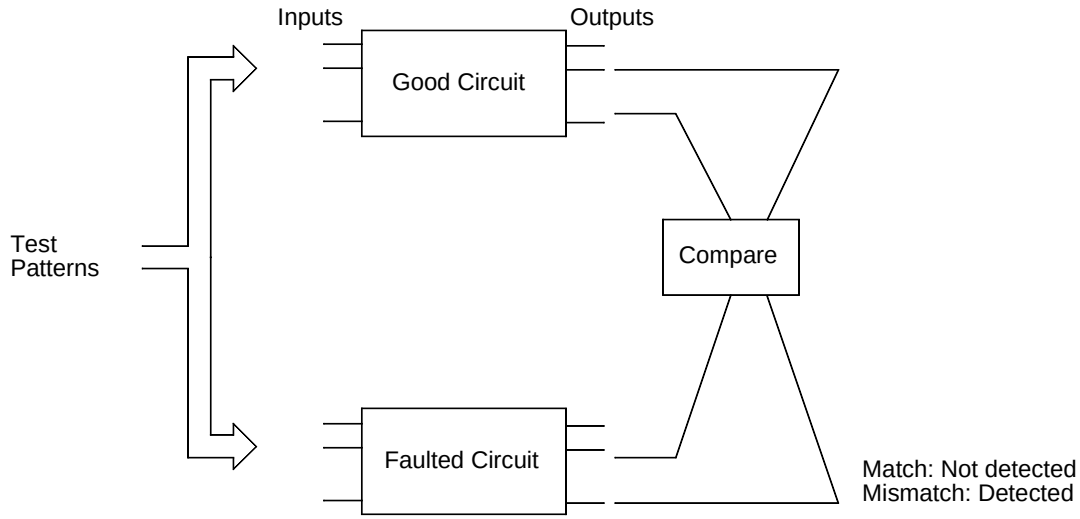
Fault Simulation Mechanism

A test pattern should detect as many potential stuck-at faults as possible. Fault simulation is often employed to grade the test pattern effectiveness. During a fault simulation, faults are “seeded” into the circuit. For example, a given node in the circuit is “assumed” to be fixed to either logic 1 or logic 0. If a faulty node is stuck at 0, then you need a test pattern that forces that node into a 1. Then the effect of the fault must be propagated to an output where you can observe it. The actual output values are compared to the corresponding output values from the fault-free circuit. If a mismatch is detected, then the fault is declared detected. After this process is repeated for a sufficient number of possible faults, an estimate, called fault coverage (F),

F = (no. of faults detected) / (no. of faults simulated)

is obtained.

Figure 6-5 Fault Simulation Mechanism

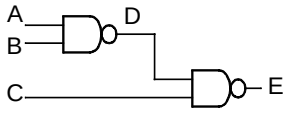


Fault Simulation vs. Toggle Simulation

Toggle simulation determines whether the test pattern thoroughly exercises the circuit, i.e., causes every node in it to change state (or "toggle"). While fault simulation checks both the controllability and observability aspects of a design, toggle simulation checks only the controllability aspect of a design. Toggle simulation is used as a fast method of assuring node controllability as a prerequisite to fault simulation, since toggle-checking can be executed as an integral part of logic simulation.

Note that test patterns exist that can control a node to a known value but can not propagate the fault information on that node to an observation point. In other words, that node is controllable but not observable. Consider the circuit and the test pattern shown in Figure 6-6 below. The test pattern provides a 100% node toggle coverage, but not a 100% fault coverage, on the circuit. Suppose node D is stuck at 1. At this time, when node C is low, node E is high in both the faulted and good circuits; when node C is high, node E is low in both the faulted and good circuits. This means the stuck-at-1 fault on node D can not be detected with this test pattern.

Figure 6-6 Toggle Coverage vs. Fault Coverage



Input			Output	
A	B	C	D	E
1	1	0	L	H
0	0	0	H	H
0	0	1	H	L

Megacell and Megafunction Constraints

Fault simulation does not cover the internal nodes of megacells and megafunctions, since they are treated as "black boxes." Only output pins are seeded with faults for these cells. In order to ensure a reasonable level of fault coverage on megacells, Toshiba strongly recommends that you insert a test logic to megacells and megafunctions so they can be tested in isolation (see Section 4.9.4, *Testing Megacells*, on page 4-114).

Toggle and Fault Simulation Services

The Toshiba ASIC sign-off simulator can execute the toggle-checking as an integral part of logic simulation. Toggle coverage is checked as standard on every ASIC design during pre-layout simulation. Some of the Toshiba-supported EDA tools offer a toggle simulation capability as well.

Fault simulation can only occur after a correct design and an expected output data set for the correct design are obtained. Being very time-consuming, fault simulation services are optional and available at an additional cost. Fault simulation is growing in importance, however, because of the need for greater confidence in large, complex circuits. If fault simulation is required, consult with your Toshiba ASIC service group. If your circuit is scan-designed, fault simulation is executed as an integral part of automatic test pattern generation.

Chapter 7

Power Estimation

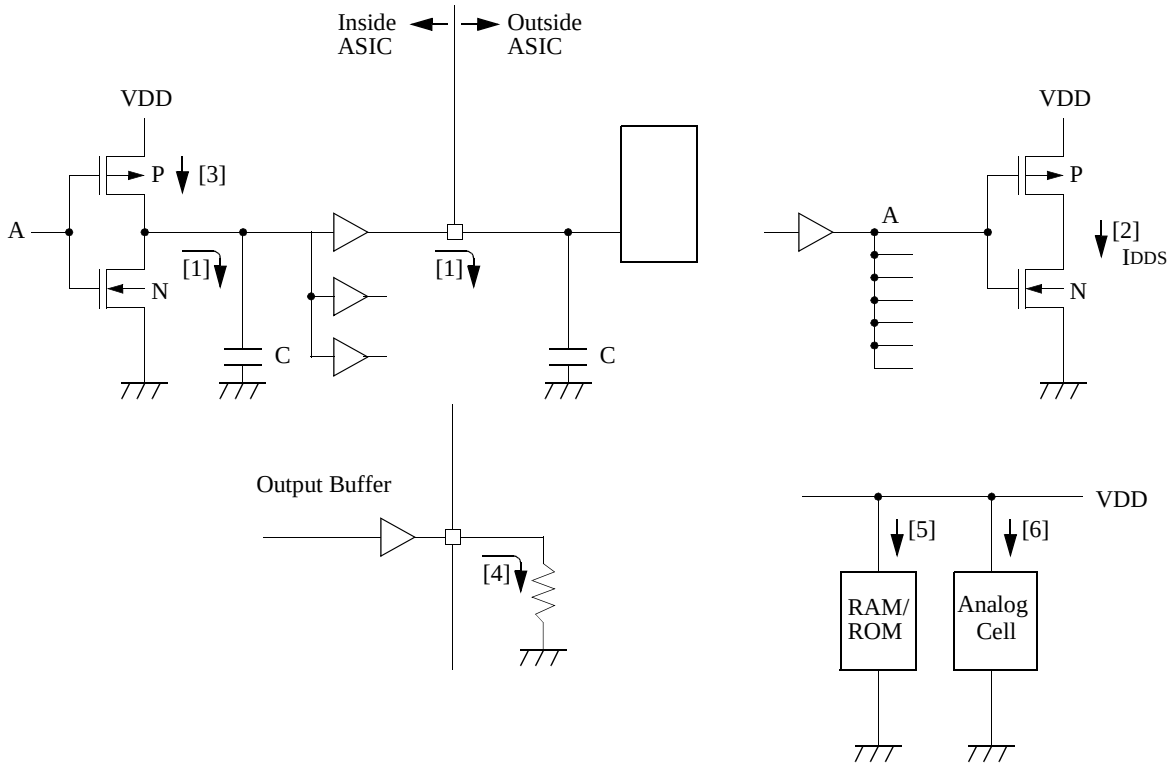
This chapter is organized as follows:

7.1 Causes of Power Dissipation in CMOS Circuits

Rules & Tips

- **Each design should be examined to see where and how power dissipation occurs. Logic designers must know the different types of power dissipation. In most, but not all, cases, a large majority of power is contributed by the charging and discharging of internal gates and output buffers.**

Figure 7-1 Power Dissipation in CMOS Circuits



The causes of power dissipation in CMOS technology are as follows:

1. *Switching power* — Known as “ac power dissipation,” this is power dissipated by the charging and discharging within the gates and as a result interconnect. It is essentially a function of the frequency of the logic switching. The charging of a capacitor (C) to a voltage (V) through a P-channel device builds up a charge (CV) and stores energy (CV to the 2nd power). This energy is later discharged through the N-channel device

paired with the P-channel device. When such switching takes place at a frequency (f), the resulting power dissipation can be expressed as $P=fCV^2$, where P is switching power. Switching power generally represents the majority of the overall power consumed.

2. *Overlap current* — Also known as "shoot-through leakage," overlap current occurs when the P- and N-channel transistors are switching from high to low or vice versa in the period when $V_{TH(N)} < V_{IN} < V_{DD} - V_{TH(P)}$, where V_{TH}=input threshold voltage, N=transistor, V_{IN}=input voltage, V_{DD}=supply voltage, and P=transistor.

   The Complementary MOS (CMOS) technology is made up of N- and P-channel transistors whose switching operation is complementary; that is, when N is on, P is off, and vice versa. In CMOS technology, both N- and P-channel transistors are on only for a brief time for input voltage transition from 0V to V_{DD}, or vice versa. Since at least one transistor is off when the element is in a steady state, very little dc current is consumed.

   However, the ramp rate of a gate becomes shallow as the load increases. As the ramp rate becomes more shallow, the driven gates spend more time in switching, where both N- and P-channel transistors are on, thus consuming excessive power as a result.

3. *Leakage dc current* — Leakage dc current continues to flow even when transistors are off. It is essentially a function of ASIC vendor's process. Leakage dc current in a properly functioning CMOS circuit is negligible (a few nano-ampere per gate).

4. *Static dc current* — Static dc current flow through ON transistors in I/O. This is normally negligible. When output buffers drive bipolar parts or other resistive load, however, power dissipation in I/O cells could increase.

5. RAM/ROM power — Memory elements such as RAMs and ROMs dissipate power during read and write operation.

6. Analog dc current

7.2 Early Chip Power Estimation

Rules & Tips

- **Early in the design phase, you will calculate the total power dissipation for the circuit, based on the number of gates, the number of output buffers, and the circuit's operating frequency. Ask Toshiba for memory power.**

This section describes a method for early power estimation for Toshiba ASIC chip designs. It is applied when an exact configuration of sequential logic has not been determined.

Equation for early power estimation is:

$$P_{total} = P_{logic} + P_{memory} + P_{IO} + P_{special} \quad (7.1)$$

where:

P_{total}:	Total power dissipated by the chip
P_{logic}:	Power dissipated by the internal logic
P_{memory}:	Power dissipated by memory cells
P_{IO}:	Power dissipated by I/O buffers
$P_{special}$:	Static power dissipated by special cells such as analog cells and GTL I/O with reference voltage source

Internal Logic

You will calculate the power requirement for the internal logic (P_{logic}), based on the number of gates and the operating frequency.

$$P_{logic} = G \times P_{gate} \times F \times SF \quad (7.2)$$

where:

G:	Gate count
P_{gate}:	Power dissipation per gate/MHz (see Table 7-1)
F:	Operating frequency (MHz).
SF:	Switching factor (0 to 1.0)

For a chip with partitions that run at different clock rates, a separate analysis is required for each partition. The switching factor (SF) is the most arbitrary number, which depends on the logic designer's ability to evaluate the average number of times that the circuit might switch in each cycle.

I/O Power

Equation for calculating I/O power (P_{IO}) is:

$$P_{IO} = P_{IOac} + P_{IOdc} \quad (7.3)$$

where:

- P_{IOac}: Switching power dissipated by output and output-mode bidirectional buffers
- P_{IOdc}: Power dissipated by leakage in input and input-mode bidirectional buffers with pull-up or pull-down

Classify the I/O buffers into functional groups, and solve the following equations (7.4) and (7.5) for each group. The total I/O power is obtained by the summation of these results. I/O power is primarily dependent on output pad loadings and the power supply voltage; it is not a function of the ASIC silicon technology used.

$$P_{IOac} = N_{out} \times P_{out} \times F \times SF \times C \quad (7.4)$$

- N_{out}: Number of output and bidirectional buffers in a group
- P_{out}: Power dissipation per IO/MHz/pF (see Table 7-1)
- F: Operating frequency (MHz)
- SF: Switching factor (0 to 1.0)
- C: Output capacitance (pF)

$$P_{IOdc} = N_{in} \times P_{leak} \times V \times SF \quad (7.5)$$

N_{in}:	Number of input and bidirectional buffers with pull-up or pull-down in a group
P_{leak}:	Power dissipated due to dc leakage per IO/MHz (see Table 7-1)
V:	Voltage swing (power supply voltage)
SF:	Switching factor (0 to 1.0)

The switching factor (SF) is an logic designer's estimate of the average number of times the input buffer is set to the logic level opposite to the pull resistance: "0" for pull-up, "1" for pull-down.

Memory Power

Toshiba ASICs offer more than ten types of memory cells, with thousands of bit/word organizations for each. Contact the Toshiba ASIC service group for the memory power requirement for your circuit. Memory power is the function of the following:

- Silicon technology (product series)
- Cell types (e.g., RAM-D)
- Organization (e.g., 256 x 8)
- Frequency of operation
- Switching factor estimate

Special Cells

For the power requirement for such cells as analog cells and GTL I/O, contact the Toshiba ASIC service group.

Table 7-1 Typical Power Dissipations

	Power Supply	Series	Pgate (mW/gate/MHz)	Pout (mW/IO/MHz/pF)	Pleak (mW/IO/MHz)
Gate Arrays	5V	TC160G	0.00515	0.025	0.070
		TC170G	0.00415	0.025	0.080
		TC190G	0.00361	0.025	0.080
	3.3V	TC160G	0.00230	0.011	0.070
		TC180G	0.00195	0.011	0.080
		TC200G	0.00155	0.011	0.050
		TC220G	0.00109	0.011	0.050
	3.3/5V	TC183G	0.00194	3.3-volt I/O: 0.011 5-volt I/O: 0.025	3.3-volt I/O: 0.050 5-volt I/O: 0.070
		TC203G	0.00154	3.3-volt I/O: 0.011 5-volt I/O: 0.025	3.3-volt I/O: 0.050 5-volt I/O: 0.075
Cell-Based ICs	5V	TC25SC	Data not available	0.025	Data not available
		TC26SC	0.00413	0.025	Data not available
		TC170C	0.00315	0.025	0.080
		TC190C	0.00229	0.025	0.080
	3.3V	TC180C	0.00143	0.011	0.080
		TC200C	0.00110	0.011	0.050
		TC220C	0.00069	0.011	0.050
	3.3/5V	TC183C	0.00141	3.3-volt I/O: 0.011 5-volt I/O: 0.025	3.3-volt I/O: 0.055 5-volt I/O: 0.075
		TC203C	0.00110	3.3-volt I/O: 0.011 5-volt I/O: 0.025	3.3-volt I/O: 0.055 5-volt I/O: 0.075
	2/3V	TC222C	Data not available	Data not available	Data not available
Embedded Arrays	5V	TC160E	0.00515	0.025	0.070
	3.3V	TC180E	0.00195	0.011	0.080
		TC200E	0.00155	0.011	0.050
		TC220E	0.00109	0.011	0.050
	3.3/5V	TC183E	0.00194	3.3-volt I/O: 0.011 5-volt I/O: 0.025	3.3-volt I/O: 0.050 5-volt I/O: 0.075
		TC203E	0.00154	3.3-volt I/O: 0.011 5-volt I/O: 0.025	3.3-volt I/O: 0.050 5-volt I/O: 0.075

* Switching power is proportional to the 2nd power of the supply voltage. For example, for 3.0V power supply, multiple the Pgate and Pout parameters by (3.0/3.3)2.

* Power dissipated due to dc leakage is proportional to the supply voltage. For example, for 3.0 V power supply, multiply the Pleak parameter by (3.0/3.3).

A power estimation work sheet is presented in Figure 7-2.

Figure 7-2 Power Estimation Work Sheet

Product Series	Series
Total Gate Count	gates

Internal (P_{logic})	# of Gates	P_{gate}	Frequency	Switching Factor	Power (mW)
Group A					
Group B					
Group C					
Group D					
Group E					
Group F					
Group G					
Group H					
Total					

External (P_{IOac})	(# of outputs) x (load)	P_{out}	Frequency	Switching Factor	Power (mW)
Group A					
Group B					
Group C					
Group D					
Group E					
Group F					
Group G					
Group H					
Total					

External (P_{IOdc})	# of inputs with pull resistor	P_{leak}	Voltage Swing	Switching Factor	Power (mW)
Group A					
Group B					
Group C					
Total					

Memory Power	mW
Special I/O Power	mW

Total Chip Power	**mW**

An example of a completed power estimation work sheet is shown in Figure 7-3.

Figure 7-3 Completed Power Estimation Work Sheet

Product Series	TC180G Series
Total Gate Count	36,000 gates

Internal (P_{logic})	# of Gates	P_{gate}	Frequency	Switching Factor	Power (mW)
Group A	7,000	0.00195	50	0.30	204.750
Group B	10,000	0.00195	25	0.30	146.250
Group C	12,000	0.00195	25	0.10	58.500
Group D	9,000	0.00195	10	0.01	1.755
Total (P_{core})					411.255

External (P_{IOac})	(# of outputs) x (load)	P_{out}	Frequency	Switching Factor	Power (mW)
Group A	4	0.0110	5	0.10	0.440
Group B	10	0.0110	50	0.20	22.000
Group C	32	0.0110	5	0.10	17.600
Total					40.040

External (P_{IOdc})	# of inputs with pull resistor	P_{leak}	Voltage Swing	Switching Factor	Power (mW)
Group A	10	0.080	3.3	0.50	1.320
Group B	8	0.080	3.3	0.50	1.056
Total					2.376

Total Chip Power	**453.671 mW**

7.3 Detailed Chip Power Estimation

Rules & Tips

- **Detailed power calculation is carried out by Toshiba. When you have completed a design, read the instructions in this section and prepare a Detailed Power Calculation Work Sheet presented in Figure 7-4.**

When you have completed a design, ask the Toshiba ASIC service group for detailed power estimation. Please take a few moments and prepare the Detailed Power Estimation Work Sheet in Figure 7-4. The procedure for detailed power calculations is applied after your design have been completed. In this procedure, the total power is obtained by the summation of the following items:

$$P_{total} = P_{clogic} + P_{slogic} + P_{clock} + P_{memory} + P_{IO} + P_{special} \quad (7.6)$$

where:

P_{total}:	Total power dissipated by the chip
P_{clogic}:	Power dissipated by the internal combinational logic
P_{slogic}:	Power dissipated by the internal sequential logic (i.e., flip-flops and latches)
P_{clock}:	Power dissipated by clock network circuitry
P_{memory}:	Power dissipated by memory cells
P_{IO}:	Power dissipated by I/Os
$P_{special}$:	Static power dissipated by special cells such as analog cells and GTL I/O with reference voltage source

- Combinational logic (P_{clogic})
  1. Partition the circuit into functional groups, and determine the number of gates required by each of the groups, ***not*** including flip-flops and latches.
  2. Provide the operating frequency per group.
  3. Estimate the switching factor per group, or the average number of gates that switch in each cycle.

The power parameter used in this sequence differ from that used in the early power estimation method.

- Sequential logic (P_{slogic})
  1. Partition the flip-flops and latches used in your design into functional groups, and provide their number per group.
  2. Provide the clock frequency per group.
  3. Estimate the switching factor per group.

- Clock network (P_{clock})

  Power dissipation in the clock network is calculated, using the sequential logic data as a basis.

- Memory (P_{memory})

  As is the case with the early power estimation, provide the memory type (e.g., RAM-D), organization (e.g., 256w x 8b), the frequency of operation, and the switching factor estimate.

- Output buffers (P_{IOac})
  1. Partition the output and output portions of bidirectional buffers into functional groups, and provide their number and the output load per group.
  2. Provide the frequency of operation per group.
  3. Estimate the switching factor per group.

- Input buffers with pull resistor (P_{IOdc})
  1. Partition the input and input portions of bidirectional buffers with pull-up or pull-down resistor into functional groups, and provide their number.
  2. Provide the voltage swing per group.
  3. Estimate the switching factor per group.

- Others

  The reference current that flows in the internal sense amp of ROM-A, GTL I/O, etc. causes excess power.

Figure 7-4 **Detailed Power Estimation Work Sheet**

(Fill in the sections surrounded by bold lines.)

Company Name:
Department & Section:
Engineer's Name:
Address:
Phone Number: ( ) - ( ) - ( ), Extension: ( )
Fax Number: ( ) - ( ) - ( )
E-mail Address:

Product Series: _____ Series
Base Array: _____
Part Number: _____
Supply Voltage: _____
Target Power: _____ mW

Combinational Logic (P_{clogic})	Gate Count	P_{comb}	Operating Frequency	Switching Factor	Power (mW)
Group A					
Group B					
Group C					
Group D					
Group E					
Group F					
Group G					
Group H					
Total					mW

Sequential Logic (P_{slogic})	# of Flip-Flops and Latches	P_{cp}	P_{seq}	Clock Frequency	Switching Factor	Power (mW)
Group A						
Group B						
Group C						
Group D						
Group E						
Group F						
Group G						
Group H						
Total						mW

Clock Network (P_{clock})	# of Flip-Flops and Latches	P_{cline}	P_{seq}	Clock Frequency	Power (mW)
Group A					
Group B					
Group C					
Group D					
Group E					
Group F					
Group G					
Group H					
Total					mW

Memory (P_{memory}) Type & Organization	Qty.	P_{ram}/MHz	Voltage Swing	Operating Frequency	Switching Factor	Power (mW)
Total						mW

Output Buffers (P_{IOac})	# of outputs	Load	P_{out}	Frequency	Switching Factor	Power (mW)
Group A						
Group B						
Group C						
Group D						
Group E						
Group F						
Group G						
Group H						
Total						mW

Input Buffers with Pull Resistor (P_{PODc})	# of inputs with pull resistor	P_{leak}	Voltage Swing	Switching Factor	Power (mW)
Group A					
Group B					
Group C					
Total					mW

Others	(e.g., ROM-A sense amp, GTL I/O)	mW

Total Chip Power	**mW**

7.4 Power Simulation

Rules & Tips

- **After layout, power simulation can be executed, using an at-speed test.**

The Toshiba VLCAD and Verilog-XL Sign-off (VSO) System offer power calculators, which use the results of logic simulation to compute power dissipation in Toshiba ASICs. They print a histogram of specified time intervals showing dynamic (or chronological) changes of circuit's power dissipation during simulation. Histograms use different characters or colors to depict different causes of power dissipation.

Required Input

The following data is required to run power simulation.

- Netlists

  Netlists can be either Toshiba TDL or Verilog-HDL format. They must be gate-level descriptions.

- Output load specifications

  Output load specifications must include capacitance loadings on output and bidirectional pins as well as the types of capacitive loads of the driven devices (CMOS or TTL).

- Physical design information

  An actual wirelength data file generated by a layout system and the Toshiba Clock Tree Synthesizer (TCTS) procesing information are required.

- Test data

  Since the power calculator makes power estimation based on the simulation behavior of the circuit, an at-speed test is required.

Precautions

- Although the power calculator can be executed anytime after logic simulation, it should be run after layout using actual wirelength data as input to ensure accurate results. Since clock networks contribute a sizable

percentage of the overall power dissipation, the power calculator computes power dissipation in clock networks and the other part of the circuit separately. When calculating power dissipation in clock networks, the power calculator considers the processing done by TCTS.

- Since the power calculator makes power estimations based on the circuit's behavior during simulation, you should submit the results of a simulation run with an at-speed at.
- The power calculation results could have an error of 20 to 30%. Remember that the power calculator only gives you a ballpark estimate of the circuit's power dissipation; it does not give a definitive measure of power dissipation. This is mainly because creating test patterns, especially for large designs, that accurately reflect the actual circuit's behavior is not always an easy task. Most of the time, simulation is performed block by block and focused on a limited function of the circuit. It is sometimes virtually impossible to generate simulation test patterns that sensitize and identify all circuit paths. In addition, library characterization, TCTS settings, and external load settings all contribute to an error in power estimation.
- For now, the power calculator is provided in the Toshiba VLCAD and Verilog-XL Sign-off (VSO) environments.

Appendix A

Initial Specifications Form

(Request for Quotation)

Initial Specifications Form

(Request for Quotation)

Date:

The purpose of this form is to collect all information needed by Toshiba to carry out rapid technical assessment of your ASIC requirement. This assessment helps us to recommend to you the best ASIC solution. Because estimates are used, the Initial Specifications Form is treated as only a guiding document.

All information supplied will be treated as confidential and will not be disclosed outside the departments concerned of Toshiba without your written consent.

Customer Information

Company Name:
Department & Section:
Engineer's Name:
Address:
Phone Number: ( ) - ( ) - ( ), Extension: ( )
Fax Number: ( ) - ( ) - ( )
E-mail Address:

I. Circuit Details

† Please give the usage and functional description of the circuit being planned.
Usage:

Functional description:

† Average service hours per day: _____ hrs.

† Is this a new design or a refinement of an existing design?

◊ New design
Have you breadboarded your design for evaluation?
◊ Yes, ◊ Evaluating now, ◊ No

◊ Refinement of an existing design with Toshiba

◊ Refinement of an existing design with another manufacturer

† Which product series do you favor?
(See Chapter 2, Choosing a Device and a Package.)

TC _____ Series
◊ No particular series favored

† Power supplies

◊ 4.75 - 5.25V, ◊ 3.0 - 3.6V, ◊ 2.7 - 3.3V
◊ 4.75 - 5.25V / 3.0 - 3.6V mixed, ◊ 4.75 - 5.25V / 2.7- 3.3V mixed, ◊ 1.8 - 2.2V / 2.7-3.3V mixed
◊ Other V_{DD} = _____ ~_____ V

† Ambient temperature (T_a)

T_a = _____ ~ _____ degrees C
Average ambient temperature: _____ degrees C
Cooling method: ◊ Natural air flow, ◊ Active cooling: _____ m/s
◊ Other _____

† Random logic blocks: _____ gates

† Memory blocks:

RAM / ROM, sync / async, ____ ports, _____ words by _____ bits, _____ blocks
RAM / ROM, sync / async, ____ ports, _____ words by _____ bits, _____ blocks
RAM / ROM, sync / async, ____ ports, _____ words by _____ bits, _____ blocks
RAM / ROM, sync / async, ____ ports, _____ words by _____ bits, _____ blocks
RAM / ROM, sync / async, ____ ports, _____ words by _____ bits, _____ blocks
RAM / ROM, sync / async, ____ ports, _____ words by _____ bits, _____ blocks

† Other specialized megacells

e.g.) 16x16 multiplier, 8251, and 8-bit A/D converter apiece

_____
_____
_____
_____

† Operating frequency

Maximum _____ MHz, Average: _____ MHz

† Does your design contain an oscillator circuit?
(See Section 4.10, Oscillator Cells, on page 4-140.*)*

◊ No
◊ If yes, what type is it?
◊ Crystal, ◊ Ceramic, ◊ C.R.
Oscillating frequency: _____ MHz

† Do you have any critical path specifications?

◊ Yes, ◊ No

If yes, please supply its information.

† Interfacing ICs
(See Section 4.2.6, Chip-to-Chip Interface, on page 4-28.*)*

Inputs: ◊ TTL, ◊ LVTTL, ◊ CMOS
◊ GTL, ◊ 5-volt PCI, ◊ 3-volt PCI, ◊ LVDS
◊ Other: _____

Outputs: ◊ TTL, ◊ LVTTL, ◊ CMOS
◊ GTL, ◊ 5-volt PCI, ◊ 3-volt PCI, ◊ LVDS
◊ Other: _____

† Number of simultaneously-switching outputs
(See Section 4.3.2, Simultaneously Switching I/Os, on page 4-38.*)*

Group 1 _____ mA x _____ output pins
_____ mA x _____ output pins
_____ mA x _____ output pins
Group 2 _____ mA x _____ output pins
_____ mA x _____ output pins
_____ mA x _____ output pins
Group 3 _____ mA x _____ output pins
_____ mA x _____ output pins
_____ mA x _____ output pins

† Number of I/O pins

Total: _____

Inputs: _____, Outputs: _____, Bidirects: _____

† Preferred package type

◊ DIP, ◊ QFJ (PLCC), ◊ PGA, ◊ (QTP) TCP, ◊ BGA, ◊ CSP

◊ QFP - Any dimensions requirements?

◊ No

◊ Yes, Mounting height: _____ mm, Lead pitch: _____ mm

† Soldering method

◊ Localized heating:

◊ Soldering iron, ◊ Pulse heater, ◊ Hot air, ◊Laser

◊ Overall heating:

◊ Infrared reflow, ◊ Vapor phase reflow, ◊ Solder dipping

◊ Other _____

† Are the Toshiba standard (fixed) VDD/VSS pin locations acceptable? *(See Section 4.3.1, Power and Ground Pins,* on page 4-36*.)*

◊ Yes, ◊ No

If no, why? _____

_____

† Is the Toshiba standard part marking acceptable for production devices? *(See Section 3.2, Formal Milestone Documents,* on page 3-6*, and Section 3.8, Prototype and Production Parts,* on page 3-18*.)*

◊ Yes, ◊ No

II. Development

† Customer interface level *(See Section 3.3, Customer Interface Levels,* on page 3-8*.)*

◊ Level 1:Schematic diagrams and unsimulated test data
◊ Level 3:Preliminary simulation using the customer's tools
◊ Level 4:Mask data generation
◊ Other:_____

† EDA tool(s)

EDA Tool	Too Version	Hardware Platform	Operating System (Version)

† Development timescale and projected prototype requirements
(See Section 3.8, Prototype and Production Parts, on page 3-18*.)*

Prototypes and Production	Date	Quantity
Selection of your ASIC partner		—
KS (plastic)		10
ES (ceramic)		
HS (plastic)		
Initial production (including risk start)		
Projected production		/month /year /product's life

† If you have any special circuit specifications, please use the space provided.

_____

_____

_____

_____

III. Quotations

If you have no objection to telling, please supply the following information.

† Did you request quotation of other ASIC vendors?

◊ No (only Toshiba)

◊ Yes

_____ Corp./Inc., _____ Corp./Inc.
_____ Corp./Inc., _____ Corp./Inc.

† Please give the priority order in choosing your ASIC partner.

____ Development cost: Target cost U.S.$ _____

____ Unit cost: Target cost U.S.$ _____

____ Development schedule

____ Development support

____ Other _____

Appendix B

Design Release Checklist

Design Release Checklist

Date:

Customer Information

Company Name:
Department & Section:
Engineer's Name:
Address:
Phone Number: ( ) - ( ) - ( ), Extension: ( )
Fax Number: ( ) - ( ) - ( )
E-mail Address:

I. Design Name (Top Module)

_____

II. Design Kit Information

- EDA tool _____, Version _____
- Design kit version _____
- Array family _____ (e.g. TC180G)
- Array type _____ (e.g. T9T83)

III. Design Details

† Operating Frequency
- Maximum _____ MHz, Average _____ MHz

- List the types and numbers of megacells, megafunctions, and oscillator cells used.

Cell Name	Organization	Number	Test Logic Style
RAM-A	256w x 8b	2	Toshiba standard
OSC4C	Crystal oscillator, 20 MHz	1	My own style

† Design-for-reliability rules

◊ Does your design NOT contain circuits prohibited in Section 4.7.1 (namely, ring oscillators, one-shot circuits, chopper circuits, hazard circuits, and cross-coupled gates)?

† Critical paths

Does your design have timing critical paths?
If yes, describe. _____

◊ Yes, ◊ No

If yes, describe. _____

_____

_____

_____

† Clock signals

♦ List clock signals below.

Net Name	Purpose	Frequency	Fanout (LU)	Driving Cell	Remark
CLK1	External input	48 MHz	Approx. 500	DRVT4	
CLK2	Internal divided clock	24 MHz	870	3x YCBUFP	

♦ Did you design your circuit so that possible clock skew problems can be avoided?

◊ Yes, ◊ No

If yes, describe. If no, explain why. _____

_____

_____

* Clock skew preventions are a must regardless of the circuit's operating frequency, or even when pre-layout simulation does not show any problems.

† Reset signals

♦ List reset signals below.

Net Name	Purpose	Sync/Async	Fanout (LU)	Driving Cell	Remark
XRESET	External input	Asynchronous	100	TLCHTU	

† Asynchronous circuits

♦ Does your design have asynchronous circuits?

◊ Yes, ◊ No

If yes, describe. _____

_____

_____

_____

♦ Do you have any special layout specifications (e.g., critical nets, soft cell grouping)?

◊ Yes, ◊ No

If yes, use the form attached.

* Not all specifications can be implemented due to layout constraints.

† Power estimate _____ mW

† Preferred pinout

Complete the Pinout Plan attached at the end of the Design Release Checklist. (You can create one with a text editor, word processor, or spreadsheet program.) Example:

Pin #	Pin Name	Direction	Buffer Type	Interface	Load	SSIs/SSOs	Frequency
1	VSS						
2	CLK16M	OUT	B8	CMOS	60 pF		16 MHz
3	ALE	IN	TLCHTU	TTL			
4	DBUS0	BID	BD4TU	CMOS	40 pF	A	
5	DBUS1	BID	BD4TU	CMOS	40 pF	A	
6	DBUS2	BID	BD4TU	CMOS	40 pF	A	

*Partition simultaneously-switching inputs (SSIs) and outputs (SSOs) into groups, and give them a label: A, B, C, and so on.

* Make copies of the attached sheets if you design has more than 100 pins.

IV. Design Verification

◊ Did you execute the Design Verifier program with no errors?

♦ Give the number of I/O pins below.
Total _____ Inputs _____, Outputs _____, Bidirects _____

♦ Give the gate count of your design and gate usage percentage below.
Gate (grid) count _____
Gate (grid) usage _____ % (including blocks)

V. Test Data Files for Automatic Tester Runs

◊ Did you ensure that all your test data files to be used for device testing meet all the tester timing constraints?

◊ Did you execute the Delay Calculator program, with the output load parameters set to 85pF, TTL for 5V output buffers and 85pF, LVTTL for 3V output buffers?

◊ Give the K-factors used below.
Best-case _____, Nominal _____, Worst-case _____

◊ Did you run best-case, worst-case, and nominal-case simulations on every test data file, and ensure that the steady state results of all three cases of simulations match?

◊ Did you ensure that strobe margins were greater than stipulated (see Section 5.3.4, *Strobe Margins*, on page 5-14)?

◊ Did you ensure that there were no external bidirectional pin conflicts?

◊ Did you ensure that there were no signal conflicts or floats on internal 3-state buses, except for those that occurred due to signal delays, lasting only briefly?

Did you ensure that the DC/I_{DDS} pattern meets the requirements for dc measurements to take place? If there are any I/O pins for which dc test requirements can not be satisfied, write them in the space provided. _____

_____

_____

◊ Did you ensure that the high-impedance functional pattern can put all 3-state and bidirectional lines in the high-impedance states?

♦ Do you want a megacell/megafunction test data created by Toshiba?

◊ Yes, ◊ No

If yes, give the I/O pin states that provide direct access to each of the megacells and megafunctions. _____

_____

_____

* For megacells or megafunctions that are not directly accessible from I/O pins, test patterns need be prepared by you, the designer.

◊ Do all your test data files to be run on the tester abide by the test step restrictions?

♦ If your design has an oscillator cell, did you insert a Toshiba-recommended test logic to your design?

◊ Yes, ◊ No

VI. At-Speed Test Data File

◊ Did you specify the actual output load parameters when you executed the Delay Calculator program?

* Complete the Pinout Plan attached at the end of the Design Release Checklist. When you created a pad load specification file, give its file name. _____

◊ Did you run best-case, worst-case, and nominal-case simulations, and ensure that the circuit works to specifications?

◊ Did you ensure that the steady state results of all three cases of simulations match?

◊ Did you check the timing behavior of internal circuit nodes?

If you have any comment, please use the space provided. _____
_____
_____
_____
_____

VII. Test Data File List

♦ Give the total number of test data files _____

♦ Give the total steps of test patterns (after expansion) _____

♦ Complete the Test Data File List below. You can create one with a text editor, word processor, or spreadsheet program.

Test Data Files

	File Name	# of Patterns	Test Cycle	Usage	Purpose
e.g.	FUNC.TSL	3,750	200 ns	FC	Counter verification
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
20					

* Use the following abbreviations in the Usage column:

FC: Functional test data
DC: DC/IDDS test data
Hz: High-impedance functional test data
SP: At-speed test data

VIII. Design Release Package

Check to see that your design release package includes the following for reverification and layout release.

† Magnetic medium

◊ 3.5” floppy disks (OS: _____) Quantity _____

◊ 1/4” tape cartridge (OS: _____) Quantity _____

◊ 8 mm tape cartridge (OS: _____) Quantity _____

◊ DAT (OS: _____) Quantity _____

◊ Other _____

* Please attach a hardcopy of the file list.

† Required files

◊ TDL-format netlist file(s)

◊ TSTL2-format test data files

◊ Pad load specification file

◊ Report files generated by the Simulation Results Verifier program (such as SRV)

* SRV report files produced for the best-case, worst-case, and nominal-case of simulations should be filed under the following file names for functional, DC/IDDS, and high-impedance functional tests.

xxxyyy.SRV

where: *xxx* is a string representing a delay case or a user-specified K-factor (e.g., WST, 186), and *yyy* is a test data name.

◊ Report file generated by the Design Verifier program (such as TDVER)

◊ Toshiba-format ROM data file (when your design has ROMs)

† Other design materials

◊ Hardcopy of schematic diagrams (Paper size: _____, Number of sheets: _____)

◊ Your preferred pinout

◊ Your preferred part marking diagram

• If you have any comment, please use the space provided.

_____

_____

_____

Special Layout Specifications

(See Section 3.7, *Special Layout Specifications*, on page 3-16.)

I. Critical Paths

Source Pin	Destination Pin	Maximum Delay (at worst-case)	Minimum Delay (at best-case)
External input DATA	External output OUT	20.0 ns	10.0 ns
F/F input I001/I0014(CP)	F/F input I010/I002(D)	10.0 ns	—

II. Preferred Soft Cell Grouping

Please consult with your Toshiba Design Center engineer.

e.g. Group internal cells of three instances of module SUB1: I001/I0014, I001/I0015, and I0001/I0016

_____

_____

_____

_____

_____

_____

- Comment

_____

_____

_____

_____

Pinout Plan (/)

Pin #	Pin Name	Direction	Buffer Type	Interface	Load	SSIs/SSOs	Frequency
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
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16							
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34							
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37							
38							
39							
40							
41							
42							
43							
44							
45							
46							
47							
48							
49							
50							

* You can create a pinout table as a computer file with a text editor, word processor, or spreadsheet program.

Pinout Plan (/)

Pin #	Pin Name	Direction	Buffer Type	Interface	Load	SSIs/SSOs	Frequency
51							
52							
53							
54							
55							
56							
57							
58							
59							
60							
61							
62							
63							
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87							
88							
89							
90							
91							
92							
93							
94							
95							
96							
97							
98							
99							
100							

Appendix C

Design Kit Request Forms

Design Kit Request

Date:

Customer Information

Company Name:
Department & Section:
Engineer's Name:
Address:
Phone Number: ( ) - ( ) - ( ), Extension: ( )
Fax Number: ( ) - ( ) - ( )
E-mail Address:

- EDA tool _____, Version _____
- Hardware platform _____ (e.g. Sun-4)
- Operating system _____, Version _____ (e.g. SunOS 4.1.3)
- Desired magnetic medium _____ (e.g. 1/4" tape cartridge)
- Array family _____ (e.g. TC180G)
- Metal layers ◊ 2 ◊ 3
- Power supply: I/O ◊ 5V ◊ 3.3V
  Core ◊ 5V ◊ 3.3V
- Operating conditions (K-factors)

	Temperature	Power supply	K-factor
Best-case	_____	_____	_____
Nominal	_____	_____	_____
Worst-case	_____	_____	_____

- Desired cells

Cell Type	Words x Bits	Rows x Columns*	Aspect Type*	Quantity

*To be filled in by Toshiba.

- Delivery date _____
- Comment

Problem Report Form

Date:

From:

Company Name:
Department & Section:
Engineer's Name:
Address:
Phone Number: ( ) - ( ) - ( ), Extension: ( )
Fax Number: ( ) - ( ) - ( )
E-mail Address:

To: _____

- EDA tool _____, Version _____
- Hardware platform _____ (e.g. Sun-4)
- Operating system _____, Version _____ (e.g. SunOS 4.1.3)
- Array family _____ (e.g. TC180G)
- Library package version _____
- Program _____, Version _____

  VLCAD and VSO print the program version at the beginning of execution. On other systems, you can generate the program version by entering the command without any options.

- Problem Description

- Materials Attached
  - Execution listing
  - Error message listing
  - Environment variable listing (printed with the MS-DOS `SET` command or UNIX `setenv` command)

Appendix D

Toshiba ASIC Product Lines

- The actual number of usable gates will depend on the type of logic design (regular vs. random) and the types and numbers of cells used, and may be more or less than indicated.
- With embedded arrays, usable gates are estimated, based on a random-logic-only design. The actual number of usable gates will depend on the type of logic design (regular vs. random) and the types and number of cells used, and may be more or less than indicated.
- Some I/O pads must be configured as VDD/VSS, depending on the number and drive of simultaneously-switching I/Os.
- In devices with 3V/5V dual I/O options, eight dedicated 5-volt power pads are peassigned. 3-volt power pads must be configured at the expense of I/O pads. Additional I/O pads may be configured as VDD/VSS, depending on the number and drive of simultaneously-switching I/Os.

3V

GA

Table D-1 TC220G Series Gate Array Product Outline

Double-Layer Metal			Triple-Layer Metal			Raw Gates	Max I/O Pads		
Part Number	Array Desig.[1)]	Usable Gates	Part Number	Array Desig.[1)]	Usable Gates		Wire Bond	TCP TBGA[2)]	PQFP[TAB] TBGA[3)]
TC220G42	T3S57	1,110,000	TC220G92	T3T57	1,934,000	3,170,070	512	768	—
TC220G40	T3S56	791,000	TC220G90	T3T56	1,378,000	2,259,600	432	648	—
TC220G36	T3S55	625,000	TC220G86	T3T55	1,090,000	1,786,824	384	576	—
TC220G32	T3S54	479,000	TC220G82	T3T54	835,000	1,386,168	336	504	—
TC220G24	T3S53	342,000	TC220G74	T3T53	593,000	898,880	272	408	548
TC220G20	T3S52	66,000	TC220G70	T3T52	462,000	700,128	240	360	484
TC220G16	T3S51	221,000	TC220G66	T3T51	385,000	526,988	208	312	420
TC220G14	T3S50	181,000	TC220G64	T3T50	315,000	430,858	192	284	380
TC220G12	T3S48	152,000	TC220G62	T3T48	267,000	360,864	176	260	348
TC220G10	T3S47	125,000	TC220G60	T3T47	220,000	297,680	160	236	316
TC220G08	T3S46	103,000	TC220G58	T3T46	182,000	245,976	144	212	288
TC220G06	T3S45	82,000	TC220G56	T3T45	144,000	182,596	128	184	248

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T8”.
3) Array designators are followed by the suffix “T6”.

Table D-2 TC200G Series Gate Array Product Outline

Double-Layer Metal			Triple-Layer Metal			Raw Gates	Max I/O Pads		
Part Number	Array Desig.[1)]	Usable Gates	Part Number	Array Desig.[1)]	Usable Gates		Wire Bond	TCP TBGA[2)]	PQFP[TAB] TBGA[3)]
TC200G42	T9V67	404,000	TC200G92	T9W67	704,000	1,154,200	512	776	—
TC200G40	T9V66	288,000	TC200G90	T9W66	503,000	824,180	432	656	—
TC200G36	T9V65	228,000	TC200G86	T9W65	398,000	652,256	384	584	—
TC200G32	T9V64	175,000	TC200G82	T9W64	306,000	501,184	336	512	—
TC200G24	T9V63	125,000	TC200G74	T9W63	218,000	329,840	272	416	556
TC200G20	T9V62	98,000	TC200G70	T9W62	170,000	257,560	240	368	492
TC200G16	T9V61	82,000	TC200G66	T9W61	142,000	194,684	208	320	428
TC200G14	T9V60	67,000	TC200G64	T9W60	117,000	159,840	192	292	388
TC200G12	T9V58	56,000	TC200G62	T9W58	98,000	134,244	176	268	356
TC200G10	T9V57	47,000	TC200G60	T9W57	81,000	110,880	160	244	324
TC200G08	T9V56	39,000	TC200G58	T9W56	67,000	92,168	144	220	296
TC200G06	T9V55	31,000	TC200G56	T9W55	53,000	68,526	128	192	256
TC200G04	T9V54	22,000	TC200G54	T9W54	38,000	44,916	104	156	208
TC200G02	T9V53	13,000	TC200G52	T9W53	22,000	26,100	80	120	160

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T8”.
3) Array designators are followed by the suffix “T6”.

3V
GA

Table D-3 TC180G Series Gate Array Product Outline

Double-Layer Metal			Triple-Layer Metal			Raw Gates	Max I/O Pads	
Part Number	Array Designator[1)]	Usable Gates	Part Number	Array Designator[1)]	Usable Gates		Wire Bonding	TCP PQFP[TAB][2)]
TC180GJ4	T9T92	194,000	TC180GT1	T9U92	340,000	485,040	416	652
TC180GF1	T9T91	151,000	TC180GT2	T9U91	264,000	377,816	368	576
TC180GB3	T9T90	113,000	TC180GT3	T9U90	199,000	283,968	320	500
TC180G84	T9T89	84,000	TC180GT4	T9U89	148,000	211,296	280	432
TC180G70	T9T88	70,000	TC180GT5	T9U88	122,000	173,700	256	392
TC180G45	T9T86	45,000	TC180GT6	T9U86	79,000	112,220	208	316
TC180G35	T9T85	35,000	TC180GT7	T9U85	61,000	87,680	184	280
TC180G26	T9T84	26,000	TC180GT8	T9U84	47,000	66,442	160	244
TC180G21	T9T83	21,000	TC180GT9	T9U83	38,000	53,750	144	220

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T”.

5V

GA

Table D-4 TC190G Series Gate Array Product Outline

Double-Layer Metal			Triple-Layer Metal			Raw Gates	Max I/O Pads		
Part Number	Array Desig.[1)]	Usable Gates	Part Number	Array Desig.[1)]	Usable Gates		Wire Bond	TCP TBGA[2)]	PQFP[TAB] TBGA[3)]
TC190G42	T9V87	404,000	TC190G92	T9W87	704,000	1,154,200	512	776	—
TC190G40	T9V86	288,000	TC190G90	T9W86	503,000	824,180	432	656	—
TC190G36	T9V85	228,000	TC190G86	T9W85	398,000	652,256	384	584	—
TC190G32	T9V84	175,000	TC190G82	T9W84	306,000	501,184	336	512	—
TC190G24	T9V83	125,000	TC190G74	T9W83	218,000	329,840	272	416	556
TC190G20	T9V82	98,000	TC190G70	T9W82	170,000	257,560	240	368	492
TC190G16	T9V81	82,000	TC190G66	T9W81	142,000	194,684	208	320	428
TC190G14	T9V80	67,000	TC190G64	T9W80	117,000	159,840	192	292	388
TC190G12	T9V78	56,000	TC190G62	T9W78	98,000	134,244	176	268	356
TC190G10	T9V77	47,000	TC190G60	T9W77	81,000	110,880	160	244	324
TC190G08	T9V76	39,000	TC190G58	T9W76	67,000	92,168	144	220	296
TC190G06	T9V75	31,000	TC190G56	T9W75	53,000	68,526	128	192	256
TC190G04	T9V74	22,000	TC190G54	T9W74	38,000	44,916	104	156	208
TC190G02	T9V73	13,000	TC190G52	T9W73	22,000	26,100	80	120	160

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T8”.
3) Array designators are followed by the suffix “T6”.

5V

GA

Table D-5 TC170G Series Gate Array Product Outline

Double-Layer Metal			Triple-Layer Metal			Raw Gates	Max I/O Pads	
Part Number	Array Designator[1)]	Usable Gates	Part Number	Array Designator[1)]	Usable Gates		Wire Bonding	TCP PQFP[TAB][2)]
TC170GJ4	T9T52	194,000	TC170GT1	T9U52	340,000	485,040	416	652
TC170GF1	T9T51	151,000	TC170GT2	T9U51	264,000	377,816	368	576
TC170GB3	T9T50	113,000	TC170GT3	T9U50	199,000	283,968	320	500
TC170G84	T9T49	84,000	TC170GT4	T9U49	148,000	211,296	280	432
TC170G70	T9T48	70,000	TC170GT5	T9U48	122,000	173,700	256	392
TC170G45	T9T46	45,000	TC170GT6	T9U46	79,000	112,220	208	316
TC170G35	T9T45	35,000	TC170GT7	T9U45	61,000	87,680	184	280
TC170G26	T9T44	26,000	TC170GT8	T9U44	47,000	66,442	160	244
TC170G21	T9T43	21,000	TC170GT9	T9U43	38,000	53,750	144	220

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T”.

Table D-6 TC160G Series Gate Array Product Outline

Double-Layer Metal			Triple-Layer Metal			Raw Gates	Max I/O Pads	
Part Number	Array Designator[1)]	Usable Gates	Part Number	Array Designator[1)]	Usable Gates		Wire Bonding	TCP PQFP[TAB][2)]
TC160GU2	T3D59	120,000	TC160GT1	T3E59	210,000	302,346	416	652
TC160GN5	T3D58	94,000	TC160GT2	T3E58	164,000	235,276	368	576
TC160GH7	T3D57	71,000				176,606	320	500
TC160GD2	T3D56	53,000				131,712	280	432
TC160GA8	T3D55	43,000				108,224	256	392
TC160G70	T3D53	28,000				70,070	208	316
TC160G54	T3D51	22,000				54,432	184	280
TC160G41	T3D49	17,000				41,360	160	244
TC160G33	T3D47	13,000				33,462	144	220
TC160G22	T3D46	9,000				22,356	120	—
TC160G16	T3D45	6,000				15,946	102	—
TC160G11	T3D43	4,000				10,640	84	—

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T”.

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Table D-7 TC140G Series Gate Array Product Outline

Part Number	Array Designator[1)]	Usable Gates	Raw Gates	Max I/O Pads	
				Wire Bonding	TCP PQFP[TAB][2)]
TC140GH2	T3D19	68,000	172,032	360	—
TC140GC8	T3D17	51,000	128,816	312	—
TC140G89	T3D16	35,000	89,194	260	—
TC140G68	T3D15	27,000	68,244	228	342
TC140G54	T3D14	21,000	54,684	204	306
TC140G44	T3D13	17,000	44,460	184	276
TC140G37	T3D12	15,000	37,024	168	252
TC140G27	T3D10	11,000	27,056	144	216
TC140G18	T3D09	7,500	18,796	120	—
TC140G12	T3D07	5,100	12,810	100	—
TC140G09	T3D05	3,600	8,976	84	—
TC140G06	T3D03	2,300	5,822	68	—
TC140G04	T3D02	1,800	4,464	60	—
TC140G02	T3D01	1,000	2,340	44	—

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T”.

5V

Table D-8 TC14L Series Gate Array Product Outline

Double-Layer Metal		Triple-Layer Metal		Max I/O Pads
Part Number	Usable Gates	Part Number	Usable Gates	
TC14L120	12,000	TC14L200	20,000	208
TC14L100	10,000	TC14L150	15,000	208
TC14L080	8,000			208
TC14L070	7,000			176
TC14L060	6,000			176
TC14L050	5,000			160
TC14L040	4,000			160
TC14L020	2,100			100
TC14L010	1,000			100

Table D-9 TC11L Series Gate Array Product Outline

Double-Layer Metal		Max I/O Pads
Part Number	Usable Gates	
TC11L007	700	44
TC11L005	500	44
TC11L003	300	44

- Ask your Toshiba Design Center engineer for array designators.

3V/5V

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Table D-10 TC203G Series Gate Array Product Outline

Double-Layer Metal			Triple-Layer Metal			Raw Gates	Max I/O Pads		
Part Number	Array Desig.[1)]	Usable Gates	Part Number	Array Desig.[1)]	Usable Gates		Wire Bond	TCP TBGA[2)]	PQFP[TAB] TBGA[3)]
TC203G42	T9X97	398,000	TC203G92	T9Y97	694,000	1,138,176	504	768	—
TC203G40	T9X96	284,000	TC203G90	T9Y96	494,000	810,648	424	648	—
TC203G36	T9X95	224,000	TC203G86	T9Y95	391,000	640,224	376	576	—
TC203G32	T9X94	171,000	TC203G82	T9Y94	299,000	489,888	328	504	—
TC203G24	T9X93	122,000	TC203G74	T9Y93	212,000	321,300	264	408	—
TC203G20	T9X92	95,000	TC203G70	T9Y92	165,000	250,020	232	360	—
TC203G16	T9X91	79,000	TC203G66	T9Y91	137,000	188,136	200	312	420
TC203G14	T9X90	65,000	TC203G64	T9Y90	112,000	153,912	184	284	380
TC203G12	T9X88	54,000	TC203G62	T9Y88	95,000	128,816	168	260	348
TC203G10	T9X87	44,000	TC203G60	T9Y87	78,000	105,952	152	236	316
TC203G08	T9X86	37,000	TC203G58	T9Y86	65,000	87,680	136	212	288
TC203G06	T9X85	29,000	TC203G56	T9Y85	51,000	64,664	120	184	248
TC203G04	T9X84	19,000	TC203G54	T9Y84	35,000	41,580	96	148	200

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T8”.
3) Array designators are followed by the suffix “T6”.

3V/5V

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Table D-11 TC183G Series Gate Array Product Outline

Double-Layer Metal			Triple-Layer Metal			Raw Gates	Max I/O Pads	
Part Number	Array Designator[1)]	Usable Gates	Part Number	Array Designator[1)]	Usable Gates		Wire Bonding	TCP PQFP[TAB][2)]
TC183GJ0	T9T72	180,000	TC183GT1	T9U72	315,000	449,604	400	628
TC183GD9	T9T71	139,000	TC183GT2	T9U71	243,000	347,256	352	552
TC183GA3	T9T70	103,000	TC183GT3	T9U70	180,000	257,560	304	476
TC183G75	T9T69	75,000	TC183GT4	T9U69	132,000	188,136	264	408
TC183G61	T9T68	61,000	TC183GT5	T9U68	107,000	152,764	240	368
TC183G38	T9T66	38,000	TC183GT6	T9U66	67,000	95,858	192	292
TC183G29	T9T65	29,000	TC183GT7	T9U65	51,000	73,292	168	256
TC183G22	T9T64	22,000	TC183GT8	T9U64	38,000	53,750	144	220
TC183G17	T9T63	17,000	TC183GT9	T9U63	30,000	42,402	128	196

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T”.

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Table D-12 TC163G Series Gate Array Product Outline

Double-Layer Metal			Triple-Layer Metal			Raw Gates	Max I/O Pads	
Part Number	Array Designator[1)]	Usable Gates	Part Number	Array Designator[1)]	Usable Gates		Wire Bonding	TCP, PQFP[TAB][2)]
TC163GS0	T3D79	112,000	TC163GT1	T3E79	196,000	280,280	400	—
TC163GL6	T3D78	87,000	TC163GT2	T3E78	151,000	216,362	352	—
TC163GG0	T3D77	64,000				160,272	304	476
TC163GB7	T3D76	47,000				117,290	264	408
TC163G95	T3D75	38,000				95,524	240	368
TC163G59	T3D73	24,000				59,664	192	292
TC163G45	T3D71	18,000				45,540	168	256
TC163G33	T3D69	13,000				33,660	144	220
TC163G26	T3D67	11,000				26,576	128	196
TC163G16	T3D66	6,500				16,422	104	—
TC163G11	T3D65	4,500				11,312	86	—
TC163G06	T3D63	2,500				6,930	68	—

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T”.

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Table D-13 TC220C Series Cell-Based IC Product Outline

Double-Layer Metal				Triple-Layer Metal				Max I/O Pads		
Part Number	Array Desig.[1]	Grid Complexity	Equivalent Gates	Part Number	Array Desig.[1]	Grid Complexity	Equivalent Gates	Wire Bond	TCP TBGA[2]	PQFP [TAB] TBGA[3]
TC220C040	T3S60	118,000	59,000	TC220C540	T3T60	196,000	98,000	104	148	200
TC220C060	T3S61	166,000	83,000	TC220C560	T3T61	274,000	137,000	128	184	248
TC220C080	T3S62	226,000	113,000	TC220C580	T3T62	372,000	186,000	144	212	288
TC220C100	T3S63	274,000	137,000	TC220C600	T3T63	450,000	225,000	160	236	316
TC220C120	T3S64	334,000	167,000	TC220C620	T3T64	546,000	273,000	176	260	348
TC220C140	T3S65	400,000	200,000	TC220C640	T3T65	654,000	327,000	192	284	380
TC220C160	T3S66	448,000	224,000	TC220C660	T3T66	720,000	360,000	208	312	420
TC220C180	T3S67	520,000	260,000	TC220C680	T3T67	836,000	418,000	224	336	452
TC220C200	T3S68	598,000	299,000	TC220C700	T3T68	962,000	481,000	240	360	484
TC220C220	T3S69	682,000	341,000	TC220C720	T3T69	1,094,000	547,000	256	384	516
TC220C240	T3S70	770,000	385,000	TC220C740	T3T70	1,236,000	618,000	272	408	548
TC220C260	T3S71	864,000	432,000	TC220C760	T3T71	1,388,000	694,000	288	432	—
TC220C280	T3S72	962,000	481,000	TC220C780	T3T72	1,546,000	773,000	304	456	—
TC220C300	T3S73	1,068,000	534,000	TC220C800	T3T73	1,714,000	857,000	320	480	—
TC220C320	T3S74	1,178,000	589,000	TC220C820	T3T74	1,890,000	945,000	336	504	—
TC220C340	T3S75	1,270,000	635,000	TC220C840	T3T75	2,048,000	1,024,000	360	540	—
TC220C360	T3S76	1,446,000	723,000	TC220C860	T3T76	2,332,000	1,166,000	384	576	—
TC220C380	T3S77	1,634,000	817,000	TC220C880	T3T77	2,634,000	1,317,000	408	612	—
TC220C400	T3S78	1,832,000	916,000	TC220C900	T3T78	2,954,000	1,477,000	432	648	—
TC220C420	T3S79	2,576,000	1,288,000	TC220C920	T3T79	4,154,000	2,077,000	512	768	—

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T8”.
3) Array designators are followed by the suffix “T6”.

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Table D-14 TC200C Series Cell-Based IC Product Outline

Double-Layer Metal				Triple-Layer Metal				Max I/O Pads		
Part Number	Array Desig.[1)]	Grid Complexity	Equivalent Gates	Part Number	Array Desig.[1)]	Grid Complexity	Equivalent Gates	Wire Bond	TCP TBGA[2)]	PQFP [TAB] TBGA[3)]
TC200C020	T9X21	24,000	12,000					80	112	152
TC200C040	T9X22	42,000	21,000					104	148	200
TC200C060	T9X23	64,000	32,000					128	184	248
TC200C080	T9X24	82,000	41,000	TC200C580	T9Y24	132,000	66,000	144	212	288
TC200C100	T9X25	98,000	49,000	TC200C600	T9Y25	160,000	80,000	160	236	316
TC200C120	T9X26	120,000	60,000	TC200C620	T9Y26	194,000	97,000	176	260	348
TC200C140	T9X27	144,000	72,000	TC200C640	T9Y27	232,000	116,000	192	284	380
TC200C160	T9X28	162,000	81,000	TC200C660	T9Y28	262,000	131,000	208	312	420
TC200C180	T9X29	188,000	94,000	TC200C680	T9Y29	304,000	152,000	224	336	452
TC200C200	T9X30	216,000	108,000	TC200C700	T9Y30	350,000	175,000	240	360	484
TC200C220	T9X31	246,000	123,000	TC200C720	T9Y31	398,000	199,000	256	384	516
TC200C240	T9X32	276,000	138,000	TC200C740	T9Y32	450,000	225,000	272	408	548
TC200C260	T9X33	310,000	155,000	TC200C760	T9Y33	504,000	252,000	288	432	—
TC200C280	T9X34	346,000	173,000	TC200C780	T9Y34	560,000	280,000	304	456	—
TC200C300	T9X35	362,000	181,000	TC200C800	T9Y35	590,000	295,000	320	480	—
TC200C320	T9X36	400,000	200,000	TC200C820	T9Y36	650,000	325,000	336	504	—
TC200C340	T9X37	458,000	229,000	TC200C840	T9Y37	748,000	374,000	360	540	—
TC200C360	T9X38	522,000	261,000	TC200C860	T9Y38	850,000	425,000	384	576	—
TC200C380	T9X39	590,000	295,000	TC200C880	T9Y39	960,000	480,000	408	612	—
TC200C400	T9X40	660,000	330,000	TC200C900	T9Y40	1,076,000	538,000	432	648	—

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T8”.
3) Array designators are followed by the suffix “T6”.

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Table D-15 TC180C Series Cell-Based IC Product Outline

Double-Layer Metal				Triple-Layer Metal				Max I/O Pads	
Part Number	Array Desig.[1)]	Grid Complexity	Equivalent Gates	Part Number	Array Desig.[1)]	Grid Complexity	Equivalent Gates	Wire Bonding	TCP PQFP[TAB][2)]
TC180C010	T9R01	10,000	5,000					68	—
TC180C020	T9R02	15,400	7,700					84	—
TC180C030	T9R03	23,000	11,500					102	—
TC180C040	T9R04	25,800	12,900					108	—
TC180C050	T9R05	32,200	16,100					120	—
TC180C060	T9R06	39,000	19,500					132	—
TC180C070	T9R07	48,400	24,200					144	216
TC180C080	T9R08	54,000	27,000					152	228
TC180C090	T9R09	59,800	29,900					160	240
TC180C100	T9R10	66,000	33,000					168	252
TC180C110	T9R11	72,400	36,200					176	264
TC180C120	T9R12	79,200	39,600					184	276
TC180C130	T9R13	86,200	43,100					192	288
TC180C140	T9R14	93,600	46,800					200	300
TC180C150	T9R15	101,200	50,600	TC180C550	T9T05	149,600	74,800	208	312
TC180C160	T9R16	110,600	55,300	TC180C560	T9T06	163,400	81,700	216	328
TC180C170	T9R17	123,200	61,600	TC180C570	T9T07	182,000	91,000	228	344
TC180C180	T9R18	136,400	68,200	TC180C580	T9T08	201,600	100,800	240	364
TC180C190	T9R19	145,600	72,800	TC180C590	T9T09	215,200	107,600	248	376
TC180C200	T9R20	156,800	78,400	TC180C600	T9T10	231,600	115,800	256	388
TC180C210	T9R21	173,400	86,700	TC180C610	T9T11	256,200	128,100	268	408
TC180C220	T9R22	190,800	95,400	TC180C620	T9T12	282,000	141,000	280	428
TC180C230	T9R23	214,600	107,300	TC180C630	T9T13	317,400	158,700	296	456
TC180C240	T9R24	228,200	114,100	TC180C640	T9T14	337,200	168,600	304	468
TC180C250	T9R25	256,200	128,100	TC180C650	T9T15	378,800	189,400	320	496
TC180C260	T9R26	283,800	141,900	TC180C660	T9T16	419,600	209,800	336	524
TC180C270	T9R27	299,200	149,600	TC180C670	T9T17	442,400	221,200	344	536
TC180C280	T9R28	340,800	170,400	TC180C680	T9T18	504,000	252,000	368	572
TC180C290	T9R29	387,800	193,900	TC180C690	T9T19	573,200	286,600	392	612
TC180C300	T9R30	437,600	218,800	TC180C700	T9T20	646,800	323,400	416	648

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T”.

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Table D-16 TC190C Series Cell-Based IC Product Outline

Double-Layer Metal				Triple-Layer Metal				Max I/O Pads		
Part Number	Array Desig.[1)]	Grid Complexity	Equivalent Gates	Part Number	Array Desig.[1)]	Grid Complexity	Equivalent Gates	Wire Bond	TCP TBGA[2)]	PQFP [TAB] TBGA[3)]
TC190C020	T9X61	24,000	12,000					80	112	152
TC190C040	T9X62	42,000	21,000					104	148	200
TC190C060	T9X63	64,000	32,000					128	184	248
TC190C080	T9X64	82,000	41,000	TC190C580	T9Y64	132,000	66,000	144	212	288
TC190C100	T9X65	98,000	49,000	TC190C600	T9Y65	160,000	80,000	160	236	316
TC190C120	T9X66	120,000	60,000	TC190C620	T9Y66	194,000	97,000	176	260	348
TC190C140	T9X67	144,000	72,000	TC190C640	T9Y67	232,000	116,000	192	284	380
TC190C160	T9X68	162,000	81,000	TC190C660	T9Y68	262,000	131,000	208	312	420
TC190C180	T9X69	188,000	94,000	TC190C680	T9Y69	304,000	152,000	224	336	452
TC190C200	T9X70	216,000	108,000	TC190C700	T9Y70	350,000	175,000	240	360	484
TC190C220	T9X71	246,000	123,000	TC190C720	T9Y71	398,000	199,000	256	384	516
TC190C240	T9X72	276,000	138,000	TC190C740	T9Y72	450,000	225,000	272	408	548
TC190C260	T9X73	310,000	155,000	TC190C760	T9Y73	504,000	252,000	288	432	—
TC190C280	T9X74	346,000	173,000	TC190C780	T9Y74	560,000	280,000	304	456	—
TC190C300	T9X75	362,000	181,000	TC190C800	T9Y75	590,000	295,000	320	480	—
TC190C320	T9X76	400,000	200,000	TC190C820	T9Y76	650,000	325,000	336	504	—
TC190C340	T9X77	458,000	229,000	TC190C840	T9Y77	748,000	374,000	360	540	—
TC190C360	T9X78	522,000	261,000	TC190C860	T9Y78	850,000	425,000	384	576	—
TC190C380	T9X79	590,000	295,000	TC190C880	T9Y79	960,000	480,000	408	612	—
TC190C400	T9X80	660,000	330,000	TC190C900	T9Y80	1,076,000	538,000	432	648	—

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T”.

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Table D-17 TC170C Series Cell-Based IC Product Outline

Double-Layer Metal				Triple-Layer Metal				Max I/O Pads	
Part Number	Array Desig.[1)]	Grid Complexity	Equivalent Gates	Part Number	Array Desig.[1)]	Grid Complexity	Equivalent Gates	Wire Bonding	TCP PQFP[TAB][2)]
TC170C010	T9V21	10,000	5,000					68	—
TC170C020	T9V22	15,400	7,700					84	—
TC170C030	T9V23	23,000	11,500					102	—
TC170C040	T9V24	25,800	12,900					108	—
TC170C050	T9V25	32,200	16,100					120	—
TC170C060	T9V26	39,000	19,500					132	—
TC170C070	T9V27	48,400	24,200					144	216
TC170C080	T9V28	54,000	27,000					152	228
TC170C090	T9V29	59,800	29,900					160	240
TC170C100	T9V30	66,000	33,000					168	252
TC170C110	T9V31	72,400	36,200					176	264
TC170C120	T9V32	79,200	39,600					184	276
TC170C130	T9V33	86,200	43,100					192	288
TC170C140	T9V34	93,600	46,800					200	300
TC170C150	T9V35	101,200	50,600	TC170C550	T9W25	149,400	74,800	208	312
TC170C160	T9V36	110,600	55,300	TC170C560	T9W26	163,400	81,700	216	328
TC170C170	T9V37	123,200	61,600	TC170C570	T9W27	182,000	91,000	228	344
TC170C180	T9V38	136,400	68,200	TC170C580	T9W28	201,600	100,800	240	364
TC170C190	T9V39	145,600	72,800	TC170C590	T9W29	215,200	107,600	248	376
TC170C200	T9V40	156,800	78,400	TC170C600	T9W30	231,600	115,800	256	388
TC170C210	T9V41	173,400	86,700	TC170C610	T9W31	256,200	128,100	268	408
TC170C220	T9V42	190,800	95,400	TC170C620	T9W32	282,000	141,000	280	428
TC170C230	T9V43	214,600	107,300	TC170C630	T9W33	317,400	158,700	296	456
TC170C240	T9V44	228,200	114,100	TC170C640	T9W34	337,200	168,600	304	468
TC170C250	T9V45	256,200	128,100	TC170C650	T9W35	378,800	189,400	320	496
TC170C260	T9V46	283,800	141,900	TC170C660	T9W36	419,600	209,800	336	524
TC170C270	T9V47	299,200	149,600	TC170C670	T9W37	442,400	221,200	344	536
TC170C280	T9V48	340,800	170,400	TC170C680	T9W38	504,000	252,000	368	572
TC170C290	T9V49	387,800	193,900	TC170C690	T9W39	573,200	286,600	392	612
TC170C300	T9V50	437,600	218,800	TC170C700	T9W40	646,800	323,400	416	648

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T”.

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Table D-18 TC26SC Series Cell-Based IC Product Outline

Ref No.	Array Designator[1)]	Grid Complexity	EquivalentGates	Max. Pads
20	T9M45	55,600	27,800	144
24	T9M46	66,700	33,350	160
26	T9M47	72,200	36,100	168
28	T9M48	77,800	38,900	176
30	T9M49	83,300	41,650	184
32	T9M50	88,900	44,450	192
38	T9M51	105,600	52,800	208
40	T9M52	111,100	55,550	216
42	T9M53	116,700	58,350	224
46	T9M54	127,800	63,900	232
48	T9M55	133,300	66,650	240
54	T9M56	150,000	75,000	256
60	T9M57	166,700	83,350	272
70	T9M58	194,400	97,200	296
80	T9M59	222,200	111,100	320
88	T9M60	244,400	122,000	336
96	T9M61	266,700	133,550	352
106	T9M62	294,400	147,200	368
120	T9M63	333,300	166,500	392
144	T9M64	400,000	200,000	424

1) Array designators are specified in the Toshiba design kit environment.

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Table D-19 TC25SC Series Cell-Based IC Product Outline

Ref No.	Array Desig.[1)]	Grid Complexity	Equivalent Gates	Max. Pads	Ref No.	Array Desig.[1)]	Grid Complexity	Equivalent Gates	Max. Pads
01	T3C01	1,400	700	24	42	T3C23	60,000	30,000	196
02	T3C02	2,800	1,400	36	46	T3C24	65,700	32,850	204
03	T3C03	4,200	2,100	44	50	T3C25	71,400	35,700	212
04	T3C04	5,700	2,850	52	54	T3C26	77,100	38,550	220
05	T3C05	7,100	3,550	60	58	T3C27	82,800	41,400	228
06	T3C06	8,500	4,250	68	62	T3C28	88,500	44,250	236
07	T3C07	10,000	5,000	72	66	T3C29	94,200	47,100	244
08	T3C08	11,400	5,700	76	70	T3C30	100,000	50,000	252
09	T3C09	12,800	6,400	80	74	T3C31	105,700	52,850	260
10	T3C10	14,200	7,100	84	78	T3C32	111,400	55,700	268
12	T3C11	17,100	8,550	92	82	T3C33	117,100	58,550	276
14	T3C12	20,000	10,000	100	86	T3C34	122,800	61,400	280
16	T3C13	22,800	11,400	108	90	T3C35	128,500	64,250	284
18	T3C14	25,700	12,850	116	94	T3C36	134,200	67,100	292
20	T3C15	28,500	14,250	124	98	T3C37	140,000	70,000	296
22	T3C16	31,400	15,700	132	106	T3C38	151,400	75,700	308
24	T3C17	34,200	17,100	140	114	T3C39	162,800	81,400	320
26	T3C18	37,100	18,550	148	122	T3C40	174,200	87,100	332
28	T3C19	40,000	20,000	156	130	T3C41	185,700	92,850	344
30	T3C20	42,800	21,400	164	138	T3C42	197,100	98,550	356
34	T3C21	48,500	24,250	176	144	T3C43	205,700	102,850	360
38	T3C22	54,200	27,100	184					

1) Array designators are specified in the Toshiba design kit environment.

3V/5V

CB

Table D-20 TC203C Series Cell-Based IC Product Outline

Double-Layer Metal				Triple-Layer Metal				Max I/O Pads		
Part Number	Array Desig.[1)]	Grid Complexity	Equivalent Gates	Part Number	Array Desig.[1)]	Grid Complexity	Equivalent Gates	Wire Bond	TCP TBGA][2)]	PQFP[TAB] TBGA[2)]
TC203C040	T3S00	38,000	19,000					96	148	200
TC203C060	T3S01	62,000	31,000					120	184	248
TC203C080	T3S02	78,000	39,000	TC203C580	T3T02	126,000	63,000	136	212	288
TC203C100	T3S03	94,000	47,000	TC203C600	T3T03	152,000	76,000	152	236	316
TC203C120	T3S04	114,000	57,000	TC203C620	T3T04	186,000	93,000	168	260	348
TC203C140	T3S05	138,000	69,000	TC203C640	T3T05	224,000	112,000	184	284	380
TC203C160	T3S06	156,000	78,000	TC203C660	T3T06	254,000	127,000	200	312	420
TC203C180	T3S07	182,000	91,000	TC203C680	T3T07	294,000	147,000	216	336	452
TC203C200	T3S08	210,000	105,000	TC203C700	T3T08	340,000	170,000	232	360	484
TC203C220	T3S09	238,000	119,000	TC203C720	T3T09	386,000	193,000	248	384	516
TC203C240	T3S10	270,000	135,000	TC203C740	T3T10	438,000	219,000	264	408	548
TC203C260	T3S11	302,000	151,000	TC203C760	T3T11	490,000	245,000	280	432	—
TC203C280	T3S12	338,000	169,000	TC203C780	T3T12	548,000	274,000	296	456	—
TC203C300	T3S13	354,000	177,000	TC203C800	T3T13	576,000	288,000	312	480	—
TC203C320	T3S14	390,000	195,000	TC203C820	T3T14	636,000	318,000	328	504	—
TC203C340	T3S15	450,000	225,000	TC203C840	T3T15	732,000	366,000	352	540	—
TC203C360	T3S16	512,000	256,000	TC203C860	T3T16	834,000	417,000	376	576	—
TC203C380	T3S17	578,000	289,000	TC203C880	T3T17	942,000	471,000	400	612	—
TC203C400	T3S18	650,000	325,000	TC203C900	T3T18	1,058,000	529,000	424	648	—
TC203C420	T3S19	862,000	431,000	TC203C920	T3T19	1,436,000	718,000	504	768	—

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T8”.
3) Array designators are followed by the suffix “T6”.

3V/5V

CB

Table D-21 TC183C Series Cell-Based IC Product Outline

Double-Layer Metal				Triple-Layer Metal				Max I/O Pads	
Part Number	Array Desig.[1)]	Grid Complexity	Equivalent Gates	Part Number	Array Desig.[1)]	Grid Complexity	Equivalent Gates	Wire Bonding	TCP PQFP[TAB][2)]
TC183C010	T9R61	5,600	2,800					52	—
TC183C020	T9R62	10,000	5,000					68	—
TC183C030	T9R63	16,200	8,100					86	—
TC183C040	T9R64	18,600	9,300					92	—
TC183C050	T9R65	24,000	12,000					104	—
TC183C060	T9R66	30,000	15,000					116	—
TC183C070	T9R67	38,200	19,100					128	194
TC183C080	T9R68	43,200	21,600					136	206
TC183C090	T9R69	48,400	24,200					144	218
TC183C100	T9R70	54,000	27,000					152	230
TC183C110	T9R71	59,800	29,900					160	242
TC183C120	T9R72	66,000	33,000					168	254
TC183C130	T9R73	72,400	36,200					176	266
TC183C140	T9R74	79,200	39,600					184	278
TC183C150	T9R75	86,200	43,100	TC183C550	T9T25	127,600	63,800	192	290
TC183C160	T9R76	94,800	47,400	TC183C560	T9T26	140,200	70,100	200	304
TC183C170	T9R77	106,600	53,300	TC183C570	T9T27	157,400	78,700	212	322
TC183C180	T9R78	118,800	59,400	TC183C580	T9T28	175,800	87,900	224	340
TC183C190	T9R79	127,400	63,700	TC183C590	T9T29	188,400	94,200	232	352
TC183C200	T9R80	138,000	69,000	TC183C600	T9T30	203,800	101,900	240	366
TC183C210	T9R81	153,400	76,700	TC183C610	T9T31	226,800	113,400	252	386
TC183C220	T9R82	170,000	85,000	TC183C620	T9T32	251,200	125,600	264	406
TC183C230	T9R83	192,600	96,300	TC183C630	T9T33	284,600	142,300	280	432
TC183C240	T9R84	205,200	102,600	TC183C640	T9T34	303,400	151,700	288	446
TC183C250	T9R85	232,000	116,000	TC183C650	T9T35	343,000	171,500	304	474
TC183C260	T9R86	258,400	129,200	TC183C660	T9T36	381,800	190,900	320	500
TC183C270	T9R87	273,000	136,500	TC183C670	T9T37	403,600	201,800	328	514
TC183C280	T9R88	312,800	156,400	TC183C680	T9T38	462,400	231,200	352	550
TC183C290	T9R89	357,800	178,900	TC183C690	T9T39	529,000	264,500	376	558
TC183C300	T9R90	405,800	202,900	TC183C700	T9T40	599,800	299,900	400	626

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T”.

2V/3V

CB

Table D-22 TC222C Series Cell-Based IC Product Outline

Double-Layer Metal				Triple-Layer Metal				Max I/O Pads		
Part Number	Array Desig.[1)]	Grid Complexity	Equivalent Gates	Part Number	Array Desig.[1)]	Grid Complexity	Equivalent Gates	Wire Bonding	TCP TBGA[2)]	PQFP[TAB] TBGA[3)]
TC222C040	T3U00	118,000	59,000	TC222C540	T3V00	196,000	98,000	96	148	200
TC222C060	T3U01	166,000	83,000	TC222C560	T3V01	274,000	137,000	120	184	248
TC222C080	T3U02	226,000	113,000	TC222C580	T3V02	372,000	186,000	136	212	288
TC222C100	T3U03	274,000	137,000	TC222C600	T3V03	450,000	225,000	152	236	316
TC222C120	T3U04	334,000	167,000	TC222C620	T3V04	546,000	273,000	168	260	348
TC222C140	T3U05	400,000	200,000	TC222C640	T3V05	654,000	327,000	184	284	380
TC222C160	T3U06	448,000	224,000	TC222C660	T3V06	720,000	360,000	200	312	420
TC222C180	T3U07	520,000	260,000	TC222C680	T3V07	836,000	418,000	216	336	452
TC222C200	T3U08	598,000	299,000	TC222C700	T3V08	962,000	481,000	232	360	484
TC222C220	T3U09	682,000	341,000	TC222C720	T3V09	1,094,000	547,000	248	384	516
TC222C240	T3U10	770,000	385,000	TC222C740	T3V10	1,236,000	618,000	264	408	548
TC222C260	T3U11	864,000	432,000	TC222C760	T3V11	1,388,000	694,000	280	432	—
TC222C280	T3U12	962,000	481,000	TC222C780	T3V12	1,546,000	773,000	296	456	—
TC222C300	T3U13	1,068,000	534,000	TC222C800	T3V13	1,714,000	857,000	312	480	—
TC222C320	T3U14	1,178,000	589,000	TC222C820	T3V14	1,890,000	945,000	328	504	—
TC222C340	T3U15	1,270,000	635,000	TC222C840	T3V15	2,048,000	1,024,000	352	540	—
TC222C360	T3U16	1,446,000	723,000	TC222C860	T3V16	2,332,000	1,166,000	376	576	—
TC222C380	T3U17	1,634,000	817,000	TC222C880	T3V17	2,634,000	1,317,000	400	612	—
TC222C400	T3U18	1,832,000	916,000	TC222C900	T3V18	2,954,000	1,477,000	424	648	—
TC222C420	T3U19	2,576,000	1,288,000	TC222C920	T3V19	4,154,000	2,077,000	504	768	—

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T8”.
3) Array designators are followed by the suffix “T6”.

3V

EA

Table D-23 TC220E Series Embedded Array Product Outline

Double-Layer Metal			Triple-Layer Metal			Raw Gates	Max I/O Pads		
Part Number	Array Desig.[1)]	Usable Gates	Part Number	Array Desig.[1)]	Usable Gates		Wire Bond	TCP TBGA[2)]	PQFP[TAB] TBGA[3)]
TC220E040	T3S80	54,000	TC220E540	T3T80	101,000	118,272	104	148	200
TC220E060	T3S81	82,000	TC220E560	T3T81	144,000	182,596	128	184	248
TC220E080	T3S82	103,000	TC220E580	T3T82	182,000	245,976	144	212	288
TC220E100	T3S83	125,000	TC220E600	T3T83	220,000	297,680	160	236	316
TC220E120	T3S84	152,000	TC220E620	T3T84	267,000	360,864	176	260	348
TC220E140	T3S85	181,000	TC220E640	T3T85	315,000	430,858	192	284	380
TC220E160	T3S86	221,000	TC220E660	T3T86	385,000	526,988	208	312	420
TC220E180	T3S87	232,000	TC220E680	T3T87	403,000	610,926	224	336	452
TC220E200	T3S88	266,000	TC220E700	T3T88	462,000	700,128	240	360	484
TC220E220	T3S89	303,000	TC220E720	T3T89	526,000	796,404	256	384	516
TC220E240	T3S90	342,000	TC220E740	T3T90	593,000	898,880	272	408	548
TC220E260	T3S91	352,000	TC220E760	T3T91	614,000	1,006,434	288	432	—
TC220E280	T3S92	392,000	TC220E780	T3T92	684,000	1,121,248	304	456	—
TC220E300	T3S93	435,000	TC220E800	T3T93	758,000	1,242,262	320	480	—
TC220E320	T3S94	479,000	TC220E820	T3T94	835,000	1,368,168	336	504	—
TC220E340	T3S95	549,000	TC220E840	T3T95	957,000	1,569,400	360	540	—
TC220E360	T3S96	625,000	TC220E860	T3T96	1,090,000	1,786,824	384	576	—
TC220E380	T3S97	756,000	TC220E880	T3T97	1,230,000	2,016,760	408	612	—
TC220E400	T3S98	791,000	TC220E900	T3T98	1,378,000	2,259,600	432	648	—
TC220E420	T3S99	1,110,000	TC220E920	T3T99	1,934,000	3,170,070	512	768	—

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T8”.
3) Array designators are followed by the suffix “T6”.

3V

EA

Table D-24 TC200E Series Embedded Array Product Outline

Double-Layer Metal			Triple-Layer Metal			Raw Gates	Max I/O Pads		
Part Number	Array Desig.[1)]	Usable Gates	Part Number	Array Desig.[1)]	Usable Gates		Wire Bond	TCP TBGA[2)]	PQFP[TAB] TBGA[3)]
TC200E020	T9X41	13,000				26,100	80	120	160
TC200E040	T9X42	22,000				44,916	104	156	208
TC200E060	T9X43	31,000				68,526	128	192	256
TC200E080	T9X44	39,000	TC200E580	T9Y44	67,000	92,168	144	220	296
TC200E100	T9X45	47,000	TC200E600	T9Y45	81,000	110,880	160	244	324
TC200E120	T9X46	56,000	TC200E620	T9Y46	98,000	134,224	176	268	356
TC200E140	T9X47	67,000	TC200E640	T9Y47	117,000	159,840	192	292	388
TC200E160	T9X48	82,000	TC200E660	T9Y48	142,000	194,648	208	320	428
TC200E180	T9X49	86,000	TC200E680	T9Y49	149,000	225,280	224	344	460
TC200E200	T9X50	98,000	TC200E700	T9Y50	170,000	257,560	240	368	492
TC200E220	T9X51	111,000	TC200E720	T9Y51	193,000	292,584	256	392	524
TC200E240	T9X52	125,000	TC200E740	T9Y52	218,000	329,840	272	416	556
TC200E260	T9X53	140,000	TC200E760	T9Y53	244,000	369,328	288	440	—
TC200E280	T9X54	144,000	TC200E780	T9Y54	251,000	411,048	304	464	—
TC200E300	T9X55	159,000	TC200E800	T9Y55	278,000	455,000	320	488	—
TC200E320	T9X56	175,000	TC200E820	T9Y56	306,000	501,184	336	512	—
TC200E340	T9X57	201,000	TC200E840	T9Y57	350,000	574,236	360	548	—
TC200E360	T9X58	228,000	TC200E860	T9Y58	398,000	652,256	384	584	—
TC200E380	T9X59	257,000	TC200E880	T9Y59	448,000	735,244	408	620	—
TC200E400	T9X60	288,000	TC200E900	T9Y60	503,000	824,180	432	656	—

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T8”.
3) Array designators are followed by the suffix “T6”.

3V

EA

Table D-25 TC180E Series Embedded Array Product Outline

Double-Layer Metal			Triple-Layer Metal			Raw Gates	Max I/O Pads	
Part Number	Array Designator[1)]	Usable Gates	Part Number	Array Designator[1)]	Usable Gates		Wire Bonding	TCP PQFP[TAB][2)]
TC180E01	T9S01	5,000				10,864	68	—
TC180E02	T9S02	7,000				16,940	84	—
TC180E03	T9S03	10,000				25,368	102	—
TC180E04	T9S04	11,000				28,574	108	—
TC180E05	T9S05	14,000				35,700	120	—
TC180E06	T9S06	17,000				43,232	132	—
TC180E07	T9S07	21,000				53,750	144	220
TC180E08	T9S08	24,000				59,928	152	232
TC180E09	T9S09	26,000				66,442	160	244
TC180E10	T9S10	29,000				73,292	168	256
TC180E11	T9S11	32,000				80,478	176	268
TC180E12	T9S12	35,000				87,680	184	280
TC180E13	T9S13	38,000				95,858	192	292
TC180E14	T9S14	42,000				104,052	200	304
TC180E15	T9S15	45,000	TC180E55	T9U05	79,000	112,220	208	316
TC180E16	T9S16	49,000	TC180E56	T9U06	86,000	122,472	216	328
TC180E17	T9S17	54,000	TC180E57	T9U07	95,000	136,116	228	348
TC180E18	T9S18	60,000	TC180E58	T9U08	106,000	151,200	240	364
TC180E19	T9S19	65,000	TC180E59	T9U09	113,000	161,448	248	376
TC180E20	T9S20	70,000	TC180E60	T9U10	122,000	173,700	256	392
TC180E21	T9S21	77,000	TC180E61	T9U11	135,000	191,632	268	412
TC180E22	T9S22	84,000	TC180E62	T9U12	148,000	211,296	280	432
TC180E23	T9S23	95,000	TC180E63	T9U13	166,000	237,752	296	456
TC180E24	T9S24	101,000	TC180E64	T9U14	177,000	252,572	304	472
TC180E25	T9S25	113,000	TC180E65	T9U15	199,000	283,968	320	500
TC180E26	T9S26	126,000	TC180E66	T9U16	220,000	314,514	336	524
TC180E27	T9S27	133,000	TC180E67	T9U17	232,000	331,526	344	540
TC180E28	T9S28	151,000	TC180E68	T9U18	264,000	377,816	368	576
TC180E29	T9S29	172,000	TC180E69	T9U19	301,000	429,756	392	612
TC180E30	T9S30	194,000	TC180E70	T9U20	340,000	485,040	416	652

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T”.

5V

EA

Table D-26 TC160E Series Embedded Array Product Outline

Double-Layer Metal			Triple-Layer Metal			Raw Gates	Max I/O Pads
Part Number	Array Designator[1)]	Usable Gates	Part Number	Array Designator[1)]	Usable Gates		
TC160EU2	T9R59	120,000	TC160ET1	T3S59	210,000	302,346	416
TC160EN5	T9R58	94,000	TC160ET2	T3S58	164,000	235,276	368
TC160EH7	T9R57	71,000				176,606	320
TC160ED2	T9R56	53,000				131,712	280
TC160EA8	T9R55	43,000				108,224	256
TC160E70	T9R53	28,000				70,070	208
TC160E54	T9R51	22,000				54,432	184
TC160E41	T9R49	17,000				41,360	160
TC160E33	T9R47	13,000				33,462	144

1) Array designators are specified in the Toshiba design kit environment.

3V/5V

EA

Table D-27 TC203E Series Embedded Array Product Outline

Double-Layer Metal			Triple-Layer Metal			Raw Gates	Max I/O Pads		
Part Number	Array Desig.[1)]	Usable Gates	Part Number	Array Desig.[1)]	Usable Gates		Wire Bond	TCP TBGA[2)]	PQFP[TAB] TBGA[3)]
TC203E040	T3S20	19,000				41,580	96	148	200
TC203E060	T3S21	29,000				64,664	120	184	248
TC203E080	T3S22	37,000	TC203E580	T3T22	65,000	87,680	136	212	288
TC203E100	T3S23	44,000	TC203E600	T3T23	78,000	105,952	152	236	316
TC203E120	T3S24	54,000	TC203E620	T3T24	95,000	128,816	168	260	348
TC203E140	T3S25	65,000	TC203E640	T3T25	112,000	153,912	184	284	380
TC203E160	T3S26	79,000	TC203E660	T3T26	137,000	188,136	200	312	420
TC203E180	T3S27	83,000	TC203E680	T3T27	144,000	217,728	216	336	452
TC203E200	T3S28	95,000	TC203E700	T3T28	165,000	250,020	232	360	484
TC203E220	T3S29	108,000	TC203E720	T3T29	188,000	284,544	248	384	516
TC203E240	T3S30	122,000	TC203E740	T3T30	212,000	321,300	264	408	548
TC203E260	T3S31	137,000	TC203E760	T3T31	238,000	360,288	280	432	—
TC203E280	T3S32	141,000	TC203E780	T3T32	245,000	401,508	296	456	—
TC203E300	T3S33	156,000	TC203E800	T3T33	271,000	444,960	312	480	—
TC203E320	T3S34	171,000	TC203E820	T3T34	299,000	489,888	328	504	—
TC203E340	T3S35	197,000	TC203E840	T3T35	343,000	562,950	352	540	—
TC203E360	T3S36	224,000	TC203E860	T3T36	391,000	640,224	376	576	—
TC203E380	T3S37	253,000	TC203E880	T3T37	441,000	722,466	400	612	—
TC203E400	T3S38	284,000	TC203E900	T3T38	494,000	810,648	424	648	—
TC203E420	T3S39	398,000	TC203E920	T3T39	694,000	1,138,176	504	768	—

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the suffix “T8”.
3) Array designators are followed by the suffix “T6”.

3V/5V

EA

Table D-28 TC183E Series Embedded Array Product Outline

Double-Layer Metal			Triple-Layer Metal			Raw Gates	Max I/O Pads	
Part Number	Array Desig.[1)]	Usable Gates	Part Number	Array Desig.[1)]	Usable Gates		Wire Bonding	TCP PQFP[TAB][2)]
TC183E01	T9S61	3,000				6,364	52	—
TC183E02	T9S62	4,000				11,172	68	—
TC183E03	T9S63	7,000				18,176	86	—
TC183E04	T9S64	8,000				20,748	92	—
TC183E05	T9S65	11,000				26,576	104	—
TC183E06	T9S66	13,000				33,462	116	—
TC183E07	T9S67	17,000				42,402	128	196
TC183E08	T9S68	19,000				47,908	136	208
TC183E09	T9S69	22,000				53,750	144	220
TC183E10	T9S70	24,000				59,928	152	232
TC183E11	T9S71	27,000				66,442	160	244
TC183E12	T9S72	29,000				73,292	168	256
TC183E13	T9S73	32,000				80,478	176	268
TC183E14	T9S74	35,000				88,000	184	280
TC183E15	T9S75	38,000	TC183E55	T9U25	67,000	95,858	192	292
TC183E16	T9S76	42,000	TC183E56	T9U26	74,000	105,350	200	304
TC183E17	T9S77	47,000	TC183E57	T9U27	83,000	118,668	212	324
TC183E18	T9S78	53,000	TC183E58	T9U28	92,000	132,104	224	340
TC183E19	T9S79	57,000	TC183E59	T9U29	99,000	141,288	232	352
TC183E20	T9S80	61,000	TC183E60	T9U30	107,000	152,764	240	368
TC183E21	T9S81	68,000	TC183E61	T9U31	119,000	170,372	252	388
TC183E22	T9S82	75,000	TC183E62	T9U32	132,000	188,136	264	408
TC183E23	T9S83	86,000	TC183E63	T9U33	150,000	214,000	280	432
TC183E24	T9S84	91,000	TC183E64	T9U34	160,000	228,072	288	448
TC183E25	T9S85	103,000	TC183E65	T9U35	180,000	257,560	304	476
TC183E26	T9S86	115,000	TC183E66	T9U36	201,000	286,688	320	500
TC183E27	T9S87	121,000	TC183E67	T9U37	212,000	302,940	328	516
TC183E28	T9S88	139,000	TC183E68	T9U38	243,000	347,256	352	552
TC183E29	T9S89	159,000	TC183E69	T9U39	278,000	396,440	376	588
TC183E30	T9S90	180,000	TC183E70	T9U40	315,000	449,604	400	628

1) Array designators are specified in the Toshiba design kit environment.
2) Array designators are followed by the sufffix “T”.

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Reader's Critique

Toshiba's CMOS ASIC Design Manual is intended to be used as a reference tool for ASIC design and technical data. Toshiba plans to update this CMOS ASIC Design Manual regularly to ensure that the latest information on ASIC products, design, support, and services is available to our customers. We'd appreciate it if you take time out to send your inputs to the nearest Toshiba ASIC design center (via fax or mail).

Date:

Did you find any mistakes in this CMOS ASIC Design Manual? Please specify, by page, any errors and/or mark up the page in which you found errors.

Is there any information that is not included in this CMOS ASIC Design Manual that you would like to see added to enhance future updates?

Please tell us how rate this manual in the following respects.

	Excellent	*Good*	*Average*	*Fair*	*Poor*
Manual organization					
Completeness and clarity of information					
Usefulness of information					
Usefulness of examples					
Ease of finding information					
Appearance of manual					
Wording					

Please complete the following information

Company Name: _____

Department & Section: _____

Engineer's Name: _____

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