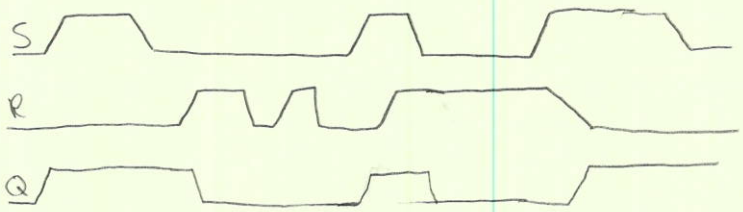
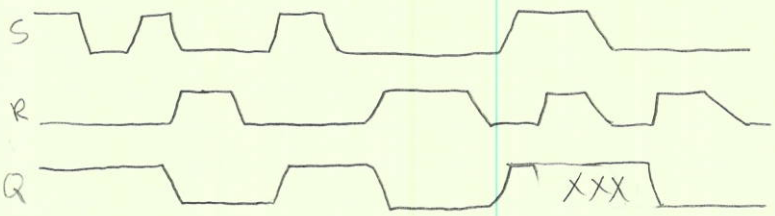
Latches and flip flops

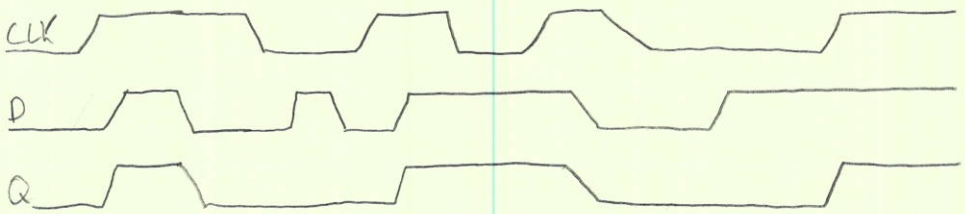
3.1 Given the input waveforms, stretch the output Q of an SR Latch



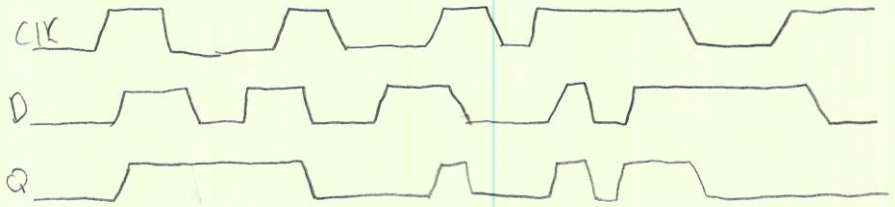
3.2 stretch the output Q of an SR Latch



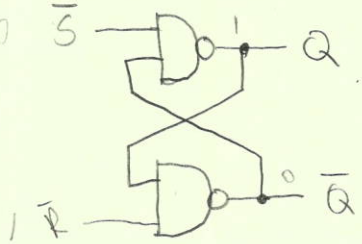
3.3 Sketch output Q of a D latch



3.4 Stretch the output Q of a D latch



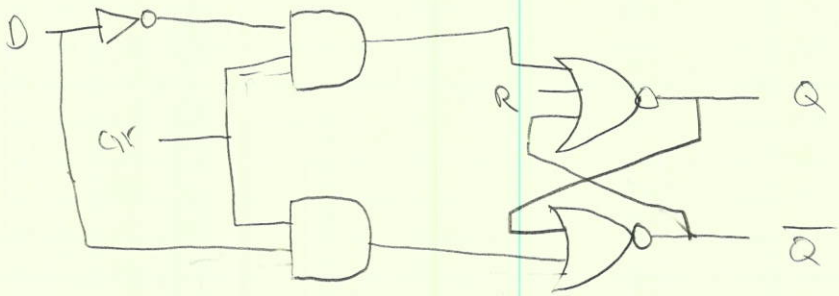
3.7 Is the circuit combinational logic or sequential logic?



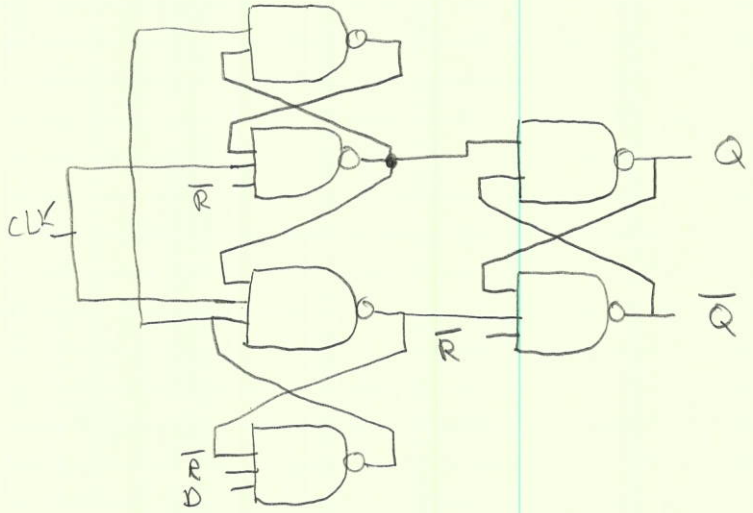
Sequential logic because it involves feedback and the output depends on previous values of the input. This is an SR Latch. Any 0 makes a 1 for a nor gate thus the truth table to the right

$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	previous	

3.12 Design an asynchronously resettable D latch using logic gates



3.13 Design an asynchronously resettable D flip flop using logic gates



3.19 Designing an elevator for 25 floors. Two inputs up / Down. Produces an output indicating the floor that the elevator is on. No 13th floor. What is the minimum # of bits of state in the controller

$25 - 1 = 24_{10}$ $24_{10} = 11000_2$ therefore need 5 bits

Must have five bits of state for 24 floors

3.3 What is the difference between latch and a flip-flop? What is preferable?

A latch allows input D to flow through to the output Q when the Clock is high. A flip-flop allows input D to flow through to Q at the clock edge. Flip-flops are preferable for systems that only have one clock while latches are preferable for systems with two clocks.