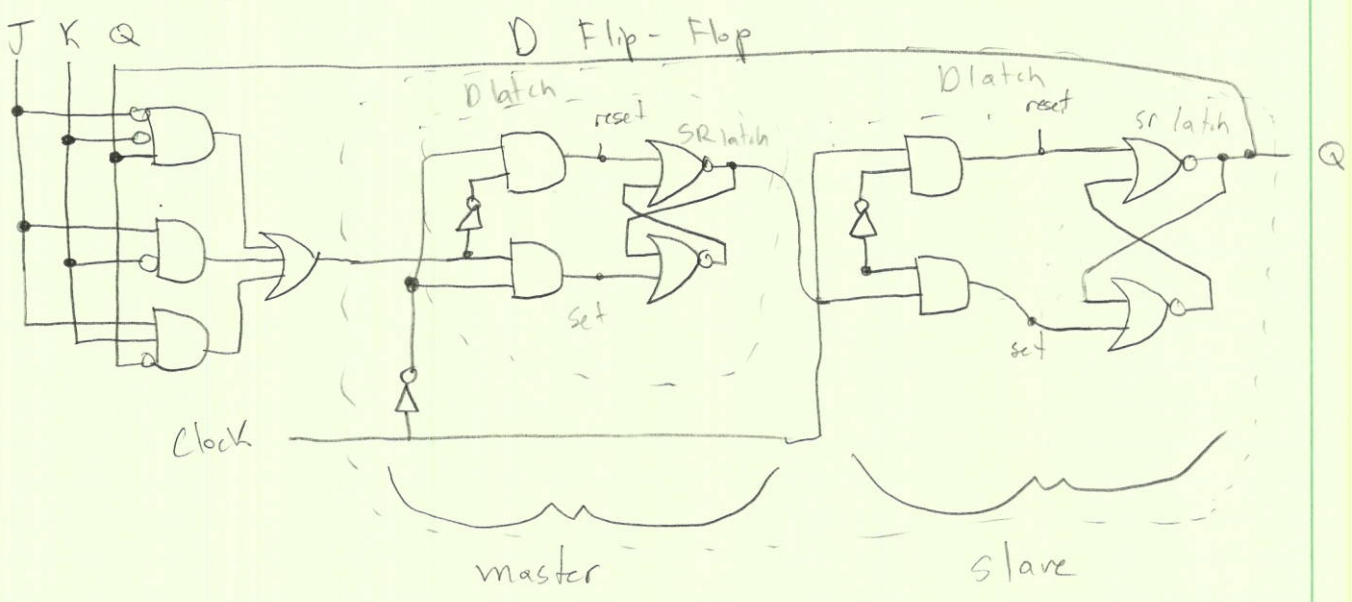
Latches and Flip Flops

1. Draw the gate level logic for a JK Flip Flop.



2. Sequential timing

3.34

A. $T = T_{cqpd} + t_{pd} + t_{setup}$

$= 35ps + (25ps + 20ps) + 30ps$

$= 110\ ps$

$F_{max} = \frac{1}{T} = \frac{1}{110 \times 10^{-12}\ s} = 9.09 \times 10^{9} = \boxed{9.09\ GHz}$

B. $F = 8\ GHz$

$T = \frac{1}{F} = \frac{1}{8\ GHz} = 125\ ps$ Clock skew $= 125ps - 110ps$

$= \boxed{15ps}$

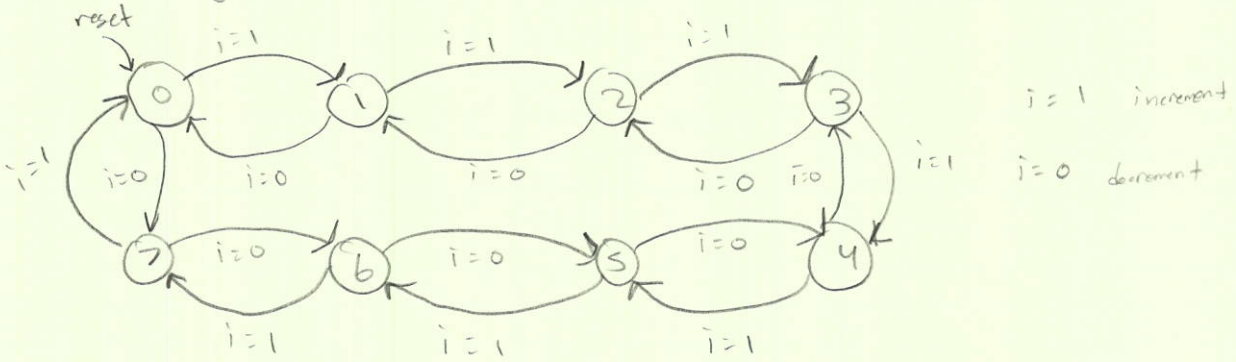
C. $t_{cqCD} + t_{CD} - t_{hold} =$ clock skew

$21ps + 15ps - 10ps = \boxed{26\ ps}$

3. Finite State Machines

1. Requirements: 3 bit up/down counter

2. State diagram



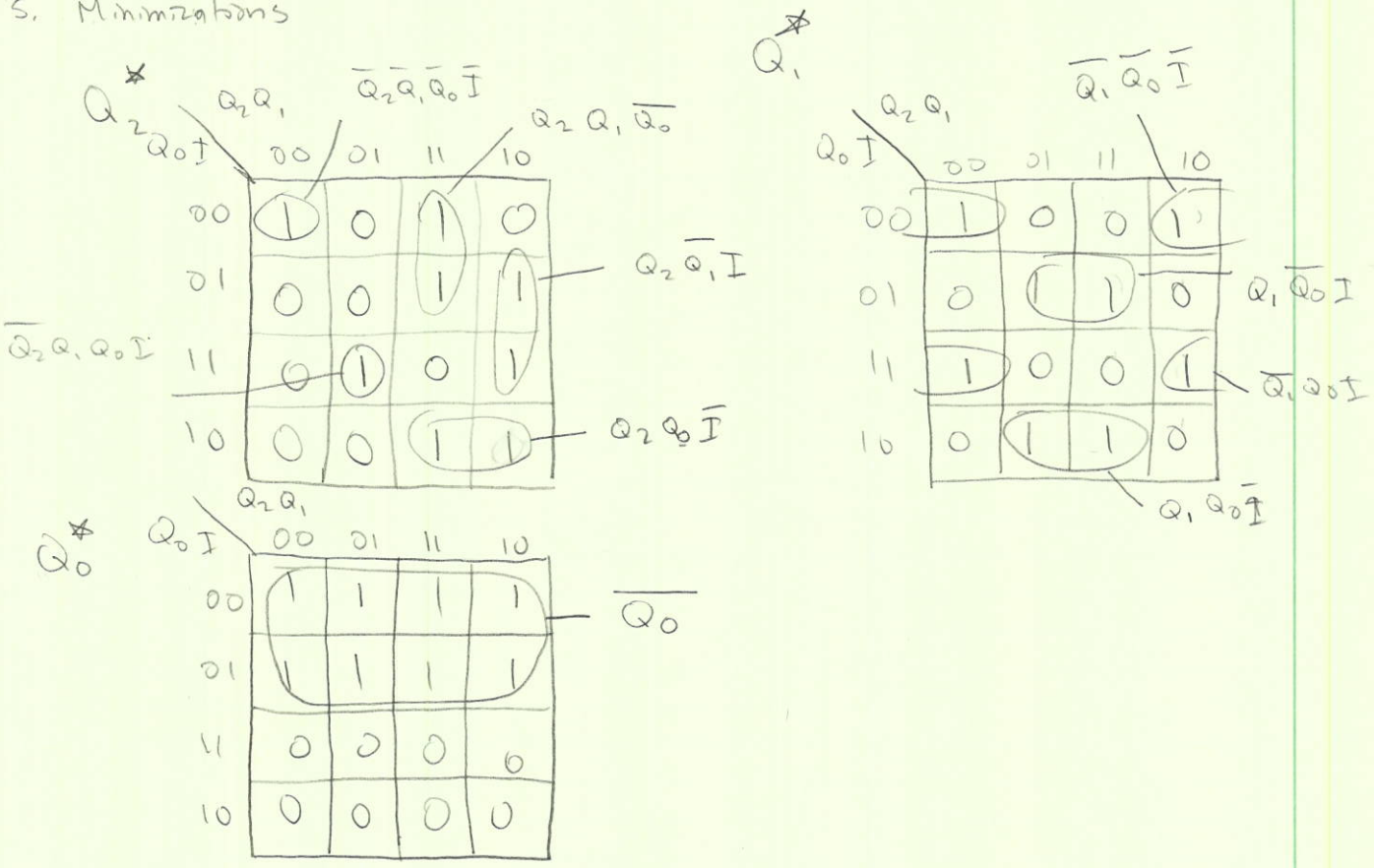
3. State assignment:

State	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

4. State Table:

State	Binary Value			Input	Next state	Next state binary		
count	Q_2	Q_1	Q_0	I	count	Q_2^*	Q_1^*	Q_0^*
0	0	0	0	0	7	1	1	1
0	0	0	0	1	1	0	0	1
1	0	0	1	0	0	0	0	0
1	0	0	1	1	2	0	1	0
2	0	1	0	0	1	0	0	1
2	0	1	0	1	3	0	1	1
3	0	1	1	0	2	0	1	0
3	0	1	1	1	4	1	0	0
4	1	0	0	0	3	0	1	1
4	1	0	0	1	5	1	0	1
5	1	0	1	0	4	1	0	0
5	1	0	1	1	6	1	1	0
6	1	1	0	0	5	1	0	1
6	1	1	0	1	7	1	1	1
7	1	1	1	0	6	1	1	0
7	1	1	1	1	0	0	0	0

5. Minimizations



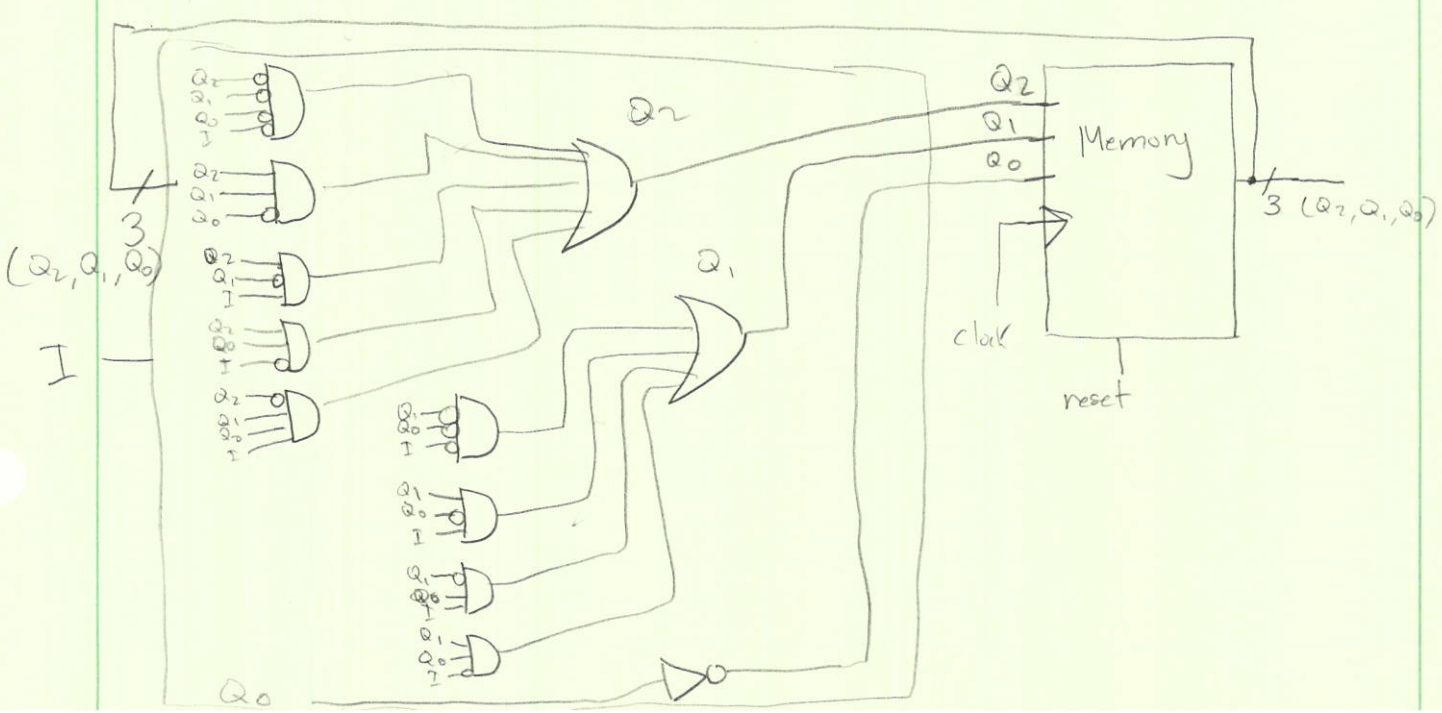
6. State Equations

$$Q_2^* = \bar{Q}_2\bar{Q}_1\bar{Q}_0\bar{I} + Q_2 Q_1 \bar{Q}_0 + Q_2\bar{Q}_1 I + Q_2 Q_0 \bar{I} + \bar{Q}_2 Q_1 Q_0 I$$

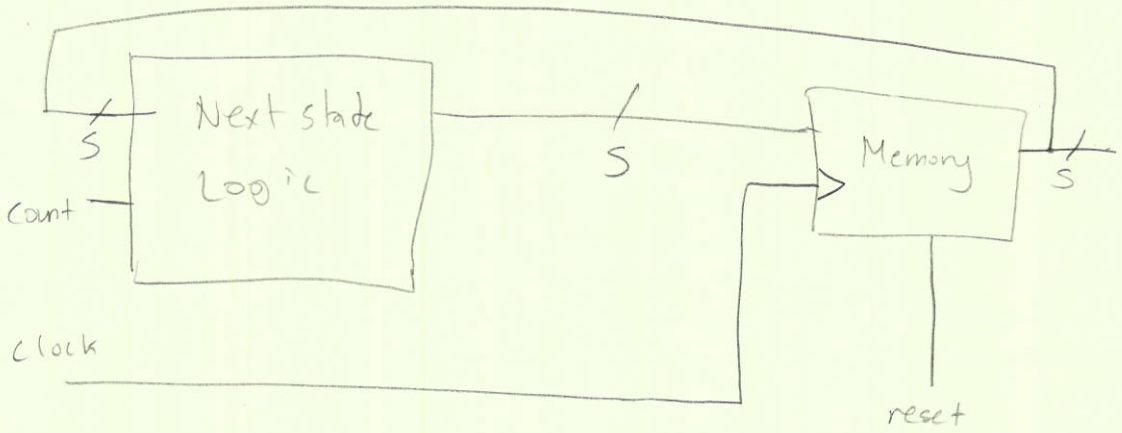
$$Q_1^* = \bar{Q}_1\bar{Q}_0\bar{I} + Q_1\bar{Q}_0 I + \bar{Q}_1 Q_0 I + Q_1 Q_0 \bar{I}$$

$$Q_0^* = \bar{Q}_0$$

7. Logic Diagram



4, Interview Question



Above is a 5 bit counter that has a reset on it because without one, there is no way to restart the count. It is made up of two logic blocks, the next state logic and the memory blocks. The outputs are fed into the next state logic to add a 1 to the count resulting in a new value when count is high