

5.1 What is the delay for the following types of 64-bit adders?
Assume that each two-input gate delay is 150 ps and that a full adder delay is 450 ps.

A. a ripple-carry adder

$$(64)(450) = \boxed{28,800 \text{ ps}}$$

B. a carry-lookahead adder with 4-bit blocks

$$t_{CLA} = t_{pg} + t_{pg\text{-block}} + \left(\frac{n}{k} - 1\right) t_{and\text{-}or} + k t_{FA}$$

$\uparrow \quad \quad \quad \uparrow \quad \quad \quad \uparrow \quad \quad \quad \uparrow \quad \quad \quad \uparrow \quad \quad \uparrow$
 150 (6)(150) 4 (2)(150) 4 450ps

$$\boxed{t_{CLA} = 7.35 \text{ ns}}$$

C. a prefix adder

$$t_{PA} = t_{pg} + (\log_2 N)(t_{pg\text{-}prefix}) + t_{xor}$$

$\uparrow \quad \quad \quad \uparrow \quad \quad \quad \uparrow \quad \quad \quad \uparrow$
 150ps 6 (2)(150) (2)(150)

$$\boxed{t_{PA} = 2.25 \text{ ns}}$$

5.2 Design two adders: a 64 bit ripple carry adder, and a 64 bit carry-lookahead adder with 4-bit blocks. Use only 2 input gates. Each two-input gate is $15 \mu\text{m}^2$, has a 50 ps delay, and has 20 fF of total gate capacitance. You may assume that the static power is negligible.

Ripple Carry

A. Compare the area, delay, and power of the adders (at 100 MHz and 1.2 V)

$$\text{Area} \quad \frac{7 \text{ gates}}{\text{adder}} \cdot 64 \text{ adders} \cdot \frac{15 \mu\text{m}^2}{\text{gate}} = \boxed{6720 \mu\text{m}^2}$$

$$\text{Delay} \quad 3 \text{ gate delays} \cdot 63 + 2 \text{ gate} =$$

$$3(50) \cdot 63 + 2(50) = 9550 \text{ ps} = \boxed{9.55 \text{ ns}}$$

Power

$$P = \frac{1}{2} C V^2 f$$

$$448 \text{ gates} \times 20 \text{ pF} = 8.96 \text{ nF}$$

$$\uparrow \quad \quad \uparrow \quad \quad \uparrow$$

8.96 nF 1.2 100

$$\frac{1}{2} (8.96) (1.2)^2 (100) = \boxed{.645 \text{ watts}}$$

Carry lookahead

$$\text{Area: } 6720 \mu\text{m} + \left(\frac{18 \text{ gates}}{\text{CLA block}} \cdot \frac{64}{4} \text{ blocks} \cdot \frac{15 \mu\text{m}^2}{\text{gate}} \right) = \boxed{11040 \mu\text{m}}$$

$$\text{Delay: } \underset{\substack{\uparrow \\ 80 \text{ ps}}}{t_{pg}} + \underset{\substack{\uparrow \\ (6)(50)}}{t_{pg-\text{block}}} + \left(\overset{\substack{\leftarrow 64 \\ N}}{K} - 1 \right) \underset{\substack{\uparrow \\ 100 \text{ ps}}}{t_{AND-\text{OR}}} + K \underset{\substack{\uparrow \\ (3 \cdot 3 + 2)(50 \text{ ps})}}{t_{FA}}$$

$$= \boxed{2400 \text{ ps}}$$

Power

$$P = \frac{1}{2} C V^2 f$$

$\uparrow \quad \uparrow \quad \uparrow$
 $14.72 \mu\text{F} \quad 1.2 \quad 100$

$$[4 \mu\text{s} + 18(16)] 20 \text{ pF} = 14720 \text{ pF}$$

$14.72 \mu\text{F}$

$$\boxed{P = 1.06 \text{ watts}}$$

B. Discuss the trade-offs between power, area, and delay

a ripple carry adder has a smaller area and also uses less power than the carry look ahead adder. The carry look ahead adder is much faster than the ripple carry.

Interview

5.1 what is the largest possible result of multiplying two unsigned N-bit numbers?

$$(2^n - 1)(2^n - 1) = 2^{2n} - 2^n - 2^n + 1 = \boxed{2^{2n} - 2^{n+1} + 1}$$