

Lab Workshop on 'FPGA Architecture and Programming using Verilog HDL' – Batch 4

Mini Project – Report

Prepared By-

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Verilog Code:

```
`timescale 1ns / 1ps

module part1(clk,
             //I0,I1,I2,I3,
             Y);
    input clk;
    // input I0, I1, I2, I3;
    output reg [3:0] Y;

    wire [1:0] cout;
    wire muxout;
    reg [3:0] dout;

    // Counter-IP core
    c_counter_binary_0 c1 (
        .CLK(clk),                // input wire CLK
        .Q(cout)                  // output wire [1 : 0] Q
    );

    // Multiplexer
    assign muxout = cout[1] ? (cout[0] ? I3:I2):(cout[0] ? I1:I0);
```

// Decoder

```
always@(cout or muxout)
    if(muxout)
    begin
        dout = 4'b0000;
        dout[cout] = 1;
    end
    else
        dout = 4'b0000;
```

// Latch

```
always@(clk)
    if(clk)
        Y <= dout;
```

// ILA

```
ila_0 g1 (
    .clk(clk),           // input wire clk
    .probe0(Y)           // input wire [3:0] probe0
);
```

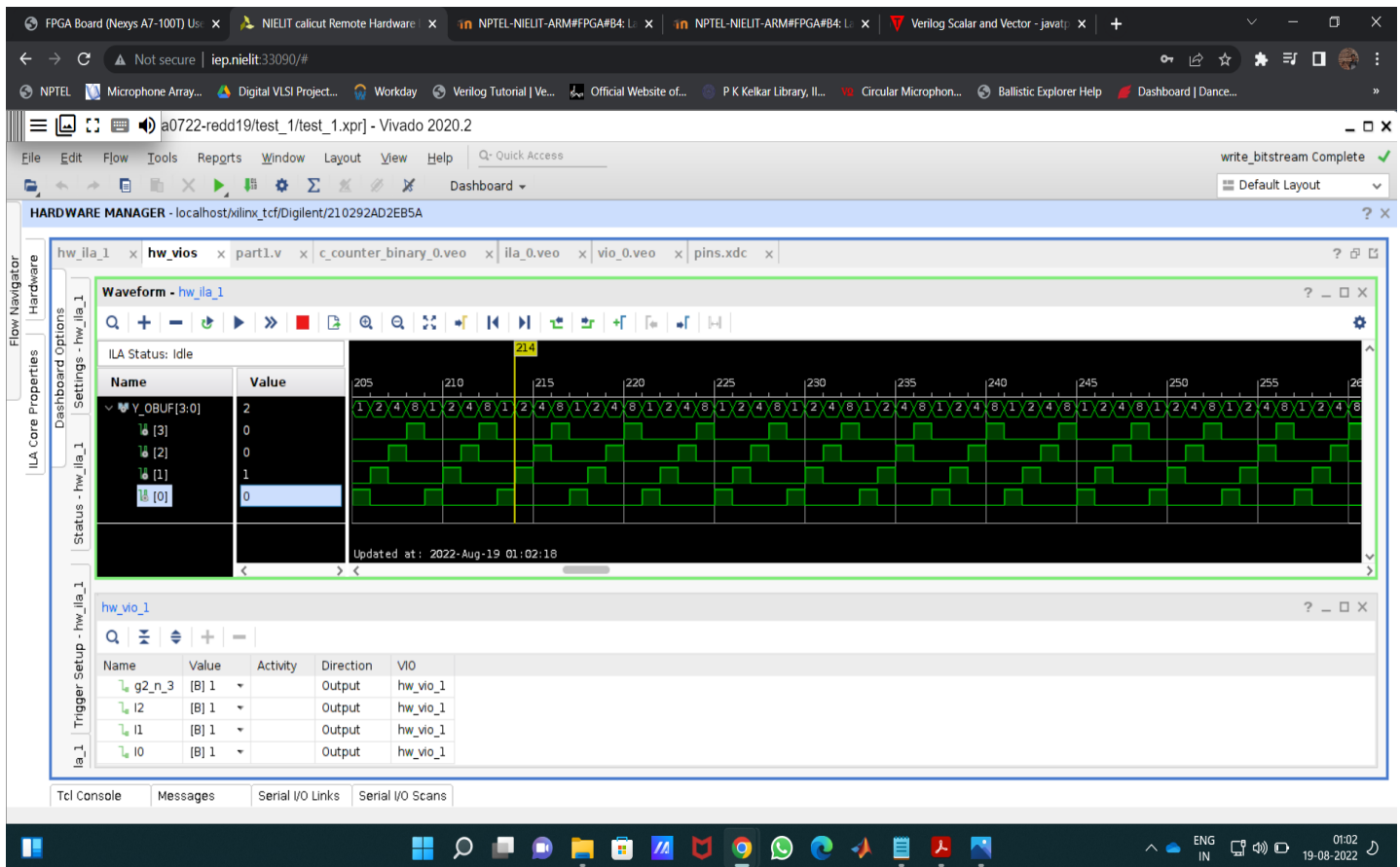
// VIO

```
vio_0 g2 (
    .clk(clk),           // input wire clk
    .probe_out0({I0,I1,I2,I3}) // output wire [3 : 0] probe_out0
);
```

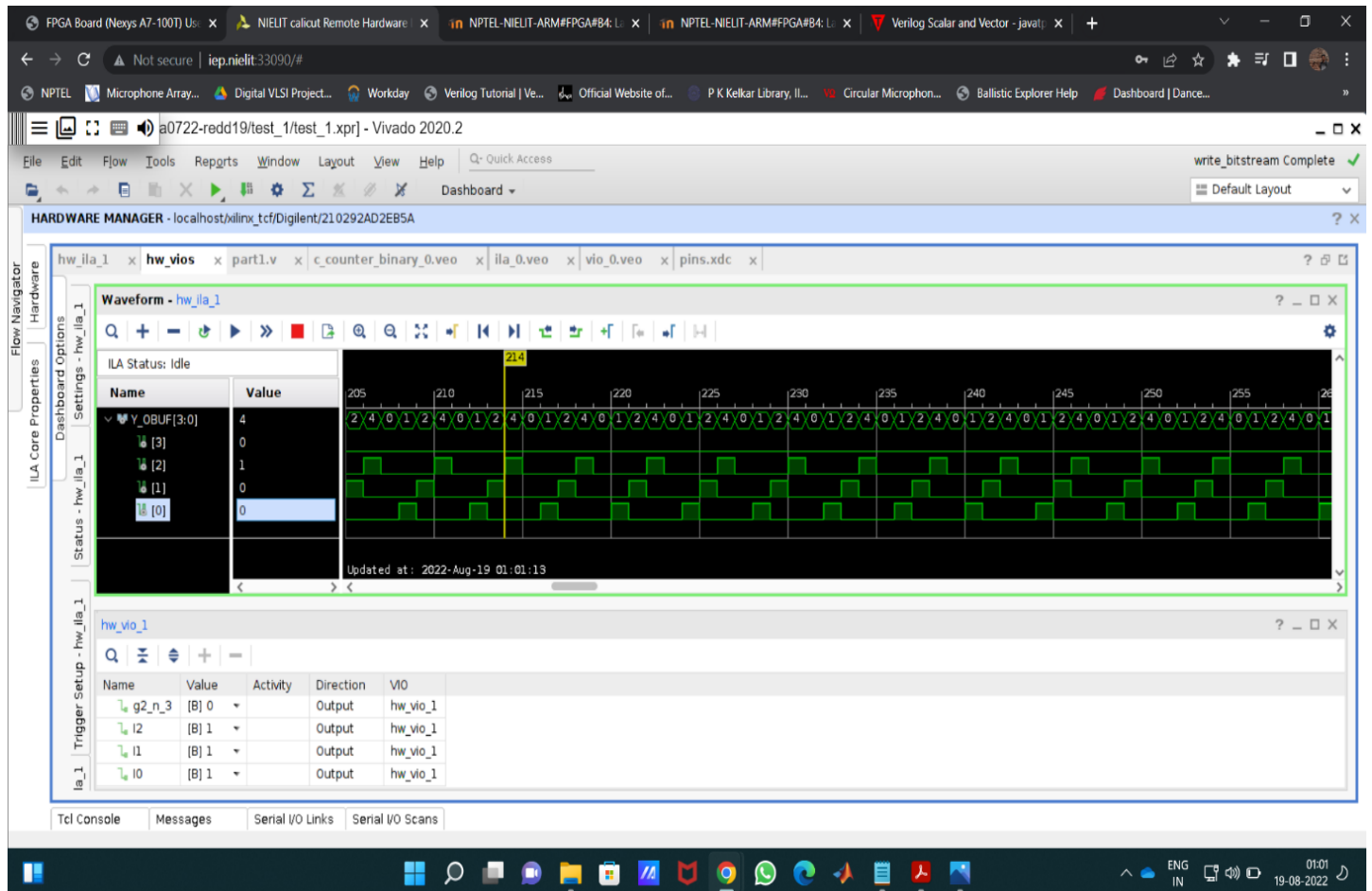
endmodule

Outputs:

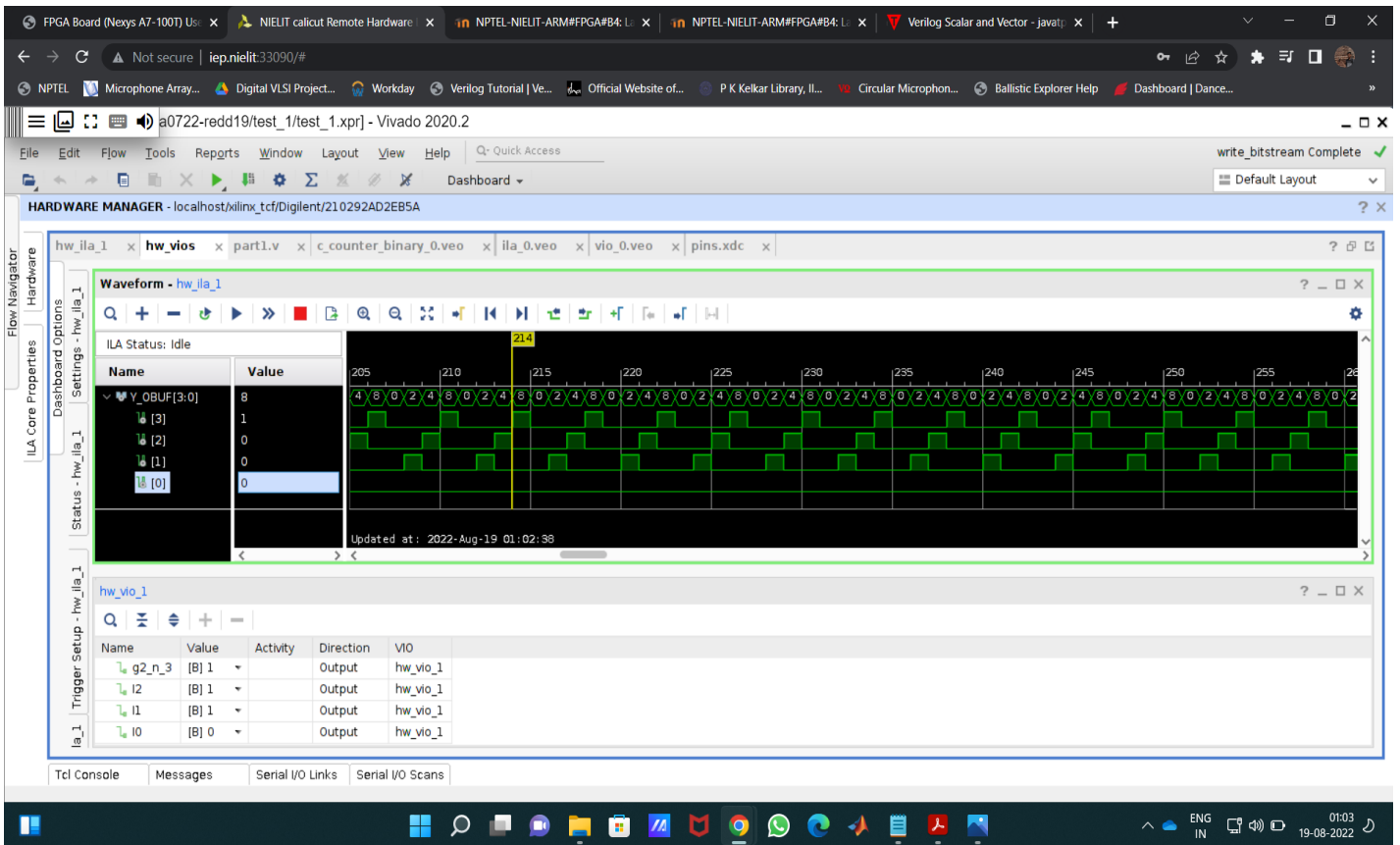
1. For input = 4'b1111:



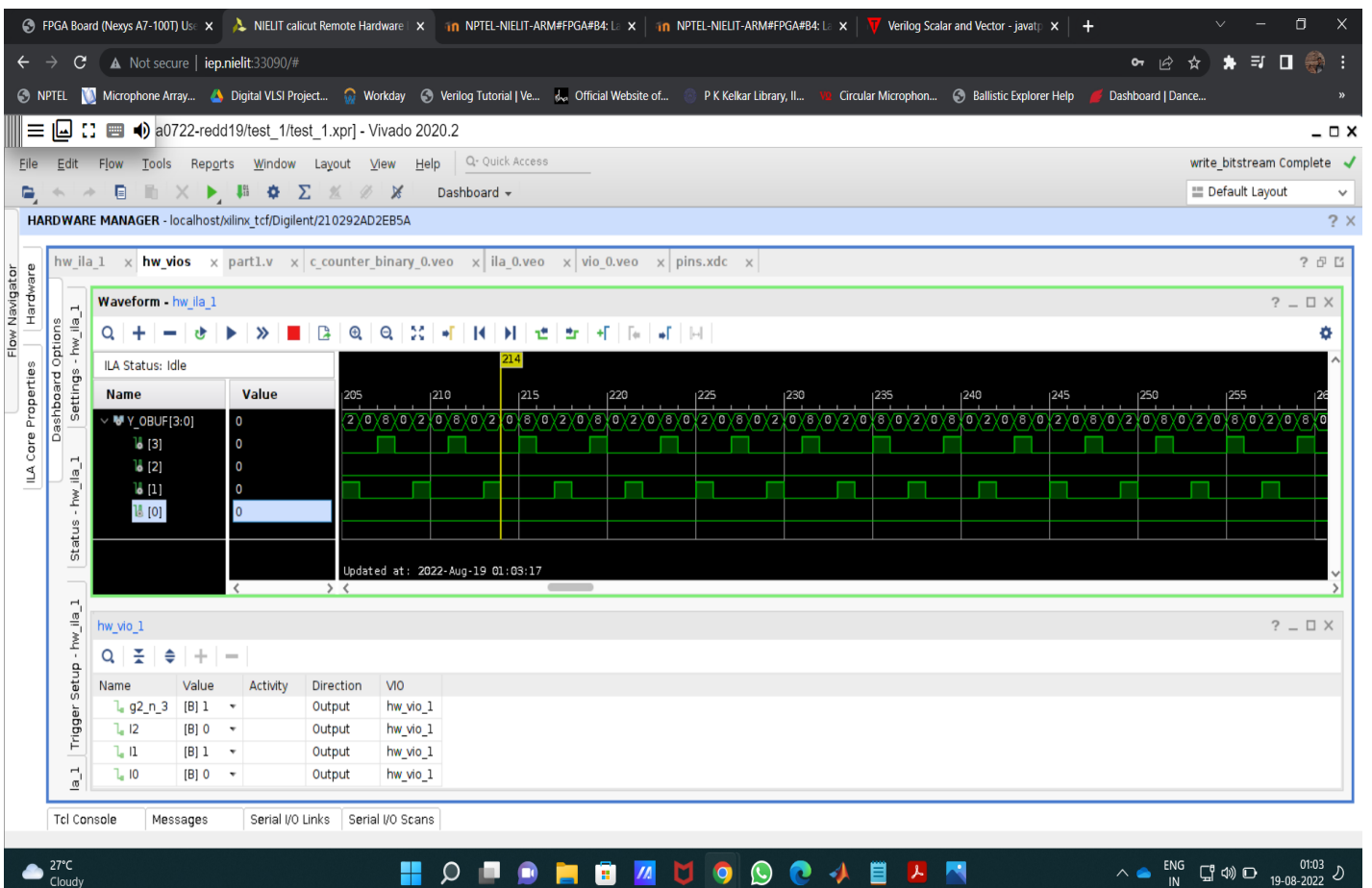
2. For input = 4'b0111:



3. For input = 4'b1110:



4. For input = 4'b1010:



5. For input = 4'b1000:

The screenshot shows the Vivado 2020.2 IDE with the Hardware Manager open. The waveform window for hw_ila_1 is displayed, showing the ILA Status as Idle. The input signal Y_0BUF[3:0] is set to 4'b1000. The waveform shows the signal values over time, with a vertical cursor at 214. The output signals g2_n_3, l2, l1, and l0 are also shown, all with values of 0.

Name	Value
Y_0BUF[3:0]	0
[3]	0
[2]	0
[1]	0
[0]	0

Name	Value	Activity	Direction	VIO
g2_n_3	[B] 1		Output	hw_vio_1
l2	[B] 0		Output	hw_vio_1
l1	[B] 0		Output	hw_vio_1
l0	[B] 0		Output	hw_vio_1

6. For input = 4'b1011:

The screenshot shows the Vivado 2020.2 IDE with the Hardware Manager open. The waveform window for hw_ila_1 is displayed, showing the ILA Status as Idle. The input signal Y_0BUF[3:0] is set to 4'b1011. The waveform shows the signal values over time, with a vertical cursor at 214. The output signals g2_n_3, l2, l1, and l0 are also shown, with values 1, 0, 1, and 1 respectively.

Name	Value
Y_0BUF[3:0]	1
[3]	0
[2]	0
[1]	0
[0]	1

Name	Value	Activity	Direction	VIO
g2_n_3	[B] 1		Output	hw_vio_1
l2	[B] 0		Output	hw_vio_1
l1	[B] 1		Output	hw_vio_1
l0	[B] 1		Output	hw_vio_1

