

## 17. Analog to Digital Converter

### 17.1 Features

- 10-bit Resolution
- 1 LSB Integral Non-linearity
- $\pm 2$  LSB Absolute Accuracy
- 65 - 260  $\mu$ s Conversion Time
- Up to 15 kSPS at Maximum Resolution
- Four Multiplexed Single Ended Input Channels
- Two differential input channels with selectable gain
- Temperature sensor input channel
- Optional Left Adjustment for ADC Result Readout
- 0 -  $V_{CC}$  ADC Input Voltage Range
- Selectable 1.1V / 2.56V ADC Voltage Reference
- Free Running or Single Conversion Mode
- ADC Start Conversion by Auto Triggering on Interrupt Sources
- Interrupt on ADC Conversion Complete
- Sleep Mode Noise Canceled
- Unipolar / Bipolar Input Mode
- Input Polarity Reversal Mode

### 17.2 Overview

The ATtiny25/45/85 features a 10-bit successive approximation Analog to Digital Converter (ADC). The ADC is connected to a 4-channel Analog Multiplexer which allows one differential voltage input and four single-ended voltage inputs constructed from the pins of Port B. The differential input (PB3, PB4 or PB2, PB5) is equipped with a programmable gain stage, providing amplification step of 26 dB (20x) on the differential input voltage before the A/D conversion. The single-ended voltage inputs refer to 0V (GND).

The ADC contains a Sample and Hold circuit which ensures that the input voltage to the ADC is held at a constant level during conversion. A block diagram of the ADC is shown in [Figure 17-1 on page 123](#).

Internal reference voltages of nominally 1.1V / 2.56V are provided on-chip. Alternatively,  $V_{CC}$  can be used as reference voltage for single ended channels. There is also an option to use an external voltage reference and turn-off the internal voltage reference.

The block diagram illustrates the internal architecture of the AD7792 ADC. Key components and their interconnections include:

- 8-BIT DATA BUS:** Connects to the ADC CTRL. & STATUS B REGISTER (ADCSRB), ADC MULTIPLEXER SELECT (ADMUX), ADC CTRL. & STATUS A REGISTER (ADCSRA), and the ADC DATA REGISTER (ADCH/ADCL).
- Registers and Control:**
  - ADCSRB:** Provides BIN and IPR signals to the MUX DECODER.
  - ADMUX:** Provides MUX2, MUX1, MUX0, and ADLAR signals to the MUX DECODER.
  - ADCSRA:** Provides ADEN, ADSC, ADIF, ADSTART, ADPS2, ADPS1, ADPS0, and ADIF signals to the CONVERSION LOGIC.
  - ADCH/ADCL:** The 16-bit ADC DATA REGISTER, with bits 15:2 connected to ADTS[2:0] and bits 1:0 connected to ADSC[9:0].
- Input and Reference:**
  - INPUT MUX:** Selects between ADC0, ADC1, ADC2, ADC3, and a TEMPERATURE SENSOR (ADC4).
  - NEG. INPUT MUX:** Selects between the input mux output and an internal 1.1V/2.56V REFERENCE.
  - REFS2:0[1]:** A 3-bit signal from the MUX DECODER to the NEG. INPUT MUX.
- Processing and Output:**
  - MUX DECODER:** Receives channel and gain selection signals and outputs CHANNEL SELECTION and GAIN SELECTION signals.
  - CONVERSION LOGIC:** Receives control signals and the output from the 10-BIT DAC. It also receives a START signal from the TRIGGER SELECT block.
  - 10-BIT DAC:** Outputs a signal to the SAMPLE & HOLD COMPARATOR.
  - SAMPLE & HOLD COMPARATOR:** Compares the DAC output with the input mux output. Its output goes to the ADC MULTIPLEXER OUTPUT.
  - GAIN AMPLIFIER:** Receives the input mux output and the GAIN SELECTION signal. Its output goes to the NEG. INPUT MUX.
- Interrupts:**
  - ADC CONVERSION COMPLETE IRQ:** Generated by an AND gate from ADIF and ADSC.
  - INTERRUPT FLAGS:** A signal from the CONVERSION LOGIC to the ADTS[2:0] register.

The ADC converts an analog input voltage to a 10-bit digital value through successive approximation. The minimum value represents GND and the maximum value represents the voltage on V<sub>CC</sub>, the voltage on the AREF pin or an internal 1.1V / 2.56V voltage reference.

The analog input channel and differential gain are selected by writing to the MUX[3:0] bits in ADMUX. Any of the four ADC input pins ADC[3:0] can be selected as single ended inputs to the ADC. ADC2 or ADC0 can be selected as positive input and ADC0, ADC1, ADC2 or ADC3 can be selected as negative input to the differential gain amplifier.

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If ADC0 or ADC2 is selected as both the positive and negative input to the differential gain amplifier (ADC0-ADC0 or ADC2-ADC2), the remaining offset in the gain stage and conversion circuitry can be measured directly as the result of the conversion. This figure can be subtracted from subsequent conversions with the same gain setting to reduce offset error to below 1 LSW.

The on-chip temperature sensor is selected by writing the code “1111” to the MUX[3:0] bits in ADMUX register when the ADC4 channel is used as an ADC input.

The ADC is enabled by setting the ADC Enable bit, ADEN in ADCSRA. Voltage reference and input channel selections will not go into effect until ADEN is set. The ADC does not consume power when ADEN is cleared, so it is recommended to switch off the ADC before entering power saving sleep modes.

The ADC generates a 10-bit result which is presented in the ADC Data Registers, ADCH and ADCL. By default, the result is presented right adjusted, but can optionally be presented left adjusted by setting the ADLAR bit in ADMUX.

If the result is left adjusted and no more than 8-bit precision is required, it is sufficient to read ADCH. Otherwise, ADCL must be read first, then ADCH, to ensure that the content of the data registers belongs to the same conversion. Once ADCL is read, ADC access to data registers is blocked. This means that if ADCL has been read, and a conversion completes before ADCH is read, neither register is updated and the result from the conversion is lost. When ADCH is read, ADC access to the ADCH and ADCL Registers is re-enabled.

The ADC has its own interrupt which can be triggered when a conversion completes. When ADC access to the data registers is prohibited between reading of ADCH and ADCL, the interrupt will trigger even if the result is lost.

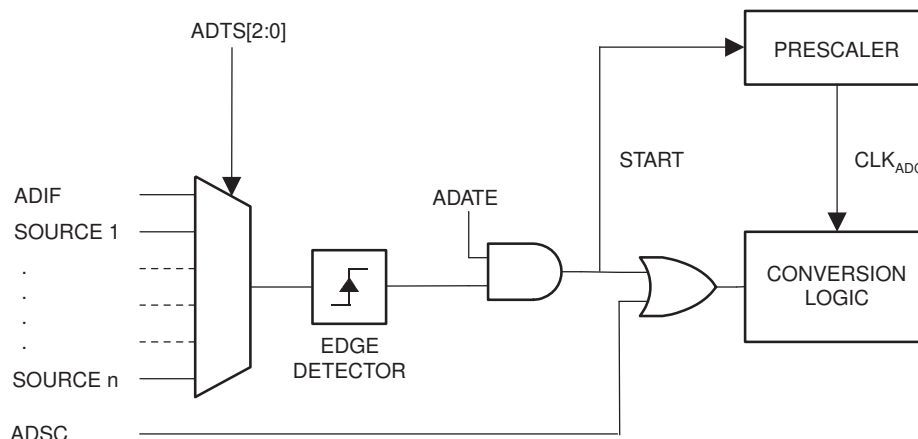
## 17.4 Starting a Conversion

A single conversion is started by writing a logical one to the ADC Start Conversion bit, ADSC. This bit stays high as long as the conversion is in progress and will be cleared by hardware when the conversion is completed. If a different data channel is selected while a conversion is in progress, the ADC will finish the current conversion before performing the channel change.

Alternatively, a conversion can be triggered automatically by various sources. Auto Triggering is enabled by setting the ADC Auto Trigger Enable bit, ADATE in ADCSRA. The trigger source is selected by setting the ADC Trigger Select bits, ADTS in ADCSRB (see description of the ADTS bits for a list of the trigger sources). When a positive edge occurs on the selected trigger signal, the ADC prescaler is reset and a conversion is started. This provides a method of starting conversions at fixed intervals. If the trigger signal still is set when the conversion completes, a new conversion will not be started. If another positive edge occurs on the trigger signal during conversion, the edge will be ignored. Note that an Interrupt Flag will be set even if the specific interrupt is disabled or the Global Interrupt Enable bit in SREG is cleared. A conversion can thus be triggered without causing an interrupt. However, the Interrupt Flag must be cleared in order to trigger a new conversion at the next interrupt event.

Using the ADC Interrupt Flag as a trigger source makes the ADC start a new conversion as soon as the ongoing conversion has finished. The ADC then operates in Free Running mode, constantly sampling and updating the ADC Data Register. The first conversion must be started by writing a logical one to the ADSC bit in ADCSRA. In this mode the ADC will perform successive conversions independently of whether the ADC Interrupt Flag, ADIF is cleared or not.

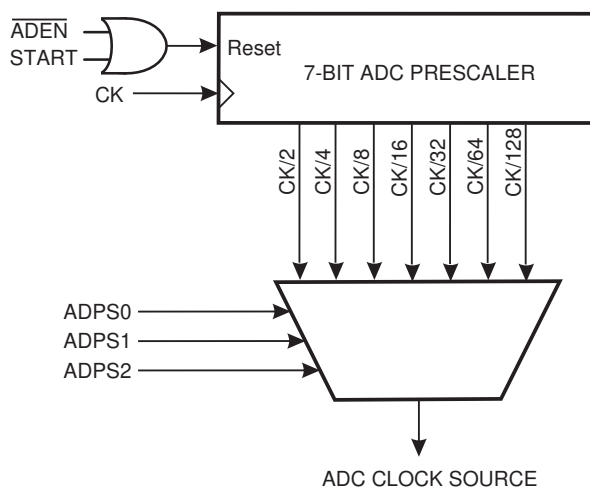
**Figure 17-2.** ADC Auto Trigger Logic



If Auto Triggering is enabled, single conversions can be started by writing ADSC in ADCSRA to one. ADSC can also be used to determine if a conversion is in progress. The ADSC bit will be read as one during a conversion, independently of how the conversion was started.

## 17.5 Prescaling and Conversion Timing

**Figure 17-3.** ADC Prescaler



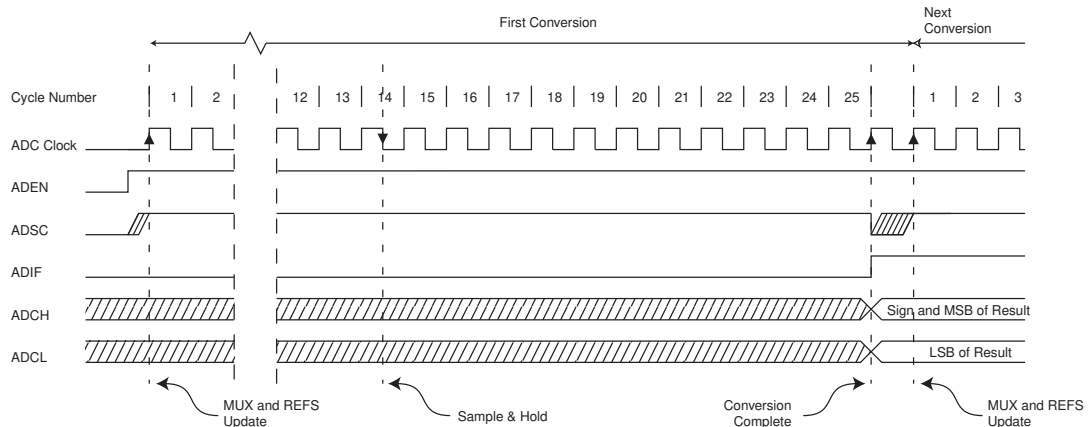
By default, the successive approximation circuitry requires an input clock frequency between 50 kHz and 200 kHz to get maximum resolution. If a lower resolution than 10 bits is needed, the input clock frequency to the ADC can be higher than 200 kHz to get a higher sample rate. It is not recommended to use a higher input clock frequency than 1 MHz.

The ADC module contains a prescaler, which generates an acceptable ADC clock frequency from any CPU frequency above 100 kHz. The prescaling is set by the ADPS bits in ADCSRA. The prescaler starts counting from the moment the ADC is switched on by setting the ADEN bit in ADCSRA. The prescaler keeps running for as long as the ADEN bit is set, and is continuously reset when ADEN is low.

When initiating a single ended conversion by setting the ADSC bit in ADCSRA, the conversion starts at the following rising edge of the ADC clock cycle.

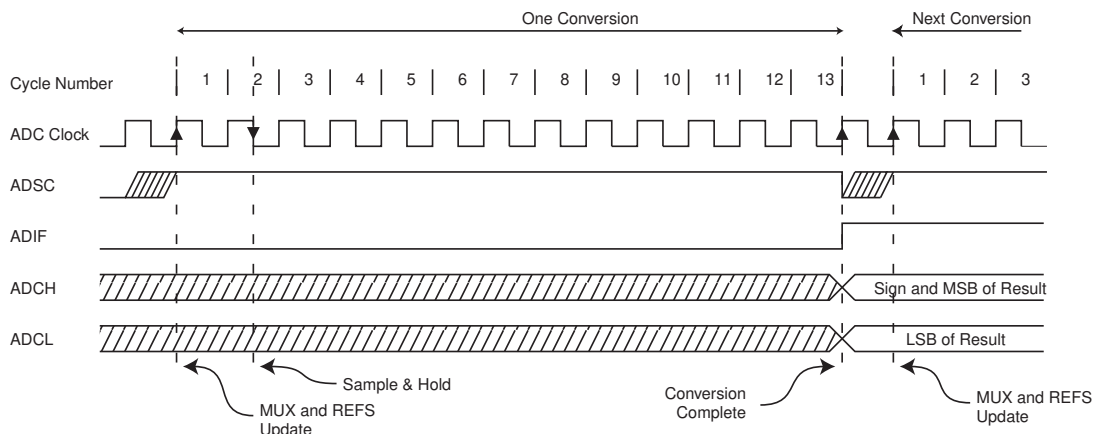
A normal conversion takes 13 ADC clock cycles. The first conversion after the ADC is switched on (ADEN in ADC-SRA is set) takes 25 ADC clock cycles in order to initialize the analog circuitry, as shown in [Figure 17-4](#) below.

**Figure 17-4.** ADC Timing Diagram, First Conversion (Single Conversion Mode)



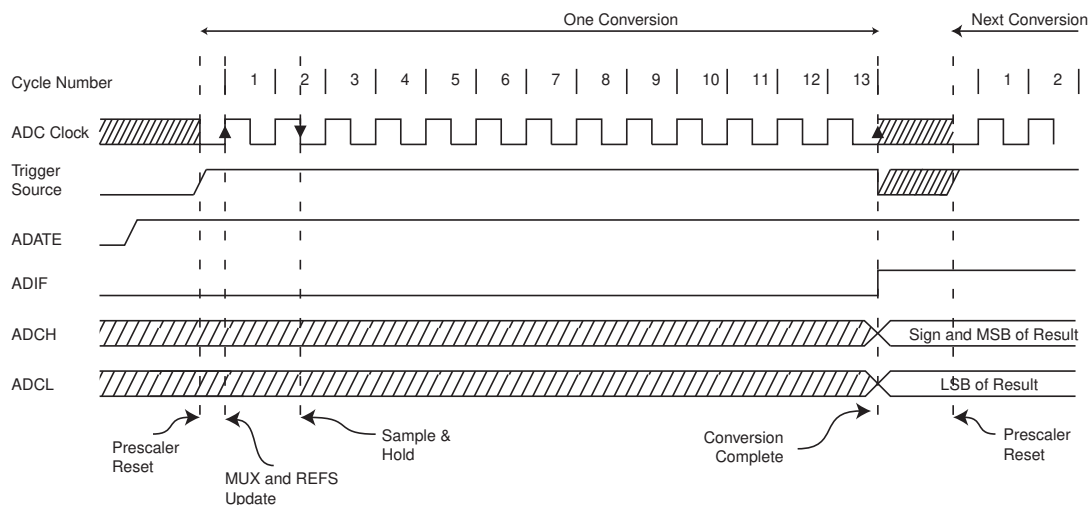
The actual sample-and-hold takes place 1.5 ADC clock cycles after the start of a normal conversion and 13.5 ADC clock cycles after the start of an first conversion. When a conversion is complete, the result is written to the ADC Data Registers, and ADIF is set. In Single Conversion mode, ADSC is cleared simultaneously. The software may then set ADSC again, and a new conversion will be initiated on the first rising ADC clock edge.

**Figure 17-5.** ADC Timing Diagram, Single Conversion



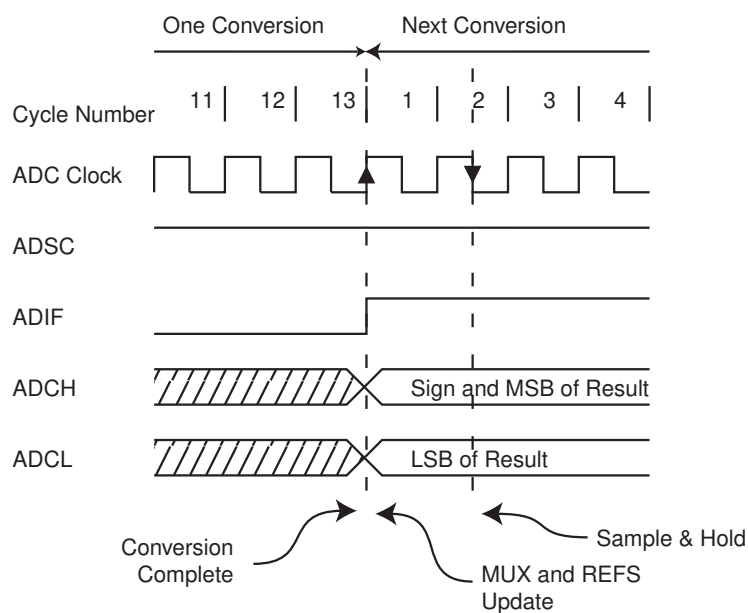
When Auto Triggering is used, the prescaler is reset when the trigger event occurs. This assures a fixed delay from the trigger event to the start of conversion. In this mode, the sample-and-hold takes place two ADC clock cycles after the rising edge on the trigger source signal. Three additional CPU clock cycles are used for synchronization logic.

**Figure 17-6.** ADC Timing Diagram, Auto Triggered Conversion



In Free Running mode, a new conversion will be started immediately after the conversion completes, while ADSC remains high.

**Figure 17-7.** ADC Timing Diagram, Free Running Conversion



For a summary of conversion times, see [Table 17-1](#).

**Table 17-1.** ADC Conversion Time

Condition	Sample & Hold (Cycles from Start of Conversion)	Total Conversion Time (Cycles)
First conversion	13.5	25
Normal conversions	1.5	13
Auto Triggered conversions	2	13.5

## 17.6 Changing Channel or Reference Selection

The MUX[3:0] and REFS[2:0] bits in the ADMUX Register are single buffered through a temporary register to which the CPU has random access. This ensures that the channels and voltage reference selection only takes place at a safe point during the conversion. The channel and voltage reference selection is continuously updated until a conversion is started. Once the conversion starts, the channel and voltage reference selection is locked to ensure a sufficient sampling time for the ADC. Continuous updating resumes in the last ADC clock cycle before the conversion completes (ADIF in ADCSRA is set). Note that the conversion starts on the following rising ADC clock edge after ADSC is written. The user is thus advised not to write new channel or voltage reference selection values to ADMUX until one ADC clock cycle after ADSC is written.

If Auto Triggering is used, the exact time of the triggering event can be indeterministic. Special care must be taken when updating the ADMUX Register, in order to control which conversion will be affected by the new settings.

If both ADATE and ADEN is written to one, an interrupt event can occur at any time. If the ADMUX Register is changed in this period, the user cannot tell if the next conversion is based on the old or the new settings. ADMUX can be safely updated in the following ways:

- When ADATE or ADEN is cleared.
- During conversion, minimum one ADC clock cycle after the trigger event.
- After a conversion, before the Interrupt Flag used as trigger source is cleared.

When updating ADMUX in one of these conditions, the new settings will affect the next ADC conversion.

### 17.6.1 ADC Input Channels

When changing channel selections, the user should observe the following guidelines to ensure that the correct channel is selected:

In Single Conversion mode, always select the channel before starting the conversion. The channel selection may be changed one ADC clock cycle after writing one to ADSC. However, the simplest method is to wait for the conversion to complete before changing the channel selection.

In Free Running mode, always select the channel before starting the first conversion. The channel selection may be changed one ADC clock cycle after writing one to ADSC. However, the simplest method is to wait for the first conversion to complete, and then change the channel selection. Since the next conversion has already started automatically, the next result will reflect the previous channel selection. Subsequent conversions will reflect the new channel selection.

### 17.6.2 ADC Voltage Reference

The voltage reference for the ADC ( $V_{REF}$ ) indicates the conversion range for the ADC. Single ended channels that exceed  $V_{REF}$  will result in codes close to 0x3FF.  $V_{REF}$  can be selected as either  $V_{CC}$ , or internal 1.1V / 2.56V voltage reference, or external AREF pin. The first ADC conversion result after switching voltage reference source may be inaccurate, and the user is advised to discard this result.

## 17.7 ADC Noise Canceler

The ADC features a noise canceler that enables conversion during sleep mode to reduce noise induced from the CPU core and other I/O peripherals. The noise canceler can be used with ADC Noise Reduction and Idle mode. To make use of this feature, the following procedure should be used:

- Make sure that the ADC is enabled and is not busy converting. Single Conversion mode must be selected and the ADC conversion complete interrupt must be enabled.
- Enter ADC Noise Reduction mode (or Idle mode). The ADC will start a conversion once the CPU has been halted.
- If no other interrupts occur before the ADC conversion completes, the ADC interrupt will wake up the CPU and execute the ADC Conversion Complete interrupt routine. If another interrupt wakes up the CPU before the ADC

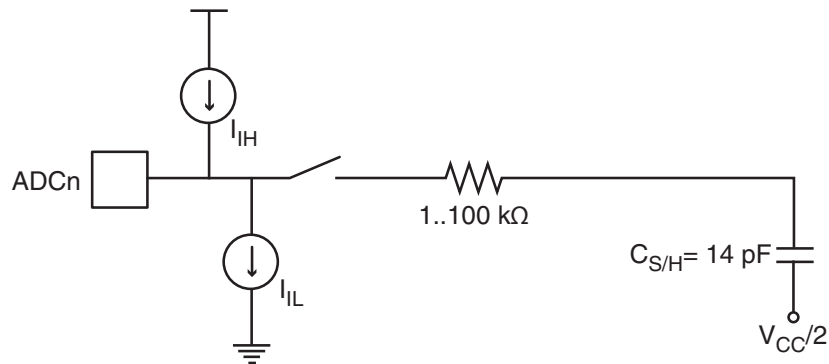
conversion is complete, that interrupt will be executed, and an ADC Conversion Complete interrupt request will be generated when the ADC conversion completes. The CPU will remain in active mode until a new sleep command is executed.

Note that the ADC will not be automatically turned off when entering other sleep modes than Idle mode and ADC Noise Reduction mode. The user is advised to write zero to ADEN before entering such sleep modes to avoid excessive power consumption.

## 17.8 Analog Input Circuitry

The analog input circuitry for single ended channels is illustrated in Figure 17-8. An analog source applied to ADCn is subjected to the pin capacitance and input leakage of that pin, regardless of whether that channel is selected as input for the ADC. When the channel is selected, the source must drive the S/H capacitor through the series resistance (combined resistance in the input path).

**Figure 17-8.** Analog Input Circuitry



The ADC is optimized for analog signals with an output impedance of approximately 10 kΩ or less. If such a source is used, the sampling time will be negligible. If a source with higher impedance is used, the sampling time will depend on how long time the source needs to charge the S/H capacitor, with can vary widely. The user is recommended to only use low impedant sources with slowly varying signals, since this minimizes the required charge transfer to the S/H capacitor.

Signal components higher than the Nyquist frequency ( $f_{ADC}/2$ ) should not be present to avoid distortion from unpredictable signal convolution. The user is advised to remove high frequency components with a low-pass filter before applying the signals as inputs to the ADC.

## 17.9 Noise Canceling Techniques

Digital circuitry inside and outside the device generates EMI which might affect the accuracy of analog measurements. If conversion accuracy is critical, the noise level can be reduced by applying the following techniques:

- Keep analog signal paths as short as possible.
- Make sure analog tracks run over the analog ground plane.
- Keep analog tracks well away from high-speed switching digital tracks.
- If any port pin is used as a digital output, it mustn't switch while a conversion is in progress.
- Place bypass capacitors as close to  $V_{CC}$  and GND pins as possible.

Where high ADC accuracy is required it is recommended to use ADC Noise Reduction Mode, as described in [Section 17.7 on page 128](#). This is especially the case when system clock frequency is above 1 MHz, or when the ADC



is used for reading the internal temperature sensor, as described in [Section 17.12 on page 133](#). A good system design with properly placed, external bypass capacitors does reduce the need for using ADC Noise Reduction Mode

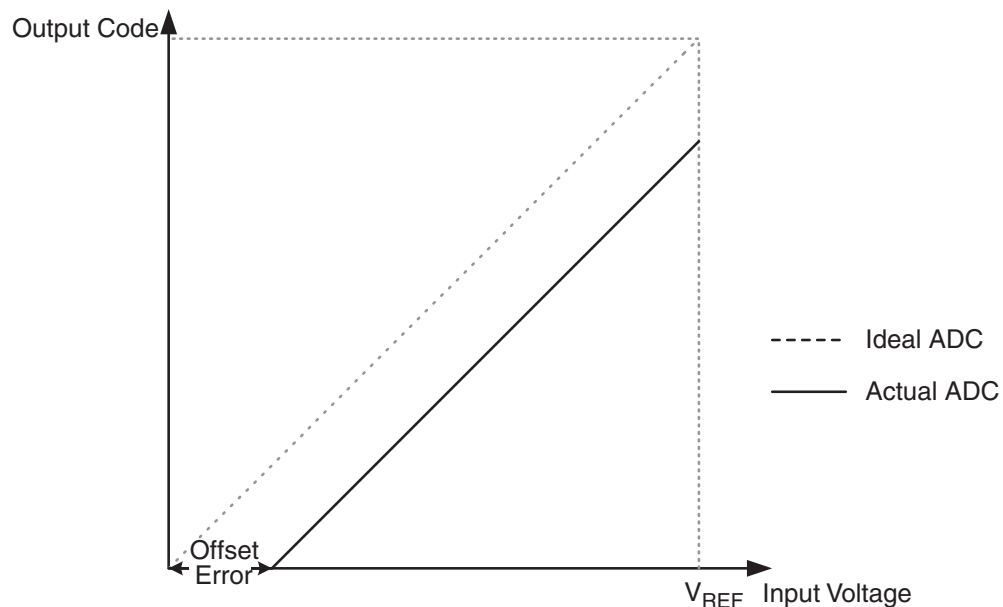
## 17.10 ADC Accuracy Definitions

An n-bit single-ended ADC converts a voltage linearly between GND and  $V_{REF}$  in  $2^n$  steps (LSBs). The lowest code is read as 0, and the highest code is read as  $2^n-1$ .

Several parameters describe the deviation from the ideal behavior, as follows:

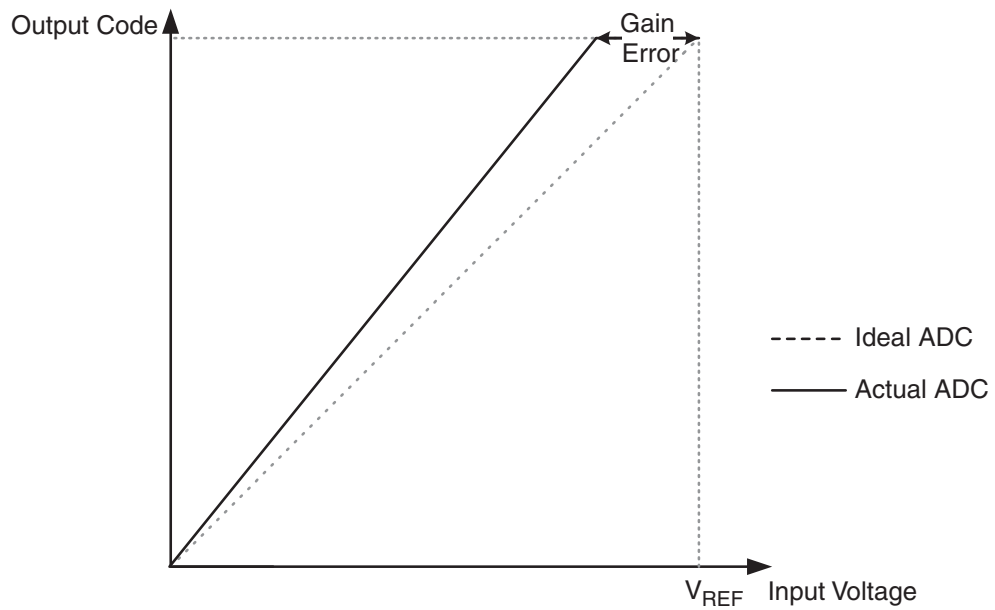
- Offset: The deviation of the first transition (0x000 to 0x001) compared to the ideal transition (at 0.5 LSB). Ideal value: 0 LSB.

**Figure 17-9.** Offset Error



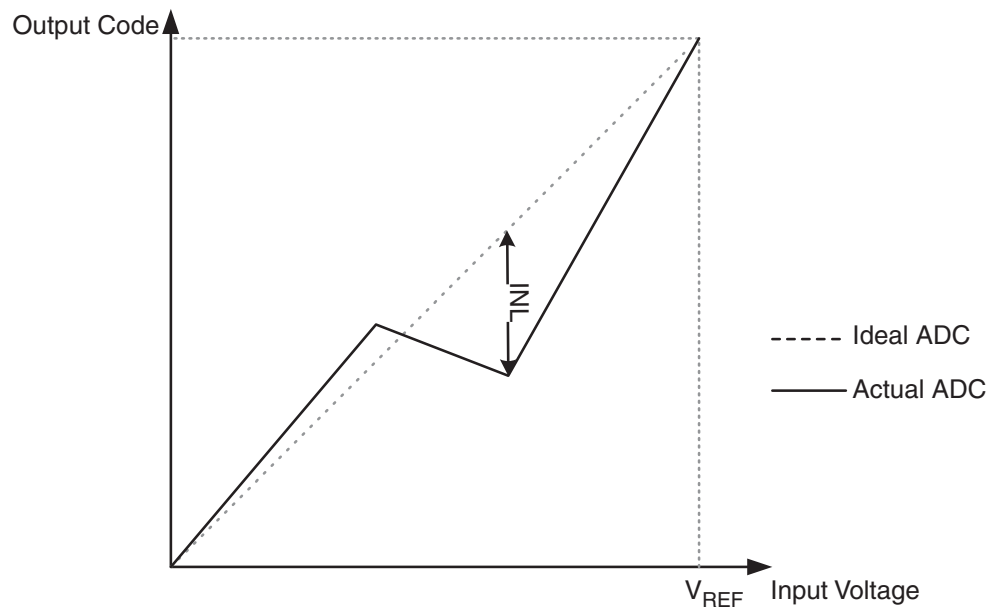
- Gain Error: After adjusting for offset, the Gain Error is found as the deviation of the last transition (0x3FE to 0x3FF) compared to the ideal transition (at 1.5 LSB below maximum). Ideal value: 0 LSB

**Figure 17-10. Gain Error**



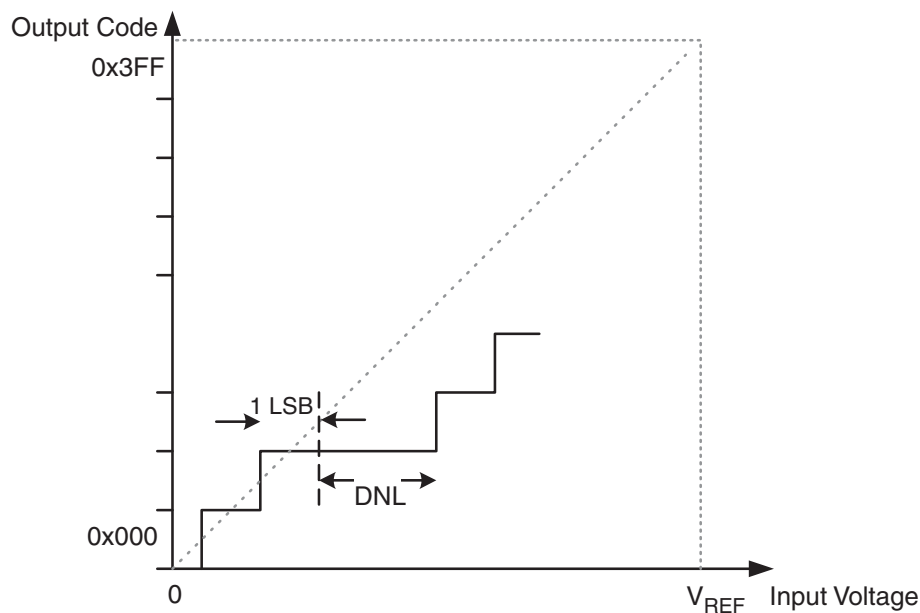
- Integral Non-linearity (INL): After adjusting for offset and gain error, the INL is the maximum deviation of an actual transition compared to an ideal transition for any code. Ideal value: 0 LSB.

**Figure 17-11. Integral Non-linearity (INL)**



- Differential Non-linearity (DNL): The maximum deviation of the actual code width (the interval between two adjacent transitions) from the ideal code width (1 LSB). Ideal value: 0 LSB.

**Figure 17-12. Differential Non-linearity (DNL)**



- **Quantization Error:** Due to the quantization of the input voltage into a finite number of codes, a range of input voltages (1 LSB wide) will code to the same value. Always  $\pm 0.5$  LSB.
- **Absolute Accuracy:** The maximum deviation of an actual (unadjusted) transition compared to an ideal transition for any code. This is the compound effect of offset, gain error, differential error, non-linearity, and quantization error. Ideal value:  $\pm 0.5$  LSB.

## 17.11 ADC Conversion Result

After the conversion is complete (ADIF is high), the conversion result can be found in the ADC Result Registers (ADCL, ADCH). The form of the conversion result depends on the type of the conversion as there are three types of conversions: single ended conversion, unipolar differential conversion and bipolar differential conversion.

### 17.11.1 Single Ended Conversion

For single ended conversion, the result is

$$ADC = \frac{V_{IN} \cdot 1024}{V_{REF}}$$

where  $V_{IN}$  is the voltage on the selected input pin and  $V_{REF}$  the selected voltage reference (see [Table 17-3 on page 134](#) and [Table 17-4 on page 135](#)). 0x000 represents analog ground, and 0x3FF represents the selected voltage reference minus one LSB. The result is presented in one-sided form, from 0x3FF to 0x000.

### 17.11.2 Unipolar Differential Conversion

If differential channels and an unipolar input mode are used, the result is

$$ADC = \frac{(V_{POS} - V_{NEG}) \cdot 1024}{V_{REF}} \cdot GAIN$$

where  $V_{POS}$  is the voltage on the positive input pin,  $V_{NEG}$  the voltage on the negative input pin, and  $V_{REF}$  the selected voltage reference (see [Table 17-3 on page 134](#) and [Table 17-4 on page 135](#)). The voltage on the positive pin must always be larger than the voltage on the negative pin or otherwise the voltage difference is saturated to zero. The result is presented in one-sided form, from 0x000 (0d) to 0x3FF (+1023d). The GAIN is either 1x or 20x.

### 17.11.3 Bipolar Differential Conversion

As default the ADC converter operates in the unipolar input mode, but the bipolar input mode can be selected by writing the BIN bit in the ADCSRB to one. In the bipolar input mode two-sided voltage differences are allowed and thus the voltage on the negative input pin can also be larger than the voltage on the positive input pin. If differential channels and a bipolar input mode are used, the result is

$$ADC = \frac{(V_{POS} - V_{NEG}) \cdot 512}{V_{REF}} \cdot GAIN$$

where  $V_{POS}$  is the voltage on the positive input pin,  $V_{NEG}$  the voltage on the negative input pin, and  $V_{REF}$  the selected voltage reference. The result is presented in two's complement form, from 0x200 (-512d) through 0x000 (+0d) to 0x1FF (+511d). The GAIN is either 1x or 20x.

However, if the signal is not bipolar by nature (9 bits + sign as the 10th bit), this scheme loses one bit of the converter dynamic range. Then, if the user wants to perform the conversion with the maximum dynamic range, the user can perform a quick polarity check of the result and use the unipolar differential conversion with selectable differential input pairs (see the Input Polarity Reversal mode ie. the IPR bit in the [“ADCSRB – ADC Control and Status Register B” on page 137](#)). When the polarity check is performed, it is sufficient to read the MSB of the result (ADC9 in ADCH). If the bit is one, the result is negative, and if this bit is zero, the result is positive.

## 17.12 Temperature Measurement

The temperature measurement is based on an on-chip temperature sensor that is coupled to a single ended ADC4 channel. Selecting the ADC4 channel by writing the MUX[3:0] bits in ADMUX register to “1111” enables the temperature sensor. The internal 1.1V reference must also be selected for the ADC reference source in the temperature sensor measurement. When the temperature sensor is enabled, the ADC converter can be used in single conversion mode to measure the voltage over the temperature sensor.

The measured voltage has a linear relationship to the temperature as described in [Table 17-2](#). The sensitivity is approximately 1 LSB / °C and the accuracy depends on the method of user calibration. Typically, the measurement accuracy after a single temperature calibration is ±10°C, assuming calibration at room temperature. Better accuracies are achieved by using two temperature points for calibration.

**Table 17-2.** Temperature vs. Sensor Output Voltage (Typical Case)

Temperature	-40°C	+25°C	+85°C
ADC	230 LSB	300 LSB	370 LSB

The values described in [Table 17-2](#) are typical values. However, due to process variation the temperature sensor output voltage varies from one chip to another. To be capable of achieving more accurate results the temperature measurement can be calibrated in the application software. The software calibration can be done using the formula:

$$T = k * [(ADCH \ll 8) \mid ADCL] + T_{OS}$$

where ADCH and ADCL are the ADC data registers,  $k$  is the fixed slope coefficient and  $T_{OS}$  is the temperature sensor offset. Typically,  $k$  is very close to 1.0 and in single-point calibration the coefficient may be omitted. Where higher accuracy is required the slope coefficient should be evaluated based on measurements at two temperatures.

## 17.13 Register Description

### 17.13.1 ADMUX – ADC Multiplexer Selection Register

Bit	7	6	5	4	3	2	1	0	
0x07	REFS1	REFS0	ADLAR	REFS2	MUX3	MUX2	MUX1	MUX0	ADMUX
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 7:6, 4 – REFS[2:0]: Voltage Reference Selection Bits**

These bits select the voltage reference ( $V_{REF}$ ) for the ADC, as shown in Table 17-3. If these bits are changed during a conversion, the change will not go in effect until this conversion is complete (ADIF in ADCSR is set). Whenever these bits are changed, the next conversion will take 25 ADC clock cycles. When differential channels and gain are used, using  $V_{CC}$  or an external AREF higher than ( $V_{CC} - 1V$ ) as a voltage reference is not recommended as this will affect the ADC accuracy.

**Table 17-3.** Voltage Reference Selections for ADC

REFS2	REFS1	REFS0	Voltage Reference ( $V_{REF}$ ) Selection
X	0	0	$V_{CC}$ used as Voltage Reference, disconnected from PB0 (AREF).
X	0	1	External Voltage Reference at PB0 (AREF) pin, Internal Voltage Reference turned off.
0	1	0	Internal 1.1V Voltage Reference.
0	1	1	Reserved
1	1	0	Internal 2.56V Voltage Reference without external bypass capacitor, disconnected from PB0 (AREF) <sup>(1)</sup> .
1	1	1	Internal 2.56V Voltage Reference with external bypass capacitor at PB0 (AREF) pin <sup>(1)</sup> .

Note: 1. The device requires a supply voltage of 3V in order to generate 2.56V reference voltage.

- **Bit 5 – ADLAR: ADC Left Adjust Result**

The ADLAR bit affects the presentation of the ADC conversion result in the ADC Data Register. Write one to ADLAR to left adjust the result. Otherwise, the result is right adjusted. Changing the ADLAR bit will affect the ADC Data Register immediately, regardless of any ongoing conversions. For a complete description of this bit, see “ADCL and ADCH – The ADC Data Register” on page 137.

- **Bits 3:0 – MUX[3:0]: Analog Channel and Gain Selection Bits**

The value of these bits selects which combination of analog inputs are connected to the ADC. In case of differential input (ADC0 - ADC1 or ADC2 - ADC3), gain selection is also made with these bits. Selecting ADC2 or ADC0 as both inputs to the differential gain stage enables offset measurements. Selecting the single-ended channel ADC4

enables the temperature sensor. Refer to [Table 17-4](#) for details. If these bits are changed during a conversion, the change will not go into effect until this conversion is complete (ADIF in ADCSRA is set).

**Table 17-4.** Input Channel Selections

MUX[3:0]	Single Ended Input	Positive Differential Input	Negative Differential Input	Gain
0000	ADC0 (PB5)	N/A		
0001	ADC1 (PB2)			
0010	ADC2 (PB4)			
0011	ADC3 (PB3)			
0100	N/A	ADC2 (PB4)	ADC2 (PB4)	1x
0101 <sup>(1)</sup>		ADC2 (PB4)	ADC2 (PB4)	20x
0110		ADC2 (PB4)	ADC3 (PB3)	1x
0111		ADC2 (PB4)	ADC3 (PB3)	20x
1000		ADC0 (PB5)	ADC0 (PB5)	1x
1001		ADC0 (PB5)	ADC0 (PB5)	20x
1010		ADC0 (PB5)	ADC1 (PB2)	1x
1011		ADC0 (PB5)	ADC1 (PB2)	20x
1100 <sup>(2)</sup>	V <sub>BG</sub>	N/A		
1101	GND			
1110	N/A			
1111 <sup>(3)</sup>	ADC4			

- Note:
1. For offset calibration, only. See [“Operation” on page 123](#).
  2. After switching to internal voltage reference the ADC requires a settling time of 1ms before measurements are stable. Conversions starting before this may not be reliable. The ADC must be enabled during the settling time.
  3. For temperature sensor.

### 17.13.2 ADCSRA – ADC Control and Status Register A

Bit	7	6	5	4	3	2	1	0	
0x06	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	ADCSRA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – ADEN: ADC Enable**

Writing this bit to one enables the ADC. By writing it to zero, the ADC is turned off. Turning the ADC off while a conversion is in progress, will terminate this conversion.

- **Bit 6 – ADSC: ADC Start Conversion**

In Single Conversion mode, write this bit to one to start each conversion. In Free Running mode, write this bit to one to start the first conversion. The first conversion after ADSC has been written after the ADC has been enabled, or if ADSC is written at the same time as the ADC is enabled, will take 25 ADC clock cycles instead of the normal 13. This first conversion performs initialization of the ADC.

ADSC will read as one as long as a conversion is in progress. When the conversion is complete, it returns to zero. Writing zero to this bit has no effect.

- **Bit 5 – ADATE: ADC Auto Trigger Enable**

When this bit is written to one, Auto Triggering of the ADC is enabled. The ADC will start a conversion on a positive edge of the selected trigger signal. The trigger source is selected by setting the ADC Trigger Select bits, ADTS in ADCSRB.

- **Bit 4 – ADIF: ADC Interrupt Flag**

This bit is set when an ADC conversion completes and the data registers are updated. The ADC Conversion Complete Interrupt is executed if the ADIE bit and the I-bit in SREG are set. ADIF is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, ADIF is cleared by writing a logical one to the flag. Beware that if doing a Read-Modify-Write on ADCSRA, a pending interrupt can be disabled. This also applies if the SBI and CBI instructions are used.

- **Bit 3 – ADIE: ADC Interrupt Enable**

When this bit is written to one and the I-bit in SREG is set, the ADC Conversion Complete Interrupt is activated.

- **Bits 2:0 – ADPS[2:0]: ADC Prescaler Select Bits**

These bits determine the division factor between the system clock frequency and the input clock to the ADC.

**Table 17-5.** ADC Prescaler Selections

ADPS2	ADPS1	ADPS0	Division Factor
0	0	0	2
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

### 17.13.3 ADCL and ADCH – The ADC Data Register

#### 17.13.3.1 ADLAR = 0

Bit	15	14	13	12	11	10	9	8	
0x05	–	–	–	–	–	–	ADC9	ADC8	ADCH
0x04	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	ADCL
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R	R	R	R	
	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

#### 17.13.3.2 ADLAR = 1

Bit	15	14	13	12	11	10	9	8	
0x05	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADCH
0x04	ADC1	ADC0	–	–	–	–	–	–	ADCL
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R	R	R	R	
	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

When an ADC conversion is complete, the result is found in these two registers.

When ADCL is read, the ADC Data Register is not updated until ADCH is read. Consequently, if the result is left adjusted and no more than 8-bit precision is required, it is sufficient to read ADCH. Otherwise, ADCL must be read first, then ADCH.

The ADLAR bit in ADMUX, and the MUXn bits in ADMUX affect the way the result is read from the registers. If ADLAR is set, the result is left adjusted. If ADLAR is cleared (default), the result is right adjusted.

- **Bits 9:0 - ADC[9:0]: ADC Conversion Result**

These bits represent the result from the conversion, as detailed in [“ADC Conversion Result” on page 132](#).

### 17.13.4 ADCSRB – ADC Control and Status Register B

Bit	7	6	5	4	3	2	1	0	
0x03	BIN	ACME	IPR	–	–	ADTS2	ADTS1	ADTS0	ADCSRB
Read/Write	R/W	R/W	R/W	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – BIN: Bipolar Input Mode**

The gain stage is working in the unipolar mode as default, but the bipolar mode can be selected by writing the BIN bit in the ADCSRB register. In the unipolar mode only one-sided conversions are supported and the voltage on the positive input must always be larger than the voltage on the negative input. Otherwise the result is saturated to the voltage reference. In the bipolar mode two-sided conversions are supported and the result is represented in the two's complement form. In the unipolar mode the resolution is 10 bits and the bipolar mode the resolution is 9 bits + 1 sign bit.

- **Bit 5 – IPR: Input Polarity Reversal**

The Input Polarity mode allows software selectable differential input pairs and full 10 bit ADC resolution, in the unipolar input mode, assuming a pre-determined input polarity. If the input polarity is not known it is actually possible to determine the polarity first by using the bipolar input mode (with 9 bit resolution + 1 sign bit ADC measurement). And once determined, set or clear the polarity reversal bit, as needed, for a succeeding 10 bit unipolar measurement.



- **Bits 4:3 – Res: Reserved Bits**

These bits are reserved bits in the ATtiny25/45/85 and will always read as zero.

- **Bits 2:0 – ADTS[2:0]: ADC Auto Trigger Source**

If ADSC in ADCSRA is written to one, the value of these bits selects which source will trigger an ADC conversion. If ADSC is cleared, the ADTS[2:0] settings will have no effect. A conversion will be triggered by the rising edge of the selected Interrupt Flag. Note that switching from a trigger source that is cleared to a trigger source that is set, will generate a positive edge on the trigger signal. If ADEN in ADCSRA is set, this will start a conversion. Switching to Free Running mode (ADTS[2:0]=0) will not cause a trigger event, even if the ADC Interrupt Flag is set.

**Table 17-6.** ADC Auto Trigger Source Selections

ADTS2	ADTS1	ADTS0	Trigger Source
0	0	0	Free Running mode
0	0	1	Analog Comparator
0	1	0	External Interrupt Request 0
0	1	1	Timer/Counter0 Compare Match A
1	0	0	Timer/Counter0 Overflow
1	0	1	Timer/Counter0 Compare Match B
1	1	0	Pin Change Interrupt Request

#### 17.13.5 DIDR0 – Digital Input Disable Register 0

Bit	7	6	5	4	3	2	1	0	
0x14	–	–	ADC0D	ADC2D	ADC3D	ADC1D	AIN1D	AIN0D	DIDR0
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 5:2 – ADC3D:ADC0D: ADC[3:0] Digital Input Disable**

When this bit is written logic one, the digital input buffer on the corresponding ADC pin is disabled. The corresponding PIN register bit will always read as zero when this bit is set. When an analog signal is applied to the ADC[3:0] pin and the digital input from this pin is not needed, this bit should be written logic one to reduce power consumption in the digital input buffer.