Basics of SMPS (Switch Mode Power Supply) PCB Layout

Summary of points for SMPS Layout:

All Current always flows in loops…(and going through a capacitor can be a part of the current loop)

Keep the switching power current loops as narrow in area as possible (eg like close differential pair traces).

Minimise the "dirty" ground (the ground that carries fast rise time power switching currents)…ie don't route the "dirty" ground all over the PCB.

Don't run power switching currents through lengths of control ground (all SMPS's have controller circuits, which are connected to the 'control' ground)…this is because power switching currents can create voltage drops across lengths of control ground and "upset" the controller. (The voltage drops are due to switching current harmonics inter-acting with stray PCB track inductances)

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Principles of SMPS PCB Layout

As you know, the main principles are…….

1…..Avoid routing Switching Power current loops (currents with high di/dt's) along lengths of ground trace that would disturb analog control circuitry through "ground bounce". (voltage 'bouncing' in the ground due to V=L.di/dt, where L is the trace stray inductance)

…this is one of the main principles, and as you know, switching current loops are unfortunately also found in the FET gate drive current loops, as well in the general power current loops (Rectifier Loop and FET loop)

I am sure you are aware of the other principles, eg,

a…. reduce the area inside current loops by keeping "go" and "return" close together as much as possible.

b…. try and keep high dv/dt traces, eg the switching node , away from sensitive things like the inputs to the PWM comparator insIde the PWM controller IC.

c…..be aware of high dv/dt nodes capacitively coupling noise into adjacent metal areas, eg, the enclosure etc.

d….Be aware of the track thickness's needed to carry high currents without overheating the PCB and the components on it.

e…..Be aware, with high currents, that if you don't have much room for decent track thickness, then the voltage drop on eg the ground track will be significant, which as you know , isn't desirable.

NB:

Regarding V=L.di/dt, this means that the bigger the "***change***" in current through an inductor, L, then the bigger the voltage generated across that inductor.

Identify the SMPS power current loops

There are 4 main power current loops in an SMPS.

(Remember that all electric currents flow in a loop.)

The area inside all these loops should be as narrow as possible. (this is to minimise the inductance of these loops, and also to minimise their radiative effect).

1…Input loop
2…Power switch loop
3…Rectifier loop
4….Output loop

Note: For some SMPS topologies, (eg Full Bridge) there might be two "power switch loops". For some SMPS topologies, (eg those with a split secondary) there might be two "rectifier loops"

Also note that in many topologies, (eg boost converter), some parts of the "power switch" loop and the "rectifier" loop may overlap each other.
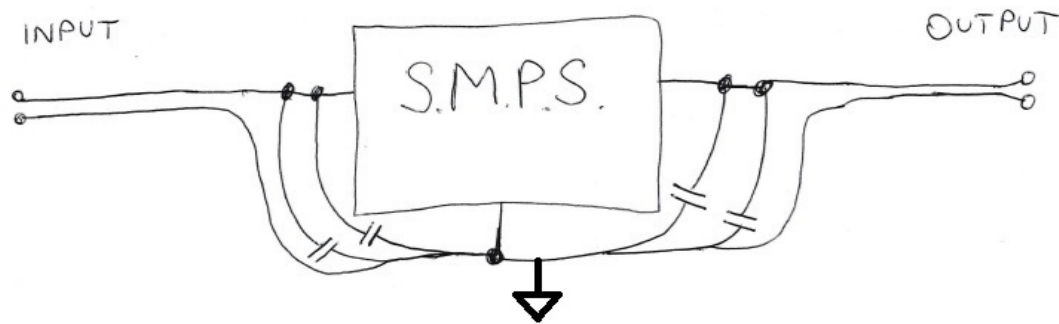
In fact, the one topology where the above 4 loops are most recogniseable and separate, is the flyback converter.

Basic diagram of the loops of an SMPS.
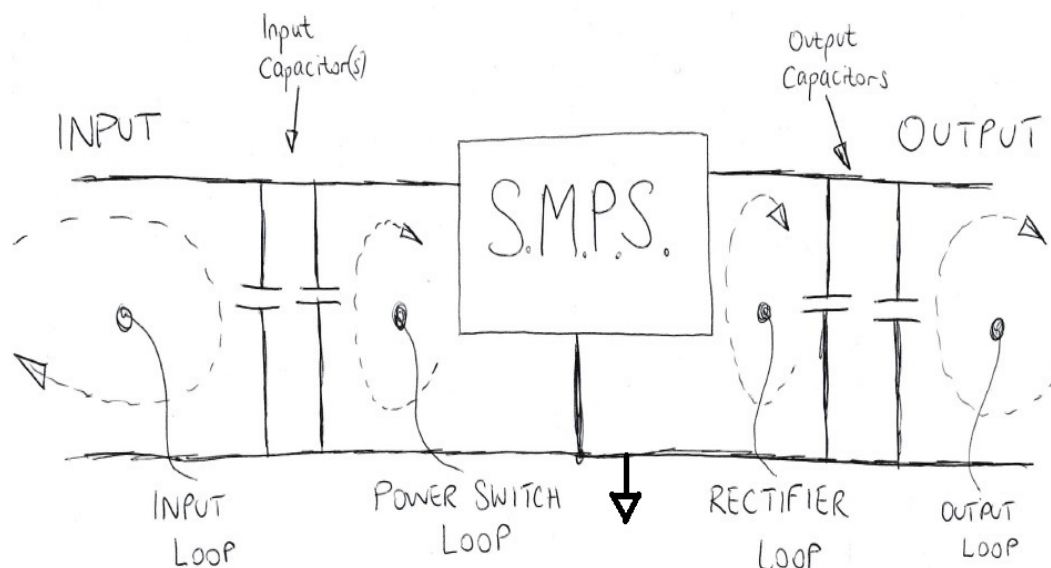
Note that these loops would actually be layed out more like the following…..

(also note that the box labelled "SMPS" refers to the switching stage of the SMPS, eg the FETs and diodes)

Note that its common to make the capacitor that's nearest the SMPS (in the input or output capacitor bank) a relatively small ceramic so that it can be "Hugged up" very close to the SMPS. (Some of the input or output capacitors may well be fairly large and so it will be more difficult to get those particular ones close in to the SMPS.)
The small ceramic that is placed very close to the SMPS makes a very small area current loop for the highest frequencies of the SMPS switching current. –This in turn is a good thing.
Remember that in a hard switched SMPS, the switching current waveform is actually composed of a large series of frequencies, which extend very high in frequency (much higher than the switching frequency). These high frequencies are called the "harmonics" of the switching frequency.

Here are the above 4 loops shown in some actual SMPS topologies:

Buck Converter:
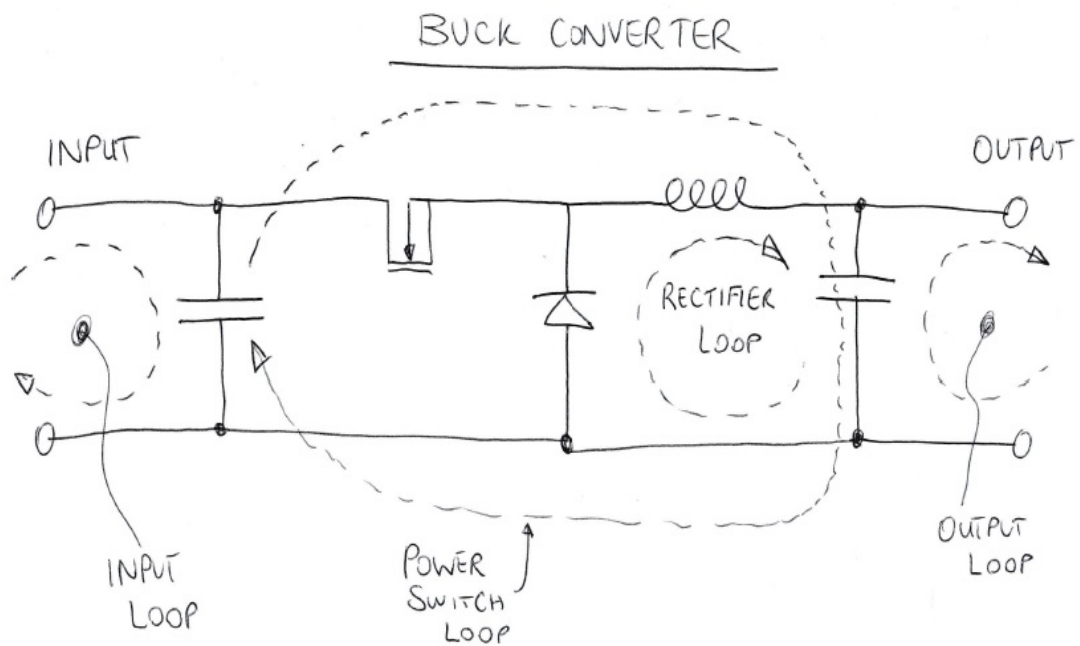
Boost Converter

Flyback converter

FLYBACK

INPUT

INPUT LOOP

POWER SWITCH LOOP

RECTIFIER LOOP

OUTPUT

OUTPUT LOOP
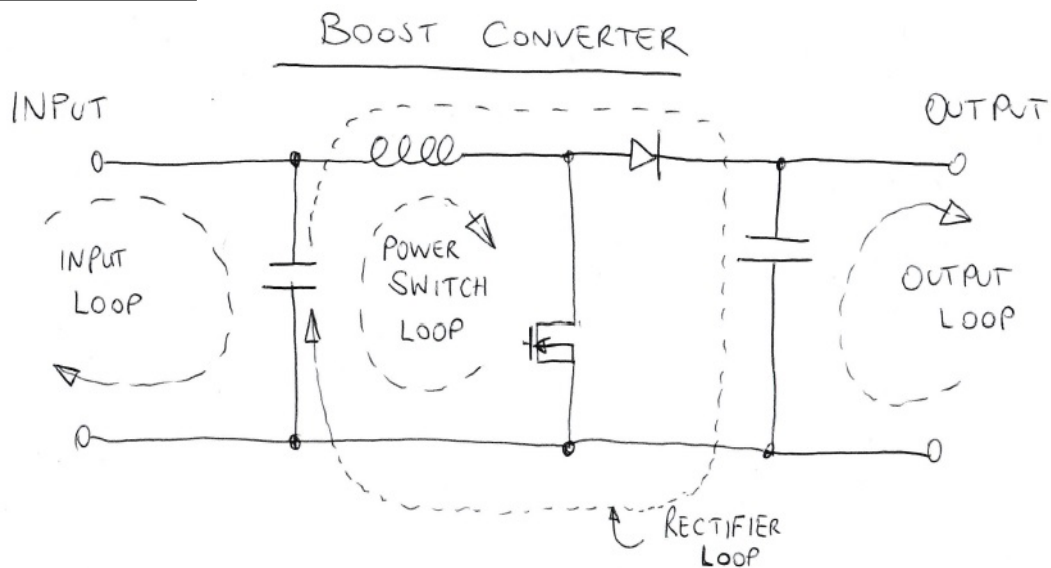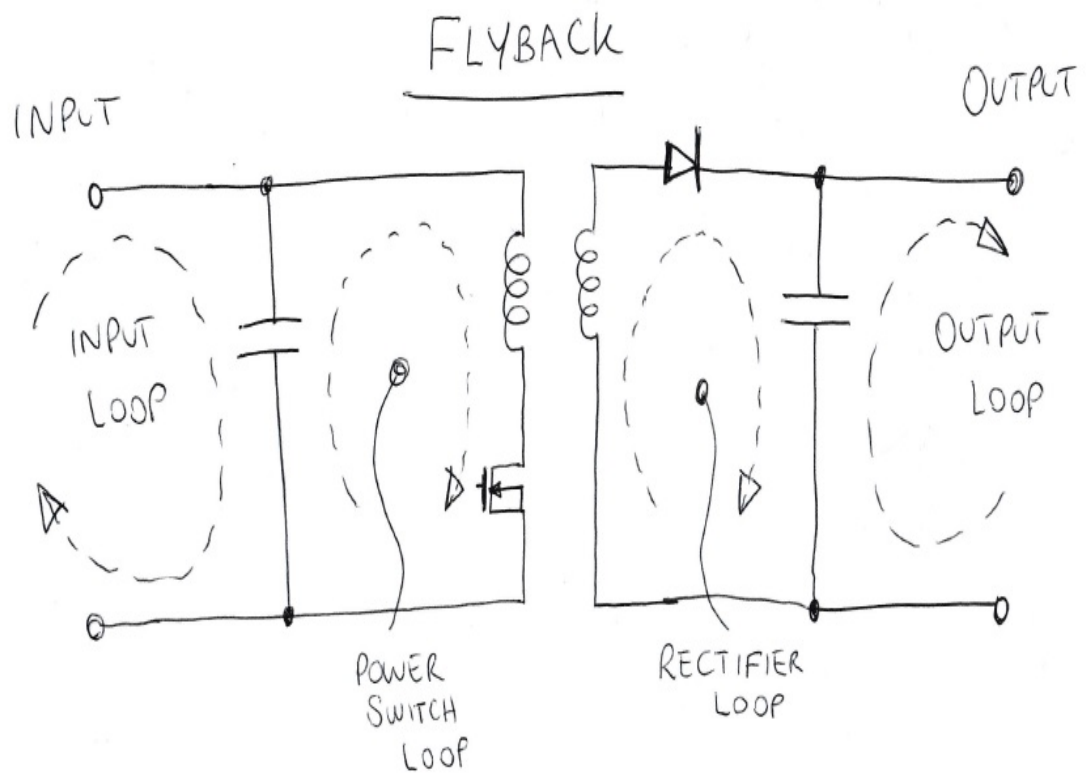
The "Dirty" Ground

The ground part of the "power switch" loop and the "rectifier" loop carrys very fast rise time power switching current. This is the kind of current that can be a nightmare for PCB layout. This is why it's called the "dirty" ground.

The Dirty ground should be minimised (as much as thermal considerations will allow) and not routed all over the PCB.

If you can't remember what is the "dirty" ground of an SMPS, then just remember that it is that bit of ground that lies in between the innermost input and output capacitors. (by "innermost" I mean near the switching stage of the SMPS, and not near the input and output connectors)

How NOT to route the 'dirty' ground of an SMPS…

INPUT   OUTPUT

S.M.P.S.

"DIRTY" GROUND BEING
ROUTED ALL OVER THE
PCB
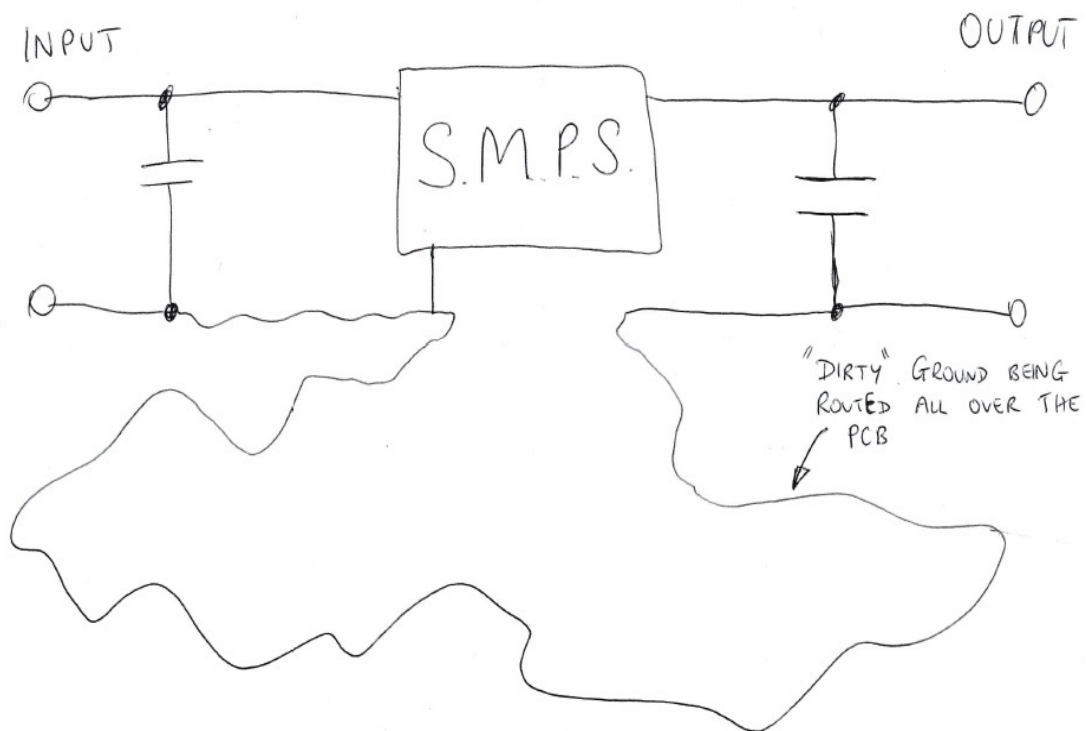
Net-Ties.
In order to help you to avoid the "dirty" ground from accidentally being routed round the PCB, it can help to use Net-Ties so that you can actually name the "dirty" ground as a different net to the main ground. A "net-tie" can just be say an 0805 resistor with its pads shorted together, which when placed allows you to call the nets at each of its pads to a different name…eg "GND" and "GND_DIRTY".

Here is an example of the use of net-ties to help you to confine the "dirty" ground…
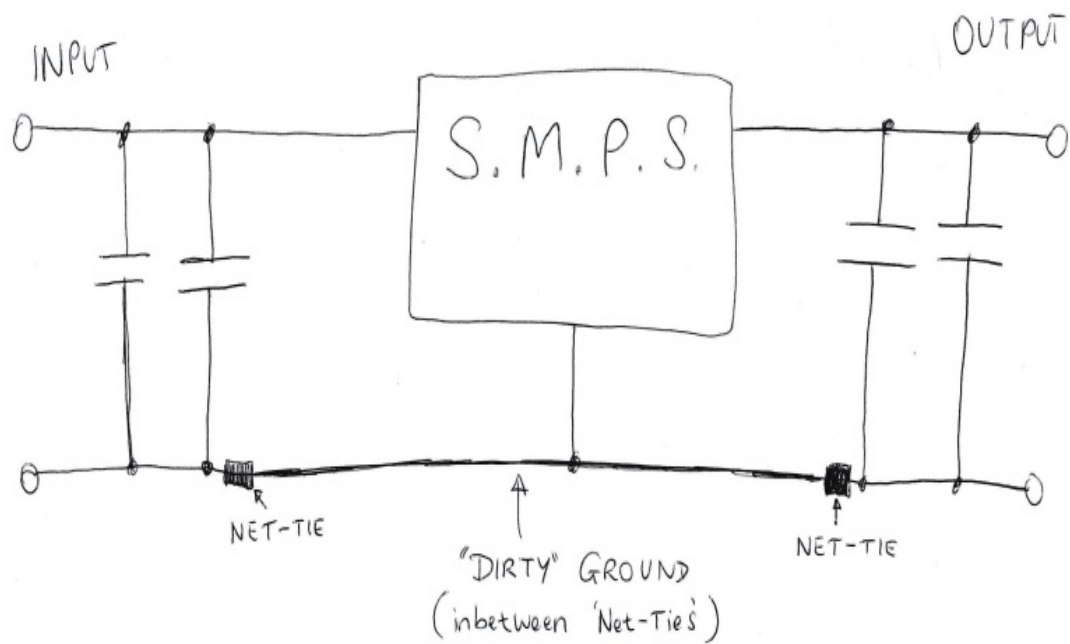
Also, as you can imagine, if the SMPS PCB also comprises various bits of general signal circuitry, (eg microcontroller circuits or whatever) then avoid those bits of general signal circuitry being grounded to the "dirty" ground, that is, avoid the following…..
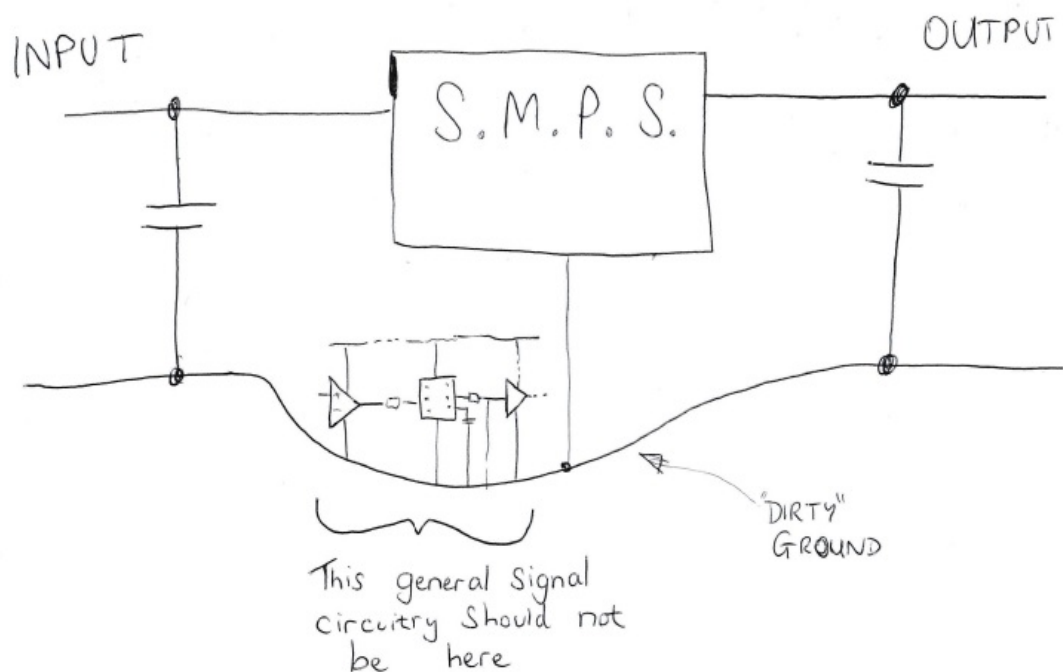
The 'input' and 'output' current loops of the SMPS

These current loops are "quieter" than the "power switch" loop and the "rectifier" loop. (ie they comprise current waveforms which are not so "jagged" in shape and have slower rise times) However, in most SMPS's the input and output capacitor banks can be relatively small , and so the current wave-shape in the 'input' and 'output' loops is still quite high in harmonic content. As such the 'input' and 'output' current loops should be routed as close diff pairs, all the way along their length, back to the input or output connector, as the case may be.
Also, if the SMPS is drawing a relatively high amount of current, then the PCB traces of the 'input' and 'output' current loops will need to be thicker than some of the signal traces.

…so in summary, this is how you would route the "input" and "output" current loops of an SMPS….
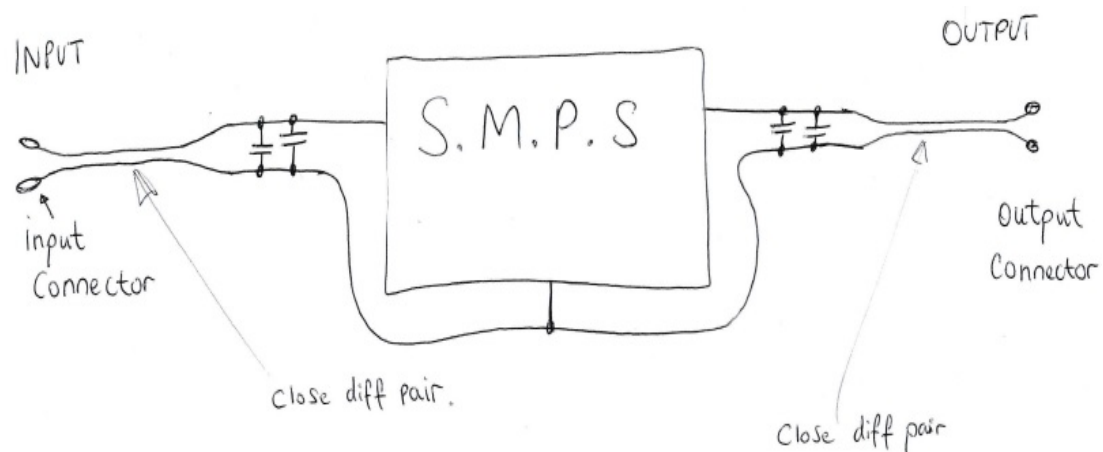
How to route the control ground

All SMPS's contain control circuitry, which is necessary to control the SMPS.

-You must be sure that the ground of the control circuitry does not get traversed by power switching currents. –If it does, then the controller may get confused because it will be receiving signals from control circuitry which is temporarily at a different potential (voltage) due to ground bounce. Ground bounce is where power switching currents traverse the stray track inductances and voltage drops are thus created across them.

We have seen how general signal circuitry should not be grounded to the "dirty" ground, however, at least some part of the control ground generally has to be grounded to the "dirty" ground. This has to be done in a specific way, -that is , done at a specific point so that power switching currents cannot traverse lengths of tracks of the control ground.

FET source sense resistor.

If the SMPS comprises a sense resistor located in the source connection of the power FET, then this sense resistor will obviously be connected to the dirty ground. The control ground and the "dirty" ground will thus "meet" at the (dirty) ground pad of the source sense resistor….
The control ground and the dirty ground must meet at this point because the controller has to measure the voltage across the source sense resistor…..therefore, the controller, and the source sense resistor must be grounded to the same 'place', which is at the same potential……as follows….

INPUT ... OUTPUT

S.M.P.S.

Source sense resistor →

'DIRTY' GROUND

SMPS Controller I.C. →

← No switching power current should flow down this trace.

CONTROL GROUND
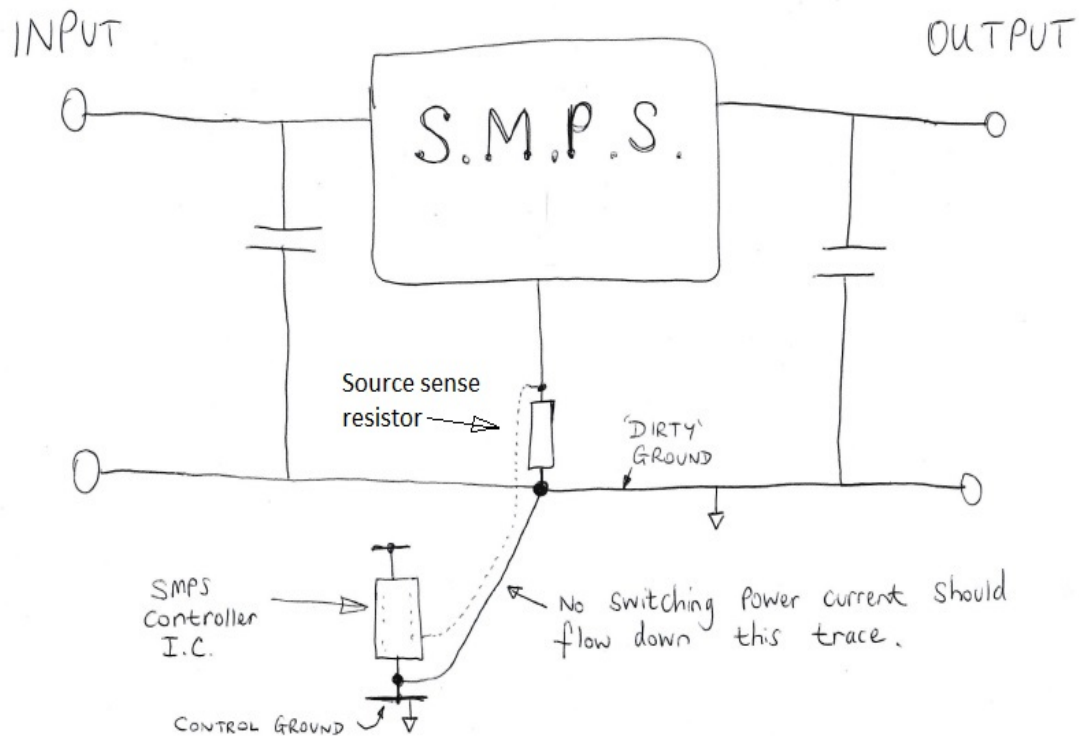
Also note from above that the connections from the source sense resistor to the Controller IC are routed as a close differential pair.

Also, its worth noting that the connection from the source sense resistor should be made to the actual pads of the source sense resistor, and not somewhere else along a trace connected to one of these pads. –If not connected to the actual pads itself, then you will end up with extra impedance (stray inductance and resistance) which you don't want. Connecting directly to the pads in this way is called "Kelvin connection". –Indeed, some sense resistors have four terminals, two of which are the normal "power" connections, and the other two are the connections for the sense traces to connect to. This is especially done when the current is high, but is also useful when the current rise time is high.

Output voltage divider

Also note that many non-isolated SMPS's feature an output voltage divider. Very often, the Controller IC actually senses the divider voltage of this divider. (for the purposes of controlling the output voltage). Once again, the lower divider resistor really needs to be grounded to the same ground as the ground of the controller IC. – this is so that the controller IC can correctly measure the divider voltage. Remember that if there is ground bounce occurring then the controller may temporarily incorrectly measure the output divider voltage.
So , as you can understand, you need to get as close to the following in order to get the best noise free operationof the SMPS Controller IC…..

INPUT   OUTPUT

S.M.P.S.

Source sense resistor

"STAR" POINT

output divider Voltage

SMPS Controller IC

CONTROL GROUND
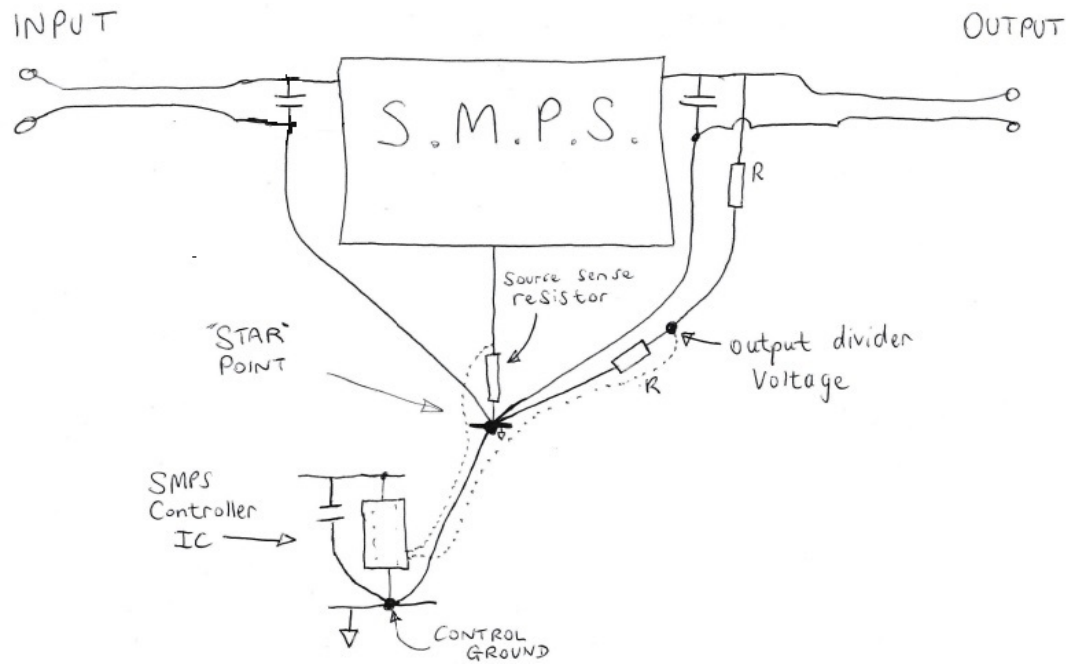
…As you can see, this is sometimes referred to as "star" grounding. Thought its important not to get foiled by jargon, and realise that all that's happening is that we are trying to reduce the problem of voltage differences occurring within the PCB ground traces due to the flow of high current switching waveforms through the stray ground inductances and resistances. (ground bounce)

Ground Bounce

This refers to the voltage differences that can occur within the ground traces of the PCB. These voltage differences are due to the flow of the high frequency harmonics of the switching power current through the stray trace inductances and resistances which are present in the ground traces. These high frequency harmonics are highly prevalent in SMPS current waveforms (especially in standard, "hard-switched" SMPS's, and especially in the 'dirty' ground of SMPS's).

Ground bounce can be a problem especially for the SMPS controller IC, since if there is ground bounce happening between its control ground and the ground at the ground pad of some resistor that it is measuring the voltage across , then the controller can get a noisy reading of the voltage. This can result in noisy, faulty operation of the controller IC, causing noisy, faulty operation of the SMPS.

Ground bounce can be an unusual concept to get our heads around, because we are used to seeing a ground trace on a PCB, and just assuming that it is all at the same voltage (ground) , but it is the nature of the high frequency harmonics of the switching power current of an SMPS that excite the stray trace inductances and cause these voltage differences within the ground copper.

Route FET gate drive traces as short, close, differential pairs.

As you know, the FET gate drive traces should go, as far as possible, as a close pair (go and return closely following each other).

This reduces the inductance of the gate drive, which is good, as inductance is not wanted in the gate drive, as for one thing it can resonate with the FET gate capacitance and ultimately cause damage to the controller IC.

Also, as you know, we must be aware that the gate drive currents are high di/dt….and as such, its best to try and avoid it (or reduce it from) traversing through the control ground.

As you know, sometimes its not possible to completely stop the 'pulsey' gate drive pulses from going through the control ground, however, if you route a gate return trace close to the gate drive trace, then the gate current will tend to mostly follow that close-by trace, as the current will "see" less impedance along the close-by trace…….as you know, tight current loops which enclose little area have overall lower inductance , and so less impedance.

As you know, using "Net-Ties" can often assist in helping to produce these closely running return traces.

A Net tie, as you know, is just a short circuit, which allows the nets on either side of it to be given different names…eg "GND_1" and "GND_2" etc etc. In Eagle Pro, a "Net-Tie" can be made by eg an 0603 resistor footprint and shorting the pads together.

Anyway, here is how the FET gate drive traces should be routed as a close pair…

Routing the FET gate drive traces
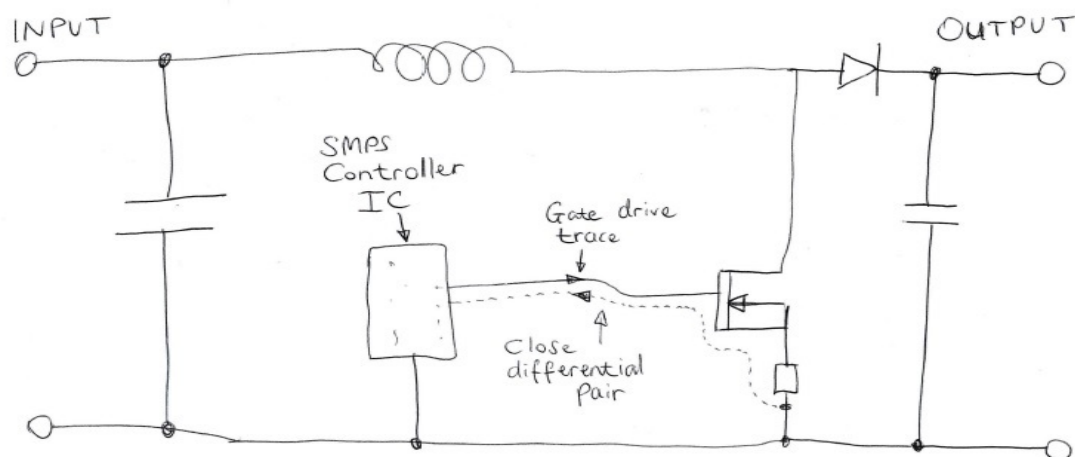
Misconceptions in SMPS layout

If an SMPS has a switching frequency of say 100KHz, its common for people to think that 100KHz is not going to cause a problem, as the impedance of a stray inductance at 100KHz is not likely to be very high. That is true, but its not the fundamental frequency of 100KHz that is the problem, -it is the higher harmonics of the switching waveform that cause the problem. If you like, it is the steep "edges" of the switching current waveform that cause the problem.

Critical & Non-Critical components.

As you know, in an SMPS's, some of the components (resistors and capacitors) that connect up to the PWM controller IC need to be located closely to the SMPS controller IC. For example, the Vcc decoupling capacitor(s), the timing resistor and/ or capacitor)

But in many SMPS's, there are many components and subcircuits which do not have to be particularly near to the SMPS controller IC…because they are just general signal circuits…….eg   you may have , say, a BJT which just enables the SMPS controller IC once the low voltage power rails get powered up.

So , as discussed, there are certain components which connect up to the SMPS controller IC whose position is not critical.

As you know, please ask the Design Engineer which these components are, because then you can leave them till last, and just slot them into any remaining gaps that you have left.
….better still, the Engineer could provide you with a highlighted schematic showing the "non-critical" components.

As you know, certain components are more critical, for example, the decoupling capacitors that connect up to the supply pin(s) of the SMPS controller IC.

Where to start the layout

Obviously this is your choice, but it'd be good to have an idea of where the innermost capacitors of the 'rectifier' and 'power switch' loops are going to go, in relation to the power transistors and diodes of the SMPS.

The probably most important thing is getting the source sense resistor placed, and making sure that you can "star" ground the LT8705 controller to the same ground at the base of the source sense resistor…..
(as you know, the traces, go and return, from the source sense resistor must be routed as a tightly close pair back to the controller)

The SMPS and its switching node(s)

As you know, in any SMPS, this node is generally the one with the highest dv/dt…..as such, it can potentially capacitively couple noise into anything that's near it….even if that is on the other side of the PCB.

In particular , most SMPS's have a PWM controller IC, which contains sensitive things such as high impedance comparator inputs and opamp inputs…..it would be best to stop the switching node copper from being routed too near these things…..eg keeping the switching node copper from being directly above or below the PWM controller.

If the switching node is on a directly opposite layer to the SMPS Controller IC, then you could lessen the problem by interposing some ground copper between them, on an interposed layer.

Its worth asking the SMPS Engineer to identify the switching node for you.

Current levels

As you know, with any SMPS, its worth asking the people what are the current levels in the power traces so you can use thick/wide enough copper etc.

<u>Rip-up-&-Re-Try</u>

As you know, Autorouters cannot be used when routing SMPS's.

I am sure you will be much better than me, but i usually find its impossible to route an SMPS just once…….i usually find I have to route it, then rip it up, then route again, then rip up again, etc etc….till eventually its right.

The worst thing for me (no doubt you won't be this bad), is to sit there and try and mentally plan out the components placement for long times……its better to just put them components in there, and route up and see how it looks, then tidy it or rip up and retry.
Once you have some components in there routed up…it soon becomes obvious how it should have been done alternately.

Silkscreen designators, Test Pads & vias

As with any PCB, one can make the SMPS test engineer's life easier by placing silkscreen designators for all SMPS components, and also placing test pads which connect up to the SMPS controller IC 's pins.

Using minimum 0.6mm vias, and no smaller (if possible), also means that these vias can be used for probing the SMPS prototype more easily.

If your PCB fabricator says he can easily go down to 0.25 mm vias, it doesn't mean you have to do all your vias at that size. (unless you really are very constrained for room)

Simulations

If you wish, its very easy for an SMPS design engineer to rig up a basic representative SMPS simulation for you on the free LTspice simulator, (from linear.com) so that you can see for yourself the flow of high rise time pulse currents in the power switch loop and rectifier loop of an SMPS.

Ground Plane

Having a ground plane is often said to be the 'be-all-and-end-all' of SMPS PCB layout...... "just put in a ground plane, and everything's going to be fine".
As you know, this is not always the case..

There's the obvious point that "ground planes" can end up not really being "planes" due to them getting cut up by (non-ground) tracks which (due to room constraints), end up getting routed on the ground plane layer as there was no room anywhere else, and it wasn't wanted to add more layers to the PCB.
Also, ground planes can also get cut up by numerous through vias from different (non-ground) nets.

Also, Page 12 of the following document, under "LAYOUT CONSIDERATIONS" reminds us that ground planes are not the be-all-and-end-all, and that noisy traces shouldn't be routed haphazardly across the ground plane......

http://application-notes.digchip.com/009/9-12820.pdf
Application Note 42004
"Using the ML4425/ML4426 BLDC Motor Controllers"

<QUOTE>
Controlling the current paths is important as well. If a groundplane is used, separate conductors (traces) should return the motor currents to the sense resistor which can connect to the ground plane near the supply ground. The same approach should be used for the supply voltage. The purpose of this technique is to keep the high current high speed signals out of the ground plane, to reduce system noise.
<UNQUOTE>

...the above quote refers to routing up a Switching BLDC Motor driver.

Current Loops

…As you know, it is no surprise that SMPS power switching current loops need to be routed with as minimal area as possible (eg as closely running diff pairs)….it's a fundamental law of PCB layout that all current loops should be routed to have as small an enclosed area as possible…..this is…

1…..so that they don't radiate much noise energy out

2…..so that they are less susceptible to have noise energy radiated into them.

3…..so that stray trace inductance is minimised

Outputs of the PCB layout package.

SMPS Test Engineers often need to review the layout of the SMPS in order that they can see if it could be the cause of problems with the operation of the SMPS.

Therefore, using a PCB Layout package with a free layout viewer is highly advantageous. (eg Eagle Pro) Failing that, if the layout package can output the layout into a format which can be viewed in a proprietary layout viewer then that is next best.

In all cases,the SMPS Test Engineer really needs to be able to highlight any net in the layout, so that he/she can follow its path, and follow the path from layer to layer through vias etc etc.

The Eagle Pro layout package is advantageous because it has a totally free-of-charge viewer, which allows the viewer to see the layout and schematic just as the PCB designer could see it, just that the viewer doesn't allow changes to be made to the layout.

A true story of PCB Layout disaster in a 5W SMPS.

Its very normal to find in electronics companies (not Jesmond) that reported PCB layout problems are viewed as being just a hoax.
Its just not thought possible that at frequencies well below microwave frequencies that PCB layout issues can really be a problem.
Often, people believe that if a switch mode power supply switches at say, 160KHz (as in LT8705), then this is just too low a frequency to give a layout problem.
-The fact is, that it is not the switching frequency that is the problem…..it is the switching edges…or rather, it is the higher harmonics of the switching frequency……or being more specific, it is rapidly changing currents flowing through stray track inductances…..high di/dt's. (V=L.di/dt)

(theres other things too but we'll leave these out or now)

Some years ago, I was at a lighting company who were doing a 5W Switch Mode LED driver (Vin = 28V, vout ~9V).
The PCB area that contained this SMPS (and its additional control circuitry) was only about 1.5cm by 3cm (double sided)
The LED driver had additional control circuitry which did the following…
1…..Allowed a micro to dim the LED light from zero to max

First of all, eight prototype PCBs were produced……

All eight prototypes did not work when sent from the PCB assemblers. Each PCB displayed the same faults. The faults were….
1…..On max setting, only 40% of the maximum current actually flowed in the LEDs
2…..The LED light could not be dimmed down to zero light output.

Initial inspection and testing showed that there were no obvious faults or drys, components misplacements, etc etc.

After some time in testing, the only notable feature that came out of the testing was a seemingly small amount of noise on the analog control voltage.

As such, it was feared there might be a PCB layout issue, (there were no other obvious problems) so the Layout was inspected by using the free Pulsonix PCB viewer. –This allows the viewer to highlight any net, or any amount of nets together, and trace the tracks paths.

It soon became obvious that the Diode of the Buck converter (an SMPS) had not been routed directly down to the ground in the switching (rectifier) current loop. Instead, the anode trace connected to this diode had been run about 2cm up the side of the PCB, and then connected to the analog control ground in that part of the PCB….As such, the Switching currents flowing in that diode were flowing right through the analog control components' grounds.

The buck diode, as you know, contains high di/dt currents…….the power of this SMPS was just a measily 5W, ….but that is the crucial point, -it's not necessarily the power, or the current magnitude that causes the problem, it's the di/dt, or the rapidness of the current changes.

This Switch Mode LED driver was using the LM3402 LED driver IC, which comprises a powerful internal FET driver, and as such, the FET was switching on very quickly indeed, causing the switching power current to display very sudden rapid changes….that is, high di/dt's.

This high di/dt was flowing through the analog control ground, and causing all the problems…..it's noteable that the extra distance that these pulse currents flowed, as a result of the poor layout, was very small, just a few cm's….and yet it still had such a big impact.

The stray inductance of such a small track length must have been tiny, and yet the size of the di/dt was so large that the created noise voltage ruined the operation of this SMPS.

….The problem was completely solved by returning to the lab, and cutting the offending track with a scalpel, and then white wiring the diode's anode to the ground directly beneath the diode…..this totally solved the problem on all eight of the prototype PCBs.

Sometimes PCB layout issues don't show up so much in motor drive circuits, as motor drives often switch at lower frequencies than SMPS's, and the switching edges can tend to be longer…the di/dt's less.

Summary of points for SMPS Layout:

All Current always flows in loops…(and going through a capacitor can be a part of the current loop)

Keep the switching power current loops as narrow in area as possible (eg like close diff pair traces).

Minimise the "dirty" ground (the ground that carries fast rime time power switching currents)…ie don't route the "dirty" ground all over the PCB.

Don't run power switching currents through lengths of control ground (all SMPS's have controller circuits, which are connected to the 'control' ground)…this is because power switching currents can create voltage drops across lengths of control ground and "upset" the controller. (The voltage drops are due to switching current harmonics inter-acting with stray PCB track inductances)