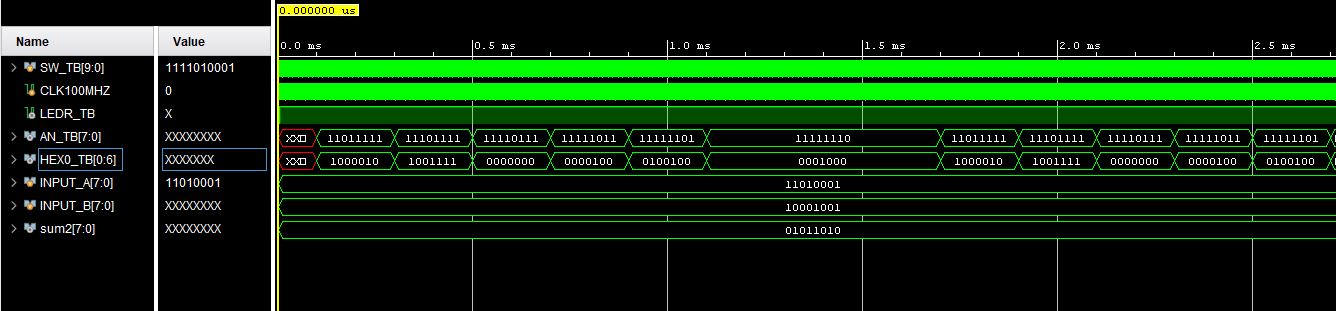
Last part of Lab3 was about registering, summing and showing the results in seven segment display. There were 3 input which were A, B and CLK. These were provided by switches. Also, we used FPGA clock (CLK100MHZ) as input for clock divider module. First value that we determined using switches was registered as input A. After CLK was changed, switches were changed, and the value was registered as input B. The hexadecimal value of input A, input B and sum of them were displayed in seven segment display at the same time. Since FPGA board had not include different HEX such as HEX0, HEX1,HEX2 etc. ,we used counter for HEX0 and AN changing. The clock of this module was divided clock which was created using FPGA clock.

 Figure-1 / Schematic of Part5

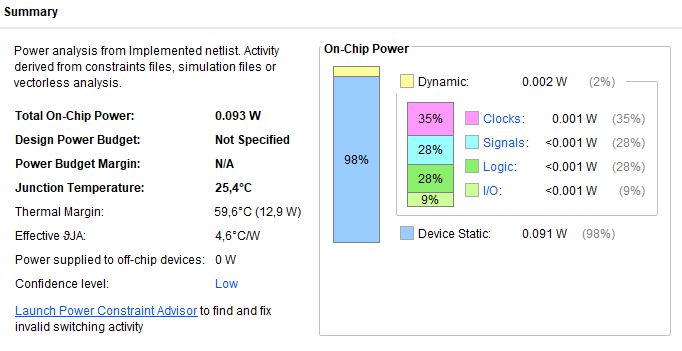
 Figure-2 / Example Simulation Result

Figure-3 / Summary