UCD School of Physics

PHYC30170 Physics Astronomy and Space Lab I

Electronics Laboratory

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Contents

1. Experiment 5

The objective of this experiment is to simulate and build a simple RC circuit driven by a square wave voltage source. The voltage across the resistor and capacitor will be observed using an oscilloscope, and the time constant of the circuit will be determined.

1.1. Theory

1.1.1 Kirchhoff's Laws

Kirchhoff has two primary and distinct laws that deal with the conservation of charge and energy within electrical circuits. These are:

Kirchhoff's Current Law (KCL): This law states that the sum of currents entering a junction (or node) in an electrical circuit must equal the sum of currents leaving that junction. Essentially, it is a statement of the conservation of electric charge.

Kirchhoff's Voltage Law (KVL): This law states that the sum of electrical charge, or the voltage drop, around any closed loop is zero. Essentially, it is a statement of the conservation of energy within an electrical circuit. [1]

1.1.2 Time Constant

The time constant, denoted by the Greek letter tau (τ), is a measure of the time it takes for a system to respond to a change in input. For electrical circuits, the time constant is often used to describe the behavior of an RC (resistor-capacitor) circuit.

The time constant for an RC circuit is given by the formula:

$$\tau = RC \tag{1}$$

And such, the solution to the equation for a circuit's voltage response over time is then given by:

$$V(t) = V_f + Ae^{-\frac{t}{\tau}} \tag{2}$$

where R is the resistance in ohms (Ω), C is the capacitance in farads (F), $V(t)$ is the voltage at time t, V_f is the final voltage, A is a constant determined by initial conditions. [1]

As the capacitor charges, the slope (which is proportional to the current) is proportional to the remaining voltage. Therefore, the waveform produced is exponential in nature. For $t \gg \tau$, the voltage across the capacitor approaches its final value V_f asymptotically. [1]

1.2. Methodology

The circuit was constructed on the TINA software as shown in Figure 1. A resistor of 1 kΩ and a capacitor of 1 μF were connected in series in the circuit. A square wave voltage source was used to drive the circuit, with a frequency of 1 kHz and an amplitude of 5 V. The voltage across the capacitor and resistor was observed using an oscilloscope.

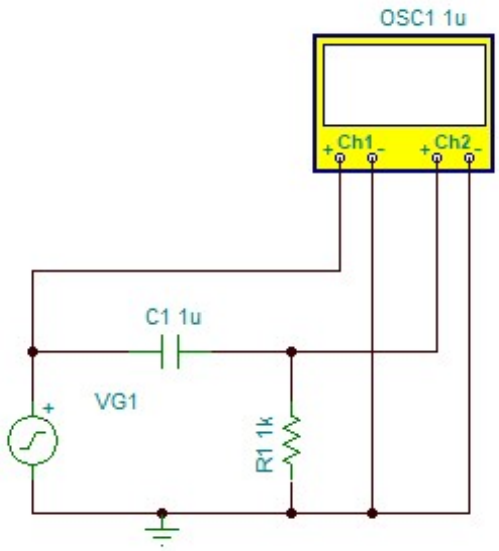


Figure 1: Experimental setup constructed on the TINA software.

A similar physical circuit was then constructed on a veroboard using the same components as in the simulation. The oscilloscope was used to supply the square wave voltage source and to observe the voltage across the capacitor and resistor.

1.3. Results

Results were gathered from both the TINA simulation and the physical circuit using the oscilloscope. The graphs produced are shown in Figures 2 and 3.

The oscilloscope shows the two channels: Channel 1 (blue) represents the input square wave voltage, while Channel 2 (green) represents the charging and discharging voltage across the capacitor.

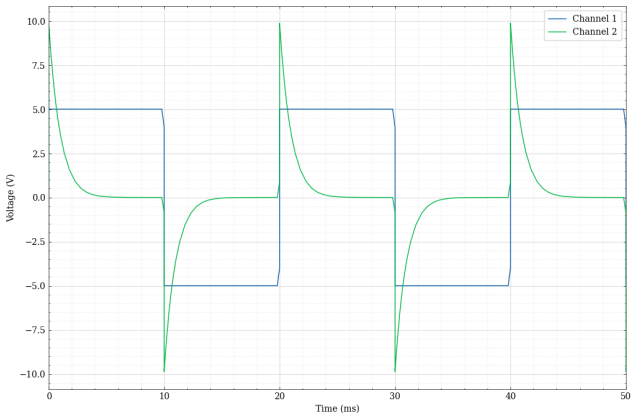


Figure 2: Oscilloscope output from the TINA simulation driven by a square wave voltage source.

The time constant for the theoretical simulation can be found directly using Equation 1 and the component values:

$$\tau = 1 \times 10^{3} \cdot 0.1 \times 10^{-6} = 1 \times 10^{-3} \text{ s}$$
$$= 1.00 \text{ ms}$$

For the practical circuit, the output observed from the oscilloscope is shown in Figure 3. The same two channels are represented.

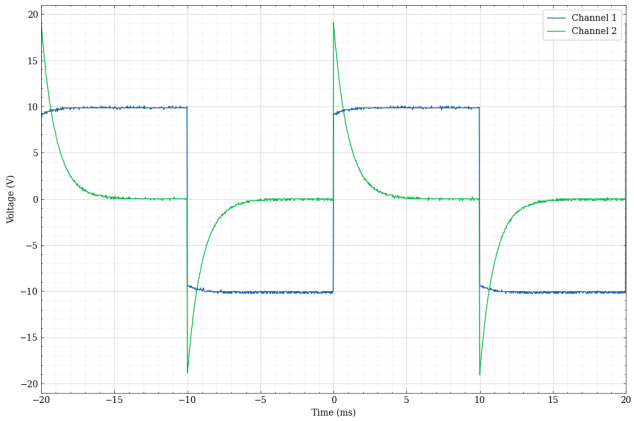


Figure 3: Oscilloscope output for the physical RC circuit driven by a square wave voltage source.

From this output, a zoomed-in section of the charging curve can be taken to measure the time constant and fitting an exponential curve to it, as shown in Figure 4.

Simple curve fitting was performed using Python's SciPy library to fit an exponential curve to the data points. The model for the exponent fitted to the curve was based on Equation 2, taking a negative exponent.

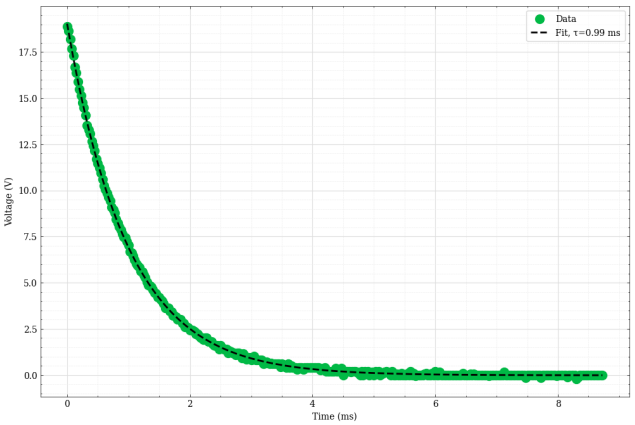


Figure 4: Zoomed-in section of the charging curve from the oscilloscope output for the physical RC circuit between 0ms and 10ms.

The output of the curve gave a time constant τ of 9.8894×10^{-4} s or 0.99 ms for the physical circuit.

Comparing the theoretical and practical time constants gives a percentage error of approximately 1.01%.

1.4. Analysis and Discussion

The experimental results obtained from the physical RC circuit closely matched the theoretical predictions from the TINA simulation, showing a strong agreement. From the calculations made, the theoretical time constant was found to be 1.00 ms, while the practical time constant obtained from the oscilloscope data through curve fitting was approximately 0.99 ms, giving a percentage error of about 1.01%, which is within the acceptable range for experimental errors.

The close correspondence between the theoretical and practical results indicates that the RC circuit behaves as expected within the range of frequencies and voltages used. The exponential charging and discharging curves observed with the oscilloscope traces confirm the transient response characteristics of RC circuits, with the voltage dropping to zero as the capacitor remained fully charged before the next cycle.

Small discrepancies between the theoretical and practical results can be attributed to several factors. These include the parasitic resistances in the lead wires and veroboard connections, which may slightly alter the effective resistance of the circuit. Additionally, the capacitor and the resistor have tolerances (typically ± 10% for the capacitor, ± 5% for the resistor), which can lead to variations

in the actual time constant. Furthermore, the oscilloscope's measurement accuracy and the resolution of the time base can also introduce minor errors in the trace readings. Despite these potential sources of error, the overall agreement between theory and experiment indicates high accuracy, making the deviation negligible for practical purposes.

Overall, the experiment successfully demonstrated the key relationship between resistance, capacitance, and the time-dependent voltage behaviour of an RC circuit and validated the theoretical models through practical implementation and measurement.

1.5. Conclusion

The objective of this experiment was to simulate and build a simple RC circuit driven by a square wave voltage source, observe the voltage across the resistor and capacitor using an oscilloscope, and determine the time constant of the circuit, comparing both the theoretical and practical values. The time constant otained from the practical circuit ($\tau = 0.99$ ms) closely matched the calculated theoretical prediction ($\tau = 1.00$ ms) with a minimal percentage error of approximately 1.01%.

This agreement validates the theoretical models for capacitor charging and discharging in an RC circuit, and validates Kirchhoff's laws in the energy and charge conservation within electrical circuits. The experiment highlighted the usefulness of simulation software like TINA for predicting circuit behaviour, as well as the importance of practical measurements using an oscilloscope.

2. Experiment 7

The objective of this experiment is to simulate and construct an RC-network voltage divider circuit. Using a signal analyser, the amplitude and phase response of the circuit will be measured over a range of frequencies to plot a Bode plot for computational, simulated, and achieved results and compared.

2.1. Theory

2.1.1 Impedance

"Impedance" can be used in place of "resistance" in order to describe circuits with linear devices, such as resistors, capacitors, and inductors, and thus generalising Ohm's law. Impedance (Z) can be referred to as the "generalised resistance" and is described by the complex relationship: impedance = resistance + reactance, or $Z = R + jX$. [1]

The generalised Ohm's law can be written as the following [2]:

$$Z = \frac{V}{I} \tag{3}$$

The reactance X applies for capacitors and inductors, which are reactive and always 90° out of phase. For resistors, they have reactance (R), which is always in phase and resistive.

For a capacitor, this reactance (X_C) is given by [1]:

$$X_C = \frac{1}{\omega C} \tag{4}$$

And thus the impedance (Z_C) of a capacitor is then [1, 2]:

$$Z_C = -\frac{j}{\omega C} = \frac{1}{j\omega C} \tag{5}$$

with C as the capacitance in farads (F) and ω as the angular frequency in hertz (Hz). The complex part of the equation accounts for the 90° phase shift in the current-voltage curve.

2.1.2 Voltage Dividers

Voltage dividers are circuits that produce a fraction of the input voltage as the output voltage for a given voltage input. They are often used to produce a particular voltage from a larger voltage, either fixed or varying. In general, the division ratio of V_{out} to V_{in} is not constant as it is dependent on the frequency ω. [1]

The Thévenin equivalent circuit, which states that "any two-terminal network of resistors and voltage sources is equivalent to a single resistor R in series with a single voltage source V", can also be generalised with impedance [1, 2]:

$$V_{out} = V_{in}\frac{R_2}{R_1 + R_2} = V_{in}\frac{Z_2}{Z_1 + Z_2} \tag{6}$$

2.1.3 Decibels

To compare the relative amplitude, or magnitudes, of two signals, the logarithmic decibel scale is used. This ratio is typically given with the relative intensities [1, 2]:

$$dB = 10 \log_{10} \frac{I_2}{I_1} \tag{7}$$

However, since the intensity $\propto$ the amplitude^2, and signal amplitudes are most commonly dealt with in circuits, Equation 7 can be rewritten [2]:

$$\begin{aligned} dB &= 10 \log_{10} \frac{V_2^2}{V_1^2} \\ &= 20 \log_{10} \frac{V_2}{V_1} \end{aligned} \tag{8}$$

As the voltage V is often the amplitude source of a circuit.

2.1.4 RC High-Pass Filter

By combining resistors and capacitors in a circuit it is possible to make frequency-dependent voltage divider with the use of the frequency-dependence in the impedance of a capacitor $Z_C = -j/\omega C$. These circuits have the abilities to reject undesired signal frequencies, only allowing the desired frequencies to pass. [1]

At high frequencies $\omega \gtrsim 1/RC$, the output is approximately equal to the input and approaches zero at low frequencies. The -3 dB point at which the curve bends and the capacitor is approximately 63% charged after a time $\tau = RC$ may be referred to as the "breakpoint" and is given by [1, 2]:

$$f_{3\,\mathrm{dB}} = \frac{1}{2\pi RC} \tag{9}$$

At $\omega = 0$ the phase shift is the expected +90°. At $\omega_{3\,\mathrm{dB}}$ the phase shift changes to +45°, and at $\omega = \infty$ the phase shift changes to a flat 0°. [1]

The bandwidth of the circuit is then described as the range over which the response does not drop by over 3 dB; or, the range of frequencies that can be rejected or passed in a voltage divider circuit. [2]

2.2. Methodology

The circuit was constructed on the TINA software as shown in Figure 5, which is identical to the circuit in experiment 5 (§1.2) with the difference of a signal analyser in place of an oscilloscope connection. The same resistor (R = 1 kΩ) and capacitor (C = 1 μF) were used. A sinusoidal wave source of 1V was used to drive the circuit.

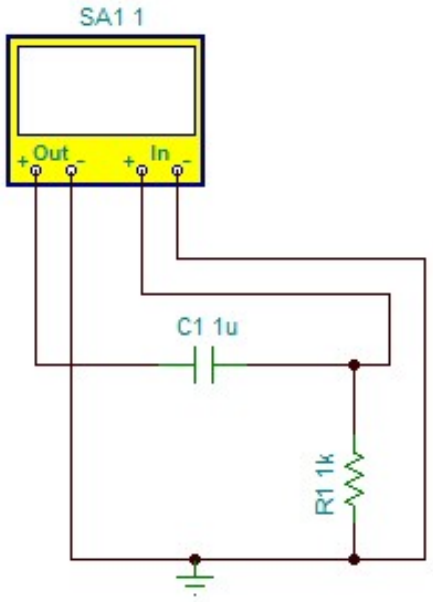


Figure 5: Experimental setup constructed on the TINA software.

The same physical circuit as used in experiment 5 (§1.2) was used for the practical measurements of this experiment.

2.3. Results

Using the generalised voltage equation (Eq. 6) and the impedance form for resistance (R, simply) and capacitance (Eq. 5), the transfer function for the gain can be approximated:

$$\begin{aligned} V_{out} &= V_{in} \frac{R}{\frac{1}{j\omega C} + R} \\ &= V_{in} \frac{j\omega RC}{1 + j\omega RC} \end{aligned}$$

Such, the ratio of V_{out}/V_{in} can be found and defined as the complex transfer function $H(j\omega)$:

$$H(j\omega) = \frac{V_{out}}{V_{in}} = \frac{j\omega RC}{1 + j\omega RC}$$

The magnitude of this function can be found by applying Equation 8 directly as it is the ratio of V_{out}/V_{in}. The phase angle can be determined by taking the arctangent of the imaginary part of the transfer function (1) divided by the real part of the transfer function (ωRC).

Plotted across a range of frequencies from 1 Hz to 1 MHz (10^0 to 10^6, as a logarithm), the gain and phase shift of the RC high-pass voltage divider circuit are found and plotted in Figure 6.

For this plot, the cutoff frequency is found to be approximately **159 Hz**.

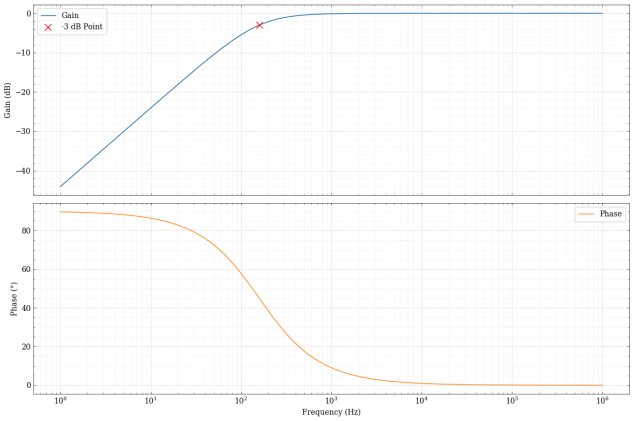


Figure 6: Bode plot from the calculations of an RC-network voltage divider circuit driven by a sine wave voltage source with $V_0 = 1$, C = 1 μF, and R = 1 kΩ.

As the magnitude (gain) was already found on a logarithmic scale (decibels), only frequency is showcased as a logarithmic scale. Despite this, the gain plot is a log-log plot, whilst the phase angle plot is a log-linear plot with the phase angles linear.

A similar graph was plotted for the TINA simulation results, shown in Figure 7 using the Signal Analysis instrument in the T&M menu, resulting in the output represented as a Bode plot (gain and phase).

For this plot, the cutoff frequency is found to be approximately **160 Hz**.

Again, a similar graph was plotted for the results obtained from the physical circuit constructed,

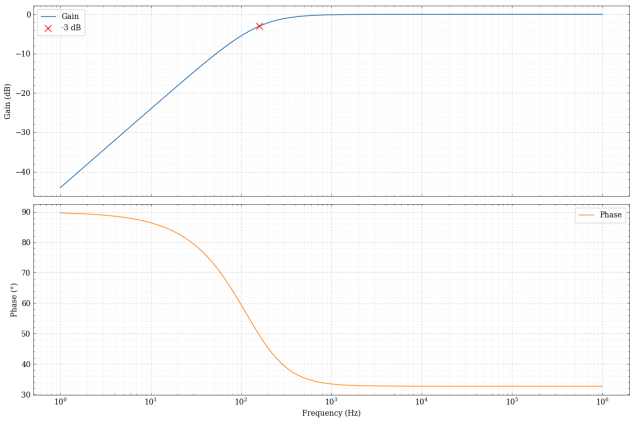


Figure 7: Bode plot from the TINA simulation of the RC-network voltage divider circuit driven by a sine wave voltage source.

shown in Figure 8. Instead of a smooth plot, logarithmic values for frequency were chosen (1 Hz, 10 Hz, 100 Hz, 1 kHz, 10 kHz, 100 kHz, 1 MHz) and the amplitude and phase responses observed. Results were tabled (Appendix, table 1) and graphed, with the magnitude/gain found with Equation 8.

For this plot, the cutoff frequency is found to be approximately **542 Hz**.

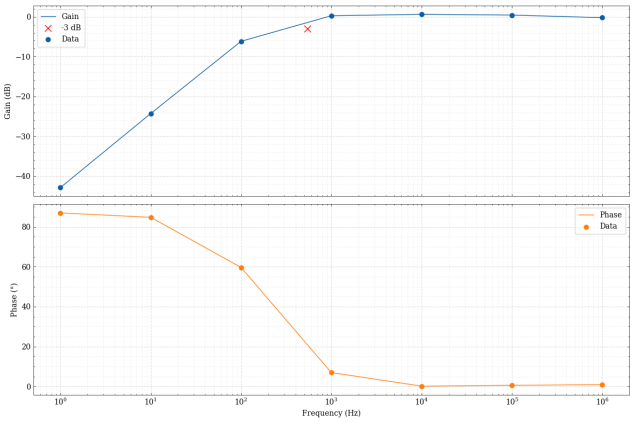


Figure 8: Bode plot from the physical RC-network voltage divider circuit driven by a sine wave voltage source.

For visual comparison of plot agreement, all obtained curves and points were plotted against each other, shown in Figure 9.

The expected cutoff frequency for this circuit can be calculated with Equation 9, and is determined to be at approximately **159 Hz**.

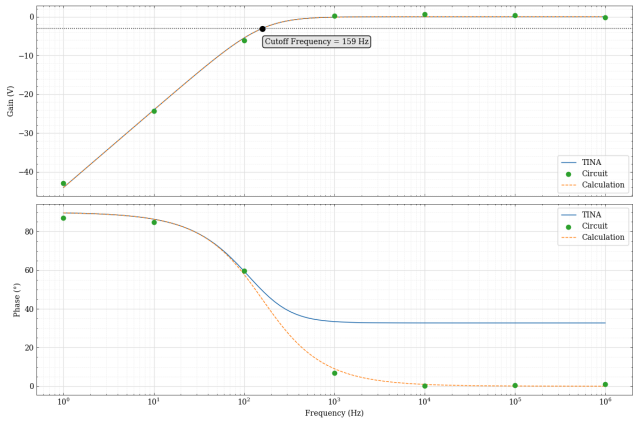


Figure 9: Comparison of the gain (top) and phase (bottom) Bode plot curves.

2.4. Analysis and Discussion

The results from the computational calculation (Fig. 6), TINA simulation (Fig. 7), and physical circuit (Fig. 8) all show the expected behaviour of an RC high-pass voltage divider. As predicted by the transfer function

$$H(j\omega) = \frac{j\omega RC}{1 + j\omega RC}$$

the output amplitude increases with frequency ω. At low frequencies ($\omega \ll 1/RC$), the capacitor impedance dominates that effectively blocks the input signal and results in a low output voltage. At high frequencies ($\omega \gtrsim 1/RC$), the gain approaches unity (0 dB) and allowing a greater portion of the signal to appear through the resistor, approaching the input voltage. The corresponding phase response transitions from approximately +90° at low frequencies to 0° at high frequencies, and a +45° phase shift at the cutoff frequency (-3 dB).

The theoretical cutoff frequency, determined with Equation 9, is found to be approximately **159 Hz** for R = 1 kΩ and C = 1 μF. This value very closely matches the value obtained from the TINA simulation of **160 Hz**, demonstrating a strong agreement between the analytical and simulated models. However, the experiment cutoff frequency for the physical circuit was measured at approximately **542 Hz**, which is an upward deviation of roughly **241%** from the calculation.

This discrepancy can be attributed to several experimental factors. The tolerance for a capacitor (often ±10%) and for a resistor (±5%) may have shifted the true RC product, directly affecting the $f_{3\,\mathrm{dB}}$ as a lower actual capacitance than the expected 1 μF would increase the cutoff frequency proportionally, similarly were it the resistor. Additionally, parasitic capacitance and resistance in the veroboard and connecting leads, and internal impedance from the oscilloscope input, can modify the circuit's effective impedance. At higher frequencies, small parasitic resistances and inductances can distort both amplitude and phase responses.

Despite deviations, the shape and trend of the experiment Bode plots agree with the theoretical expectations (Fig. 9). The gain plot displays the behaviour expected as discussed, while the phase response plot displays a smooth decrease toward 0° from +90°. These results confirm that the constructed circuit functions as a high-pass filter voltage divider, allowing greater frequencies to pass while holding back lower frequencies.

Overall, the experiment successfully illustrated the principles of the frequency-dependent impedance, the relationship between gain and phase in a reactive circuit, and the analytical calculation of the cutoff frequency expected for such circuit. The minor quantitative discrepancies can be explained by the realistic non-ideal component behaviours and measurement limitations.

2.5. Conclusion

The aim of this experiment was to investigate the frequency response of an RC high-pass filter voltage divider circuit and produce a Bode plot for the values obtained, alongside determining its cutoff frequency, through analytical, simulated, and experimental approaches. The results obtained for the analytical and TINA simulation were in excellent agreement, both predicting a cutoff frequency near **159-160 Hz**.

The result obtained from the physical experiment circuit, however, yielded a higher cutoff frequency of approximately **542 Hz**, a discrepancy from the other obtained values that may be attributed to component tolerances and parasitic effects within the measurement setup. Despite this, the overall gain and phase behaviour matched the expected curve form, validating the fundamental relationship between impedance and frequency in RC circuits.

The experiment results provided an effective

demonstration to the usefulness of visualising both amplitude and phase response in a Bode plot, bridging theoretical results with practical measurements.

3. Experiment 12

The objective of this experiment is to build and simulate a resistor-diode circuit and experimentally measure the produce I-V curve. Additionally, by driving a sinusoidal wave through the circuit the effect of the diode on the wave can be visualised with an oscilloscope. Then, by adding a capacitor in parallel with the resistor the characteristic curve of the circuit observed will change. Comments are then made on the observed graphs.

3.1. Theory

3.1.1 Diodes

Diodes are non-linear devices in the frequency domain, as opposed to the time domain devices (§1.1.2). As opposed to a linear response of doubling signal responses per applied signal, diodes are two-terminal semiconductor devices that control the flow of power. The two terminals are the positive anode and the negative cathode. The diode's arrow (anode terminal) points in the direction of the forward current flow, known as the "forward voltage drop" (typically 0.6 V for silicon diodes).

While the forward current bias diodes are measured in the milliamp range, the reverse current bias diodes are measured in the nanoamp range. Diodes in reverse current configurations are never of any consequence until the reverse breakdown voltage is reached. Typically, at quite high voltages, a general-purpose diode would break down and short.

Diodes do not have an associated resistance, and therefore do not obey Ohm's law. Additionally, because of this fact, diodes in a circuit also do not have a Thévenin equivalent equation. [1]

3.1.2 Rectifiers

A rectifier changes an alternating current (ac) to a direct current (dc) and is one of the most common and simplest applications of a diode in a circuit. For a sine-wave input much higher than the forward drop of a diode, the resulting output will be half-wave in an unfiltered circuit. It is called this way as only half of the input waveform is used. [1]

3.1.3 Power Filtering & Ripple Voltage

The rectified waveforms are only "dc" in the sense that the polarity does not change, though a lot of periodic variations in the steady voltage remain, known as the "ripple" voltage. This ripple "dc" can be smoothed out in order to generate a genuine dc supply with the use of a relatively large-value capacitor. The capacitor charges up to peak voltage output during the diode conduction, and the output voltage is provided by the stored charge ($Q = CV$) during charging cycles. However, due to the nature of the diode as a rectifier, it does not allow the capacitor to discharge back through the ac source. [1]

The capacitor value is chosen such that,

$$R_{\text{load}}C \gg 1/f$$

with C as the capacitance in farads (F), R as the resistance in ohms (Ω), and f as the ripple frequency in hertz (Hz). The capacitor is chosen in this way so that the time constant for discharging is much longer than the time between recharging, ensuring a small ripple. [1]

This way, when the ripple voltage is small compared to the dc voltage supply, the approximation of the ripple voltage is easily determined as one can assume that the load current stays constant in this case. As such [1]:

$$\Delta V = \frac{I}{C}\Delta t \qquad \left(\text{from } I = C\frac{dV}{dt}\right)$$

This can also be expressed with the waveform produced by a half-wave rectifier, approximated for Δt as the capacitor begins charging again in less than half a cycle [1]:

$$\Delta V = \frac{I_{\text{load}}}{fC} \tag{10}$$

with V as the voltage in volts (V), I_{load} as the load current in amps (A), f as the frequency in hertz (H), and C as the capacitance in farads (F). For a small ripple, viewing the initial discharge curve as a ramp is more accurate than if an exponential discharge formula and curve were used. [1]

3.2. Methodology

The circuit was constructed and simulated on the TINA software as shown in Figure 10. A digital multimeter was used to find and determine the current in the circuit as it passed through a 470 Ω resistor and 1N4148 diode. A variable voltage supply source was used, with a range of voltages observed chosen to be 0-1.5 V.

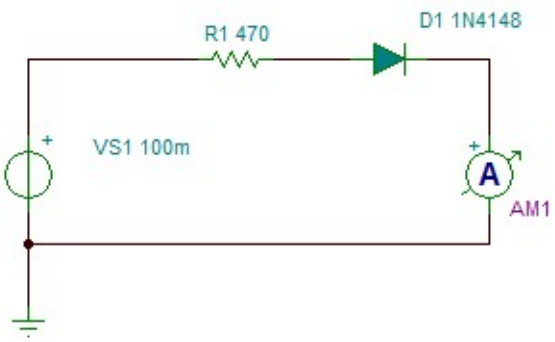


Figure 10: Experimental setup constructed on the TINA software.

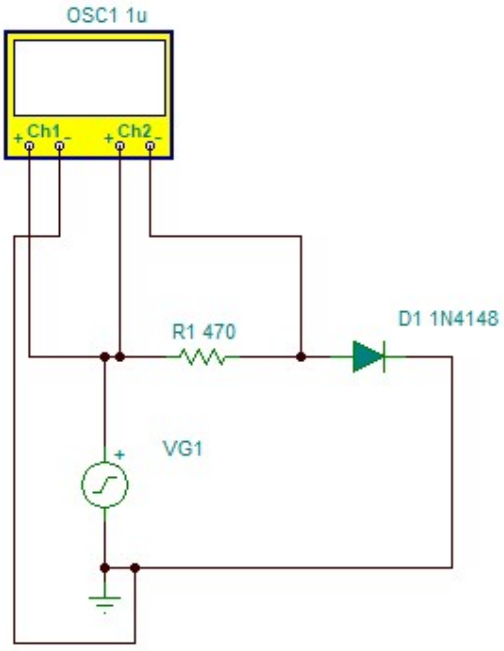


Figure 11: Experimental setup constructed on the TINA software, driven by a sinusoidal waveform.

With the same circuit as in Figure 10, an oscilloscope was connected in place of the digital multimeter, measuring the input voltage across the entire circuit and the output voltage through the diode and resistor, as shown in Figure 11. A voltage/amplitude of 3 V and frequency of 500 Hz was used.

A sinusoidal waveform was driven through the circuit and the rectifier properties of the diode were observed graphically on the oscilloscope.

A capacitor of 10 μF was then attached in parallel with the resistor, as seen in Figure 12 and an oscilloscope was connected to the circuit, measuring the input voltage across the entire circuit and the output voltage through the resistor and parallel capacitor, and the resulting diode output.

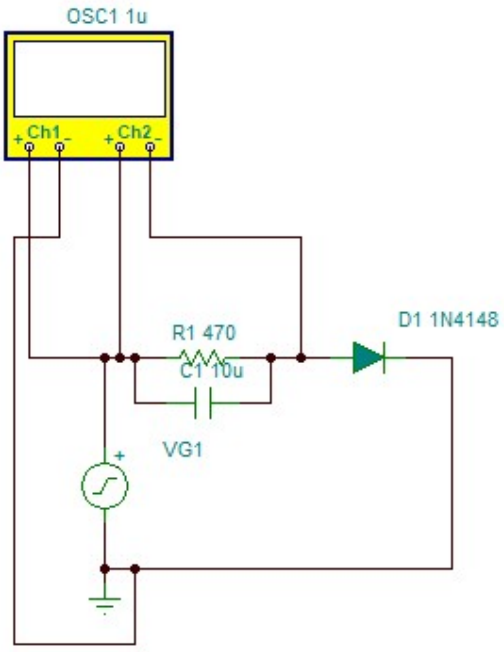


Figure 12: Experimental setup constructed on the TINA software, with a capacitor in parallel with the resistor and driven by a sinusoidal waveform.

A sinusoidal waveform was driven through the circuit and the rectifier properties of the diode were observed graphically on the oscilloscope, with the addition of the expected capacitor charging and discharging ramp.

3.3. Results

By simulating the constructed circuit in TINA, an I-V plot can be graphed with the built-in DC transfer characteristic mode. With a voltage range of the chosen 0-1.5 V, the output graph and curve is shown in Figure 13. It shows the expected "knee" for a forward biased diode at the threshold frequency where a clear surge in current is ob-

served.

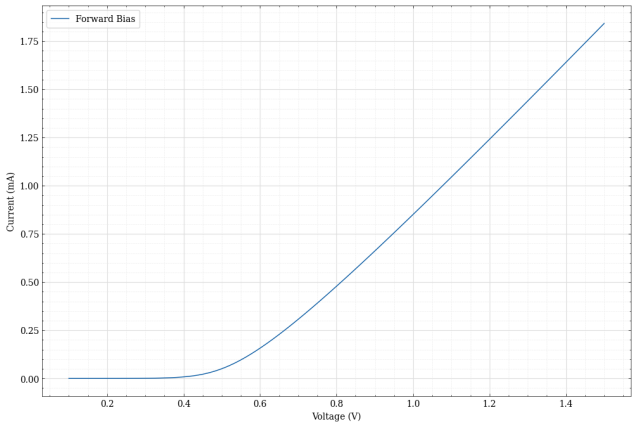


Figure 13: Forward-bias diode characteristic I-V curve simulated on the TINA software.

The same was then done on the physical experimental circuit for the same varying range of voltages 0-1.5 V and a table then created of the values obtained (Appendix, table 2). The values were then plotted on an I-V graph and compared with the theoretical TINA curve by overlaying it, as shown in Figure 14.

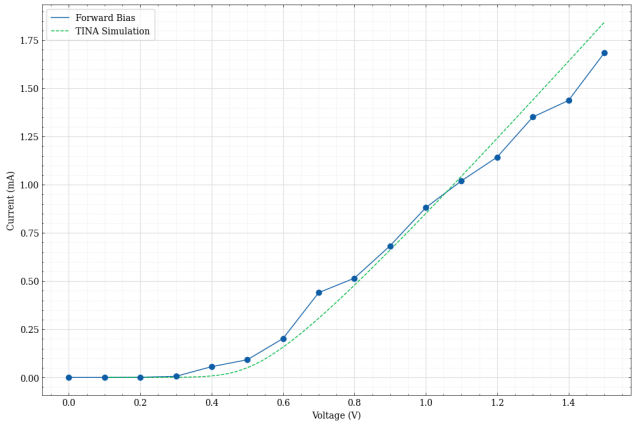


Figure 14: Forward-bias diode characteristic I-V curve obtained from the physical experimental circuit with the TINA curve overlaid for comparison.

Similarly can be done for the reverse-bias of the diode by inputting negative voltages on the TINA software with the same DC transfer characteristic mode included in the toolkit. The resulting curve, when the voltage range is rather large (-100-0 V, in this case), clearly shows the expected breakdown curve of the diode shorting, as shown in Figure 15, with a "knee" in the -80 V to -70 V range.

Closer to zero, at a smaller range (-5-0 V), the small step down of the current through the diode can be visualised, as seen in Figure 16. This value

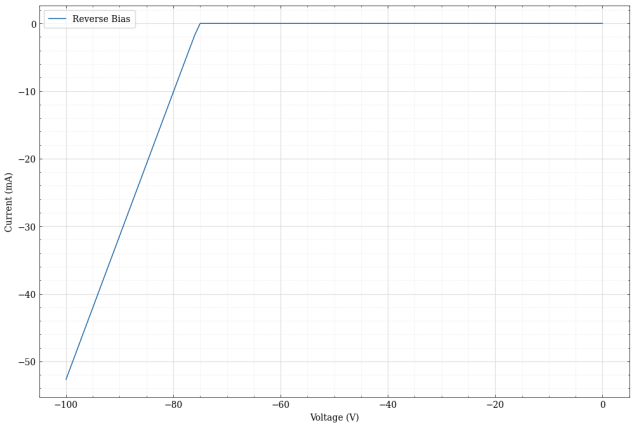


Figure 15: Reverse-bias diode characteristic I-V curve simulated on the TINA software, showing the breakdown voltage drop.

is still very close to zero but is not exactly zero.

As reverse-biased diode currents are measure in nanoamps, and due to the limited equipment available, a graph could not be made for the true values of the reverse-bias diode with the physical experimental circuit as all values measured with the improper digital multimeter would just show as zero (Appendix, table 2).

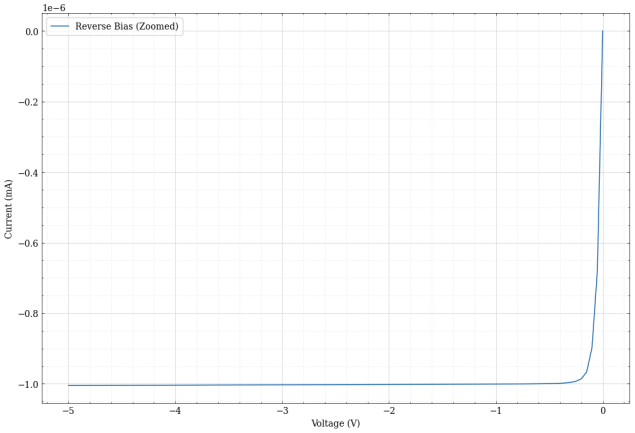


Figure 16: Forward-bias diode characteristic I-V curve simulated on the TINA software, showing the voltage curve close to 0 V.

When connected to an oscilloscope and driven by a sinusoidal waveform, the diode acts as a rectifier for the voltage, resulting in a half-wave output as shown in Figure 17 for the TINA simulation.

Similarly, when connected to an oscilloscope and driven by a sinusoidal waveform, the physical experimental circuit diode acts as a rectifier for the voltage, resulting in a half-wave output visualised on the oscilloscope, as shown in Figure 18.

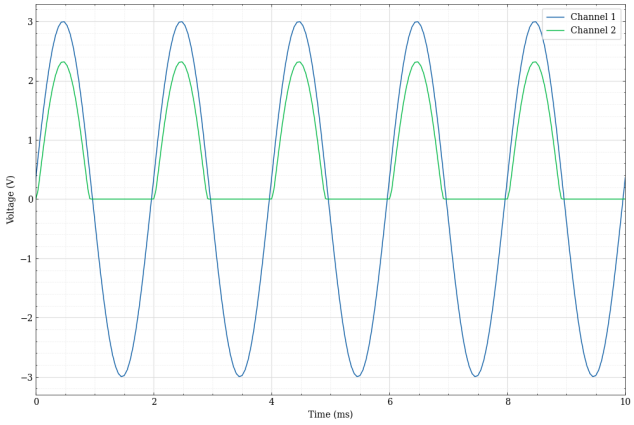


Figure 17: Resitor-diode circuit simulated on TINA driven by a sinusoidal waveform and visualised on an oscilloscope.

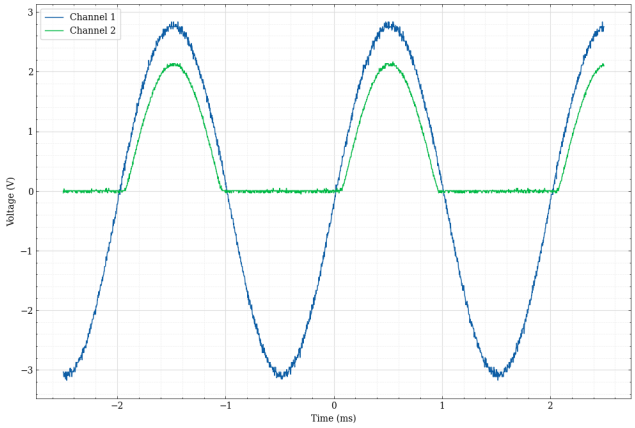


Figure 18: Resitor-diode physical experimental circuit driven by a sinusoidal waveform and visualised on an oscilloscope.

When a capacitor is added in parallel with the resistor in the TINA simulation circuit, the oscilloscope output resembles a half-wave with the capacitor discharging periods observed as ramps during the period of the diode rectifier cycle, shown in Figure 19.

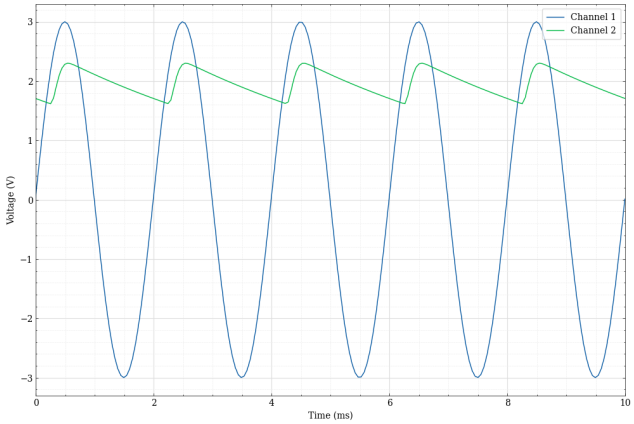


Figure 19: Resitor-capacitor-diode circuit simulated on TINA driven by a sinusoidal waveform and visualised on an oscilloscope.

Similarly, when a capacitor is added in parallel with the resistor in the physical experimental circuit and driven by a sinusoidal wave observed on an oscilloscope, the resultant output voltage is a ramp curve of the capacitor discharging during the diode cycle, and thus the flattened, rejected sections of the half-wave output, as shown in Figure 20.

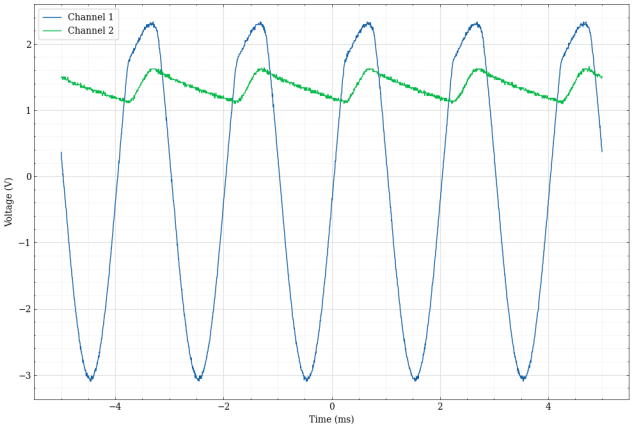


Figure 20: Resitor-capacitor-diode physical experimental circuit driven by a sinusoidal waveform and visualised on an oscilloscope.

3.4. Analysis and Discussion

The diode circuits both simulated and experimentally constructed demonstrated the expected nonlinear behaviour of semiconductor diodes. The forward-biased I-V characteristic curves (Figs. 13-14) show a near-zero current for small voltages followed by a rapid exponential increase at the "knee" once the threshold voltage is achieved, which is approximately 0.7 V for silicon diodes (1N4148). [2] The experimental data is observed to closely resemble with the TINA simulated curve, confirming the theoretical model of the diode conduction. Minor deviations between the experimental and simulated curves can be attributed to limitations in measurement equipment, diode manufacturing tolerances, and variation of the current read by the digital multimeter, alongside possible parasitic resistances of the physical circuit and power supply.

For the reverse-bias graphs, the simulated curve (Figs. 15-16) show the expected negligible reverse current (near-zero), with the breakdown region at

around -80 V to -70 V. The experimental setup could not measure this effect accurately due to the current being on the nanoamp scale, which is below the sensitivity of the provided digital multimeter. However, the overall trend is consistent with the theory, in which there is minimal current until breakdown, shorting the diode and confirming its rectifying properties.

When driven by a sinusoidal waveform, the diode-resistor circuit produced a half-wave rectified output (Figs. 17-18), matching theoretical expectations. During the positive half-cycle, the diode conducted once the threshold frequency was obtained, allowing the current to flow through the resistor. During the negative half-cycle, the diode became reverse-biased, which effectively blocked the current flow, generating the half-wave output waveform discussed. The TINA simulation showed a sharp, ideal cutoff while the experimental waveform is more rounded and marginally weakened. This difference could be due to the waveform generator's output impedance of 50 Ω, parasitic resistances in the veroboard and components, and non-ideal diode switching behaviour. These effects collectively cause a smoother transition and lower peak output voltage in the experimental waveform when compared to the simulation, which is idealised.

When the capacitor was added to the circuit in parallel with the resistor, the circuit acted as a half-wave rectifier with smoothing (Figs. 19-20), which aligns with theory. The capacitor charges to the peak voltage during conduction and discharges slowly through the resistor during the non-conducting half-cycle of the diode rectifier, producing the characteristic ramp waveform. The TINA simulation produced a well-defined decay between peaks, while the experimental curve showed a slower charging period of the capacitor and slightly faster voltage drop with less smoothing. These discrepancies can be attributed to the non-ideal real-world capacitor having as effective internal resistance and leakage current, reducing the time constant that determines the charging and discharging rates. The additional further impedance provided by the waveform generator further limited the peak charging current, preventing the capacitor from fully reaching the input voltage during each cycle.

Across all parts of the experiment, the expected theoretical behaviour of the circuit was observed with minor discrepancies across the physical experimental circuits, though these qualitative differences were explained by component tolerances, instrument impedances, and non-ideal behaviours present in the real-world components.

3.5. Conclusion

The experiment successfully demonstrated the expected theoretical behaviour of a diode circuit and their application as rectifiers and high-pass filters (for an RC circuit). The I0V characteristic curve confirmed the expected forward threshold voltage of approximately 0.7 V for silicon diodes, of which 1N4148 is, and negligible reverse current below the breakdown region. The half-wave rectifier circuit effectively converted the ac input into a dc output with a "ripple" voltage, which was smoothed with the charging and discharging of a capacitor in the circuit parallel to the resistor.

The theoretical simulated results from the TINA software showed strong qualitative agreement with the experimental data, though slight differences between values were observed with the output voltages and waveform shapes. These differences were primarily caused by the waveform generator's internal output impedance of 50 Ω, which limited current flow and introduced a small voltage drop, as well as the non-ideal behaviours of real-world components and circuit connections.

4. Experiment 19

The objective of this experiment was to simulate a transistor circuit on the TINA software and explore how it functions as a current amplifier.

4.1. Theory

4.1.1 Bipolar Transistors

Transistors are very small semiconductor diodes and have two types: field-effect transistors (FETs) and bipolar (junction) transistors, which is the most common type of transistor. [1, 2]

A bipolar transistor is a three-terminal device with collector, base, and emitter terminals. They function as such that, when a small current is applied to the base, a much larger current can be controlled flowing through the collector and emitter. It is available in two flavours: npn (negative-positive-negative) and pnp (positive-negative-positive), and such that the pnp is just

the reversed polarity of the npn transistor. [1]

For an npn transistor, they must be operated such that the base and collector are positive with respect to the emitter; and for a pnp transistor, they must be operated such that the base and collector are negative with respect to the emitter. [2]

The base-emitter and base-collector circuits behave like diodes: a small current applied controls the current flowing between the base and the emitter, so the base-emitter would be conducting while the base-collector would be reverse-biased, compared to a diode. Additionally, the maximum values of the collector current (I_C), the base current (I_B), and collector-emitter voltage (V_{CE}) cannot be emitted, or the transistor will short. [1]

4.1.2 Transistors as Current Amplifiers

If all of the rules of the bipolar transistor are followed and met, the current of the collector will be approximately proportional to the base current, and such can be written as [1, 2]:

$$h_{\mathrm{FE}} = \frac{I_C}{I_B} \tag{11}$$

This value, h_{FE}, is known as the "current gain" and is typically between the values of 10 and 1000. It is this value that makes the transistor act as a diode, as discussed. It depends on the collector current, collector-emitter voltage, and the temperature. It follows as such that, for a base more positive than the emitter by 0.6-0.8 V, that a very large current will flow, and such a base resistor should always be present in order to limit the current through the junction and prevent damage to the component. [1, 2]

4.2. Methodology

The common emitter circuit was simulated on the TINA software, as shown in Figure 21. A 2N4400 (npn) transistor was used and properly arranged with a base resistor 1 kΩ resistance and a variable resistor that was set to the same value of 1 kΩ resistance. An ammeter was attached across the collector and the base to gather the readings of the current passing through the terminals.

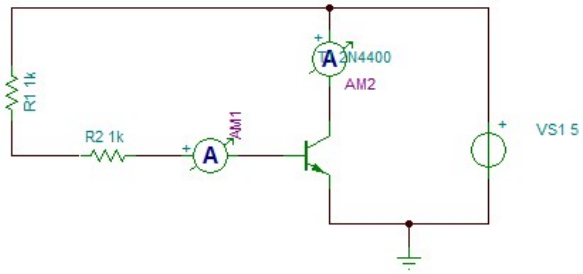


Figure 21: Experimental setup constructed on the TINA software of a common emitter transistor circuit.

Using the DC transfer characteristic function in the TINA software and measuring across the ammeters, a plot of the diode-like behaviour of the transistor can be seen. Careful care must be taken in order to not exceed the maximum collector current specified in the component manual, which is 1 A, but the device is recommended for applications up to 500 mA. [2]

4.3. Results

The resulting graph of the base and collector current sweeps for the current amplifier is shown in Figure 13. As R_B increases both I_B and I_C decrease inversely, as expected. The curve exhibits a typical diode-like exponential behaviour at low input resistances (i.e. high base currents), confirming the non-linear conduction characteristics of the base-emitter junction discussed.

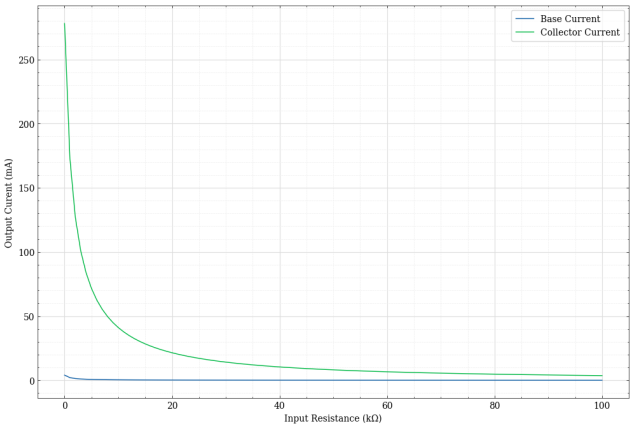


Figure 22: Graph of the base resistance and collector resistance of the common emitter transistor circuit.

From the data, the transistor's current gain was estimated to be approximately (as an average over all values obtained):

$$h_{\mathrm{FE}} = \frac{I_C}{I_B} \approx 96$$

This is consistent with the range of expected current gain values, which is 20-150 for the 2N4400 transistor (dependent on V_{CE} and I_C). [3]

4.4. Analysis and Discussion

The simulated results confirm that the common-emitter transistor configuration functions as a current amplifier, in which a small change in the base current results in a much larger proportional change in the collector current. The relationship between I_C and I_B follows the theoretical model $I_C = h_{\mathrm{FE}} I_B$, with h_{FE} as the "current gain".

In the low-resistance region ($\sim 1\,\mathrm{k\Omega}$), the base-emitter junction becomes very strongly forward-biased, leading to a rapid rise in I_B and a corresponding smaller increase in I_C. This is the "active" region of the transistor in which the current amplification occurs. At higher resistances, both currents fall exponentially, showcasing that as the base current decreases, the collector current also reduces proportionally.

At higher resistances ($\gtrsim 50\,\mathrm{k\Omega}$) a clear "cutoff" region is visible, in which the base current becomes too small to forward-bias the base-emitter junction, and so $I_C \to 0$ as expected for a non-conducting transistor. Additionally, at very low input resistance (R_B) the voltage drop becomes minimal exponentially as the I_C reaches a limiting value despite increasing I_B.

The ratio obtained for the current gain of this circuit ($h_{\mathrm{FE}} \approx 96$) falls within the expected range of possible values for the 2N4400 transistor, which is 20-150 (dependent on V_{CE} and I_C). [3], validating the circuit simulation.

Overall, the experiment demonstrates how a transistor converts small base-current variations into large collector-current changes, which is a fundamental principle of the transistor functions and applications.

4.5. Conclusion

The objective of the experiment was to simulate and investigate the operation of a common emitter npn transistor circuit and verify its behaviour as a current amplifier. The results obtained from the TINA simulation (Fig. 13) clearly displayed the characteristic relationship between the base and collector currents and confirmed the expected amplification behaviour.

The estimated current gain ($h_{\mathrm{FE}} \approx 96$) falls within the manufacturer specified range for the 2N4400 transistor, which validates the simulation and theoretical analysis. The observed behaviour demonstrated the expected regions of the transistor curve and confirmed that the collector current is directly controlled by the base current.

5. Experiment 20

The objective of this experiment was to simulate a common-emitter transistor circuit with the TINA software and observe the effect of the switching action of the load resistor for a range of resistances.

5.1. Theory

5.1.1 Transistor as a Switch

A transistor switch is when a small control current allows a much larger current to flow in a different circuit by operating in its cutoff and saturation regions. When the base-emitter junction is not forward biased (i.e. $I_B \approx 0$) the transistor is in cutoff and "off", so no collector current flows and the transistor acts like an open mechanical switch. When sufficient base current is applied, the transistor begins entering saturation, where the collector-emitter voltage drops to a small value. In this region, the transistor in conductive and acts as a closed mechanical switch. [1]

Typically, the transistor is driven to "hard" saturation in order to ensure reliable switching. This can be done by:

$$I_B \geq \frac{I_C}{h_{\mathrm{FE}}}$$

This guarantees saturation as the current gain value drops at low collector-to-base voltages, and thus the transistor acts a current-driven switch, where a small base current controls a larger collector current. Choosing a base resistor conservatively ensures plenty of excess base current, which further guarantees driving the switch into "hard" saturation. A diode in series with the collector can also prevent collector-base conduction on the negative cycles of ac supplies, for example. [1]

5.2. Methodology

The common-emitter transistor circuit was constructed on the TINA software for transistor switching analysis as shown in Figure 23. A 2N4400 transistor was used, two power sources attached to the circuit (one varying, one constant at +6 V) and the voltage across the transistor was measured. The resistor across the collector was kept at R = 1 kΩ.

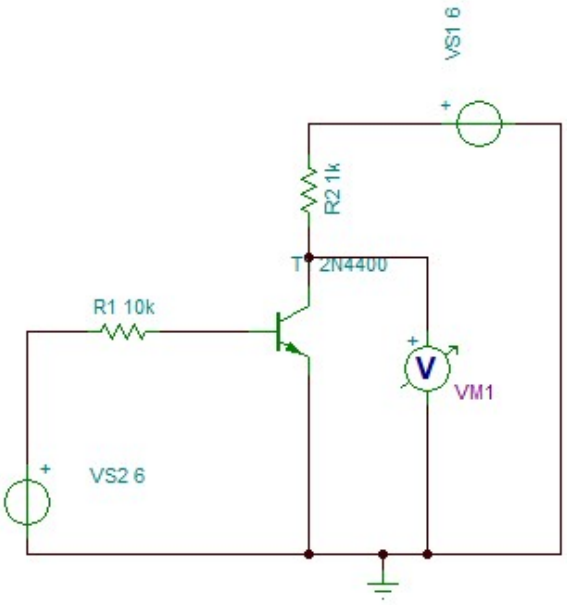


Figure 23: Experimental setup constructed and simulated on the TINA software for a transistor as a switch.

Using the 'select control target' function of the TINA software on the base resistor, the values were varied for 10 Ω, 100 Ω, 1 kΩ, and 10 kΩ, and the effect of the different base resistor values on the switching action was visualised through a curve using TINA's DC transfer characteristic function.

5.3. Results

The curves obtained for the characteristic behaviour of a transistor as a switch were obtained and plotted, varying with the base resistor (R_B) values.

For a 10 Ω base resistor, shown in Figure 24, the cutoff region is observed to be very small and takes a long time to reach saturation, which does not fully approach zero. Therefore, this does not make a very fast nor effective switch.

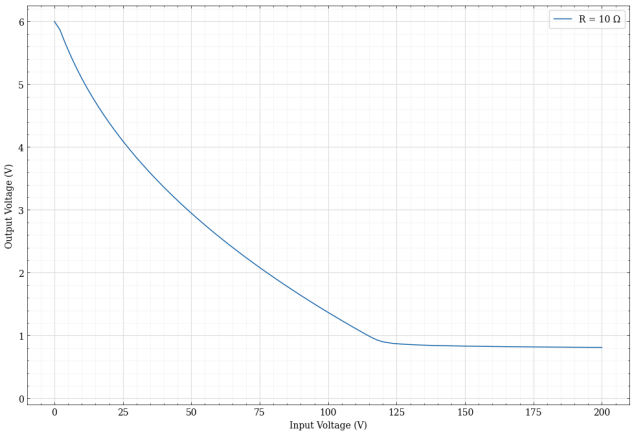


Figure 24: Transistor as a switch curve for a 10 Ω base resistor.

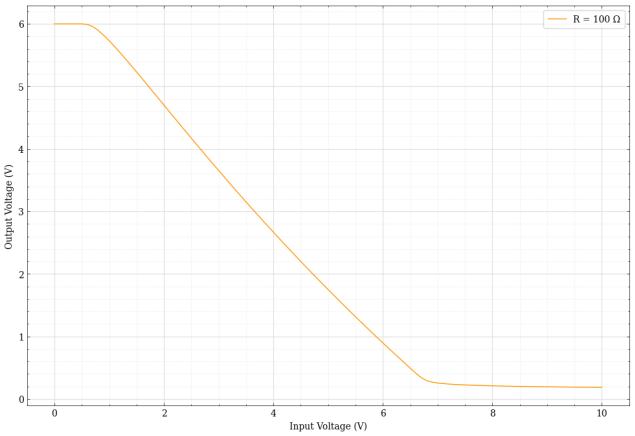


Figure 25: Transistor as a switch curve for a 100 Ω base resistor.

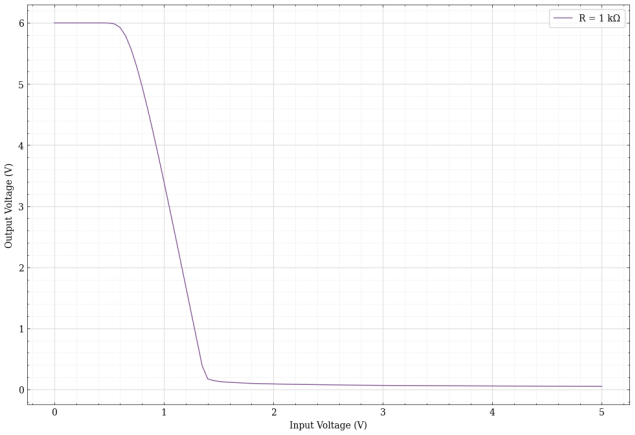


Figure 26: Transistor as a switch curve for a 1 kΩ base resistor.

For a 100 Ω base resistor, shown in Figure 25, the cutoff region is observed to be larger and the decreasing slope to zero (ground) to fall faster, though not as fast as ideal for rapid switching. This value also does not fully approach zero but gets closer than the 10 Ω base resistor value did.

For a 1 kΩ base resistor, shown in Figure 26, the cutoff region is observed as sufficiently large with a rapid fall approaching zero as the transistor reaches saturation close to zero, this ensures rapid switching action in the circuit.

For a 10 kΩ base resistor, shown in Figure 27, the cutoff region is large relative to the scale of the graph, but the fall of the curve to zero (ground) is very rapid and approaches zero the closest.

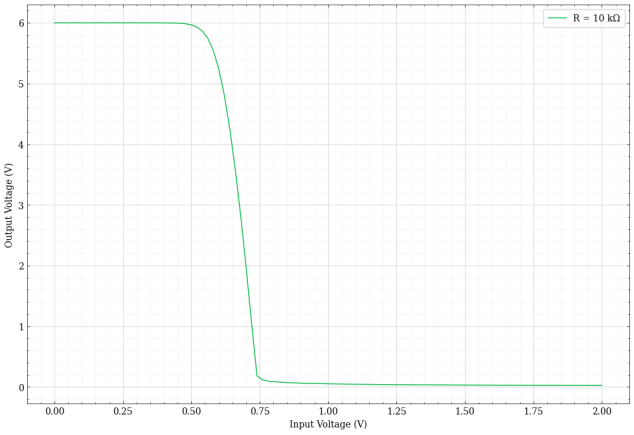


Figure 27: Transistor as a switch curve for a 10 kΩ base resistor.

All graphs display the expected behaviour of a transistor behaviour as a switch, with clearly visible cutoff and saturation regions approaching ground (zero).

5.4. Analysis and Discussion

The simulated common-emitter circuit produced the expected transistor switching behaviour between the cutoff and saturation regions discussed in the theoretical model. By varying the base resistor values, the base current was altered, which directly controlled the transistor's conduction into cutoff (non-conducting) or saturation (conducting).

For low base resistor values (R = 10 Ω), the base current was sufficiently large to forward-bias the base-emitter junction strongly. Despite the transistor reaching saturation, the transition was not sharp, and the collector-emitter voltage did not fully approach zero. This behaviour indicates that the transistor was over-driven, in which excessive base current does not yield further switching improvement and instead reduces efficiency. Additionally, very low base resistance risks exceeding the recommended base current limits, which may lead to the overheating and damage of a transistor in a physical circuit.

Increasing the basre resistor to R = 100 Ω improved the switching response rate, showing a more distinct transition between cutoff and saturation. However, some residual collector-emitter voltage remained at saturation. The transistor, while sufficiently driven into conduction, was not yet in the optimal switching regime.

The most effective switching occurred at R = 1 kΩ, in which a clean and rapid transition to saturation from cutoff was observed. The collector-emitter voltage approached its expected low saturation value, indicating that the required switching condition $I_B \geq I_C/h_{\mathrm{FE}}$ was satisfied without excessive drive current. This demonstrated effective switching performance, achieving near-ideal "on-off" control.

For very high base resistance (R = 10 kΩ), the transistor moved toward the cutoff region as the base current was insufficient to maintain strong forward-bias. Although the cutoff region became more pronounced, the transistor did not always reach "hard" saturation which indicates incomplete switching. This reinforces the requirement for a suitable supplied base current such that the transistor is reliably turned "on".

Overall, the results illustrate the importance of selecting an appropriate base resistor when using a transistor as a switch. Too small of a value may lead to inefficient or potentially damaging current flow, while too large of a value may prevent the transistor from reaching "hard" saturation. The simulation confirmed the theoretical expectations for the switching behaviour of a transistor and emphasised the balance in choosing a base resistor to ensure reliable, quick, and efficient electrical switching.

5.5. Conclusion

The objective of this experiment was to investigate the behaviour of an npn transistor in a common-emitter configuration when used as a switch. By varying the value of the base resistor, the switching performance of the transistor was observed through the transition from the cutoff region to the saturation region. The results demonstrated that the transistor can act as an effective electronic switch when the base resistor is appropriately chosen, and therefore the base current ap-

propriately controlled. A very small base resistance resulted in excessive base drive and inefficient switching action, while a very large resistance prevented the transistor from reaching "hard" saturation.

The optimal switching characteristics were observed for intermediate resistance values for the base resistor, where the transistor was driven most reliably into "hard" saturation with a clean and rapid transition from cutoff to saturation. Thus, the experiment confirmed the theoretical principles and expectations of transistor switching and emphasised the importance of selecting suitable base resistor values.

6. Experiment 21

The objective of this experiment was to simulate and construct a light sensitive alarm using the properties of a transistor as a switch and a light-dependent resistor (LDR) to drive an LED to switch on in darkness and switch off in brightness.

6.1. Theory

6.1.1 LED Driver

Light-emitting diodes (LEDs) are similar to the silicon signal diodes previously used and discussed but with a larger voltage drop; as in, a range of 1.5-3.5 V typically rather than the ordinary diode's ∼0.7 V. Such, as voltage across the LED increases, the current begin conducting within the LED range and current increases rapidly as more voltage is applied, allowing the LED to light up. In comparison, the I-V behaviour curve of an LED is much steeper. [1]

Using an npn transistor as a switch, the LED can be constructed as such to light up in response to a digital signal line at high voltage value, choosing the collector resistor in a way that determines the provided current to the LED. The base resistor must also then be chosen in a way that ensures saturation, acting as a switch and therefore the collector resistor acts as the operating current. [1]

6.2. Methodology

The common-emitter circuit was constructed and simulated on the TINA software, shown in Figure 28. This ensured that the LED nor transistor would be damaged by any incorrect resistor or current values. The dc voltage supply was set at 5 V. The LDR resistance was assumed at 1.2 kΩ and the resistor across the base junction was set to 1 kΩ.

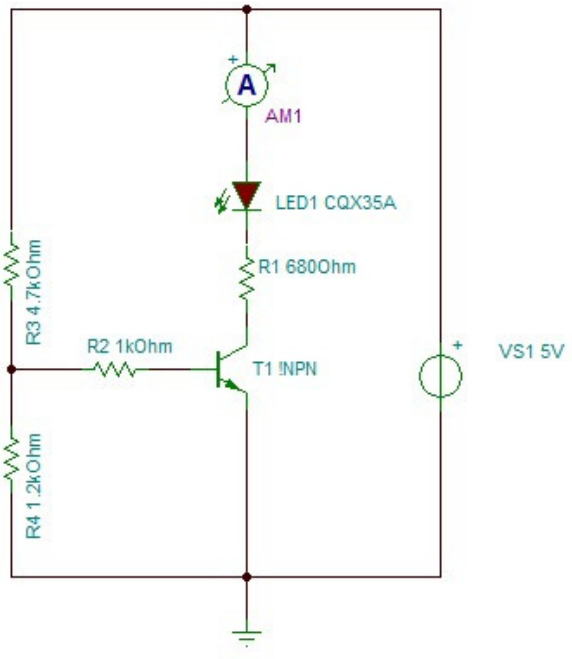


Figure 28: Experimental setup constructed on the TINA software.

The load resistor (across the collector) was determined with Ohm's law and LED specifications for the threshold (assumed 1.8 V for the voltage drop necessary):

$$R_{\text{load}} = \frac{V}{I} = \frac{5 - 1.8}{5 \times 10^{-3}} = 640\,\Omega$$

The closest value in the lab to the calculated resistance was 680 Ω, and hence that was the resistor used.

To determine the value necessary for the base resistor (across the base and the LDR), the values for "bright" and "dim" of the LDR were found with a digital multimeter. For "bright", this was determined as 32 Ω, and for "dim" this was determined as 0.522 MΩ. Using $R_B = \sqrt{R_{\text{bright}} \cdot R_{\text{dim}}}$ the value for the base resistor was determined to be approximately 4.1 kΩ, but was chosen as 4.7 kΩ from the available resistors in the lab.

6.3. Results

The LED turned on as intended in "dim" conditions and turned off in "bright" conditions, dependent on the LDR light exposure.

On the TINA software, by explicitly changing the LDR condition to "day" and "night", this was visualised on the simulated circuit.

Experimentally, due to complications with the veroboard connections (i.e. forgetting to break connections across a vertically connected resistor), the base resistor value was assumed wrong and doubled (by coordinator suggestion), and such the "dim" conditions are a completely bright room, and the "bright" conditions are very bright lights held up at very close proximities to the LDR sensor. It is not a very effective light alarm.

To estimate the cost of operating the circuit over the course of one year, the current drawn by the LED when switched on must be considered. The LED forward voltage was assumed to be approximately 1.8 V, and the supply voltage was 5 V. With a load (collector) resistor of 680 Ω, the current through the LED is given by Ohm's Law:

$$I = \frac{V_{\text{sup}} - V_{\text{LED}}}{R_l} = \frac{5 - 1.8}{680} = 4.7\,\text{mA}$$

The power consumed by the circuit when the LED is on is therefore:

$$P = VI = (5)(4.7 \times 10^{-3}) = 0.0235\,\text{W}$$

Assuming the LED is on for 12 hours per day:

$$\text{Energy per day} = 0.0235 \cdot 12 = 0.282\,\text{Wh}$$

Over the course of one year, or 365 days:

$$\begin{aligned}\text{Energy per year} &= 0.282 \cdot 365 = 103\,\text{Wh} \\ &= 0.103\,\text{kWh}\end{aligned}$$

If electricity is assumed to cost €0.18 per kWh:

$$\text{Cost per year} = 0.103 \cdot 0.18 = 0.0185$$

Therefore, approximately, the total annual cost to power the circuit would be **€0.02** per year. This shows that the circuit consumes very little electrical power in normal operation, as expected with LEDs.

6.4. Analysis and Discussion

The results obtained from the constructed circuit confirm the epxected behaviour of the transistor operating as a switch controlled by the LDR. In "bright" conditions, where the resistance of the LDR is low, the voltage at the transistor base remained too small to forward-bias the base-emitter junction. As a result, the transistor was in the cut-off region and no collector current flowed, which ensured that the LED remained off. In "dim" conditions, the resistance of the LDR increased significantly, which raised the base voltage and therefore allowed the forward-biasing of the base-emitter junction. Consequently, the transistor entered the saturation region, which allowed current to flow through the collector-emitter path and therefore turn the LED on. This demonstrates the intended automatic light-sensitive switching behaviour.

The calculated resistor values ensured that the transistor operated correctly. The load resistor was chosen to limit the LED current to safe operating levels, preventing damage to either the LED or transistor. The base resistor value was determined using the geometric mean of the measured LDR resistances in individually chosen "bright" and "dim" conditions lighting variations. However, in the physical circuit, connection difficulties and unintended conductive paths on the veroboard caused confusion, leading to the switching of the base resistor to a higher value and therefore altering the "bright" and "dim" conditions previously calculated, requiring a very strong light to switch the LED off. While this reduced the practical sensitivity, the switching behaviour was still observed and matched the theoretical model.

The cost calculations showed that the power consumption for such a circuit are extremely low, with an estimated annual cost of approximately **€0.02** per year, assuming 12 hours of LED operation per day. This highlights the efficiency of the transistor-controlled switching LED circuits and their suitability for long-duration, power-efficient applications, such as nightlights, alarms, and sensor-triggered indicators. Overall, the ex-

periment showcased how an npn transistor can be effectively used as a switch and how variations in input resistance (via the LDR) can be used to automate a circuit to environmental conditions.

6.5. Conclusion

The objective of this experiment was to construct and test a light-sensitive switching circuit using an npn transistor and an LDR to control an LED. The circuit successfully switched the LED on in "dim" conditions and off in "bright" conditions, confirming the expected behaviour of the transistor switching between cutoff and saturation regions.

While the practical limitations in the veroboard assembly affected the sensitivity threshold, the desired core switching function of the transistor remained consistent with theoretical predictions. The calculated power usage further showed the efficiency of the circuit as it consumed very little energy to operate continuously over a full year. This experiment effectively demonstrated the transistor switching capabilities and the use of LDRs as light-based control elements in low-power electronic systems.

7. Experiment 25

The objective of this experiment was to create a circuit with an operational amplifier (op-amp) and generate a gain of 20 dB, driven by a 1 kHz sinewave and comparing the input and output in an oscilloscope. Then, by inserting a capacitor, the effect on the signal bandwidth was observed and discussed.

7.1. Theory

7.1.1 Operational Amplifiers

The operational amplifier (op-amp) is a very high-gain amplifier device with a single-ended output. Real-world op-amps have much high gain ($10^5 \sim 10^6$) and lower output impedances, allowing them to swing through most, if not all, of the voltage supply range, often using a split supply (i.e. full negative to positive range). [1]

Op-amps have two input terminals: the inverting (-) and non-inverting (+) inputs that function as expected, the output going positive when the non-inverting input goes more positive than the inverting input. The symbols associated only serve to inform of the relative phase of the output, which is important when keeping the negative feedback as negative. [1, 4]

In circuit diagrams, the power-supply connections are often not shown and there is no grounding terminal. This is due to the nature of the op-amp having such a high open-loop gain that the characteristics depend only on the feedback network for any reasonable close-loop gain. [1, 4]

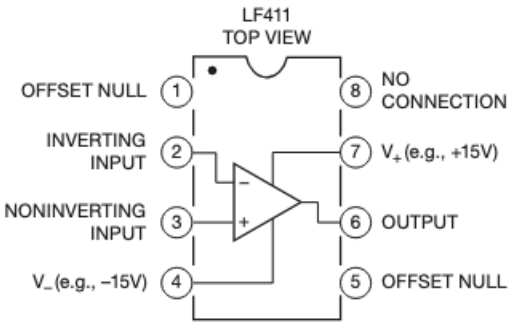


Figure 29: Pin connections for LF411 op-amp in 8-pin DIP. [1]

The pin connections of a LF411 op-amp in an 8-pin DIP, for reference, are shown in Figure 29. The dot, or notch, in the upper left corner indicates the first pin and therefore where to begin counting from. To count the pins, follow them counterclockwise, viewing them from the top. [1]

7.1.2 Negative Feedback

Negative feedback is the process in which coupling the output voltage back, some input can be cancelled by returning the input with an opposing phase angle, which can improve characteristics such as linearity, response unity, and predictability. [1, 4]

As op-amps are often used in high-loop-gain limits, very small input voltages would drive the op-amp into saturated output states. A closed-loop voltage gain (A_{cl}) can be used controlled and reduced with a negative feedback such that the op-amp functions as a linear amplifier. The feedback network can be either frequency- or amplitude-dependent, where frequency would make a linear amplifier and amplitude a non-linear amplifier. [1, 4]

7.1.3 The Golden Rules

The two golden rules may be used to understand an op-amp with negative feedback [1, 2]:

I. The output attempts to do whatever necessary to make the voltage difference between inputs zero.

II. The inputs draw no current.

These rules can be assumed as the op-amp voltage is so high that any small difference between inputs will swing output over the full range, and the op-amps use very little current (often in the picoamp range), and such the following can be generalised and rounded to give the two golden rules. [1]

7.1.4 The Non-Inverting Amplifier

An op-amp in a closed-loop non-inverting amplifier configuration is driven with a controlled voltage gain and the input signal is applied to the non-inverting (+) input. The output is applied back to the inverting (-) input through the closed feedback loop that is formed by an input resistor R_i and a feedback resistor R_f. [4]

With the first golden rule, it can be imposed that the inverting input is equal to the non-inverting voltage, such that $V_- = V_{\text{in}}$. Therefore, using Ohm's law, the current flowing through the input must be $I_i = V_{\text{in}}/R_i$. [2]

From the second law, since the inputs draw no current, it can be imposed that $I_i = I_f$ as all of I_i must flow also through R_f. Hence [2]:

$$\begin{aligned} V_{\text{out}} &= V_- + I_f R_f \\ &= V_{\text{in}} + I_i R_f \\ &= V_{\text{in}} + \frac{V_{\text{in}}}{R_i} R_f \\ &= V_{\text{in}} \left(1 + \frac{R_f}{R_i}\right) \\ \therefore A_{\text{cl}} = \frac{V_{\text{out}}}{V_{\text{in}}} &= \left(1 + \frac{R_f}{R_i}\right) \end{aligned} \tag{12}$$

This is such that the gain is always greater than the unity, which is independent of the open-loop gain (A_{ol}), and is controllable with the negative feedback network. [2]

7.2. Methodology

The physical experiment circuit was set up as required with the circuit diagram shown in Figure 30. The pin connections were determined with guidance of Figure 29 and carefully arrange on the veroboard. The circuit was driven with a 1 kHz sinusoidal wave and the $V_C C$ was taken to be ± 12 V.

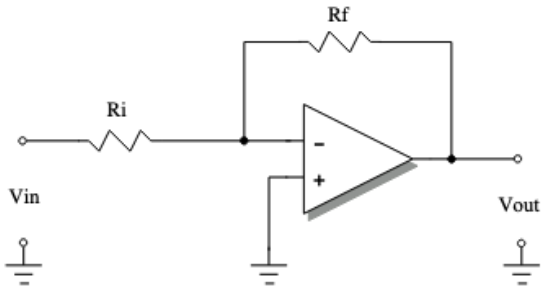


Figure 30: Circuit diagram of the experimental setup. [2]

An LM741 op-amp was used and the resistor components were chosen with Equation 12 and Equation 8 to give a gain of 20 dB. It follows:

$$20 \log_{10} \left(\frac{V_{\text{out}}}{V_{\text{in}}}\right) = 20$$

As $A_{\text{cl}} = V_{\text{out}} V_{\text{in}}$, it becomes:

$$\begin{aligned} \log_{10}(A) &= 1 \\ A &= 10^1 \\ &= 10 \end{aligned}$$

Substituting into Equation 12, the ratio of the resistors is found:

$$\begin{aligned} 10 &= 1 + \frac{R_f}{R_i} \\ 9 &= \frac{R_f}{R_i} \\ \therefore 9R_i &= R_f \end{aligned}$$

From the laboratory components available, this was chosen to be $R_i = 220\,\Omega$ and $R_f = 2\,k\Omega$, which is approximately the ratio calculated.

The capacitor value was chosen with the use of Equation 9, and found that:

$$f = \frac{1}{2\pi RC}$$
$$C = \frac{1}{2\pi R_f f}$$

The closest value of capacitor available in the lab was 10 μF, which was also the one we were consulted to use. This capacitor was then added in parallel with R_f on the physical experiment circuit.

7.3. Results

The characteristic Bode plot curves obtained for the non-inverting amplifier circuit **without** the capacitor remained approximately constant at around 20 dB for low and mid-range frequencies, as seen in Figure 31. The output displayed a flat magnitude response from 10 Hz up to approximately 10^4 Hz.

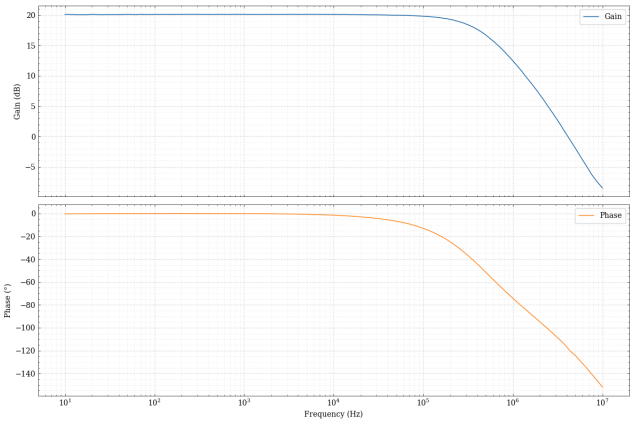


Figure 31: Oscilloscope gain and phase curves obtained from the op-amp circuit with no capacitor.

This indicates that the amplifier maintained the intended close-loop gain of 10 in this region. Beyond this point from $10^5 - 10^7$ Hz the gain fell steadily, decreasing as the frequency kept increasing. The phase response remained close to 0° at low frequencies and progressively shifted to negative values as frequency increased, approaching approximately -140° at the highest measured frequency (10^7 Hz).

The characteristic Bode plot curves obtained for the non-inverting amplifier circuit **with** the capacitor in parellel to the feedback resistor R_f, the gain became clearly frequency-dependent, as shown in Figure 32, even at low frequencies. The gain remained close to 20 dB from 10-30 Hz, after which it decreased gradually and approached zero.

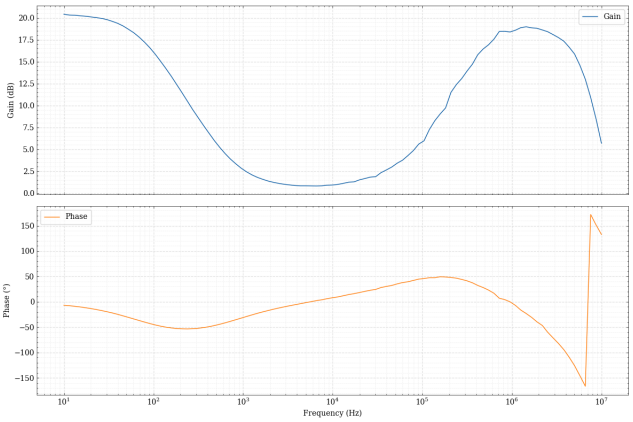


Figure 32: Oscilloscope gain and phase curves obtained from the op-amp circuit with a capacitor.

With the oscilloscope data shown in the Bode plot, at around 200-300 Hz the gain falls to 10 dB, and at around 3k-10^4 Hz falls close to 0 dB. The phase angle response shifted progressively more negative with increasing frequency, reaching values below -140° at higher frequencies. This shows how the capacitor significantly lowered the amplifier's bandwidth by introducing a frequency-dependent feedback network behaviour.

7.4. Analysis and Discussion

The results obtained confirmed the expected behaviour of the non-inverting amplifier circuit both with and without a capacitor. Without the capacitor, the close-loop gain matched the theoretical value:

$$A_{\text{cl}} = 1 + \frac{r_f}{R_i} \approx 10$$

The corresponding flat region of the Bode plot magnitude curve indicated that the amplifier functioned well within its mid-band in which the open-loop gain of the op-amp was high enough to sustain the desired close-loop gain. The eventual fall in gain and shift in phase at higher frequencies is consistent with the finite gain-bandwidth product of the op-amp.

When the capacitor was added in parallel with the feedback resistor, the feedback became frequency-dependent. At low frequencies, the capacitor behaved as having high impedance, which made the feedback loop effectively resistive and maintained the original closed-loop gain. As frequency increased, the impedance of the capacitor decreased, which in turn increased the proportion of feed-

back and thus reduced gain. This produced the observed low-pass amplifier behaviour, supported by the gradual shift of the phase angle towards negative as reactive feedback introduces phase lag as frequency increases.

The measured frequency at which gain begins to drop (cutoff) is consistent with the value expected from the RC time constant value of the feedback network. The experiment therefore showcased the direct relationship between feedback impedance and the amplifier-frequency response, demonstrating how reactive feedback can be used alter the bandwidth and improve high-frequency stability.

7.5. Conclusion

The objective of the experiment was to construct a non-inverting amplifier circuit with an op-amp and characterising its frequency response both with and without a capacitor introduced parallel to the feedback resistor.

The amplifier without the capacitor exhibited a stable mid-band gain of approximately 20 dB, with the gain falling towards zero at higher frequencies as expected from the op-amp's finite bandwidth.

When the capacitor was introduced into the circuit, the circuit displayed a reduced bandwidth and a frequency-dependent gain, confirming the behaviour of an active low-pass configuration with the addition of a reactive component.

The experimental results were consistent with the theoretical expectations and effectively demonstrated the influence of negative feedback and reactive components on the amplifier frequency response and bandwidth.

8. Experiment 27

The objective of this experiment was to design and simulate a 4-bit Digital-to-Analogue Converter (DAC) with resistors, switches, and an op-amp, choosing the resistors in a way that produced a range of voltages from 0 V to -3 V.

8.1. Theory

8.1.1 Summing Amplifier

The summing amplifier is a variation of the inverting amplifier which sums the currents from each of the input branches and the resulting current flows through the feedback resistor. So, the input current would obey Ohm's law $V_1/R_1 + V_2/R_2 + \cdots + V_N/R_N$. For equal resistor values, this would be $V_{\text{out}} = -(V_1 + V_2 + \cdots + V_N)$, and such the output voltage as a linear combination becomes [1, 2]:

$$V_{\text{out}} = -R_f \left(\frac{V_1}{R_1} + \cdots + \frac{V_N}{R_N} \right) \tag{13}$$

The output voltage is then the amplified voltage of the circuit. Inputs can be positive or negative and do not have to be necessarily equal. With four inputs, for example, each of which is either +1 V or zero ("on" or "off"), representing values 1, 2, 4, 8, by using input resistors according to the binary value ratios, the output will be equal to the binary count input. This is the basis for a digital-to-analogue converter (DAC), which convert a binary input value into a corresponding analogue output, producing a voltage or current that is directly proportional to the digital value provided. [1]

8.1.2 Digital Logic

Input signals are often in discrete form so the use of electronic circuits and devices is consequently natural and appropriate as they operate with signal representations of 0s and 1s. Thus, it can be beneficial to convert continuous (analogue) data to a digital form through the use of analogue-to-digital converters (ADC) or digital-to-analogue converters (DAC) to represent and store data with a computer or signal processor, for example. With the use of digital systems, this can also reduce "noise" in data that may otherwise be picked up by analogue forms, allowing it to be reconstructed without error. [1]

Typically, a system can only be in two states at any point, for example, a transistor can either be saturated or non-conducting, "on" or "off", respectively. These states are associated with either a 1 or a 0, known as "bits" which store the information of the current state of that device at a given time. [1]

Computers work in "byte" systems which store 8-bits per byte, though they are often organised by 16-, 32-, or 64-bit "words", such that a word is then 2, 4, or 8 bytes respectively. This allows computers to store large amounts of information in a concise and organised manner. [1] For example, this report file is 4 megabytes, or 4 $\times 10^6$ bytes, which would make it a total of 32 $\times 10^6$ bits (for

a 64-bit modern computer)!

8.2. Methodology

The inverting summing amplifier circuit setup was constructed and simulated on the TINA software, as shown in Figure 33, to create a 4-bit DAC. With the goal of outputting a desired range of 0 V to -3 V (inverted from positive input), a binary system was chosen such that 2^n with n = 4-bit system. Such, the ladder resistors were chosen as 1 kΩ, 2 kΩ, 4 kΩ, 8 kΩ (§8.1.1), with input voltage set at 5 V.

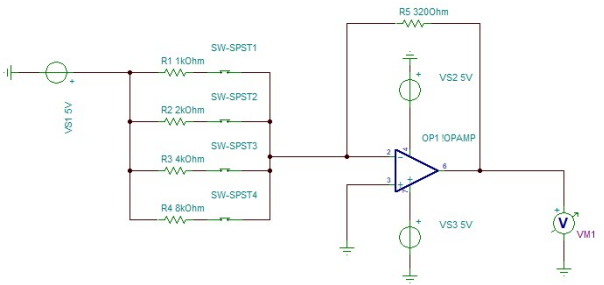


Figure 33: 4-bit inverting amplifier circuit constructed on the TINA software.

The feedback resistor across the op-amp was then chosen with Equation 13:

$$\begin{aligned} -3 &= -R_f \left(\frac{5}{1k} + \frac{5}{2k} + \frac{5}{4k} + \frac{5}{8k} \right) \\ &= -R_f \left(\frac{3}{320} \right) \\ \therefore R_f &= 320\,\Omega \end{aligned}$$

The feedback resistor was then to 320 Ω.

8.3. Results

By switching the analogue switches "on" or "off", the behaviour of the resistors were observed and tabled (Appendix, table 3). When all switches were "on", the desired output of -3 V was achieved, and when all switches were "off" the expected 0 V was approached (very small value).

8.4. Analysis and Discussion

The 4-bit DAC circuit constructed using an inverting summing amplifier circuit on the TINA software successfully demonstrated the conversion of discrete digital input states into a continuous analogue output voltage. Each binary input combination corresponded to a specific weighted contribution determined by the resistor network, with the op-amp producing a negative output proportional to the sum of the weighted voltages.

The measured output voltages showed a near-linear relationship with the binary input values, confirming that the circuit operated as expected according to theoretical predictions. The maximum output of -3 V was achieved when all of the switches were "on" (i.e. "1111"), while the output approached close to 0 V when all of the switches were "off" (i.e. "0000").

The op-amp's high open-loop gain ensured that the virtual grounding at the inverting input remained stable, allowing for the accurate summing of the input currents. However, any offset voltage or input bias current would still produce small errors, which are particularly noticeable at lower binary values, where the analogue voltage steps are smallest. Overall, the experiment demonstrated how analogue summing amplifiers can be adapted to function as DAC circuits using binary-weighted inputs. The close correspondence between measured outputs and expected outputs validated theoretical predictions and proper operation of the DAC.

8.5. Conclusion

The objective of this experiment was to design and simulate a 4-bit DAC using a summing amplifier configuration. The circuit successfully produced distinct analogue voltage levels corresponding to each binary input combination, showcasing the principle of the digital-to-analogue conversion. The experiment therefore confirmed the theoretical operation of the DAC circuit and demonstrated practical use of op-amps with digital logic in analogue systems.

References

[1] P. Horowitz, W. Hill, and I. Robinson, *The art of electronics*. Cambridge university press Cambridge, 1989, vol. 2.

[2] UCD, "3Y Electronics 2023-," *3rd Year Astro and Space Physics Laboratory Manual*, n.d.

[3] M. Electronics, "2n4400 npn general purpose transistor datasheet," Mouser Electronics, Datasheet, 2015, [Accessed 26-October-2025]. [Online]. Available: https://www.mouser.com/datasheet/2/149/2N4400-193292.pdf

[4] T. Floyd, *Electronic Devices: Conventional Current Version*. Prentice Hall, 2012. [Online]. Available: https://books.google.ie/books?id=2D7lwAEACAAJ

List of Figures

Appendix

Table 1: Table for the values obtained for the physical experimental circuit corresponding to Fig. 8.

f (Hz)	V_{in} (V)	V_{out}	ϕ (°)
1	8.52	61.1m	87
10	1.01	61.2m	84.8
100	1.02	502m	59.68
1k	970m	1.00	6.95
10k	950m	1.02	0.14
100k	970m	1.02	0.56
1M	930m	970m	0.90

Table 2: Table of the values obtained from the digital multimeter for the physical experimental circuit corresponding to Fig. 14.

V (V)	I_{forward} (mA)	I_{reverse} (mA)
0	0	0
0.1	0	⋮
0.2	0.001	⋮
0.3	0.006	⋮
0.4	0.056	⋮
0.5	0.092	⋮
0.6	0.202	⋮
0.7	0.440	⋮
0.8	0.515	⋮
0.9	0.683	⋮
1.0	0.881	⋮
1.1	1.020	⋮
1.2	1.143	⋮
1.3	1.351	⋮
1.4	1.437	⋮
1.5	1.683	⋮

Table 3: Table of the binary switch combinations and respective output voltages for the DAC circuit (§8).

Binary	V (V)
1111	-3
1110	-2.8
1101	-2.6
1011	-2.2
0111	-1.4
1100	-2.4
1010	-2
0110	-1.2
1001	-1.8
0101	-1
0011	-600m
0001	-200m
0010	-400m
0100	-800m
1000	-1.6
0000	-6.4u

ElectronicsLab

October 27, 2025

[1]:
```
import numpy as np
import matplotlib.pyplot as plt
from scipy.optimize import curve_fit

import scienceplots
```

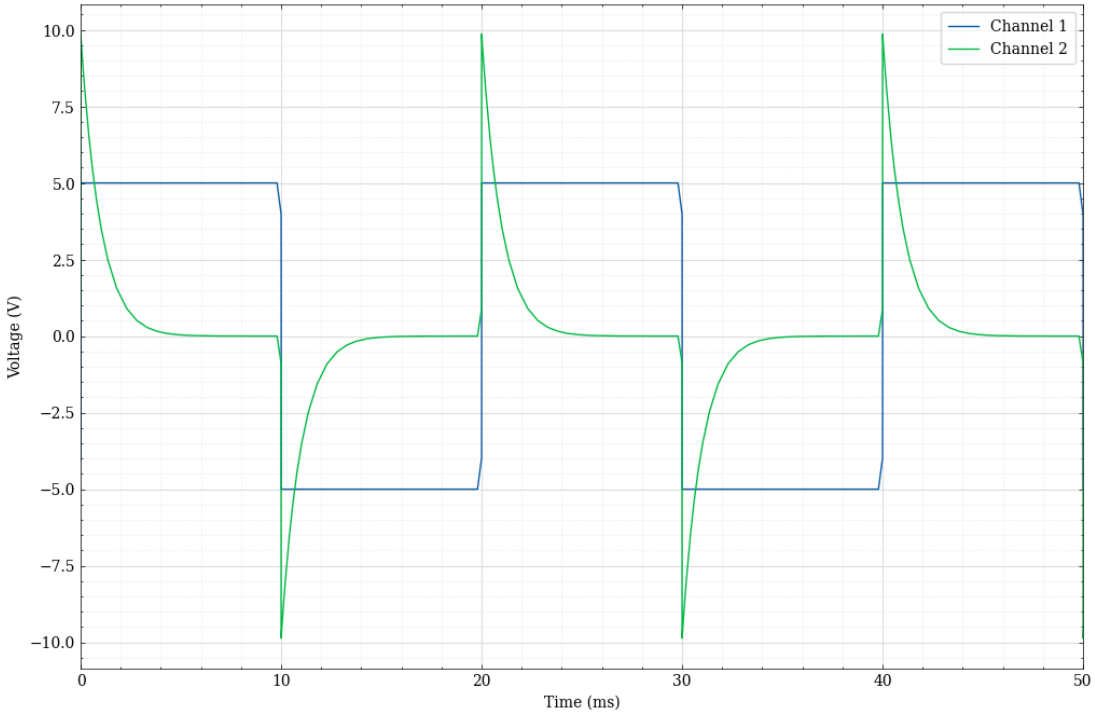
[2]:
```
plt.style.use('science')

plt.rcParams['figure.figsize'] = [12, 8]
plt.rcParams['text.usetex'] = False

plt.rcParams['axes.prop_cycle'] = plt.cycler(color=[
'#0C5DA5', '#00B945', '#FF9500', '#FF2C00', '#845B97', '#474747', '#9e9e9e'
])
```

1 Ex 5

[3]:
```
ex5 = np.loadtxt("/Users/JoanaUCD/Library/CloudStorage/
 ↪OneDrive-UniversityCollegeDublin/Labs/labs-files/labs_code/Labs-Code/
 ↪labcode_s3/ex5.txt", skiprows=1)

ex5_x = ex5[:,0]
ex5_ch1 = ex5[:,1]
ex5_ch2 = ex5[:,2]
```

[4]:
```
fig, ax = plt.subplots()

ax.plot(ex5_x * 1e3, ex5_ch1, label='Channel 1')
plt.xlim([0,50])

ax.plot(ex5_x * 1e3, ex5_ch2, label='Channel 2')

plt.xlabel('Time (ms)')
plt.ylabel('Voltage (V)')

ax.minorticks_on()
ax.grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
```

```
ax.grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
 ↪zorder=1)

ax.legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.show()
```

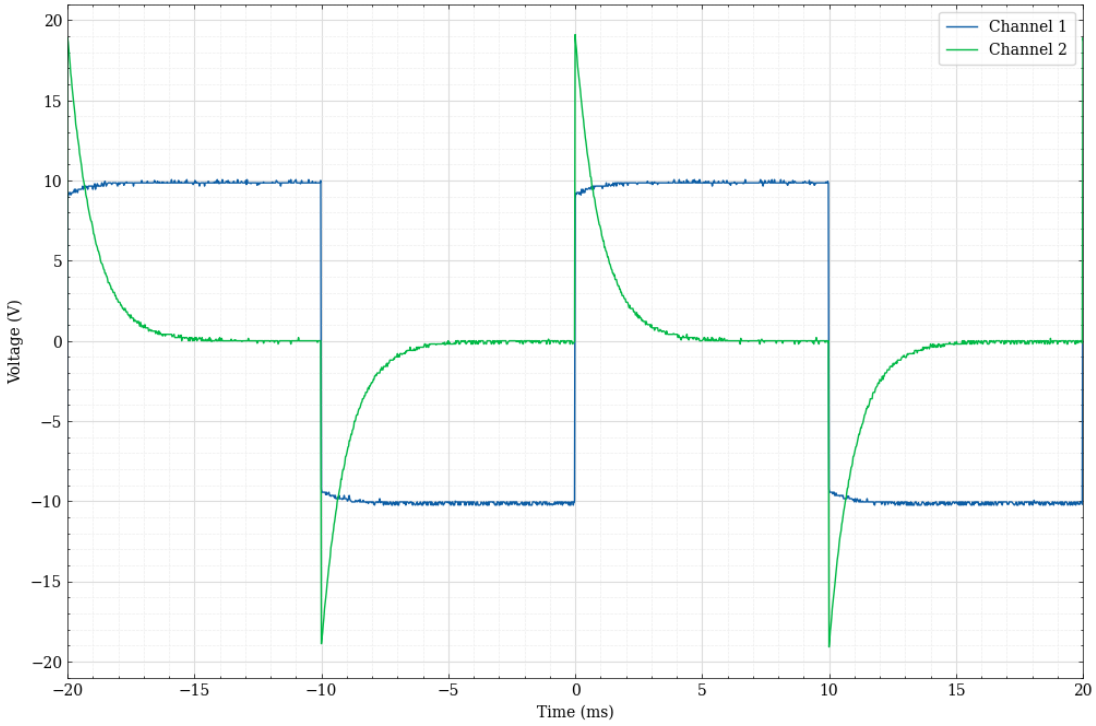


[5]:
```
ex5 = np.loadtxt("/Users/JoanaUCD/Library/CloudStorage/
 ↪OneDrive-UniversityCollegeDublin/Labs/labs-files/labs_code/Labs-Code/
 ↪labcode_s3/exp5_osl2.txt", skiprows=2)

ex5_x_osc = ex5[:,0]
ex5_ch1_osc = ex5[:,1]
ex5_ch2_osc = ex5[:,2]
```

[6]:
```
"""
# Add markers to see where indices are
for i in range(0, len(ex5_x_osc), 100):
    plt.text(ex5_x_osc[i]*1e3, ex5_ch2_osc[i], str(i), fontsize=8)
"""
```

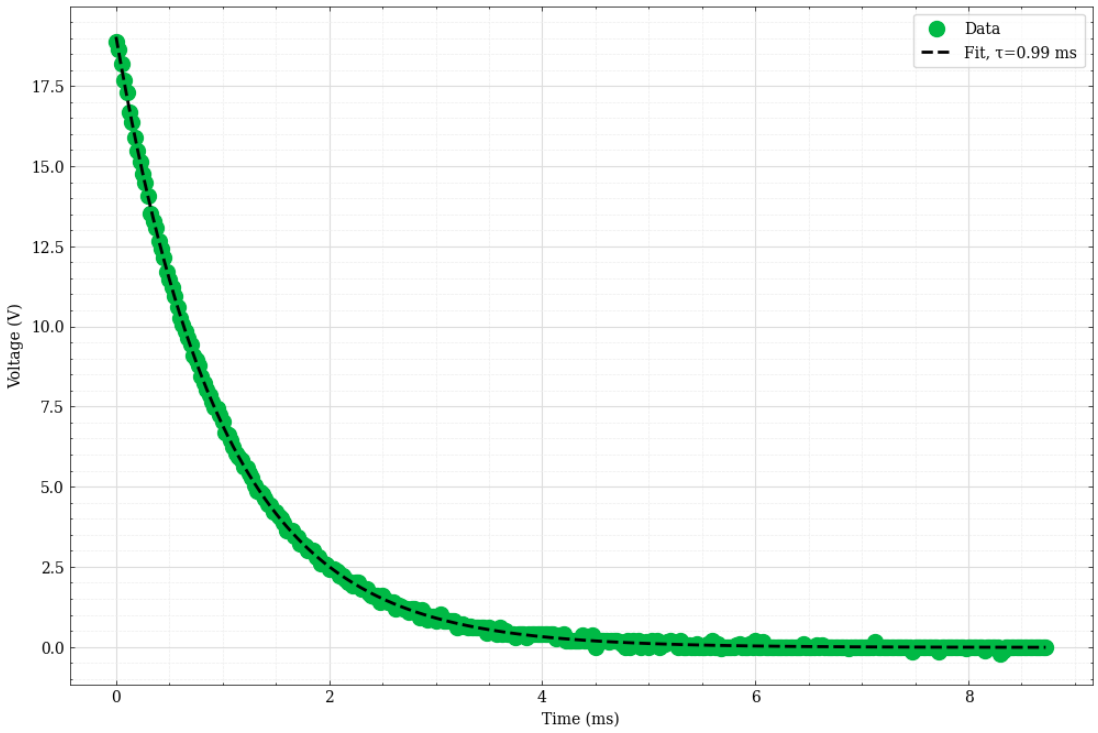
[6]:
```
'\n# Add markers to see where indices are\nfor i in range(0, len(ex5_x_osc),
100):\n    plt.text(ex5_x_osc[i]*1e3, ex5_ch2_osc[i], str(i), fontsize=8)\n'
```

[7]:
```
fig, ax = plt.subplots()

ax.plot(ex5_x_osc * 1e3, ex5_ch1_osc, label='Channel 1')
plt.xlim([-20,20])

ax.plot(ex5_x_osc * 1e3, ex5_ch2_osc, label='Channel 2')

plt.xlabel('Time (ms)')
plt.ylabel('Voltage (V)')

ax.minorticks_on()
ax.grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
ax.grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
 ↪zorder=1)

ax.legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.show()
```



[8]:
```
t = ex5_x_osc.copy()
ch1 = ex5_ch1_osc.copy()
ch2 = ex5_ch2_osc.copy()
```

[9]:
```
def exp_model(t, Vinf, A, tau):
    return Vinf - A*np.exp(-t/tau) # Want decay to Vinf, therefore negative sign

start, end = 200, 550   # adjust indices
t_fit = t[start:end] - t[start]
v_fit = ch2[start:end]

p0 = (np.mean(v_fit[-50:]), v_fit[0] - np.mean(v_fit[-50:]), 0.01)
popt, pcov = curve_fit(exp_model, t_fit, v_fit, p0=p0)
Vinf, A, tau = popt

plt.plot(t_fit * 1e3, v_fit, 'o', label='Data', color='#00B945', markersize=10)
plt.plot(t_fit * 1e3, exp_model(t_fit, *popt), '--', label=f'Fit,  ={tau * 1e3:.
 ↪2f} ms', color='black', linewidth=2)

plt.xlabel('Time (ms)')
plt.ylabel('Voltage (V)')

plt.minorticks_on()
plt.grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
plt.grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
 ↪zorder=1)

plt.legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.show()

print(f"Decay constant   = {tau:.4e}s  ({tau*1e3:.2f} ms)")
```




```
Decay constant   = 9.8894e-04s  (0.99 ms)
```

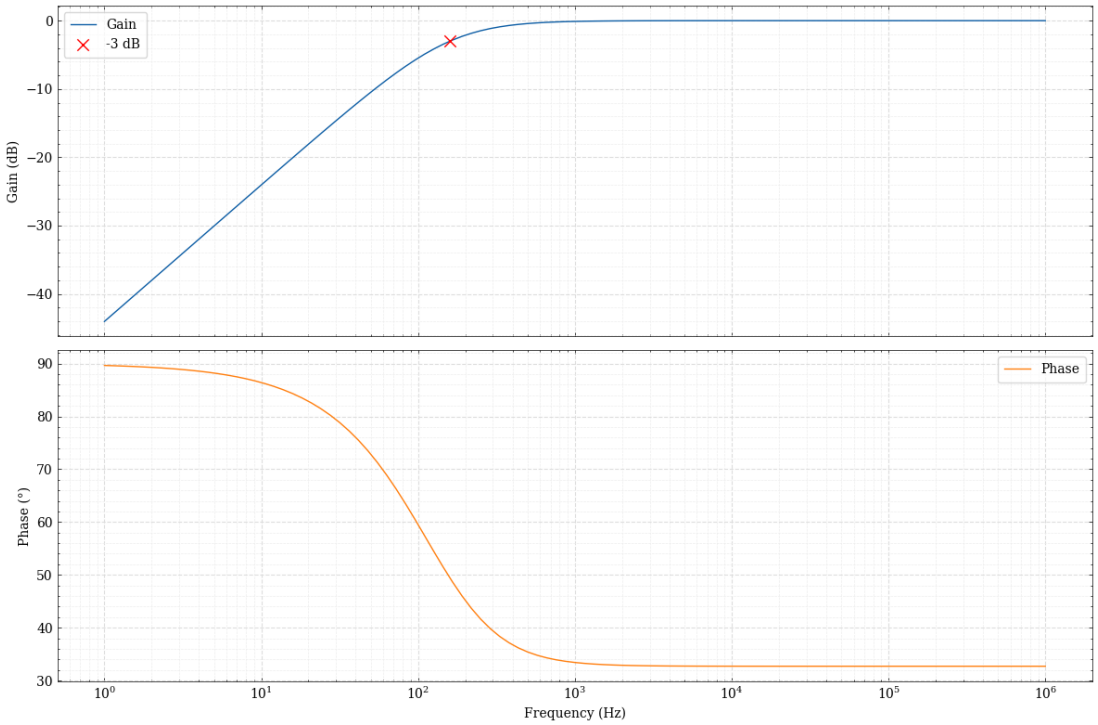
2 Ex 7

[10]:
```
ex7 = np.loadtxt("/Users/JoanaUCD/Library/CloudStorage/
↪OneDrive-UniversityCollegeDublin/Labs/labs-files/labs_code/Labs-Code/
↪labcode_s3/ex7.txt", skiprows=1)

ex7_freq = ex7[:,0]
ex7_gain = ex7[:,1]
ex7_phase = ex7[:,1]

ex7_gain = 20 * np.log10(ex7_gain)
ex7_phase = 90 - np.degrees(ex7_phase)
```

[11]:
```
def find_cutoff(f, mag, target):
    # Convert to numpy
    f = np.array(f)
    mag = np.array(mag)

    # Find indices where the curve crosses target
    idx = np.where(np.diff(np.sign(mag - target)))[0]
```

```
    if len(idx) == 0:
        return None  # No crossing found

    i = idx[0]
    # Linear interpolation between the two points around the crossing
    f1, f2 = f[i], f[i+1]
    m1, m2 = mag[i], mag[i+1]

    return f1 + (target - m1) * (f2 - f1) / (m2 - m1)

cutoff = find_cutoff(ex7_freq, ex7_gain, -3)
print("Cutoff frequency  ", cutoff, "Hz")

fig, ax = plt.subplots(2, 1, sharex=True)

ax[0].semilogx(ex7_freq, ex7_gain, label='Gain')
ax[0].scatter(cutoff, -3, color='red', s=80, marker='x', zorder=4, label='-3␣
 ↪dB')
ax[0].set_ylabel('Gain (dB)')
ax[0].grid(which='both', linestyle='--', linewidth=0.5)

ax[0].minorticks_on()
ax[0].grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
ax[0].grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
 ↪zorder=1)
ax[0].legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

ax[1].semilogx(ex7_freq, ex7_phase, label='Phase', color='tab:orange')
ax[1].set_xlabel('Frequency (Hz)')
ax[1].set_ylabel('Phase (°)')
ax[1].grid(which='both', linestyle='--', linewidth=0.5)

ax[1].minorticks_on()
ax[1].grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
ax[1].grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
 ↪zorder=1)
ax[1].legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.tight_layout()

plt.show()
```

```
Cutoff frequency   160.13176634130096 Hz
```

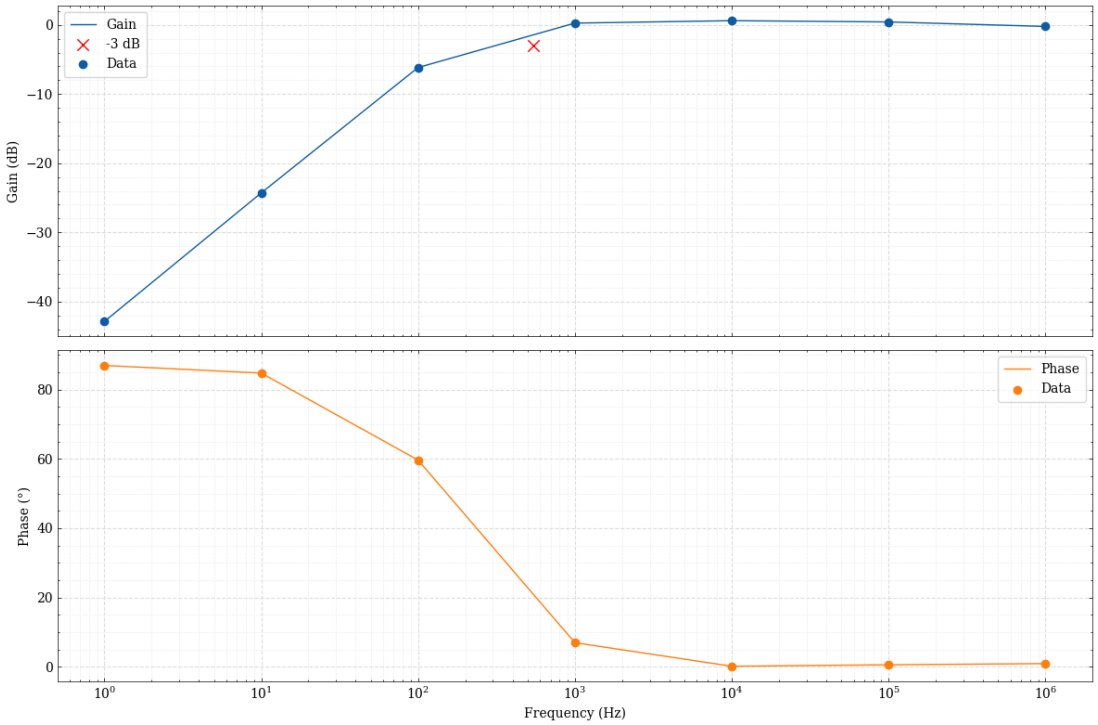


[12]:
```
ex7_f = np.array([1, 10, 100, 1000, 10000, 100000, 1000000])
ex7_Vin = np.array([8.52, 1.01, 1.02, 970e-3, 950e-3, 970e-3, 930e-3])
ex7_Vout = np.array([61.1e-3, 61.6e-3, 502e-3, 1, 1.02, 1.02, 907e-3])
ex7_Phase = np.array([87, 84.8, 59.68, 6.95, 0.14, 0.56, 0.9])

ex7_PPhase = 90 - ex7_Phase

ex7_Gain = 20 * np.log10(ex7_Vout / ex7_Vin)
```

[13]:
```
def find_cutoff(f, mag, target):
    # Convert to numpy
    f = np.array(f)
    mag = np.array(mag)

    # Find indices where the curve crosses target
    idx = np.where(np.diff(np.sign(mag - target)))[0]

    if len(idx) == 0:
        return None  # No crossing found

    i = idx[0]
    # Linear interpolation between the two points around the crossing
    f1, f2 = f[i], f[i+1]
```

```
    m1, m2 = mag[i], mag[i+1]

    return f1 + (target - m1) * (f2 - f1) / (m2 - m1)

cutoff = find_cutoff(ex7_f, ex7_Gain, -3)
print("Cutoff frequency  ", cutoff, "Hz")

fig, ax = plt.subplots(2, 1, sharex=True)

ax[0].semilogx(ex7_f, ex7_Gain, label='Gain')
ax[0].scatter(cutoff, -3, color='red', s=80, marker='x', zorder=4, label='-3␣
 ↪dB')
ax[0].scatter(ex7_f, ex7_Gain, zorder=3, label='Data')
ax[0].set_ylabel('Gain (dB)')
ax[0].grid(which='both', linestyle='--', linewidth=0.5)

ax[0].minorticks_on()
ax[0].grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
ax[0].grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
 ↪zorder=1)
ax[0].legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

ax[1].semilogx(ex7_f, ex7_Phase, label='Phase', color='tab:orange')
ax[1].scatter(ex7_f, ex7_Phase, label='Data', color='tab:orange', zorder=3)
ax[1].set_xlabel('Frequency (Hz)')
ax[1].set_ylabel('Phase (°)')
ax[1].grid(which='both', linestyle='--', linewidth=0.5)

ax[1].minorticks_on()
ax[1].grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
ax[1].grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
 ↪zorder=1)
ax[1].legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.tight_layout()

plt.show()
```

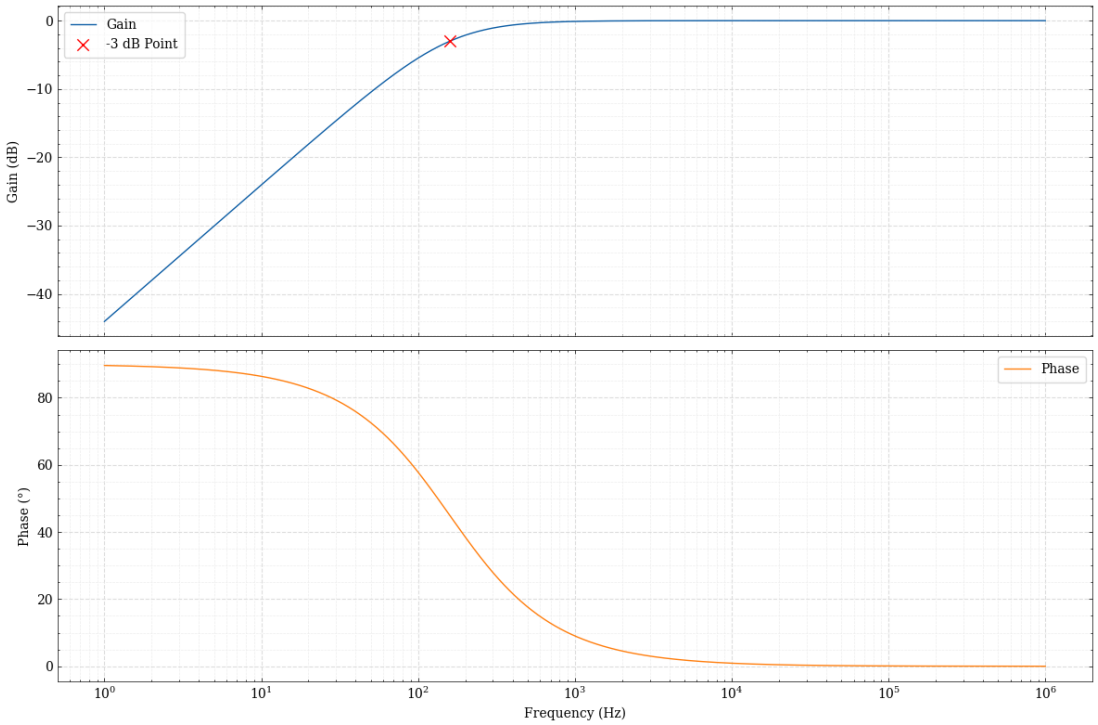
```
Cutoff frequency   542.5284014261945 Hz
```



[14]:
```
V0 = 1
C = 1e-6
R = 1e3

f = np.logspace(0, 6, 1000) # 1 Hz to 1 MHz log-scale, 1000 points between
omega = 2 * np.pi * f

H = 1j * omega * R * C / (1 + 1j * omega * R * C)

mag = np.abs(H)
mag = 20 * np.log10(mag)
phase = np.angle(H, deg=True)

def find_cutoff(f, mag, target):
    # Convert to numpy
    f = np.array(f)
    mag = np.array(mag)

    # Find indices where the curve crosses target
    idx = np.where(np.diff(np.sign(mag - target)))[0]

    if len(idx) == 0:
        return None  # No crossing found
```

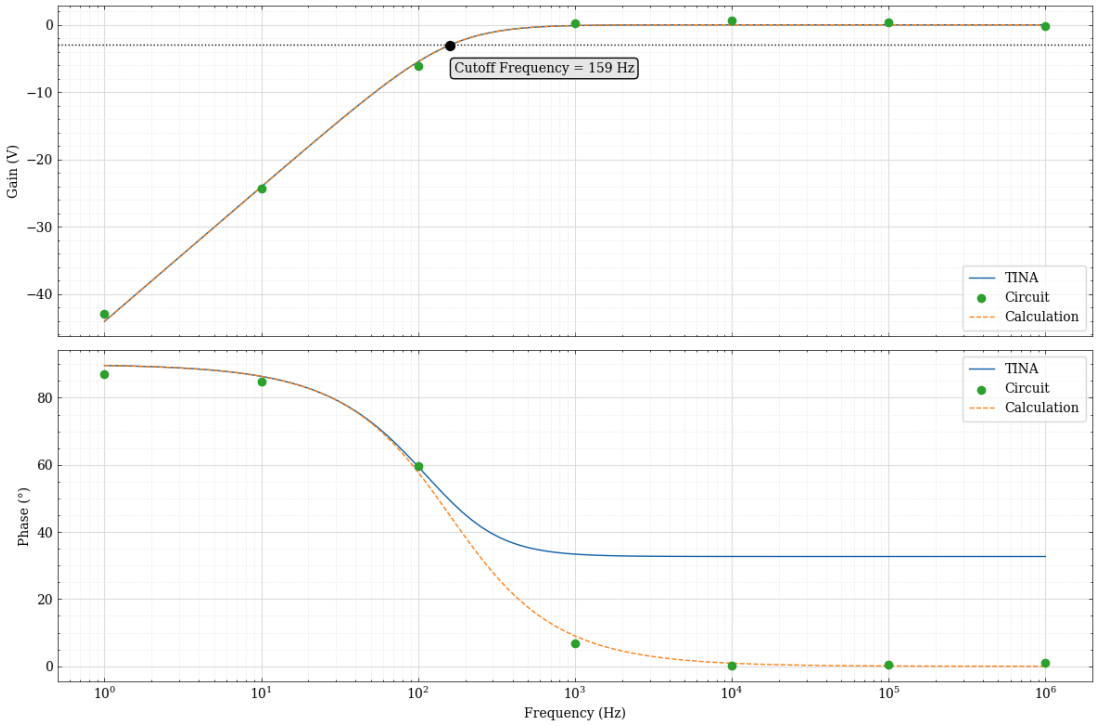
```
    i = idx[0]
    # Linear interpolation between the two points around the crossing
    f1, f2 = f[i], f[i+1]
    m1, m2 = mag[i], mag[i+1]

    return f1 + (target - m1) * (f2 - f1) / (m2 - m1)

cutoff = find_cutoff(f, mag, -3)
print("Cutoff frequency  ", cutoff, "Hz")

fig, ax = plt.subplots(2, 1, sharex=True)

ax[0].semilogx(f, mag, label='Gain')
ax[0].scatter(cutoff, -3, color='red', s=80, marker='x', zorder=4, label='-3 dB␣
 ↪Point')
ax[0].set_ylabel('Gain (dB)')
ax[0].grid(which='both', linestyle='--', linewidth=0.5)

ax[0].minorticks_on()
ax[0].grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
ax[0].grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
 ↪zorder=1)
ax[0].legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

ax[1].semilogx(f, phase, label='Phase', color='tab:orange')
ax[1].set_xlabel('Frequency (Hz)')
ax[1].set_ylabel('Phase (°)')
ax[1].grid(which='both', linestyle='--', linewidth=0.5)

ax[1].minorticks_on()
ax[1].grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
ax[1].grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
 ↪zorder=1)
ax[1].legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.tight_layout()

plt.show()
```

```
Cutoff frequency   159.53860495032134 Hz
```



[15]:
```
gain_3db = np.interp(159, f, mag)

fig, ax = plt.subplots(2, 1, sharex=True)

ax[0].semilogx(ex7_freq, ex7_gain, label='TINA')
ax[0].scatter(ex7_f, ex7_Gain, label='Circuit', color='tab:green', marker='o',␣
 ↪zorder=3)
ax[0].scatter(159, gain_3db, color='black', s=50, zorder=4)
ax[0].annotate('Cutoff Frequency = 159 Hz', xy=(159, gain_3db), xytext=(170,␣
 ↪gain_3db-4), bbox=dict(fc='0.9', boxstyle='round'))
ax[0].axhline(y=-3, linestyle=':', color='black')
ax[0].semilogx(f, mag, label='Calculation', color='tab:orange', linestyle='--')

ax[0].set_ylabel('Gain (V)')
ax[0].minorticks_on()
ax[0].grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
ax[0].grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
 ↪zorder=1)
ax[0].legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)


ax[1].semilogx(ex7_freq, ex7_phase, label='TINA')
```

```
ax[1].scatter(ex7_f, ex7_Phase, label='Circuit', color='tab:green', marker='o',␣
 ↪zorder=3)
ax[1].semilogx(f, phase, label='Calculation', color='tab:orange',␣
 ↪linestyle='--')

ax[1].set_xlabel('Frequency (Hz)')
ax[1].set_ylabel('Phase (°)')
ax[1].minorticks_on()
ax[1].grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
ax[1].grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
 ↪zorder=1)
ax[1].legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.tight_layout()

plt.show()
```



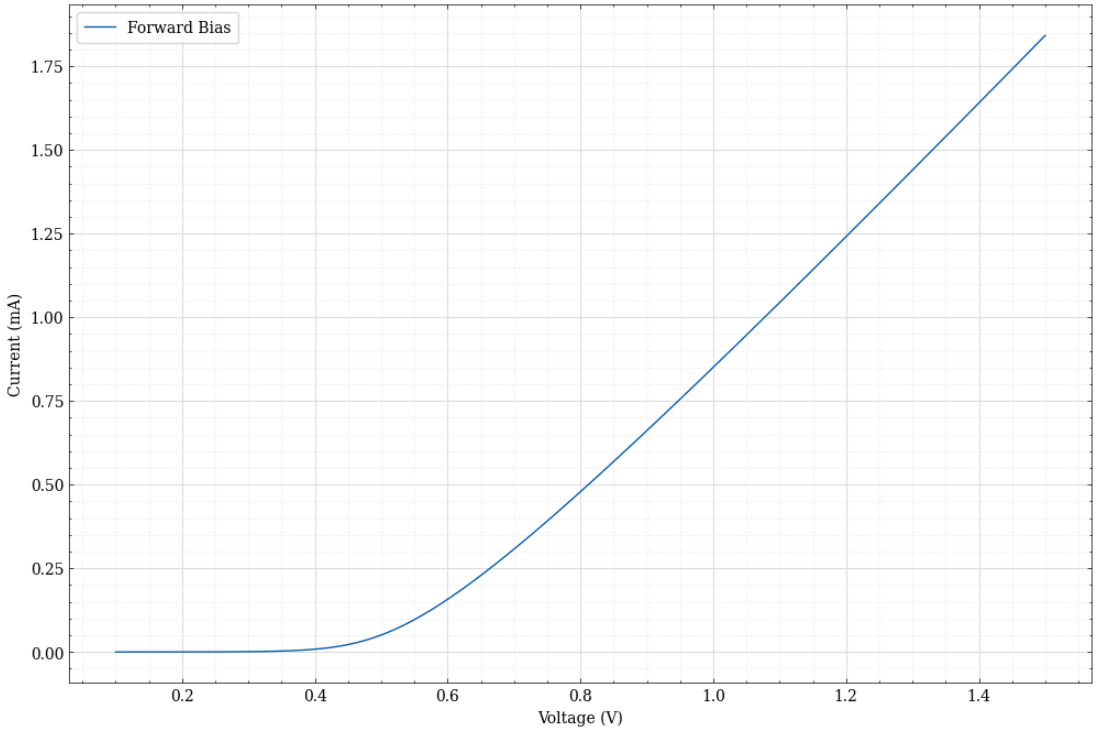
3 Ex 12

3.1 a.

3.1.1 Theory

[16]:
```
ex12a = np.loadtxt("/Users/JoanaUCD/Library/CloudStorage/
↪OneDrive-UniversityCollegeDublin/Labs/labs-files/labs_code/Labs-Code/
↪labcode_s3/ex12a.txt", skiprows=1)

V_for = ex12a[:,0]
I_for = ex12a[:,1]
```

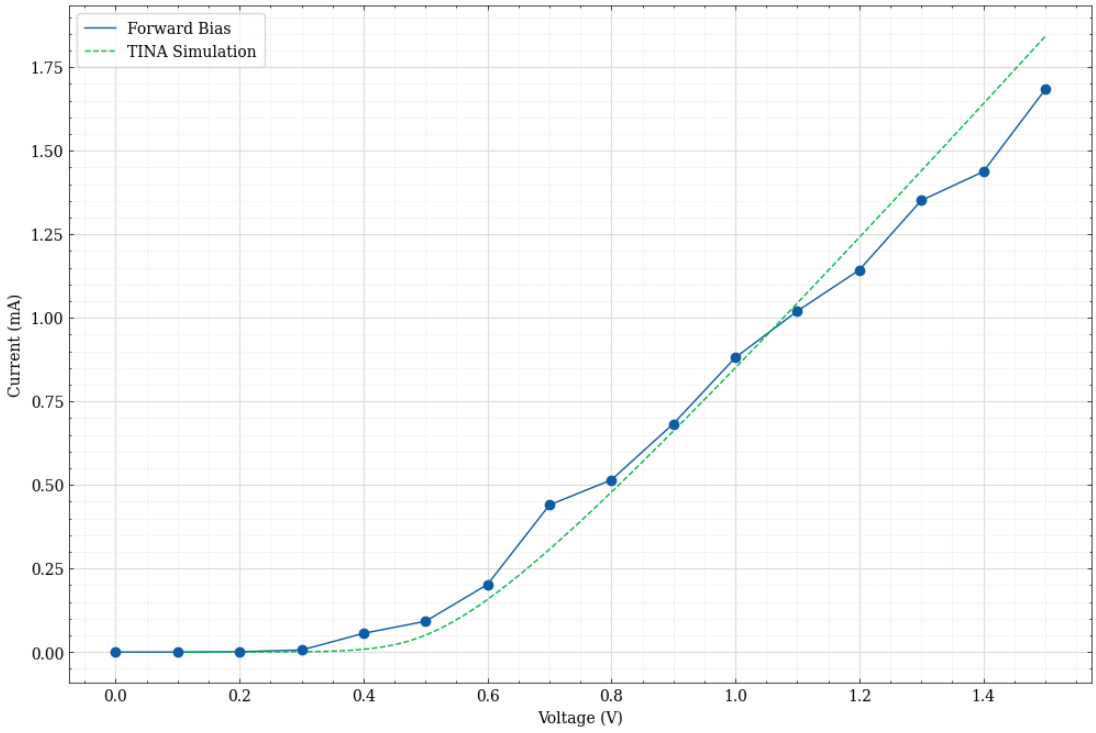
[17]:
```
plt.plot(V_for , I_for *1e3, label='Forward Bias')

plt.xlabel("Voltage (V)")
plt.ylabel("Current (mA)")

plt.minorticks_on()
plt.grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
plt.grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
↪zorder=1)

plt.legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.show()
```



3.1.2 Ammeter

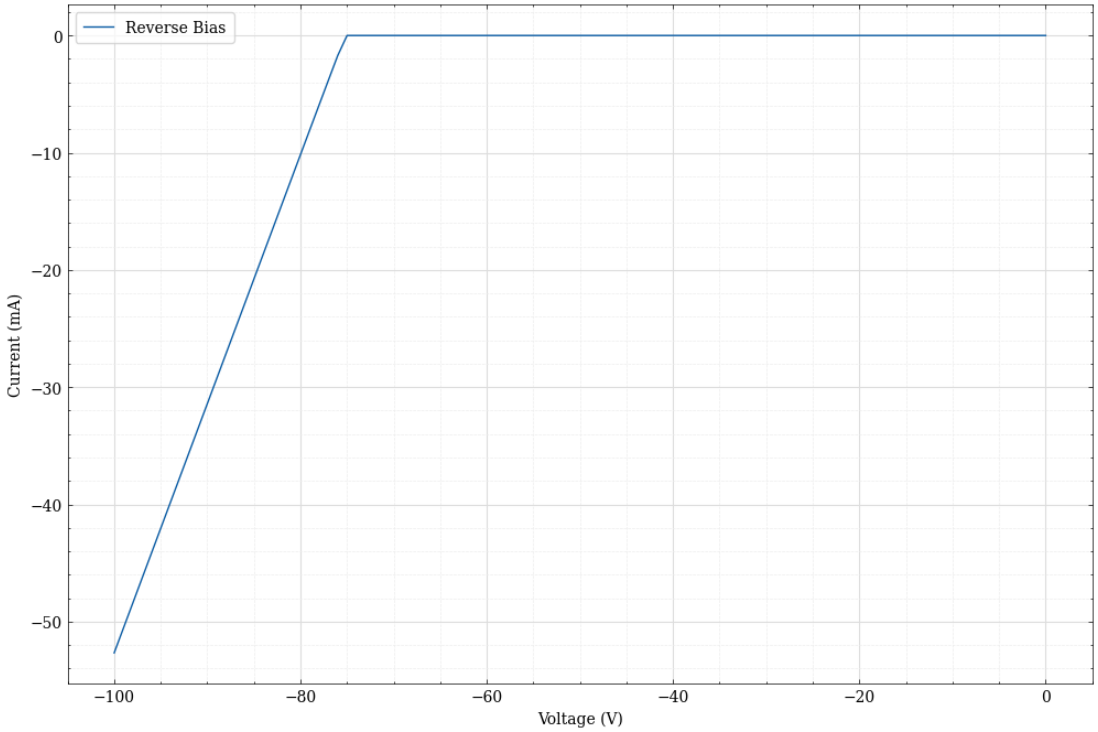
[18]:
```
ex12_for_am_V = np.array([0,0.1,0.2,0.3,0.4,0.5,0.6,0.7,0.8,0.9,1.0,1.1,1.2,1.
↪3,1.4,1.5])
ex12_for_am_I = np.array([0,0,0.001,0.006,0.056,0.092,0.202,0.440,0.515,0.683,0.
↪881,1.020,1.143,1.351,1.437,1.683])
```

[19]:
```
plt.plot(ex12_for_am_V, ex12_for_am_I, label='Forward Bias')
plt.scatter(ex12_for_am_V, ex12_for_am_I, color='#0C5DA5', zorder=3)

plt.plot(V_for , I_for *1e3, label='TINA Simulation', linestyle='--')

plt.xlabel("Voltage (V)")
plt.ylabel("Current (mA)")

plt.minorticks_on()
plt.grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
plt.grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
↪zorder=1)

plt.legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.show()
```



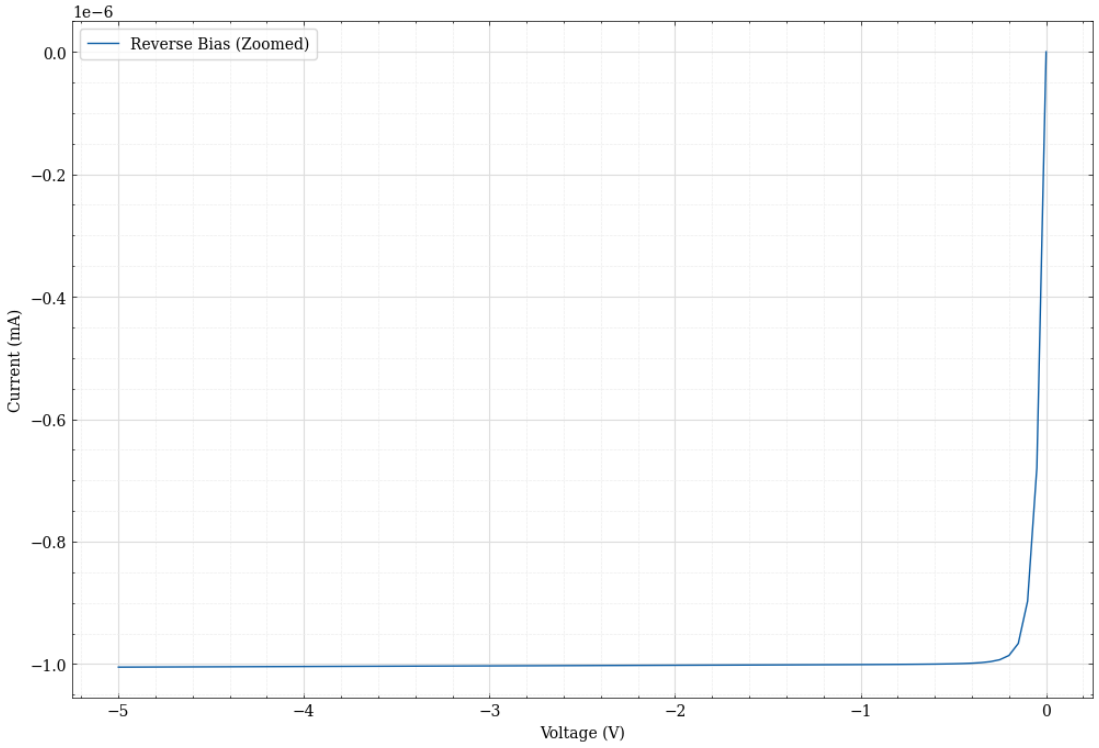
[20]:
```
ex12a_rev = np.loadtxt("/Users/JoanaUCD/Library/CloudStorage/
↪OneDrive-UniversityCollegeDublin/Labs/labs-files/labs_code/Labs-Code/
↪labcode_s3/ex12a_rev.txt", skiprows=1)

V_rev = ex12a_rev[:,1]
I_rev = ex12a_rev[:,2]
```

[21]:
```
plt.plot(V_rev , I_rev * 1e3, label='Reverse Bias')

plt.xlabel("Voltage (V)")
plt.ylabel("Current (mA)")

plt.minorticks_on()
plt.grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
plt.grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
↪zorder=1)

plt.legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.show()
```



[22]:
```
ex12a_rev_zoom = np.loadtxt('/Users/JoanaUCD/Library/CloudStorage/
 ↪OneDrive-UniversityCollegeDublin/Labs/labs-files/labs_code/Labs-Code/
 ↪labcode_s3/ex12a_rev_zoom.txt', skiprows=1)

V_rev_zoom = ex12a_rev_zoom[:,1]
I_rev_zoom = ex12a_rev_zoom[:,2]
```

[23]:
```
plt.plot(V_rev_zoom , I_rev_zoom * 1e3, label='Reverse Bias (Zoomed)')

plt.xlabel("Voltage (V)")
plt.ylabel("Current (mA)")

plt.minorticks_on()
plt.grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
plt.grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
 ↪zorder=1)

plt.legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.show()
```

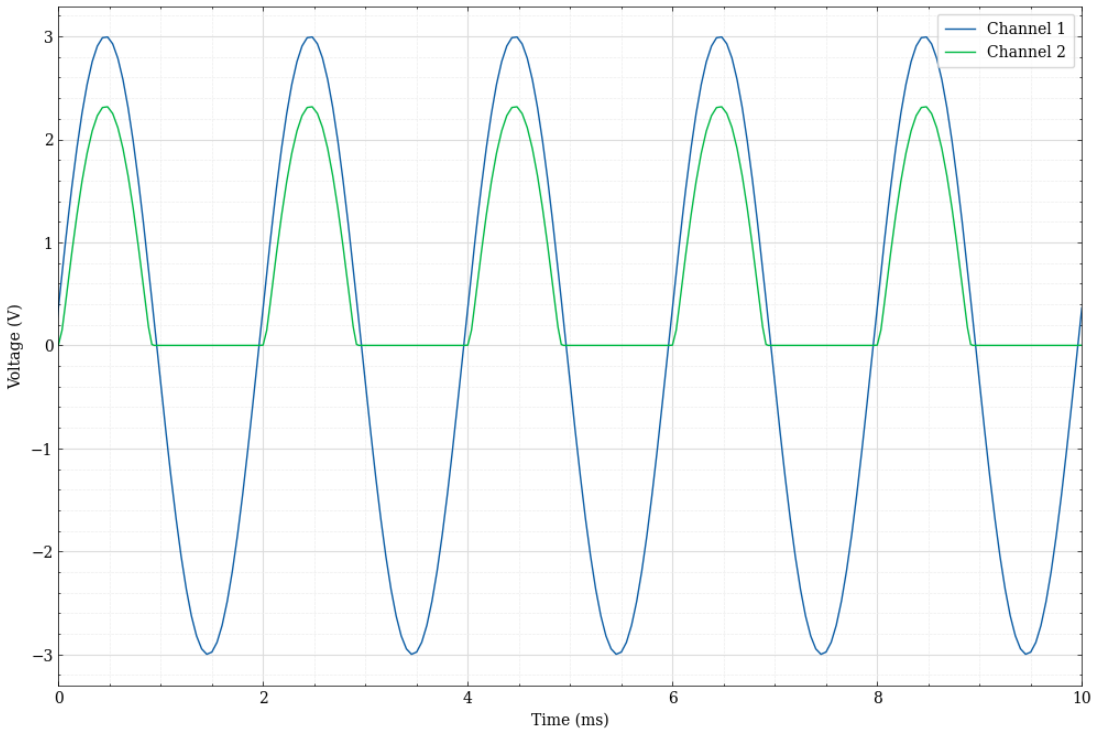


3.2 b.

3.2.1 Theory

[24]:
```
ex12b_nocap = np.loadtxt('/Users/JoanaUCD/Library/CloudStorage/
 ↪OneDrive-UniversityCollegeDublin/Labs/labs-files/labs_code/Labs-Code/
 ↪labcode_s3/exp12b.txt', skiprows=1)

ex12b_nocap_time = ex12b_nocap[:,0]
ex12b_nocap_ch1 = ex12b_nocap[:,1]
ex12b_nocap_ch2 = ex12b_nocap[:,2]
```

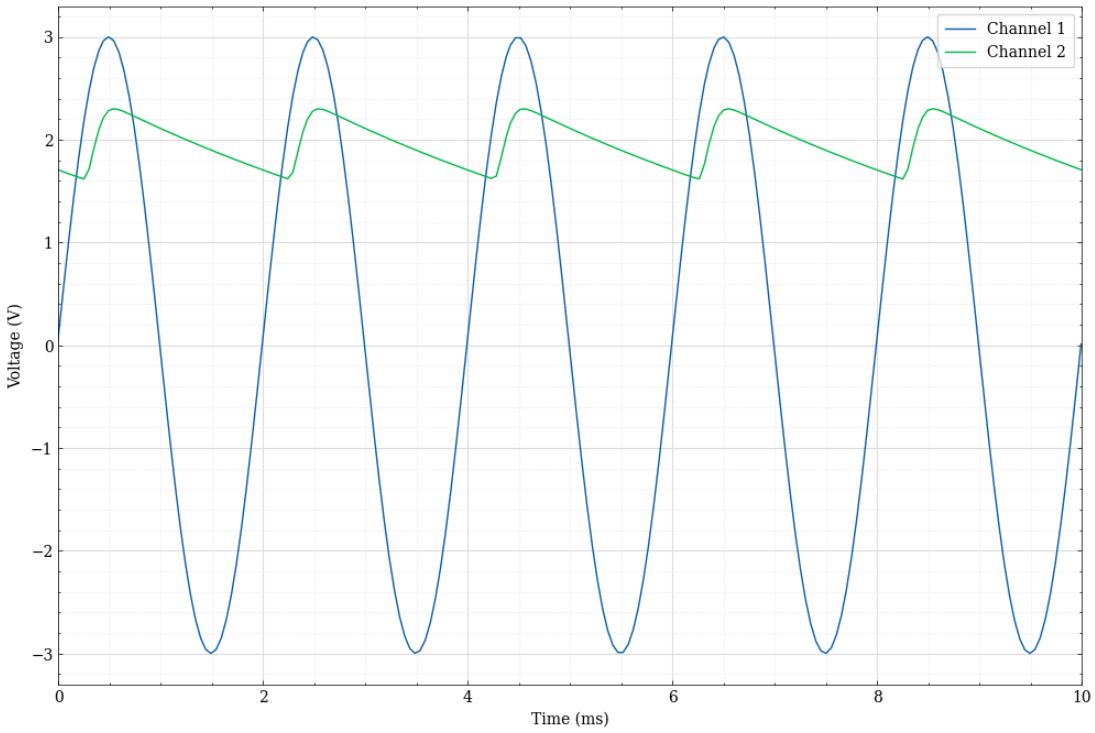
[25]:
```
fig, ax = plt.subplots()

ax.plot(ex12b_nocap_time * 1e3, ex12b_nocap_ch1, label='Channel 1')
plt.xlim([0,10])

ax.plot(ex12b_nocap_time * 1e3, ex12b_nocap_ch2, label='Channel 2')

plt.xlabel('Time (ms)')
plt.ylabel('Voltage (V)')

ax.minorticks_on()
ax.grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
ax.grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
 ↪zorder=1)

ax.legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.show()
```



[26]:
```
ex12b_cap = np.loadtxt('/Users/JoanaUCD/Library/CloudStorage/
↪OneDrive-UniversityCollegeDublin/Labs/labs-files/labs_code/Labs-Code/
↪labcode_s3/exp12b_cap.txt', skiprows=1)

ex12b_cap_time = ex12b_cap[:,0]
ex12b_cap_ch1 = ex12b_cap[:,1]
ex12b_cap_ch2 = ex12b_cap[:,2]
```

[57]:
```
fig, ax = plt.subplots()

ax.plot(ex12b_cap_time * 1e3, ex12b_cap_ch1, label='Channel 1')
plt.xlim([0,10])

ax.plot(ex12b_cap_time * 1e3, ex12b_cap_ch2, label='Channel 2')

plt.xlabel('Time (ms)')
plt.ylabel('Voltage (V)')

ax.minorticks_on()
ax.grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
ax.grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
↪zorder=1)
```

```
ax.legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.show()
```

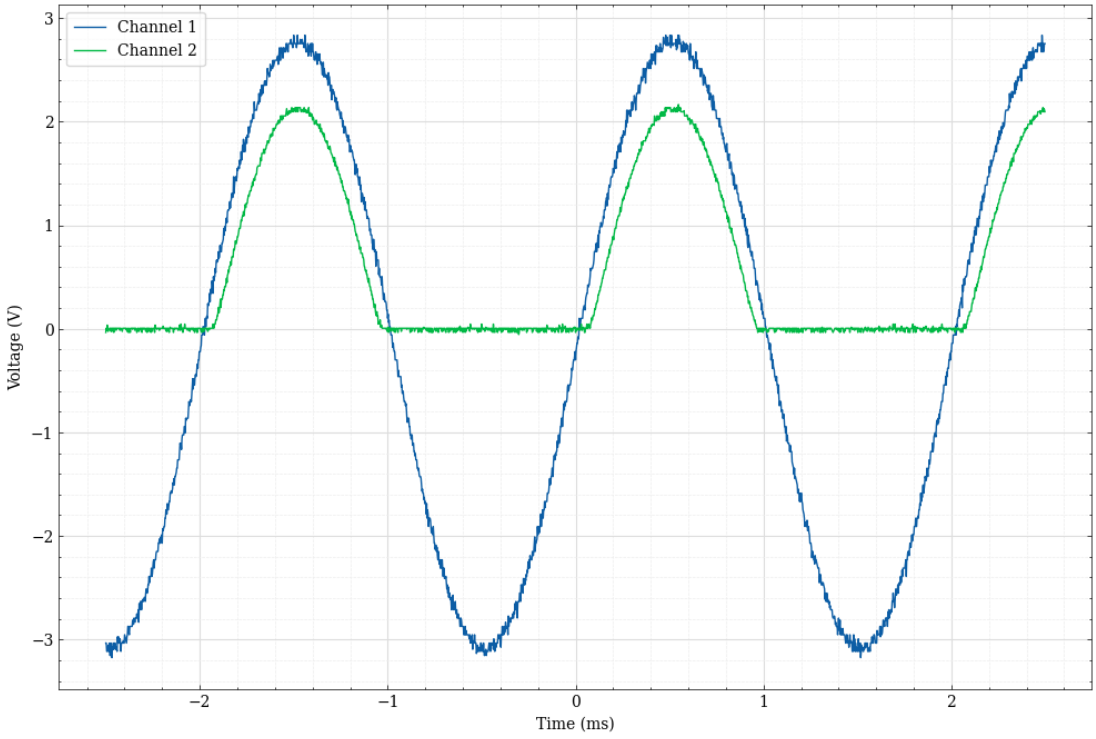


3.2.2 Oscilloscope

[28]:
```
ex12b_nocap_osc = np.loadtxt('/Users/JoanaUCD/Library/CloudStorage/
↪OneDrive-UniversityCollegeDublin/Labs/labs-files/labs_code/Labs-Code/
↪labcode_s3/osc_ex12b.txt', skiprows=1)

ex12b_nocap_time_osc = ex12b_nocap_osc[:,0]
ex12b_nocap_ch1_osc = ex12b_nocap_osc[:,1]
ex12b_nocap_ch2_osc = ex12b_nocap_osc[:,2]
```

[50]:
```
fig, ax = plt.subplots()

ax.plot(ex12b_nocap_time_osc * 1e3, ex12b_nocap_ch1_osc, label='Channel 1')

ax.plot(ex12b_nocap_time_osc * 1e3, ex12b_nocap_ch2_osc, label='Channel 2')

plt.xlabel('Time (ms)')
plt.ylabel('Voltage (V)')
```

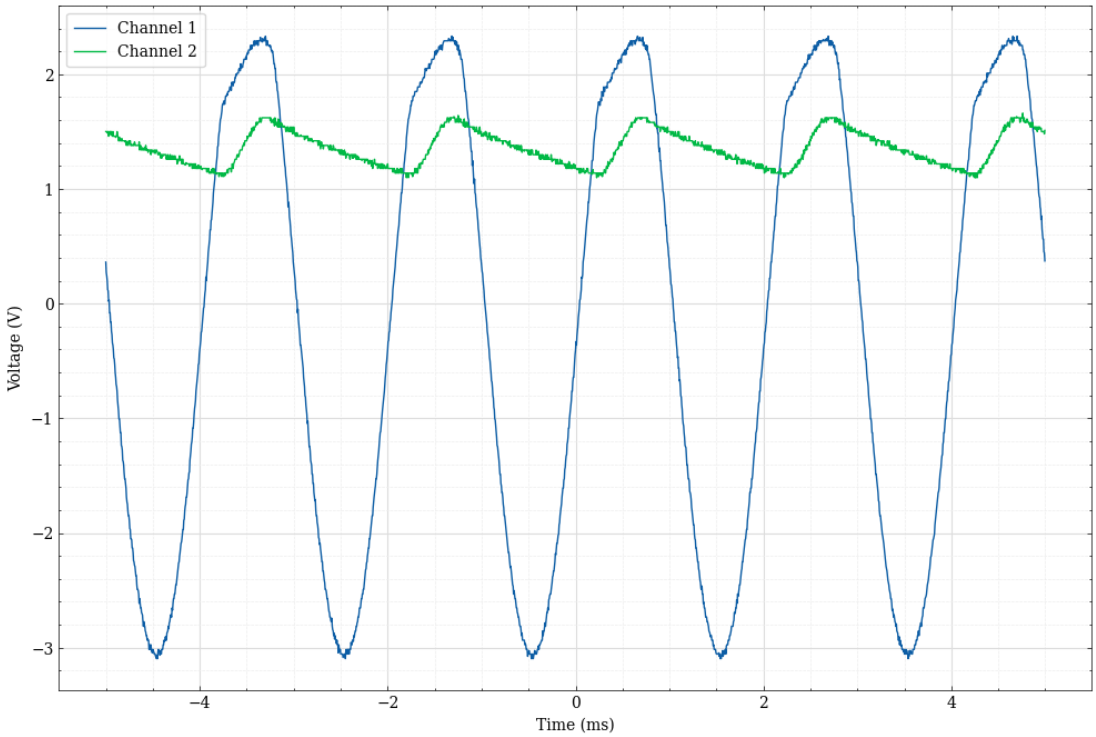
```
ax.minorticks_on()
ax.grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
ax.grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
 ↪zorder=1)

ax.legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.show()
```



[59]:
```
ex12b_cap_osc = np.loadtxt('/Users/JoanaUCD/Library/CloudStorage/
 ↪OneDrive-UniversityCollegeDublin/Labs/labs-files/labs_code/Labs-Code/
 ↪labcode_s3/osc_ex12b_cap.txt', skiprows=1)

ex12b_cap_time_osc = ex12b_cap_osc[:,0]
ex12b_cap_ch1_osc = ex12b_cap_osc[:,1]
ex12b_cap_ch2_osc = ex12b_cap_osc[:,2]
```

[58]:
```
fig, ax = plt.subplots()

ax.plot(ex12b_cap_time_osc * 1e3, ex12b_cap_ch1_osc, label='Channel 1')

ax.plot(ex12b_cap_time_osc * 1e3, ex12b_cap_ch2_osc, label='Channel 2')
```

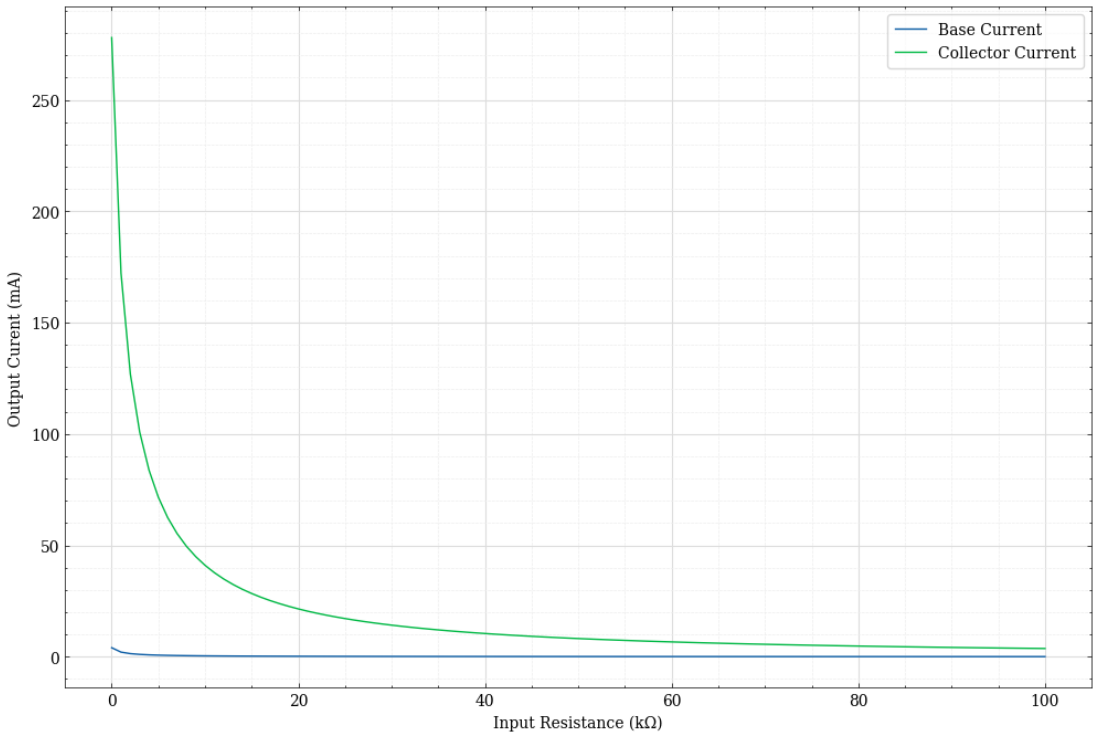
```
plt.xlabel('Time (ms)')
plt.ylabel('Voltage (V)')

ax.minorticks_on()
ax.grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
ax.grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
 ↪zorder=1)

ax.legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.show()
```



4 Ex 19

[32]:
```
ex19 = np.loadtxt('/Users/JoanaUCD/Library/CloudStorage/
 ↪OneDrive-UniversityCollegeDublin/Labs/labs-files/labs_code/Labs-Code/
 ↪labcode_s3/ex19.txt', skiprows=1)

input = ex19[:,0]
am1 = ex19[:,1]
am2 = ex19[:,2]
```

[63]:
```
fig, ax = plt.subplots()

ax.plot(input * 1e-3, am1 * 1e3, label='Base Current')

ax.plot(input * 1e-3, am2 * 1e3, label='Collector Current')

plt.xlabel('Input Resistance (kΩ)')
plt.ylabel('Output Curent (mA)')

ax.minorticks_on()
ax.grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
ax.grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
 ↪zorder=1)

ax.legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.show()

hfe = np.average(am2 / am1)
print(hfe)
```

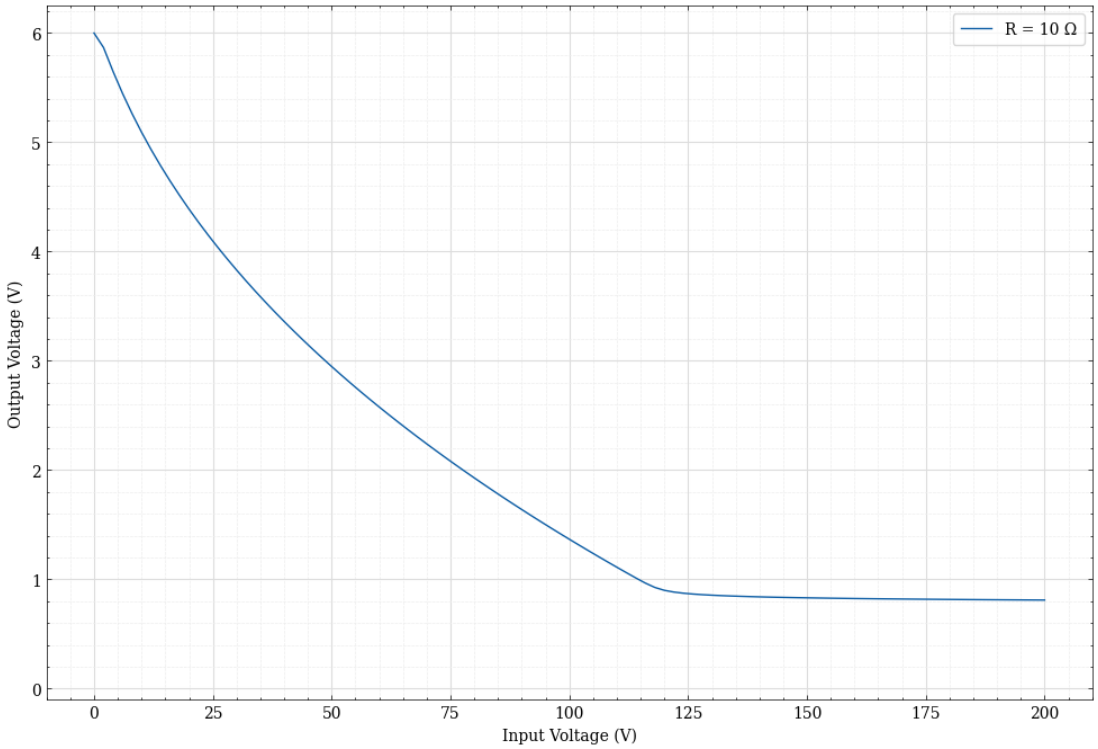



```
96.21463033275784
```

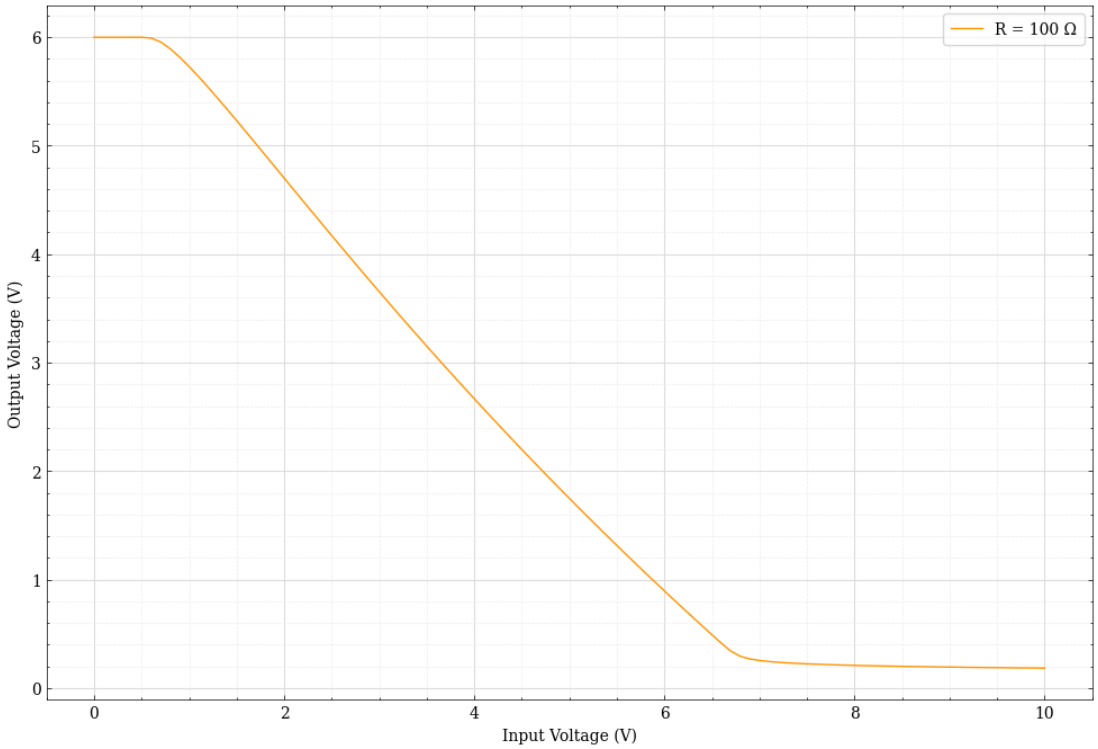
5 Ex 20

[34]:
```
ex20_r10 = np.loadtxt('/Users/JoanaUCD/Library/CloudStorage/
↪OneDrive-UniversityCollegeDublin/Labs/labs-files/labs_code/Labs-Code/
↪labcode_s3/ex20_r10.txt', skiprows=1)
ex20_r100 = np.loadtxt('/Users/JoanaUCD/Library/CloudStorage/
↪OneDrive-UniversityCollegeDublin/Labs/labs-files/labs_code/Labs-Code/
↪labcode_s3/ex20_r100.txt', skiprows=1)
ex20_r1k = np.loadtxt('/Users/JoanaUCD/Library/CloudStorage/
↪OneDrive-UniversityCollegeDublin/Labs/labs-files/labs_code/Labs-Code/
↪labcode_s3/ex20_r1000.txt', skiprows=1)
ex20_r10k = np.loadtxt('/Users/JoanaUCD/Library/CloudStorage/
↪OneDrive-UniversityCollegeDublin/Labs/labs-files/labs_code/Labs-Code/
↪labcode_s3/ex20_r10000.txt', skiprows=1)

ex20_input_r10 = ex20_r10[:,0]
ex20_output_r10 = ex20_r10[:,1]
ex20_input_r100 = ex20_r100[:,0]
ex20_output_r100 = ex20_r100[:,1]
ex20_input_r1k = ex20_r1k[:,0]
ex20_output_r1k = ex20_r1k[:,1]
ex20_input_r10k = ex20_r10k[:,0]
ex20_output_r10k = ex20_r10k[:,1]
```

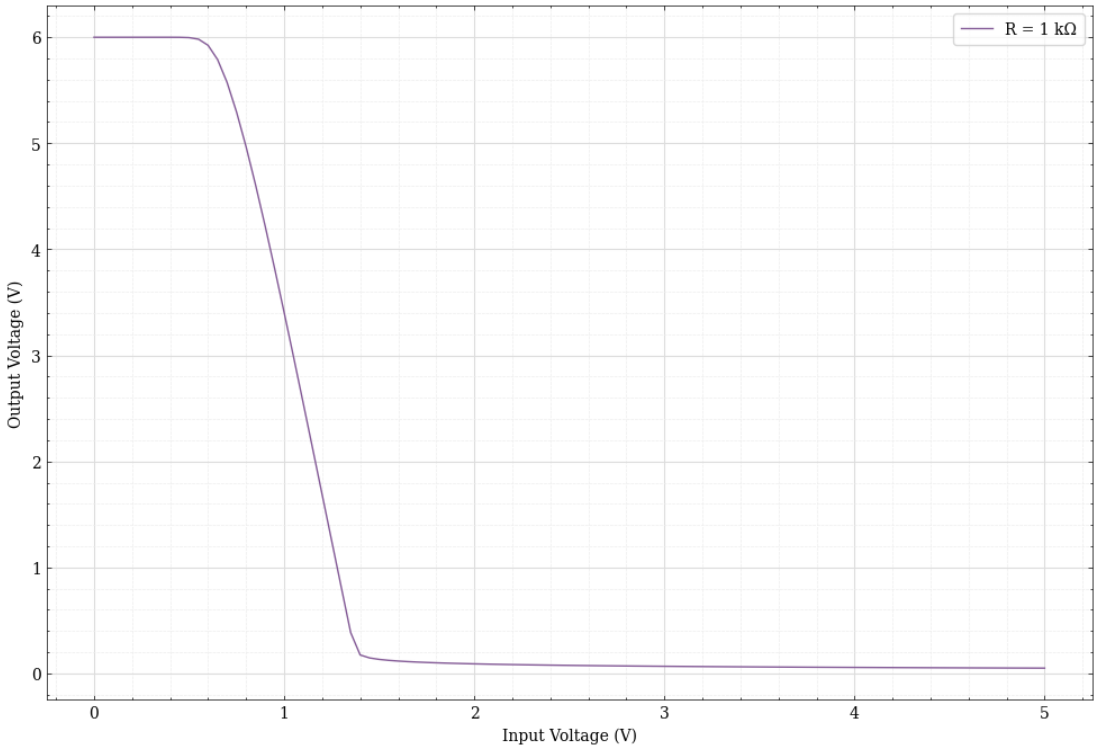
[64]:
```
plt.plot(ex20_input_r10, ex20_output_r10, label='R = 10 Ω')

plt.xlabel('Input Voltage (V)')
plt.ylabel('Output Voltage (V)')

plt.ylim([-0.1,6.25])

plt.minorticks_on()
plt.grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
plt.grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
↪zorder=1)

plt.legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.show()
```



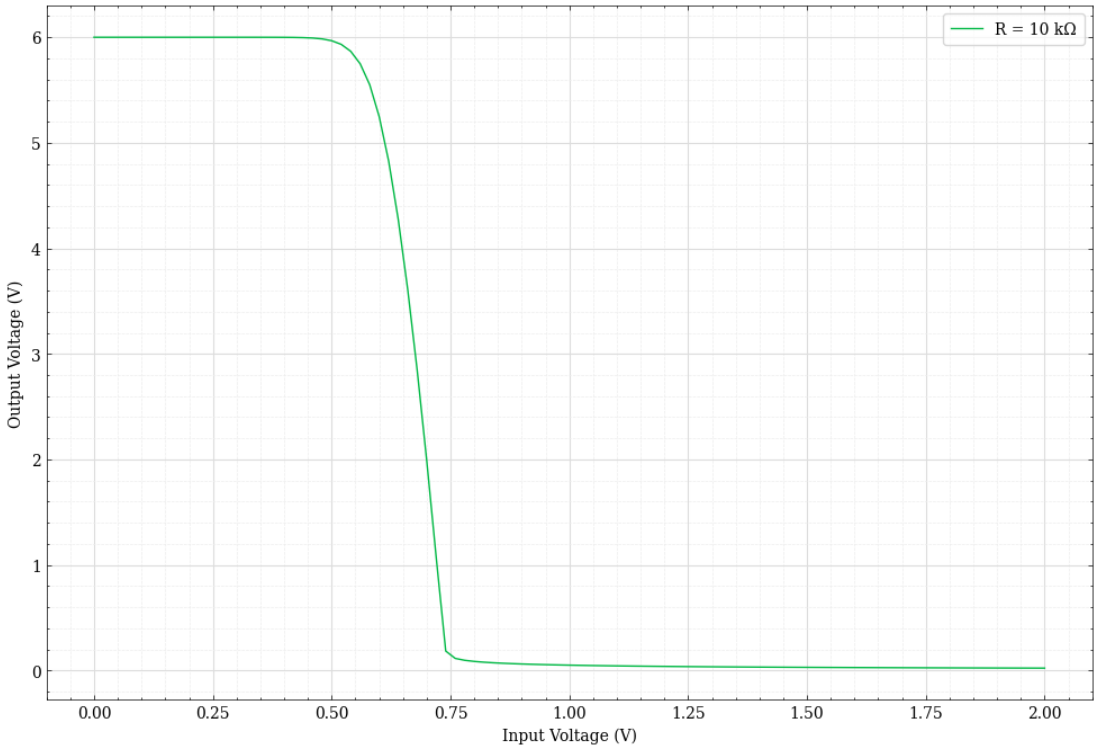
[66]:
```
plt.plot(ex20_input_r100, ex20_output_r100, color='#FF9500', label='R = 100 Ω')

plt.xlabel('Input Voltage (V)')
plt.ylabel('Output Voltage (V)')

plt.minorticks_on()
plt.grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
plt.grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
↪zorder=1)

plt.legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.show()
```



[67]:
```
plt.plot(ex20_input_r1k, ex20_output_r1k, color='#845B97', label='R = 1 kΩ')

plt.xlabel('Input Voltage (V)')
plt.ylabel('Output Voltage (V)')

plt.minorticks_on()
plt.grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
plt.grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
 ↪zorder=1)

plt.legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.show()
```



[68]:
```
plt.plot(ex20_input_r10k, ex20_output_r10k, color='#00B945', label='R = 10 kΩ')

plt.xlabel('Input Voltage (V)')
plt.ylabel('Output Voltage (V)')

plt.minorticks_on()
plt.grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
plt.grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
↪zorder=1)

plt.legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.show()
```

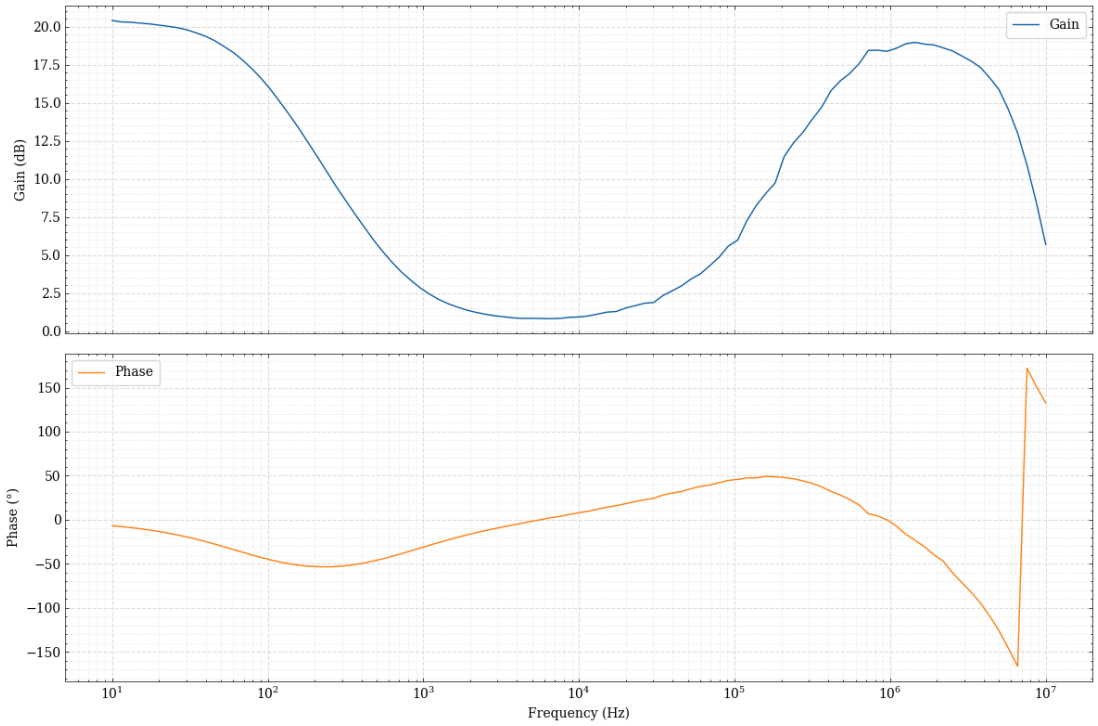


6 Ex 25

[39]:
```
ex25_cap = np.loadtxt('/Users/JoanaUCD/Library/CloudStorage/
↪OneDrive-UniversityCollegeDublin/Labs/labs-files/labs_code/Labs-Code/
↪labcode_s3/ex25_cap.txt', skiprows=1)

ex25_cap_f = ex25_cap[:,0]
ex25_cap_amp = ex25_cap[:,1]
ex25_cap_gain = ex25_cap[:,2]
ex25_cap_phase = ex25_cap[:,3]
```

[40]:
```
fig, ax = plt.subplots(2, 1, sharex=True)

ax[0].semilogx(ex25_cap_f, ex25_cap_gain, label='Gain')
ax[0].set_ylabel('Gain (dB)')
ax[0].grid(which='both', linestyle='--', linewidth=0.5)

ax[0].minorticks_on()
ax[0].grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
ax[0].grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
↪zorder=1)
ax[0].legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)
```

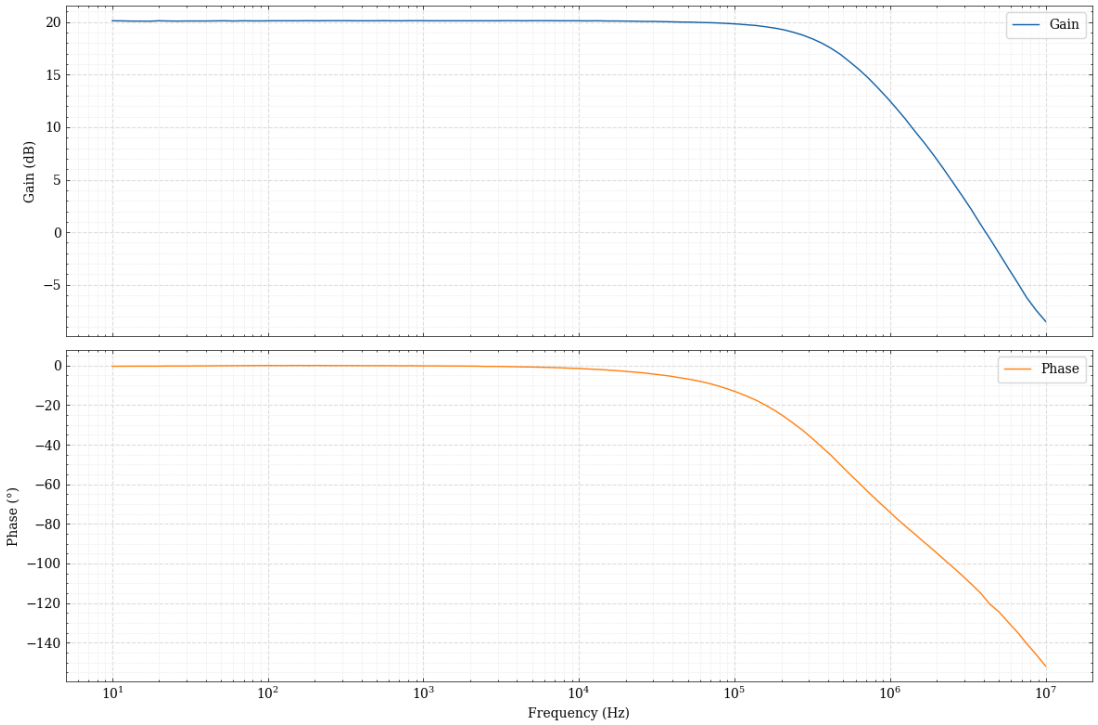
```
ax[1].semilogx(ex25_cap_f, ex25_cap_phase, label='Phase', color='tab:orange')
ax[1].set_xlabel('Frequency (Hz)')
ax[1].set_ylabel('Phase (°)')
ax[1].grid(which='both', linestyle='--', linewidth=0.5)

ax[1].minorticks_on()
ax[1].grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
ax[1].grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
 ↪zorder=1)
ax[1].legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.tight_layout()

plt.show()
```



[42]:
```
ex25_nocap =np.loadtxt('/Users/JoanaUCD/Library/CloudStorage/
 ↪OneDrive-UniversityCollegeDublin/Labs/labs-files/labs_code/Labs-Code/
 ↪labcode_s3/ex25_nocap.txt', skiprows=1)

ex25_nocap_f = ex25_nocap[:,0]
ex25_nocap_amp = ex25_nocap[:,1]
ex25_nocap_gain = ex25_nocap[:,2]
```

```
ex25_nocap_phase = ex25_nocap[:,3]
```

[43]:
```
fig, ax = plt.subplots(2, 1, sharex=True)

ax[0].semilogx(ex25_nocap_f, ex25_nocap_gain, label='Gain')
ax[0].set_ylabel('Gain (dB)')
ax[0].grid(which='both', linestyle='--', linewidth=0.5)

ax[0].minorticks_on()
ax[0].grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
ax[0].grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
 ↪zorder=1)
ax[0].legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

ax[1].plot(ex25_nocap_f, ex25_nocap_phase, label='Phase', color='tab:orange')
ax[1].set_xlabel('Frequency (Hz)')
ax[1].set_ylabel('Phase (°)')
ax[1].grid(which='both', linestyle='--', linewidth=0.5)

ax[1].minorticks_on()
ax[1].grid(True, which="major", linewidth=0.8, color="#DDDDDD", zorder=2)
ax[1].grid(True, which="minor", linewidth=0.5, color="#EEEEEE", linestyle="--",␣
 ↪zorder=1)
ax[1].legend(frameon=True, fancybox=True, framealpha=0.75, borderpad=0.5)

plt.tight_layout()

plt.show()
```


Gain
Gain (dB)
20
15
10
5
0
−5
Phase
Phase (°)
0
−20
−40
−60
−80
−100
−120
−140
10^1
10^2
10^3
10^4
10^5
10^6
10^7
Frequency (Hz)