Name: _____

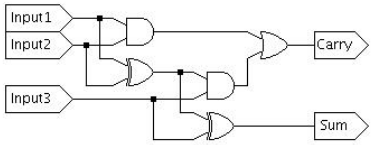
Practice Test 1

Updated: February 6, 2016

Test 1 is (tentatively) Thursday, 11 February during lab time.

Problems 1, 3, and 4 are due for credit at the beginning of class on Friday, 5 February. Problem 2, is extra credit.

All homework problems as well as the practice tests from CS 251 should also be considered part of this practice test. (In other words, the test will contain problems similar to homework problems and may contain problems related to combinatorial and sequential circuits.)



1. Compute the worst-case gate delay for both ripple-carry adders shown below. Both adders use the same full adder (shown at right). Show your work (i.e., explain how your arrived at your answer).

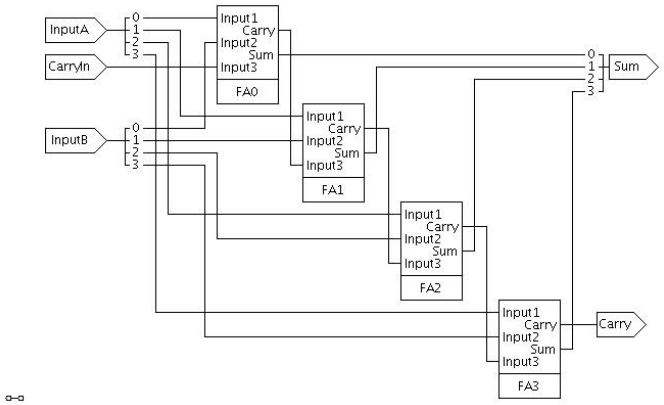


Figure 1: "Fast" Ripple-carry adder

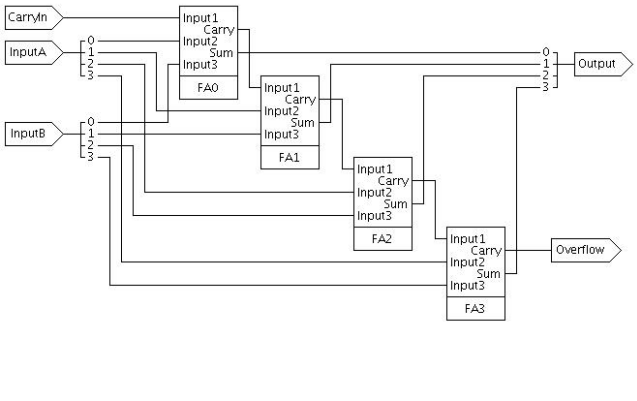


Figure 2: "Slow" Ripple-carry adder

2. For each circuit in problem 1, find an example input that requires the maximum amount of time.

3. Complete the characteristic table for the circuit shown below:

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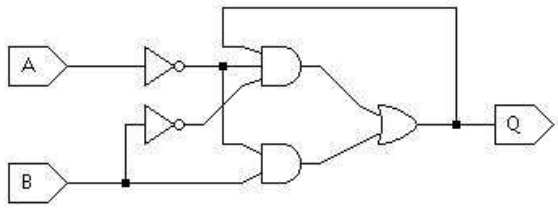
A_n	B_n	Q_n	Q_{n+1}
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

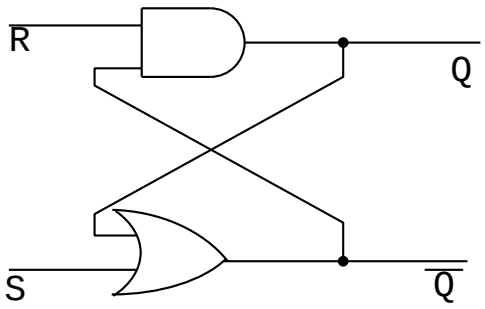


What fundamental circuit has the same characteristic table?

4. Use Boolean Algebra to show how the circuit in problem 3 is equivalent to one of the fundamental circuits used to build CPUs. Prove the Boolean expressions for each *circuit* are equivalent. (Don't use the sum of products from the characteristic table.)

5. Complete the characteristic table for the circuit shown below: Note, there is no clock pulse here. Your answers should show the states Q and $\bar{Q}$ after they have reached a steady state given R, S, and current values of Q and $\bar{Q}$. If the given inputs will produce a non-deterministic output (i.e., the output depends on which gate changes first), write "random" in the row.

R	S	Q_{now}	$\bar{Q}_{now}$	Q_{next}	$\bar{Q}_{next}$
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		



6. Choose a row labeled "random", and explain why the output is random.

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7. Show how to build a SR latch (clocked or unclocked).
8. Show how to build a D latch (clocked or unclocked).
9. Show how to build a D flip-flop from two D latches.
10. Show how to add an enable input to a D latch or flip-flop.
11. Review the Sequential Circuits homework.
12. Show how to build a register file using only AND, OR, NOT, NOR, NAND, and XOR gates.
13. Explain at a high level how a carry lookahead adder works, and why its running time is $O(\log n)$.
14. Explain at a high level how a carry select adder works, and why its running time is $O(\log n)$.