ECEN3763 - Homework Week 4

Fall, 2021

Due Monday February 7th, 11:59pm – 15 Points

You may use the following for this homework assignment:

1. CycloneV DeviceHandbook (in Reference Material > CycloneV)
2. DE10-Standard_User_manual (in Reference Material > Terasic DE10-Standard)
3. Terasic SystemBuilder (CD image in Reference Material > Terasic DE10-Standard)
4. Quartus Pin Planner (Quartus)

The topic of Homework Week 4 is FPGA I/O and the skills needed for successful design.

Problem 1 – 9 pts, 0.6 pt each

Use the SystemBuilder tool to create a set of project files that contain all peripherals (except the HPS, GPIO Header, and HSMC Header). Open the project, then in Quartus go to Assignments > Pin Planner.

In the CycloneV design used on the DE10-Standard board, what I/O standards are used for the following signals / signal groups?

a) Clock_50 _____

b) Clock2_50 _____

c) Clock3_50 _____

d) Clock4_50 _____

e) KEY[3:0] _____

f) SW[9:0] _____

g) LEDR[9:0] _____

h) HEX displays _____

i) SDRAM _____

j) Video_in _____

k) VGA _____

l) Audio _____

m) ADC _____

n) I2C _____

o) IR _____

Problem 2 – 6 pts

For all the signals and signal groups shown in Problem1, how many signals are assigned to each I/O Bank, and what is the I/O voltage assigned to each bank?

To find this information, have the project open in Quartus, and go to Assignments > Pin Planner. The spreadsheet in the bottom tab will contain the information.

Bank 3A #Pins _____ Voltage: _____

Bank 3B #Pins _____ Voltage: _____

Bank 4A #Pins _____ Voltage: _____

Bank 5A #Pins _____ Voltage: _____

Bank 5B #Pins _____ Voltage: _____

Bank 8A #Pins _____ Voltage: _____