ECEN3763 - Homework Week 13

Spring, 2022

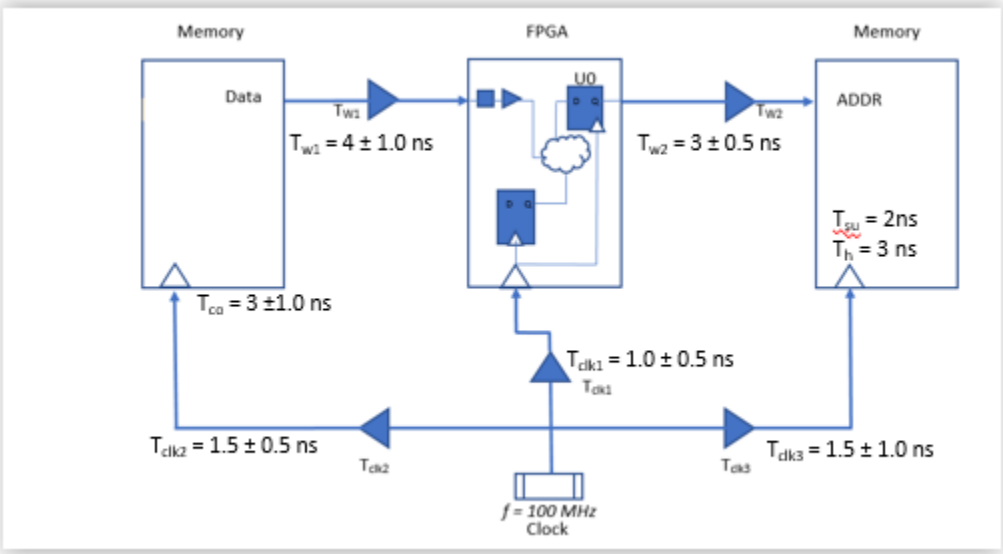
Due Monday April 18th, end of day

15 points

The purpose of this homework is to practice creation of I/O timing constraints. Use the equations found in the Lecture 23 and 24 slides.

For part 2, use the provided Quartus project to create the actual constraints used.

Part 1: Problem (2 points each, total of 8 points)



Based on the above diagram, calculate the set_input_delay min and max values, and also calculate the set_output_delay min and max values. Show your work.

Part 2: Create the I/O Timing Constraints and View in Timing Analyzer (7 points)

Like everything one does in Quartus, there are many ways to create timing constraints. Using the graphical tools in Timing Analyzer might seem to be the easiest way to create constraints, use of these tools often masks the important details on why constraints are created the way they are. For this reason we will not use the graphical tools, but instead will create these constraints manually.

1. Compile the provided project, ignore the lack of pin assignments.

2. Open your favorite text editor and create a new file with a .sdc extension. Name this file something different than the current SDC file.

3. Open the Quartus Qhelp utility for reference. You can do this by opening a terminal and entering quartus_sh –qhelp. You will want to refer to the Tcl sdc package.

4. Create the FPGA clock constraint, and two virtual clock constraints for the component driving the input signals, and for the component driving the output signals.

   Note: The only difference between the FPGA and virtual clocks are that the virtual clocks do not have a target. To include the target, use [get_ports clock] to the end of your create_clock command for the FPGA.

5. Create set_input_delay constraints for the inputs. I will give you the constraint the the max set_input_delay, use this as guidance to create the min constraint.

```
set_input_delay -clock v_clock_in -max [expr {4 + 5 – ( }] [get_ports datain*]
```

6. Create the set_output_delay constraints.

7. Add the constraint file to your project and recompile.

8. Open Timing Analyzer, click on Update Timing Netlist in the Tasks pane on the left. Run the following reports and capture the information for the questions below;

a. Reports > Slack >Report Slack Summary and Report Hold Summary

Are any values negative, and if so, setup or hold? _____

What is the failing value reported (Slack, not End Point TNS)? _____

b. Reports > Diagnostic > Report Unconstrained Paths

Do you see 0 unconstrained paths? _____

c. Reports > Diagnostic > Report SDC

In the Report Pane on the left side of the screen, under the heading SDC Assignments, look at the Set Input Delay and Set Output Delay entries.

What are the two delay values reported in the Set Input Delay Screen?

_____

What are the two delay values reported in the Set Output Delay Screen?

_____