ECEN3763 Lab Weeks 12, 13, 14
Interface to Analog to Digital Converter
Spring, 2022
Due April 28th, 2022, end of day
105 points

Note: This lab is due on the final day of the semester. You must submit this lab no later than April 28th, no late submission extensions will be given.
You have been warned……..

Summary:

Your boss is leaving on vacation, returning on Friday, April 29th. Coincidentally, April 29th is the day of a major customer demonstration that must go well in order for the company to survive.

Before your boss left, he stopped by your desk and said that an Analog to Digital Converter (ADC) must be added to the system prior to the customer demonstration. It is up to you to make this happen. Unfortunately, no one else at the company knows anything about ADCs or FPGAs.

The only support the boss offered was an old SystemVerilog module that would convert a 12 bit binary value to 4 binary coded decimal (BCD) digits.

Instructions:

1. Design a circuit that performs continuous voltage conversion using an LTC2308 ADC
2. Use a Terasic DE10-Standard board and display the input voltage values (base 10) on 4 HEX displays (0000 to 4095)
3. The ADC channel is selected with SW[2:0] (000 = channel 0, 111 = channel 7)
4. The range of input voltage is 0v – +4.095v

Resources:

1. Datasheet for a LTC2308 Analog to Digital converter
2. User manual and schematic for the DE10-Standard board you will use to prototype your

design
3. A brief writeup describing the resources on the DE10-Standard board
4. bin2bcd.sv module to convert 12 bit unsigned binary value to 4 BCD digits

Submission and Grading:

Note: Please put all files in a single (.zip or .7z or .tar or .gz) archive for upload to Canvas

1. A .qar file of your design (please include the .cdf programming file)
2. A short video demonstrating operation of your design (no more than 1 to 2 minutes in length, shorter the better). **Submit a video even if your design is not working, use the video to explain how much progress was made**.
3. A screen capture from either SignalTap or Modelsim showing one complete sample conversion cycle. **If your design is not working, include a screen capture of your SignalTap or simulation progress at the end of the project**.
4. A brief informal report discussing the problems you ran into, areas of the project that confused you, and if you were not able to complete the lab, the status of the work submitted.

This lab will be graded as follows (105 points total):

Quartus project that compiles and downloads to board	25 points
Correct operation of design	40 points
Video demonstration	15 points
Conversion cycle waveforms	20 points
Informal report	5 points