S A Z E N T O DISPLAY CO.LTD

LIQUID CRYSRAL DISPLAY MODULE

Product Specification

CUSTOMER					
PRODUCT NUMBER	WCG12864B1FSDNB	WCG12864B1FSDNBG			
CUSTOMER APPROVAL		Date 2008/3/20			

INTERNAL APPROVALS									
Quality Mgr	Quality Mgr Product Mgr Mech. Eng Electr. Eng								
	Suny	Pat Chang	VINCEN						

- ☐ Approval for Specification only
- ☑ Approval for Specification and Sample

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REVISION STATUS

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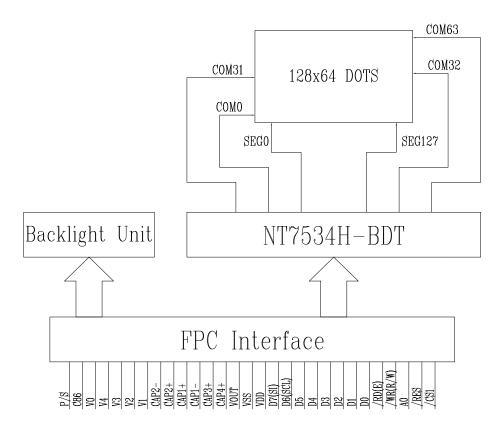
TABLE OF CONTENTS

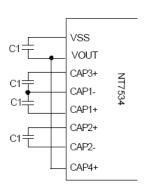
No	0.	CONTENTS	AGE
RE	VISI	ON STATUS	2
TA	BLE	OF CONTENTS	3
1.	GE	NERAL DESCRIPTION	4
2.	FU	NCTIONAL BLOCK DIAGRAM	5
3.	ME	CHANICAL SPECIFICATION	6
4.	PIN	N DESCRIPTION	7
5.	ELE	ECTRICAL CHARACTERISTICS	8
6.	INS	STRUCTION SET	13
7.	OP	TICAL CHARACTERISTICS	15
8.	QU	IALITY SPECIFICATIONS	16
9.	REI	LIABILITY	22
10). H <i>A</i>	ANDLING PRECAUTION	23

1. GENERAL DESCRIPTION

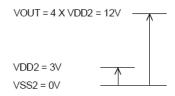
No.	Item	Specification	Unit
1	Outline Dimension	$35.7(W) \times 45.4(H) \times 3.3 max(T)$	mm
2	Number of Dots	128(W) × 64(H)	pixels
3	Active Area	27.116(W) × 18.028(H)	mm
4	Viewing Area	31(W) × 21(H)	mm
5	Dot Size	0.192(W) × 0.262(H)	mm
6	Dot Pitch	0.212(W) × 0.282(H)	mm
7	Display Mode	Transflective/Positive	-
8	Display Type	FSTN	-
9	Driving Method	1/65 Duty , 1/9 Bias	-
10	Viewing Direction	6 o'clock	-
11	Input Interface	Parallel and serial interface	-
12	Backlight Unit	LED (Blue)	-
13	Driver IC	NT7534H-BDT	-
14	Weight	-	g

2. FUNCTIONAL BLOCK DIAGRAM



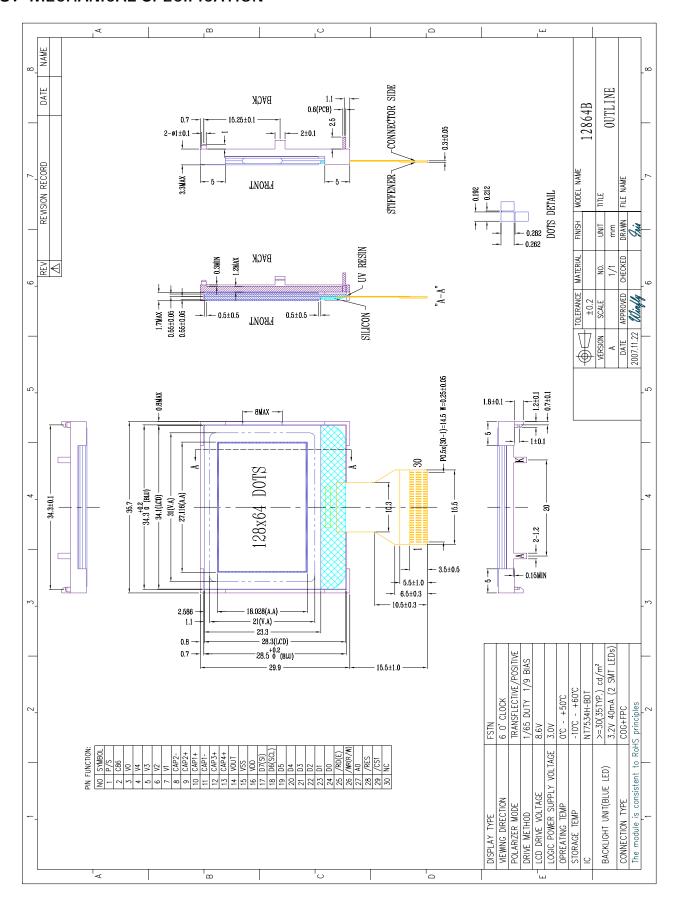


4x step-up voltage circuit



4x step-up voltage relationships

3. MECHANICAL SPECIFICATION



4. PIN DESCRIPTION

No.	Symbol	I/O	Function	Remark
1	P/S	I	P/S="H": Parallel data input, P/S="L": serial data input.	
2	C86	I	C86="H": 6800 series MPU interface; C86="L": 8080 series MPU interface.	
3	V0		LCD driver supply voltages. The voltage determined by LCD cell is	
4	V4		impedangce-converted by a resistive driver or an operation amplifier for application. Voltages should be the following	
5	V3	Р	relationship: V0>V1>V2>V3>V4>VSS	
6	V2		When the on-chip operating power circuit is on, the following are given	
7	V1		to V1 to V4 by the on-chip power circuit .Voltage selection is performed by the set LCD bias command.	
8	CAP2-			
9	CAP2+			
10	CAP1+			
11	CAP1-	0	Capacitor for internal DC/DC voltage converter.	
12	CAP3+			
13	CAP4+			
14	VOUT	Р	DC/DC voltage converter output.	
15	VSS	Р	Ground for logic circuit.	
16	VDD	Р	Supply voltage of logic control circuit.	
17	D7(SI)			
18	D6(SCL)			
19	D5		This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected,	
20	D4	1./0	then D7 serves as the serial data input terminal and D6 serves as	
21	D3	1/0	the serial lock input terminal. At this time, D0-D5 are set to high impedence. When the chip select is inactive, D0 to D7 are set to	
22	D2	r	high impedance.	
23	D1			
24	D0			
25	/RD(E)	I	Operation (data read/write) enable signal.	
26	/WR(R/W)	I	Read/write select signal.	
27	Α0	I	Select register. 0: Instruction register (for write) busy flag & address counter(for read), 1: Data register(for write and read).	
28	/RES	ı	When /RES is setto "L", the setting are initialized the /RES operation is performed by the /RES signal level.	
29	/CS1	I	This is the chip select signal. When /CS1="L" and CS2="H", then the chip select becomes active, and data/command I/O is enabled.	

5. Electrical Characteristics

5.1 ABSOLUTE MAXIMUM RATINGS

Itom	Cumbal	Val	ues	Hoit	Damank
Item	Symbol	Min	Max.	Unit	Remark
Supply Voltage for Logic	VDD - VSS	-0.3	4.0	٧	
Input Voltage	VIN	-0.3	12	٧	
Operating Temp.	Тор	0	50	°C	
Storage Temp.	Tst	-10	60	°C	

5.2 DC ELECTRICAL CHARACTERISTICS

5.2.1 LCD DC CHARACTERISTICS

Typical Operating Conditions (Ta=25℃)

Item		Symbol	Test		Values	Unit	Remark	
11	em	Symbol	condition	Min	Тур	Max.	Ullit	Remark
Logic Supp	oly Voltage	VDD - VSS	-	-	3.0	-	٧	
LCD	Drive	V LCD		8.4	8.6	8.8	٧	
Input	V IH	V _{DD} =	-	0.8 VDD	-	VDD	٧	
Voltage	VIL	$3.0V \pm 5\%$	-	VSS	-	0.2 VDD	٧	
Output	Vон	V _{DD} =	-	0.8 VDD	-	VDD	٧	
Voltage	Vol	$3.0V \pm 5\%$	-	VDD	-	0.2 VDD	٧	
Current Co	onsumption	Idd	-	-	0.27	2	mA	

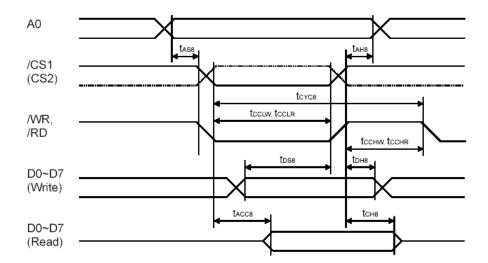
5.2.2 BACKLIGHT UNIT (GND=0V)

Condition Ta=25°C

ltem	Symbol		Values	Unit	Remark	
item	Symbol	Min	Тур	Max.	Ullit	Remark
Forward Current	IF	-	40	-	mA	
Forward Voltage	VF	-	3.2	-	٧	IF= 40mA
Backlight Luminous	-	45	50	-	cd/m ²	IF= 40mA
Emission wavelength	λр	467	470	473	nm	IF=40mA

5.3 AC TIMING DIAGRAMS

System bus read/write characteristics 1 (8080 Series MPU)



 $(VDD = 2.7 \sim 3.6V, Ta = -40 \sim +85^{\circ}C)$

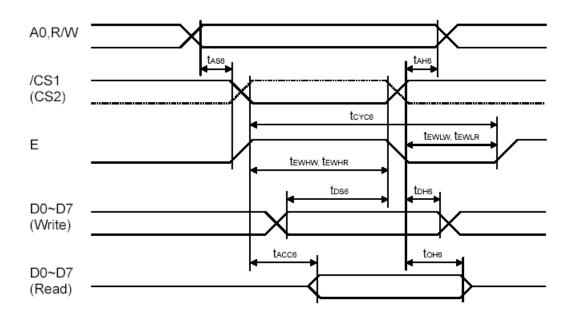
Symbol	Parameter	Min.	Тур.	Max.	Unit	Condition
Танв	Address hold time	0	-	-	ns	A0
Tasa	Address setup time	0	-	-	ns	AU
tcyc8	System cycle time	240	-	-	ns	
tccLw	Control low pulse width (write)	90	-	-	ns	WR
tccLR	Control low pulse width (read)	120	-	-	ns	/RD
tсснw	Control high pulse width (write)	100	-	-	ns	/WR
tccнr	Control high pulse width (read)	60	-	-	ns	/RD
T _{DS8}	Data setup time	40	-	-	ns	D0~D7
Трн8	Data hold time	10	-	-	ns	D04D1
tacc8	/RD access time	-	-	140	ns	D0~D7, CL = 100pF
Тснв	Output disable time	5	-	50	ns	D0~D7, GL = 100pF

 $(VDD = 1.8 \sim 2.7V, Ta = -40 \sim +85^{\circ}C)$

Symbol	Parameter	Min.	Тур.	Max.	Unit	Condition
tans	Address hold time	0	-	-	ns	A0
tass	Address setup time	0	1	1	ns	AU
tcyc8	System cycle time	400	1	-	ns	
tccLw	Control low pulse width (write)	150	-	-	ns	/WR
tcclr	Control low pulse width (read)	150	-	-	ns	/RD
tccнw	Control high pulse width (write)	120	-	-	ns	/WR
tccнr	Control high pulse width (read)	120	-	-	ns	/RD
tosa	Data setup time	80	-	-	ns	D0~D7
ton8	Data hold time	30	-	-	ns	D0~D7
tacc8	/RD access time	-	-	240	ns	D0~D7, CL = 100pF
tснв	Output disable time	10	-	100	ns	D0~D7, GL = 100pF

^{*1.} The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less. $(t_r + t_f) < (tcycs - tcclw - tcchw)$ for write, $(t_r + t_f) < (tcycs - tcclr - tcchr)$ for read.

System bus read/write characteristics 2 (6800 Series MPU)



^{*2.} All timing is specified using 20% and 80% of VDD as the reference.

^{*3.} tccLw and tccLR are specified as the overlap interval when /CS1 is low (CS2 is high) and /WR or /RD is low.

 $(VDD = 2.7 \sim 3.6V, Ta = -40 \sim +85^{\circ}C)$

				(*22		
Symbol	Parameter	Min.	Тур.	Max.	Unit	Condition
tan6	Address hold time	0	-	-	ns	A0. R/W
tase	Address setup time	0	-	-	ns	A0, R/VV
tcyc6	System cycle time	240	-	-	ns	
tewnw	Control high pulse width (write)	90	-	-	ns	E
tewnr	Control high pulse width (read)	120	-	-	ns	E
tewLw	Control low pulse width (write)	100	-	-	ns	E
tewLR	Control low pulse width (read)	60	-	-	ns	E
tose	Data setup time	40	-	-	ns	D0~D7
tone	Data hold time	10	-	-	ns	D0~D1
tacc6	/RD access time	-	-	140	ns	D0~D7
toн6	Output disable time	5	-	50	ns	CL = 100pF

 $(VDD = 1.8 \sim 2.7V, Ta = -40 \sim +85^{\circ}C)$

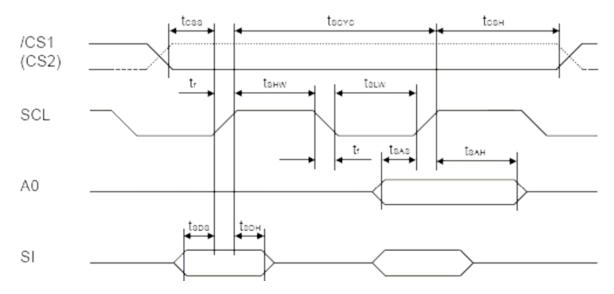
Symbol	Parameter	Min.	Тур.	Max.	Unit	Condition	
tah6	Address hold time	0	-	-	ns	A0, R/W	
tase	Address setup time	0	-	-	ns	A0, N/VV	
tcyc6	System cycle time	400	-	-	ns		
tewnw	Control high pulse width (write)	150	-	-	ns	E	
tewnr	Control high pulse width (read)	150	-	-	ns	E	
tewLw	Control low pulse width (write)	120	-	-	ns	E	
tewLR	Control low pulse width (read)	120	-	-	ns	E	
tos6	Data setup time	80	-	-	ns	D0~D7	
tDH6	Data hold time	30	1	-	ns	00~07	
tacc6	/RD access time	-	-	240	ns	D0~D7	
tоне	Output disable time	10	-	100	ns	CL = 100pF	

^{*1.} The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less. $(t_r + t_f) < (t_{CYC6} - t_{EWLW} - t_{EWHW})$ for write, $(t_r + t_f) < (t_{CYC6} - t_{EWLR} - t_{EWHR})$ for read.

^{*2.} All timing is specified using 20% and 80% of VDD as the reference.

^{*3.} tewnw and tewnr are specified as the overlap interval when /CS1 is low (CS2 is high) and E is high.

System bus read/write characteristics 3 (Serial Interface Timing)



 $(VDD = 2.7 \sim 3.6V, Ta = -40 \sim +85^{\circ}C)$

	(VBB = 2.7 = 3.0 V, 1a = -40 = +03					
Symbol	Parameter	Min.	Тур.	Max.	Unit	Condition
tscyc	Serial clock cycle	120	-	-	ns	SCL
tsHW	Serial clock H pulse width	60	-	-	ns	SCL
tsLw	Serial clock L pulse width	60	-	-	ns	SCL
tsas	Address setup time	30	-	-	ns	A0
tsan	Address hold time	20	-	-	ns	A0
tsos	Data setup time	30	-	-	ns	SI
tsph	Data hold time	20	-	-	ns	SI
tcss	Chip select setup time	20	-	-	ns	/CS1, CS2
tcsH	Chip select hold time	40	-	-	ns	/CS1, CS2

^{*1.} The input signal rise time and fall time (tr, tr) is specified as 15ns or less.

^{*2.} All timing is specified using 20% and 80% of VDD as the standard.

6. Instruction Set

Table 14. Command Table

								Code					
Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
(1) Display OFF	0	1	0	1	0	1	0	1	1	1	0	AEh AFh	Turn on LCD panel when high, and turn off when low
(2) Display Start Line Set	0	1	0	0	1		Disp	lay Sta	art Ade	dress		40h to 7Fh	Specifies RAM display line for COM0
(3) Page Address Set	0	1	0	1	0	1	1	F	age A	Addres	s	B0h to B8h	Set the display data RAM page in Page Address register
(4) Column Address Col	0	1	0	0	0	0	1	Н		Colum Iress	ın	00h	Set 4 higher bits and 4 lower bits of column address of display data
(4) Column Address Set	0	1	0	0	0	0	0	L		Colum Iress	n	to 18h	RAM in register
(5) Read Status	0	0	1		Sta	itus	•	0	0	0	0	ΧХ	Reads the status information
(6) Write Display Data	1	1	0				Write	Data				XX	Write data in display data RAM
(7) Read Display Data	1	0	1				Read	Data				XX	Read data from display data RAM
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0	A0h A1h	Set the display data RAM address SEG output correspondence
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0	A6h A7h	Normal indication when low, but full indication when high
(10)Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0	A4h A5h	Select normal display (0) or entire display on
(11)LCD Bias Set	0	1	0	1	0	1	0	0	0	1	0	A2h A3h	Sets LCD driving voltage bias ratio
(12)Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	E0h	Increments column address counter during each write
(13)End	0	1	0	1	1	1	0	1	1	1	0	EEh	Releases the Read-Modify-Write
(14)Reset	0	1	0	1	1	1	0	0	0	1	0	E2h	Resets internal functions
(15)Common Output Mode Select	0	1	0	1	1	0	0	0 1	*	*	*	C0h to CFh	Select COM output scan direction *: invalid data
(16)Power Control Set	0	1	0	0	0	1	0	1	Oper	ation \$	Status	28h to 2Fh	Select the power circuit operation mode
(17)V0 Voltage Regulator Internal Resistor ratio Set	0	1	0	0	0	1	0	0	Res	istor F	Ratio	20h to 27h	Select internal resistor ratio Rb/Ra mode
(18)Electronic Volume mode Set	0	1	0	1	0	0	0	0	0	0	1	81h	
Electronic Volume Register Set	0	1	0	*	*		Electr	onic C	ontrol	Value		хх	Sets the V0 output voltage electronic volume register
(19)Set Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0	ACh ADh	Sets static indicator ON/OFF 0: OFF, 1: ON
Set Static Indicator Register	0	1	0	*	*	*	*	*	*	- 		хх	Sets the flash mode
(20)Power Save	0	1	0	1	-	-	-	-	-	-	-	-	Compound command of Display OFF and Entire Display ON
(21)NOP	0	1	0	1	1	1	0	0	0	1	1	E3h	Command for non-operation

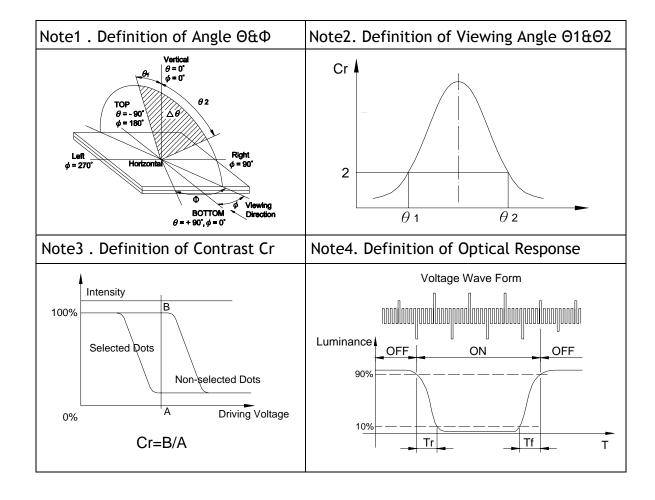
Command Table (continue)

								Code					
Command	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
(22)Oscillation Frequency Select	0	1	0	1	1	1	0	0	1	0	0 1	E4h E5h	Select the oscillation frequency
(23)Partial Display mode Set	0	1	0	1	0	0	0	0	0	1	0	82h 83h	Enter/Release the partial display mode
(24)Partial Display Duty Set	0	1	0	0	0	1	1	0	D	uty Ra	tio		Sets the LCD duty ratio for partial display mode
(25)Partial Display Bias Set	0	1	0	0	0	1	1	1	Bi	as Ra	tio		Sets the LCD bias ratio for partial display mode
(26)Partial Start Line Set	0	1	0	1	1	0	1	0	0	1	1	D3h	Enter Partial Start Line Set
Partial Start Line Set	0	1	0	1	1		Pa	Partial Start Line		хх	Sets the LCD Number of partial display start line		
(27)N-Line Inversion Set	0	1	0	1	0	0	0	0	1	0	1	85h	Enter N-Line inversion
Number of Line Set	0	1	0	*	*	*		Num	ber of	Line		хх	Sets the number of line used for N-Line inversion
(28)N-Line Inversion Release	0	1	0	1	0	0	0	0	1	0	0	84h	Exit N-Line Inversion
(29)DC/DC Clock Set	0	1	0	1	1	1	0	0	1	1	0	E6h	Set DC/DC Clock Frequency
DC/DC Clock Division Set	0	1	0	1	1	0	0	Clock Division		xx	Set the Division of DC/DC Clock Frequency		
(30)Test Command	0	1	0	1	1	1	1	*	*	*	*	F1h to FFh	IC test command. Do not use!
(31)Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	F0h	Command of test mode reset

Note: Do not use any other command, or system malfunction may result.

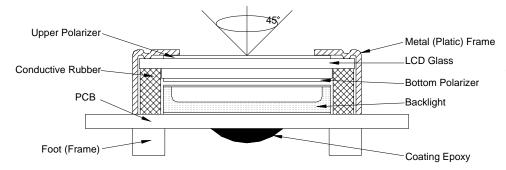
7. OPTICAL CHARACTERISTICS

Itom	Symbol	Values			l lni+	Conditions	Tomp	Remark
Item	Symbol	Min	Тур	Max.	Unit	Conditions	теттр	Remark
Viewing angle	02 -01	30	84	-	Dog	_	25℃	1,2
Viewing angle	Ф	60	90	-	Deg.	-		1,2
Contrast Ratio	Cr	2	5	-	-	Θ=0° Φ=0°	25 ℃	3
Posponso Timo(riso)	Т.,	-	63	250		Θ=0° Φ=0°	25 ℃	
Response Time(rise)	Tr	-	950	1150	ms		0℃	4
Response Time(fall)	T.C	-	120	250	ms	Θ=0°	25℃	4
	Tf	-	950	1150		Ф=0°	0℃	



8. QUALITY SPECIFICATIONS

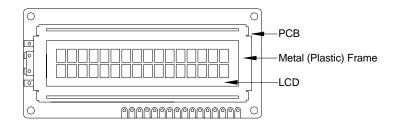
- 8 .1 LCM Appearance and Electric Inspection Condition
 - 8.1.1 Inspection will be done by placing LCM 30cm away from inspector's eyeballs under normal illumination.



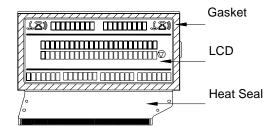
8.1.2 View Angle: with in 45° around perpendicular line.

8.2 DEFINITION

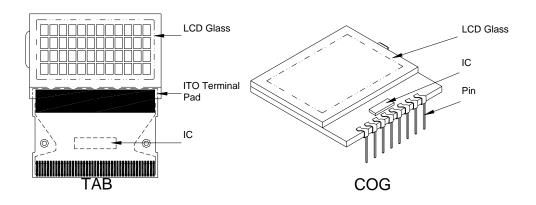
8.2.1 COB



8.2.2 Heat Seal



8.2.3 TAB AND COG



8.3 SAMPLING PLAN AND ACCEPTANCE

8.3.1 Sampling Plan

MIL - STD - 105E (\parallel) ordinary single inspection is used.

8.3.2 Acceptance

Major defect:

AQL = 0.25%

Minor defect:

AQL = 0.65%

8.4 CRITERIA

8.4.1 COB

Defect	Inspection Item	Inspection Standards	
Major	PCB copper flakes peeling off	Any copper flake in viewing Area should be greater than 1.0mm ²	Reject
Major	Height of coating epoxy	Exceed the dimension of drawing	Reject
Major	Void or hole of coating epoxy	Expose bonding wire or IC	Reject
Major	PCB cutting defect	Exceed the dimension of drawing	Reject

8.4.2 SMT

Defect	Inspection Item	Inspection Standa	ırds
Minor	Component marking not readable		Reject
Minor	Component height	Exceed the dimension Of drawing	Reject
Major	Component solder defect (missing, extra, wrong component or wrong orientation)		Reject
Minor	Component position shift component soldering pad X D A A A A A A A A A A A A	X < 3/4Z Y > 1/3D	Reject Reject
Minor	Component tilt component soldering pad	Y > 1/3D	Reject
Minor	Insufficient solder component PAD ← PCB	θ <u><</u> 20°	Reject

8.4.3 METAL (PLASTIC) FRAME

Defect	Inspection Item		nspection Standar	⁻ ds		
Major	Crack / breakage	Any	where	Reject		
		W	L	Acceptable of Scratch		
		w<0.1mm	Any	Ignore		
		0.1 <u><</u> w<0.2mm	L <u><</u> 5.0mm	2		
Minor	Frame Scratch	0.2 <u><</u> w<0.3mm	L <u><</u> 3.0mm	1		
7411101	Trame seracen	w <u>></u> 0.3mm	Any	0		
		Note: 1. Above criteria applicable to scratch lines with distance greater than 5mm. 2. Scratch on the back side of frame (not visible) can be ignored.				
				Acceptable of Dents / Pricks		
		Φ<	2			
	Frame Dent , Prick	1.0<0	1			
Minor	$\Phi = \frac{L + W}{2}$	1.5	0			
	2	Note: 1. Above criteria applicable to any two dents / pricks with distance greater than 5mm 2. Dent / prick on the back side of frame (not visible) can be ignored				
Minor	Frame Deformation	Exceed the dimension of drawing				
Minor	Metal Frame Oxidation		Any rust			

8.4.4 FLEXIBLE FILM CONNECTOR (FFC)

Defect	Inspection Item	Inspection Standards			
Minor	Tilted soldering	Within the angle $+5^{\circ}$	Acceptable		
Minor	Uneven solder joint /bump		Reject		
Minor	Hole $\Phi = \frac{L + W}{L}$	Expose the conductive line	Reject		
Millor	2	Φ > 1.0mm	Reject		
Minor	Position shift	Y > 1/3D	Reject		
Minor		X > 1/2Z	Reject		

8.4.5 SCREW

Defect	Inspection Item	Inspection Standards	
Major	Screw missing/loosen		Reject
Minor	Screw oxidation	Any rust	Reject
Minor	Screw deformation	Difficult to accept screw driver	Reject

8.4.6 HEATSEAL \ TCP \ FPC

Defect	Inspection Item	Inspection Standards	
Major	Scratch expose conductive layer		Reject
Minor	HS Hole $\Phi = \frac{L + W}{2}$	Φ> 0.5mm	Reject
Major	Adhesion strength	Less than the specification	Reject
Minor	Position shift	Y > 1/3D	Reject
MIIIOI	X	X > 1/2Z	Reject
Major	Conductive line break	55 750 v	Reject

8.4.7 LED BACKING PROTECTIVE FILM AND OTHERS

Defect	Inspection Item	Inspection Standards				
		Acceptable number of units				
		Φ <u><</u> 0.10mm	lgnore			
Minor		0.10<Φ <u><</u> 0.15mm	2			
	LED dirty, prick	0.15<Φ <u><</u> 0.2mm	1			
		Φ>0.2mm	0			
		The distance between any two spots should be ≥5mm Any spot/dot/void outside of viewing area is acceptable				
Minor	Protective film tilt	Not fully cover LCD	Reject			
Major	COG coating	Not fully cover ITO circuit	Reject			

8.4.8 ELECTRIC INSPECTION

Defect	Inspection Item	Inspection Standards	
Major	Short		Reject
Major	Open		Reject

8.4.9 INSPECTION SPECIFICATION OF LCD

Defect	Insp	ect Item			Inspection Standards					
Minor L	Linear Defect	* Glass Scratch * Polarizer Scratch * Fiber and Linear	W	W <u><</u> 0.03		0.0	0.03 <w<u><0.05</w<u>		V>0.05	
			L		L<5			L<3		Any
			ACC. NO.	1				1		Reject
		material	Note	L is the length and W is the width of the defect						the
		* Foreign material	Ф	Ф <u><</u>	0.1	0.1<Ф<	0.15).15<Φ <u><</u> ().2	Φ>0.2
Minor	Black Spot and Polarizer Pricked	between glass and polarizer or glass and glass * Polarizer hole or * Protuberance by external force	ACC. NO.	3E/ 100r	A / mm²	2		1		0
			Note	Φ is the average diameter of the defect. Distance between two defects > 10mm.						
Minor	White Spot and Bubble in Polarizer	 Unobvious transparant foreign material between glass and glass or glass and polarizer Air protuberance between polarizer and glass 	Φ	Ф <u><</u> 0.3		0.3	0.3<Φ <u><</u> 0.5		.5<Ф	
			ACC. NO.	3EA	SEA / 100mm ²			1		0
			Note	Φ is the average diameter of the defect. Distance between two defects > 10mm.						
Minor	Segment Defect		Φ	Φ <u><</u> (0.10	0.10<Ф	<u><</u> 0.20	0.20<Ф	<u><</u> 0.25	Φ>0.25
			ACC. NO.	3EA 100m		2		1		0
				W is more than 1/2 segment width Reject						
			Note	$\Phi = \frac{L + W}{2}$ Distance between two defect is 10mm						
Minor	Protuberant Segment	Φ = (L + W) / 2	Φ	Ф <u><</u> 0	0.10	0.10<Ф	< <u>0.20</u>	0.20<Φ <u><</u> 0.25		Φ>0.25
			W	Glı	ue	W <u><</u> 1/2 W <u><</u> 0	_	_	W <u><</u> 1/2 Seg W <u><</u> 0.2	
			ACC. NO.	3E/ 100n		2		1		0
Minor	Assembly Mis-alignment	B	1. Segment							
			В	B B).4mm	0.4 <b< td=""><td colspan="2">.4<b<u><1.0mm B></b<u></td><td>.0mm</td></b<>	.4 <b<u><1.0mm B></b<u>		.0mm
			В-	A	_	<1/2B		_		<0.25
			Jud	ge	Acce	eptable	Acce	eptable	Acce	ptable
			2. Dot Matrix							
			Deformation>2° Reject							
Minor	Stain on LCD Panel Surface		Accept when stains can be wiped lightly with a soft cloth or a similar one. Otherwise, judged according to the above items: "Black spot" and "White Spot"							

9. RELIABILITY

NO.	Item	Condition	Criterion			
1	High Temperature Operating	50℃, 96Hrs				
2	Low Temperature Operating	0℃, 96Hrs				
3	High Humidity	50°C, 90%RH, 96Hrs				
4	High Temperature Storage	60°C, 96Hrs				
5	Low Temperature Storage	-10℃, 96Hrs	No defect in cosmetic and operational			
6	Whenting	Random wave	function allowable.			
		10 ~ 100Hz	Total current Consumption should			
	Vibration	Acceleration: 2g	be below double of initial value.			
		2 Hrs per direction (X,Y,Z)				
7		0℃ to 25℃ to 50℃				
	Thermal Shock	(60Min) (5Min) (60Min)				
		16Cycles				
8	ESD Testing	Contract Discharge Voltage: +1 ~ 5kV and -1 ~ -5kV	There will be discharged ten times at every discharging voltage cycle.			
		+1 ~ 5KV dHU -1 ~ -5KV				
		Air Discharge Voltage: +1 ~ 8kV and -1 ~ -8kV	The voltage gap is 1kV.			

Note: 1) Above conditions are suitable for SAZENTO standard products.

2) For restrict products, the test conditions listed as above must be revised.

10. HANDLING PRECAUTION

(1) MOUNTING METHOD

The panel of the LCD Module consists of two thin glass plates with polarizers which easily get damaged since the Module is fixed by utilizing fitting holes in the printed circuit board. Extreme care should be taken when handling the LCD Modules.

(2) CAUTION OF LCD HANDLING & CLEANING

When cleaning the display surface, use soft cloth with solvent (recommended below) and wipe lightly.

- Isopropyl alcohol
- Ethyl alcohol
- Trichloro trifloro thane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface. Do not use the following solvent:

- Water
- Ketone
- Aromatics

(3) CAUTION AGAINST STATIC CHARGE

The LCD Module use C-MOS LSI drivers, so we recommend that you connect any unused input terminal to VDD or VSS, do not input any signals before power is turned on. And ground your body, Work/assembly table. And assembly equipment to protect against static electricity.

(4) PACKAGING

- Modules use LCD elements, and must be treated as such. Avoid intense shock and falls from a height.
- To prevent modules from degradation. Do not operate or store them exposed directly to sunshine or high temperature/humidity.

(5) CAUTION FOR OPERATION

- It is indispensable to drive LCD's within the specified voltage limit since the higher voltage than the limit shorten LCD life. An electrochemical reaction due to direct current causes LCD deterioration, Avoid the use of direct current drive.
- Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD's show dark color in them. However those phenomena do not mean malfunction or out of order with LCD's. Which will come back in the specified operating temperature range.
- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
- A slight dew depositing on terminals is a cause for electro-chemical reaction resulting in

terminal open circuit. Usage under the relative condition of 40°C, 50%RH or less is reequired.

(6) STORAGE

In the case of storing for a long period of time (for instance.) For years) for the purpose or replacement use, The following ways are recommended.

- Storage in a polyethylene bag with sealed so as not to enter fresh air outside in it, And with no desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light is. Keeping temperature in the specified storage temperature range.
- Storing with no touch on polarizer surface by the anything else. (It is recommended to store them as they have been contained in the inner container at the time of delivery)

(7) SAFETY

- It is recommendable to crash damaged or unnecessary LCD into pieces and wash off liquid crystal by using solvents such as acetone and ethanol. Which should be burned up later.
- When any liquid crystal leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water.