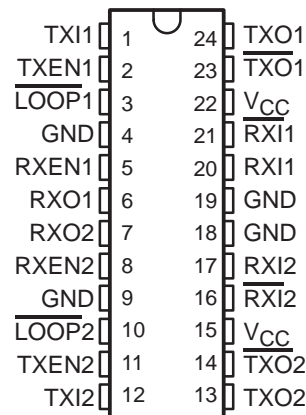


- Meets or Exceeds the Requirements of IOS 8802.3:1989 and ANSI/IEEE Std 802.3-1988
- Interdevice Loop-Back Paths for System Testing
- Squelch Function Implemented on the Receiver Inputs
- Drivers Will Drive a Balanced 78-Ω Load
- Transformer Coupling Not Required in System
- Power-Up/Power-Down Protection (Glitch Free)
- Isolated Ground Pins for Reduced Noise Coupling
- Fault-Condition Protection Built into the Device
- Driver Inputs Are Level-Shifted ECL Compatible

**DW OR NT PACKAGE  
(TOP VIEW)**



### description

The SN75ALS085 is a monolithic, high-speed, advanced low-power Schottky, dual-channel driver/receiver device designed for use in the AUI of ANSI/IEEE Std 802.3-1988. The two drivers on the device drive a 78-Ω balanced, terminated twisted-pair transmission line up to a maximum length of 50 meters. In the off (idle) state, the drivers maintain minimal differential output voltage on the twisted-pair line and, at the same time, remain within the required output common-mode range.

With the driver enable (TXEN) high, upon receiving the first falling edge into the driver input, the differential outputs will rise to full-amplitude output levels within 25 ns. The output amplitude is maintained for the remainder of the packet. After the last positive packet edge is transmitted into the driver, the driver will maintain a minimum of 70% full differential output for a minimum of 200 ns, then decay to a minimum level for the reset (idle) condition within 8 μs. Disabling the driver by taking the driver enable low will also force the output into the idle condition after the normal 8-μs timeout. While operating, the drivers are able to withstand a set of fault conditions and not suffer damage due to the faults being applied. The drivers power up in the idle state to ensure that no activity is placed on the twisted-pair cable that could be interpreted as network traffic.

The line receiver squelch function interfaces to a differential twisted-pair line terminated external to the device. The receiver squelch circuit allows differential receive signals to pass through as long as the input amplitude and pulse duration are greater than the minimum squelch threshold. This ensures a good signal-to-noise ratio while the data path is active and prevents system noise from causing false data transitions during line shutdown and line-idle conditions. The RXO outputs default to a high level and the RXEN outputs default to a low level while the squelch function is blocking the data path through the receiver (idle). The line receiver squelch will become active within 50 ns when the input squelch threshold is exceeded. RXEN will be driven high when the squelch circuit is allowing data to pass through the receiver. The receiver squelch circuit can also withstand a set of fault conditions while operating without causing permanent damage to the device.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# SN75ALS085

## LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

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### description (continued)

The purpose of the loop functions is to provide a means by which system data path verification can be done to isolate faulty interfaces and assist in network diagnosis. The LOOP pins are TTL compatible and must be held high for normal operation. When  $\overline{\text{LOOP1}}$  is taken low, the output of driver 1 (TXO1) immediately goes into the idle state. Also, the input to receiver 1 is ignored and a path from TXI1 to RXO1 is established. When  $\overline{\text{LOOP1}}$  is taken back high, driver 1 and receiver 1 revert back to their normal operation. When  $\overline{\text{LOOP2}}$  is taken low, a similar data path is established between TXI1 and RXO2. TXEN1 must be high for the loop functions to operate and TXEN1 can be used to gate the loop function if desired. During loop operation, the respective receiver enable output (RXEN) will reflect the status of TXEN1.

### Function Tables

RECEIVER –  $\overline{\text{LOOP}} = \text{H}$

RXI	PREVIOUS RXEN	OUTPUTS	
		RXEN	RXO
$V_{\text{ID}} = 1315 \text{ mV to } -175 \text{ mV}, t_{\text{W}} < 25 \text{ ns}$	L	L	H
$V_{\text{ID}} = -275 \text{ mV to } -1315 \text{ mV}, t_{\text{W}} > 50 \text{ ns}$	X	H	L
$V_{\text{ID}} = 318 \text{ mV to } 1315 \text{ mV}, t_{\text{W}} < 142 \text{ ns}$	H	H	H
$V_{\text{ID}} = 318 \text{ mV to } 1315 \text{ mV}, t_{\text{W}} > 187 \text{ ns}$	X	L	H

H = high level, L = low level, X = don't care

DRIVER –  $\overline{\text{LOOP}} = \text{H}$

TXI	TXEN	PREVIOUS TXO	OUTPUT TXO
L	L	Idle	Idle
H	L	Idle	Idle
↓	H	Idle	L
L	H	Active	L
$\text{H} < 260 \mu\text{s}$	H	Active	H
$\text{H} > 8 \mu\text{s}$	H	Active	Idle
L	$\text{L} > 8 \mu\text{s}$	Active	Idle
$\text{H} < 260 \text{ ns}$	$\text{L} > 8 \mu\text{s}$	Active	Idle
$\text{H} < 260 \text{ ns}$	$\text{L} < 260 \text{ ns}$	Active	H
$\text{H} > 8 \mu\text{s}$	$\text{L} < 260 \text{ ns}$	Active	Idle
L	$\text{L} < 260 \text{ ns}$	Active	L

$\text{H} = V_{\text{I}} \geq V_{\text{T max}}, \text{L} = V_{\text{I}} \leq V_{\text{T min}}$

# SN75ALS085

## LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

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### Function Tables (continued)

LOOP										
INPUTS						OUTPUTS				
LOOP1	LOOP2	TXI1	TXEN1	RXI1	RXI2	RXO1	RXO2	RXEN1	RXEN2	TXO1
L	L	L	H	X	X	L	L	H	H	Idle
L	L	H	H	X	X	H	H	H	H	Idle
L	L	X	L	X	X	H	H	L	L	Idle
L	H	L	H	X	Normal	L	Normal	H	Normal	Idle
L	H	H	H	X	Normal	H	Normal	H	Normal	Idle
L	H	X	L	X	Normal	H	Normal	L	Normal	Idle
H	L	L	H	Normal	X	Normal	L	Normal	H	Idle
H	L	H	H	Normal	X	Normal	H	Normal	H	Idle
H	L	X	L	Normal	X	Normal	H	Normal	L	Idle
H	H	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal

H = high level, L = low level, X = don't care

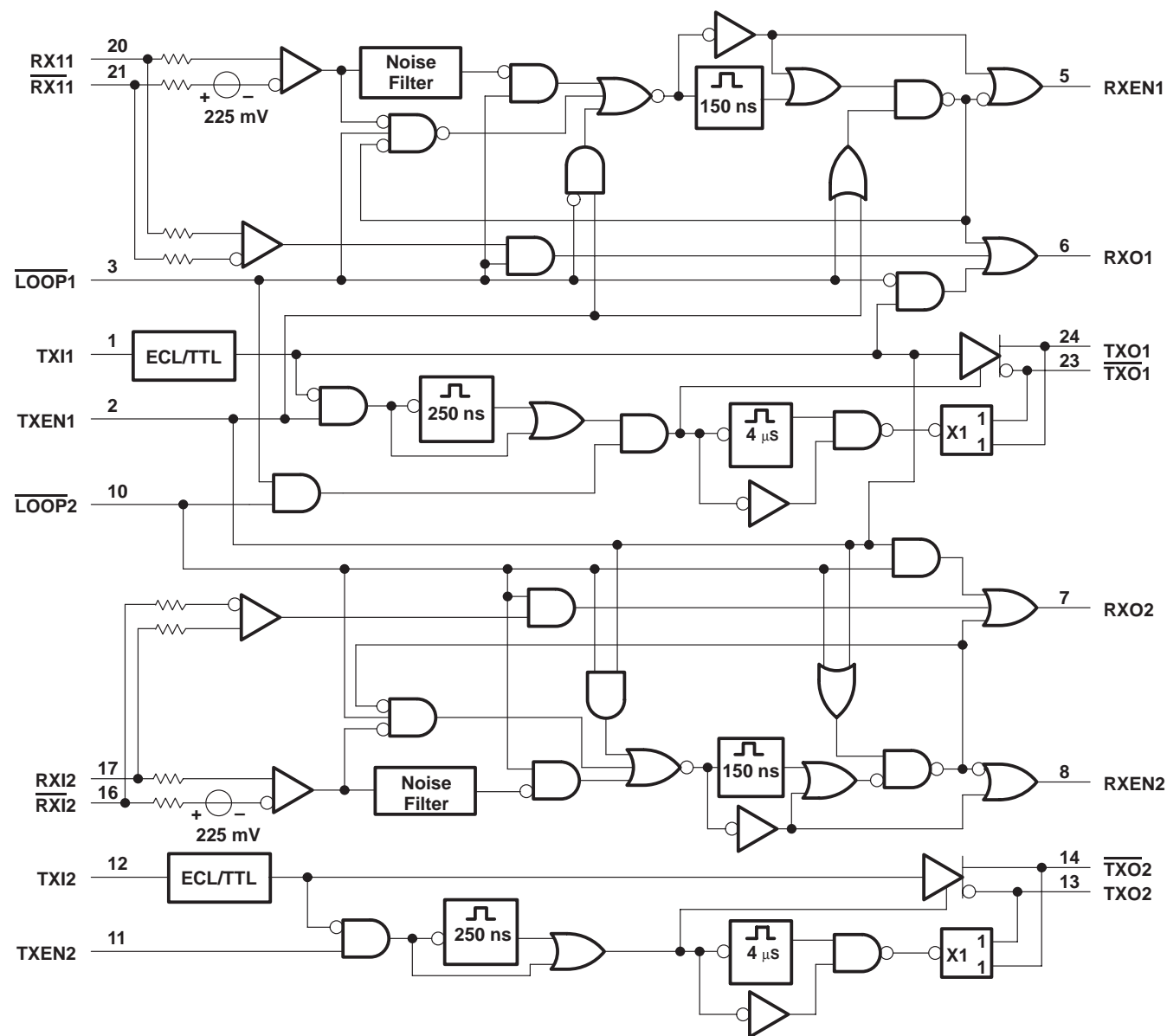


# SN75ALS085

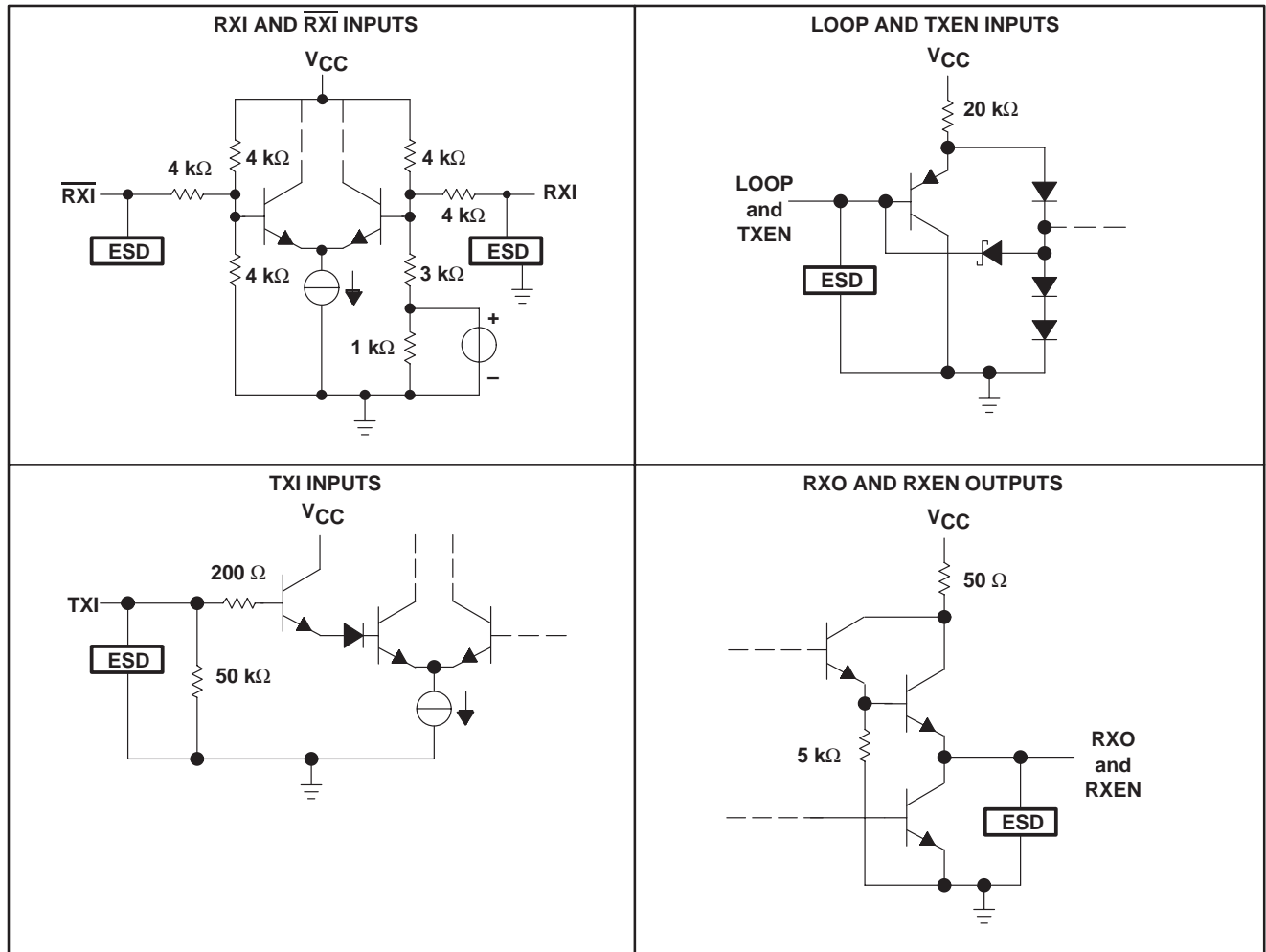
## LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

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### logic diagram (positive logic)



schematics of inputs and outputs



# SN75ALS085

## LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	6 V
TXI and $\overline{LOOP}$ input voltage, $V_I$	5.5 V
TXO and $\overline{TXO}$ output voltage, $V_O$	16 V
RXI and $\overline{RXI}$ input voltage, $V_I$	16 V
RXO and RXEN output voltage, $V_O$	5.5 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range, $T_{stg}$	– 65 °C to 150 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
DW	1350 mW	10.8 mW/°C	864 mW
NT	1250 mW	10.0 mW/°C	800 mW

### recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$	4.75	5	5.25	V
Common-mode voltage at RXI inputs, $V_{IC}$	1		4.2	V
Differential voltage between RXI inputs, $V_{ID}$	±318		±1315	mV
High-level input voltage, $\overline{LOOP}$ and TXEN, $V_{IH}$	2			V
Low-level input voltage, $\overline{LOOP}$ and TXEN, $V_{IL}$			0.8	V
High-level output current, RXO and RXEN, $I_{OH}$			– 0.4	mA
Low-level output voltage, RXO and RXEN, $I_{OL}$			16	mA
Setup time, driver mode, TXEN high before TXI↓, $t_{su1}$ (see Figure 7)	10			ns
Setup time, loop mode, $\overline{LOOP}$ low before TXEN↑, $t_{su2}$ (see Figure 9)	15			ns
Setup time, loop mode, TXEN high before TXI↓, $t_{su3}$ (see Figure 9)	10			ns
Hold time, loop mode, TXEN high after TXI↑, $t_{h1}$ (see Figure 8)	10			ns
Hold time, loop mode, $\overline{LOOP}$ low after TXEN↓, $t_{h2}$ (see Figure 8)	15			ns
Operating free-air temperature, $T_A$	0		70	°C



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## LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

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**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V <sub>IK</sub>	Clamp voltage at all inputs		I <sub>I</sub> = −18 mA		−1.5		V
V <sub>(TO)</sub>	Driver input (TXI) threshold voltage		T <sub>A</sub> = 0°C	V <sub>CC</sub> = 4.75 V	3.202	3.752	V
				V <sub>CC</sub> = 5 V	3.389	3.998	
				V <sub>CC</sub> = 5.25 V	3.577	4.244	
			T <sub>A</sub> = 25°C	V <sub>CC</sub> = 4.75 V	3.213	3.797	V
				V <sub>CC</sub> = 5 V	3.400	4.043	
				V <sub>CC</sub> = 5.25 V	3.588	4.289	
			T <sub>A</sub> = 70°C	V <sub>CC</sub> = 4.75 V	3.239	3.849	V
				V <sub>CC</sub> = 5 V	3.426	4.095	
				V <sub>CC</sub> = 5.25 V	3.614	4.341	
Receiver differential input threshold voltage					−275		mV
V <sub>OC</sub>	Driver output (TXO) common-mode voltage		Idle	TXEN at 0.8 V, LOOP2 at 2 V, See Figure 1	1	4.2	V
			Active	TXEN at 2 V, LOOP2 at 2 V, See Figure 1	1	4.2	
			Active	TXEN at 2 V, LOOP2 at 2 V, See Figure 1	1	4.2	
V <sub>OD</sub>	Driver output (TXO) differential voltage		Idle	TXEN at 0.8 V, LOOP2 at 2 V, See Figure 1	±40		mV
			Active	TXEN at 2 V, LOOP2 at 2 V, See Figure 1	−600	1315	
			Active	TXEN at 2 V, LOOP2 at 2 V, See Figure 1	600	1315	
V <sub>OH</sub>	High-level output voltage		RXO, RXEN	I <sub>OH</sub> = −0.4 mA	2.4		V
V <sub>OL</sub>	Low-level output voltage		RXO, RXEN	I <sub>OL</sub> = 16 mA	0.5		V
I <sub>IH</sub>	High-level input current		TXEN, $\overline{\text{LOOP}}$	V <sub>I</sub> = 2 V	20		μA
			TXI	V <sub>I</sub> = 4.5 V	400		
			$\overline{\text{RXI}}$ , RXI	V <sub>ID</sub> = −0.5 V, V <sub>IC</sub> = 1 V to 4.2 V	1000		
I <sub>IL</sub>	Low-level input current		TXEN, $\overline{\text{LOOP}}$	V <sub>I</sub> = 0.8 V	−200		mA
			TXI	V <sub>I</sub> = 3.1 V	100		
				V <sub>I</sub> = 0.3 V	4 10		
			$\overline{\text{RXI}}$ , RXI	V <sub>ID</sub> = 0.5 V, V <sub>IC</sub> = 1 V to 4.2 V	1000		
I <sub>OD</sub>	Driver differential output current		Idle	TXEN at 0.8 V, LOOP2 at 2 V, See Figure 2	±4		mA
I <sub>OS</sub>	Short-circuit output current†		RXO, RXEN	V <sub>O</sub> at 0 V, RXI at 2 V	−40	−150	mA
I <sub>CC</sub>	Supply current			$\overline{\text{LOOP}}$ 2 at 2 V, TXI at 4.5 V, TXEN at 2 V, Outputs open	225		mA

<sup>†</sup> Not more than one output should be shorted at a time, and the duration of the test should not exceed 1 second.

# SN75ALS085

## LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

SLLS054B – APRIL 1989 – REVISED MAY 1995

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)**

PARAMETER	TEST CONDITIONS†	MIN	MAX	UNIT
Driver fault condition current	TXO shorted to $\overline{\text{TXO}}$ , Current measured in short		150	mA
	TXO at 0 V, $\overline{\text{TXO}}$ is open, Current measured at TXO		150	
	TXO is open, $\overline{\text{TXO}}$ at 0, Current measured at $\overline{\text{TXO}}$		150	
	TXO at 0 V, $\overline{\text{TXO}}$ at 0 V, Current measured at TXO and $\overline{\text{TXO}}$		150	
	TXO at 16 V, $\overline{\text{TXO}}$ is open, Current measured at TXO		150	
	TXO is open, $\overline{\text{TXO}}$ at 16 V, Current measured at TXO		150	
	TXO at 16 V, $\overline{\text{TXO}}$ at 16 V, Current measured at TXO and $\overline{\text{TXO}}$		150	
Receiver fault condition current	RXI shorted to $\overline{\text{RXI}}$ , Current measured in short		10	mA
	RXI at 0 V, $\overline{\text{RXI}}$ is open, Current measured at RXI		3	
	RXI is open, $\overline{\text{RXI}}$ at 0 V, Current measured at RXI		3	
	RXI at 0 V, $\overline{\text{RXI}}$ at 0 V, Current measured at RXI and $\overline{\text{RXI}}$		3	
	RXI at 16 V, $\overline{\text{RXI}}$ at open, Current measured at RXI		10	
	RXI at open, $\overline{\text{RXI}}$ at 16 V, Current measured at $\overline{\text{RXI}}$		10	
	RXI at 16 V, $\overline{\text{RXI}}$ at 16 V, Current measured at RXI and $\overline{\text{RXI}}$		10	

† Fault conditions should be measured on only one channel at a time.



# SN75ALS085

## LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

SLLS054B – APRIL 1989 – REVISED MAY 1995

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

### driver

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t <sub>PLH</sub> Propagation delay time, low-to-high level output	TXI	TXO, $\overline{\text{TXO}}$	TXEN at 2 V, See Figure 3		15	ns
t <sub>PHL</sub> Propagation delay time, high-to-low level output	TXI	TXO, $\overline{\text{TXO}}$	TXEN at 2 V, See Figure 3		15	ns
t <sub>PIL</sub> Propagation delay time, idle-to-low level output	TXI	TXO, $\overline{\text{TXO}}$	TXEN at 2 V, See Figure 4		25	ns
t <sub>PIL</sub> Propagation delay time, idle-to-low level output	TXEN	TXO, $\overline{\text{TXO}}$	TXI at 3.2 V, See Figure 5		25	ns
t <sub>w</sub> Output pulse duration from low-to-high level to 70% output level		TXO, $\overline{\text{TXO}}$	TXEN at 2 V, See Figure 6	260	8000	ns
V <sub>OD(U)</sub> Driver output differential undershoot voltage	TXI	TXO, $\overline{\text{TXO}}$	TXEN at 2 V, See Figure 6		–100	mV
t <sub>sk</sub> Driver caused signal skew t <sub>PLH</sub> – t <sub>PHL</sub>	TXI	TXO, $\overline{\text{TXO}}$	TXEN at 2 V, See Figure 3		±3	ns
t <sub>r</sub> Rise time, TXO, $\overline{\text{TXO}}$			TXEN at 2 V, See Figure 3	1	5	ns
t <sub>f</sub> Fall time, TXO, $\overline{\text{TXO}}$			TXEN at 2 V, See Figure 3	1	5	ns

### receiver

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t <sub>PLH</sub> Propagation delay time, low-to-high level output	$\overline{\text{RXI}}$ , RXI	RXO	V <sub>IC</sub> = 1 V to 4.2 V, See Figure 10		15	ns
t <sub>PHL</sub> Propagation delay time, high-to-low level output	$\overline{\text{RXI}}$ , RXI	RXO	V <sub>IC</sub> = 1 V to 4.2 V, See Figure 10		15	ns
t <sub>PLH</sub> Start-up delay time, low-to-high level output	$\overline{\text{RXI}}$ , RXI	RXEN	V <sub>IC</sub> = 1 V to 4.2 V, V <sub>ID</sub> = –500 mV, See Figure 12		55	ns
t <sub>PHL</sub> Shutdown delay time, high-to-low level output	$\overline{\text{RXI}}$ , RXI	RXEN	V <sub>IC</sub> = 1 V to 4.2 V, V <sub>ID</sub> = 500 mV, See Figure 12	142	181	ns
t <sub>sk</sub> Receiver caused signal skew (t <sub>PLH</sub> – t <sub>PHL</sub> )	$\overline{\text{RXI}}$ , RXI	RXO	V <sub>IC</sub> = 1 V to 4.2 V, V <sub>ID</sub> = 500 mV, See Figure 10		±3	ns
t <sub>w</sub> Pulse duration at RXI and RXI (to not activate squelch)			V <sub>IC</sub> = 1 V to 4.2 V, V <sub>ID</sub> = –175 mV, See Figure 11	25		ns
t <sub>w</sub> Pulse duration at RXI and RXI (to activate squelch)			V <sub>IC</sub> = 1 V to 4.2 V, V <sub>ID</sub> = –275 mV, See Figure 11		50	ns
t <sub>r1</sub> Rise time, RXO			V <sub>IC</sub> = 1 V to 4.2 V, V <sub>ID</sub> = ±500 mV, See Figure 10	1	8	ns
t <sub>r2</sub> Rise time, RXEN			V <sub>IC</sub> = 1 V to 4.2 V, V <sub>ID</sub> = ±500 mV, See Figure 12	1	8	ns
t <sub>f1</sub> Fall time, RXO			V <sub>IC</sub> = 1 V to 4.2 V, V <sub>ID</sub> = ±500 mV, See Figure 10	1	8	ns
t <sub>f2</sub> Fall time, RXEN			V <sub>IC</sub> = 2.5 V, V <sub>ID</sub> = ±500 V, See Figure 12	1	8	ns
t <sub>v</sub> RXO valid after RXEN high			See Figure 10	–10	15	ns



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LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature

loop

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t <sub>PLH</sub> Propagation delay time, low-to-high level output	TXI	R XO	LOOP at 0.8 V, TXEN at 2 V, See Figure 13		30	ns
t <sub>PHL</sub> Propagation delay time, high-to-low level output	TXI	R XO	LOOP at 0.8 V, TXEN at 2 V, See Figure 13		30	ns
t <sub>PLH</sub> Propagation delay time, low-to-high level output	TXEN	R XEN	LOOP at 0.8 V, See Figure 14		50	ns
t <sub>PHL</sub> Propagation delay time, high-to-low level output	TXEN	R XEN	LOOP at 0.8 V, See Figure 14		50	ns

PARAMETER MEASUREMENT INFORMATION

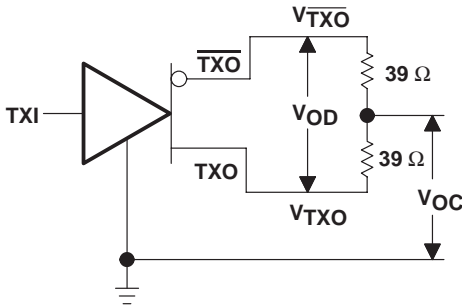


Figure 1. Driver Test Circuit

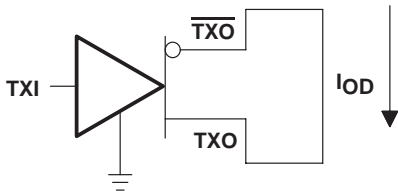
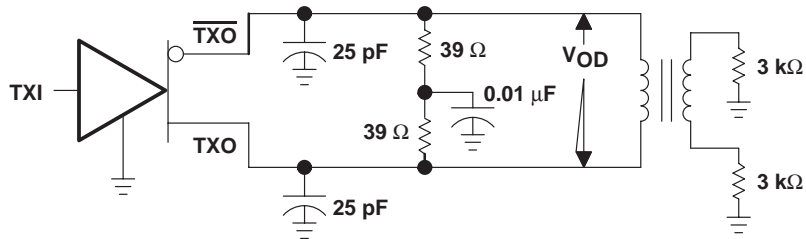
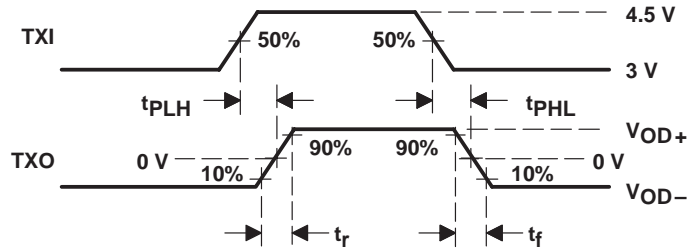


Figure 2. Driver Test Circuit

### PARAMETER MEASUREMENT INFORMATION



#### TEST CIRCUIT



#### VOLTAGE WAVEFORMS

#### TRANSFORMER SPECIFICATIONS

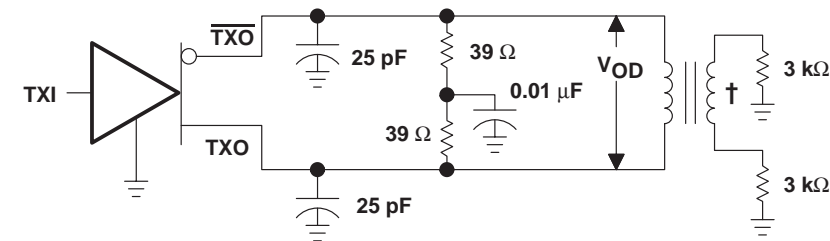
Turns Ratio	1:1
Magnetizing Inductance	26 to 30 $\mu$ H
Winding Resistance	0.6 $\Omega$ Max
Rise Time 10% to 90%	5 ns Max
Interwinding Capacitance	25 pF
Leakage Inductance	0.25 $\mu$ H Max
Inductive Q	1250 Min

**Figure 3. Test Circuit and Voltage Waveforms**

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LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

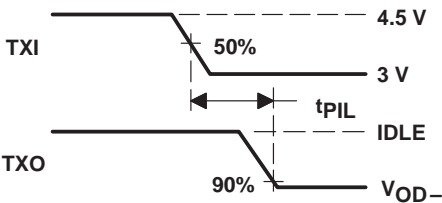
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PARAMETER MEASUREMENT INFORMATION



† See Figure 3

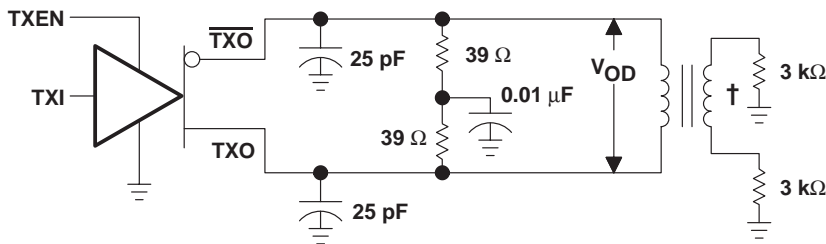
TEST CIRCUIT



VOLTAGE WAVEFORMS

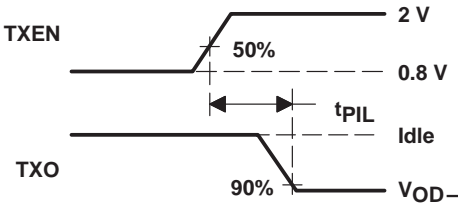
NOTE: Input  $t_r \leq 5$  ns;  $t_f \leq 5$  ns

Figure 4. Test Circuit and Voltage Waveforms



† See Figure 3

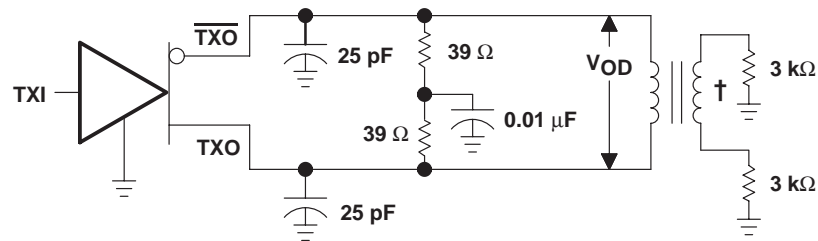
TEST CIRCUIT



VOLTAGE WAVEFORMS

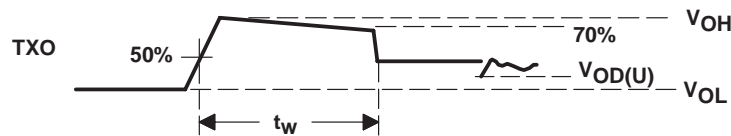
Figure 5. Test Circuit and Voltage Waveforms

## PARAMETER MEASUREMENT INFORMATION



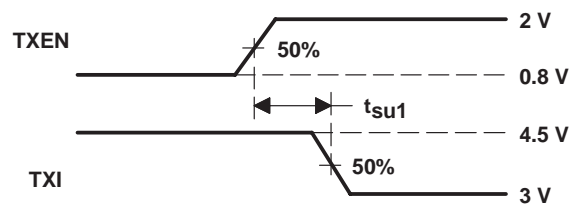
† See Figure 3

TEST CIRCUIT



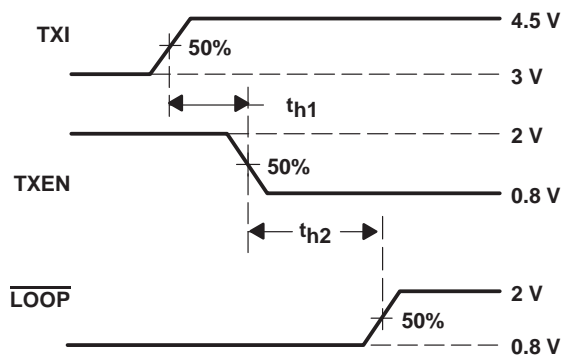
VOLTAGE WAVEFORMS

Figure 6. Test Circuit and Voltage Waveforms



NOTE: Input  $t_r \leq 5$  ns;  $t_f \leq 5$  ns

Figure 7



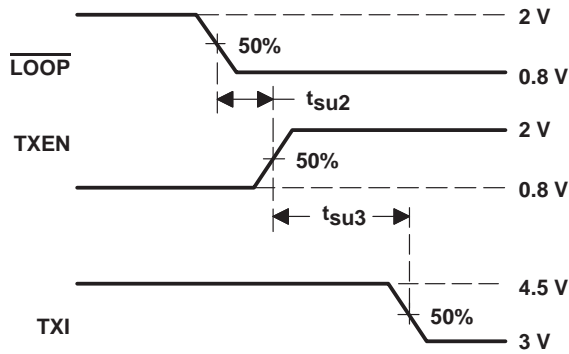
NOTE: Input  $t_r \leq 5$  ns;  $t_f \leq 5$  ns

Figure 8

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LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

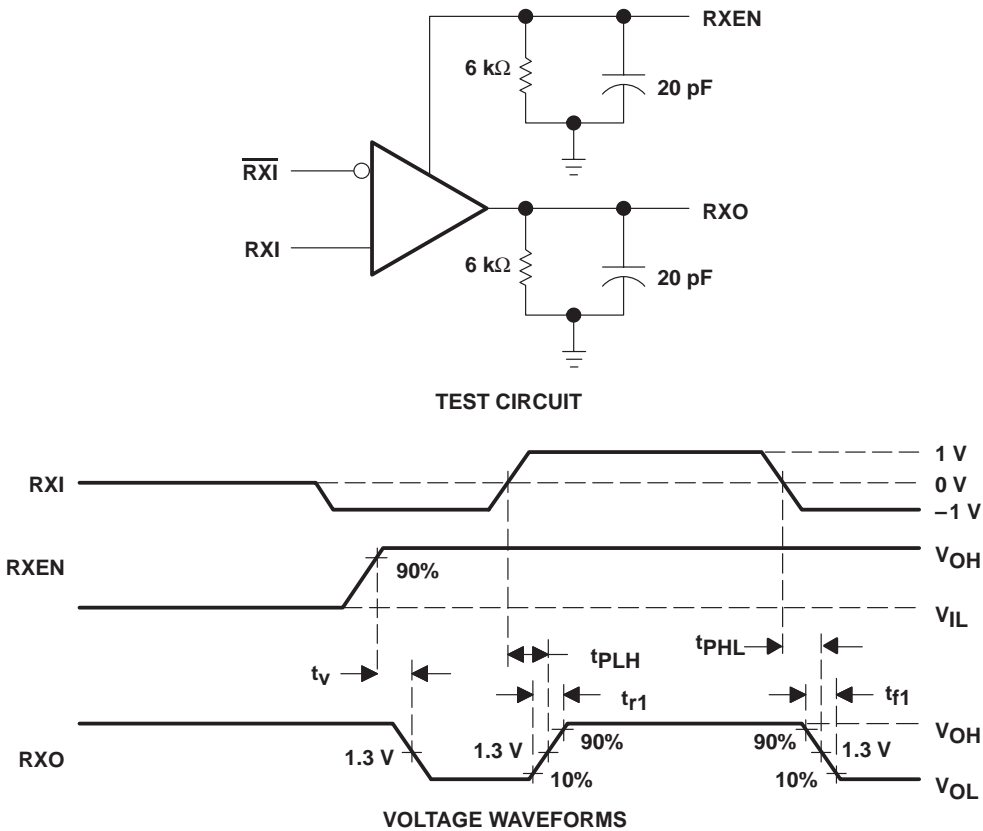
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PARAMETER MEASUREMENT INFORMATION



NOTE: Input  $t_r \leq 5 \text{ ns}$ ;  $t_f \leq 5 \text{ ns}$

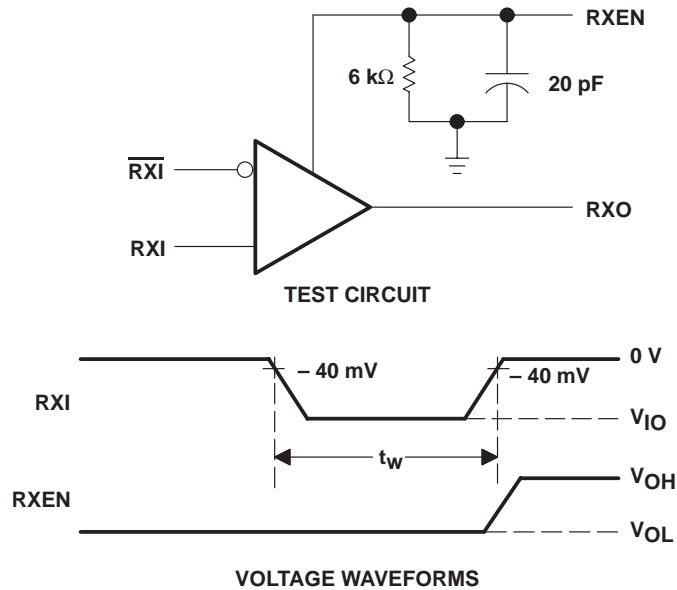
Figure 9



NOTE: Input  $t_r \leq 5 \text{ ns}$ ;  $t_f \leq 5 \text{ ns}$

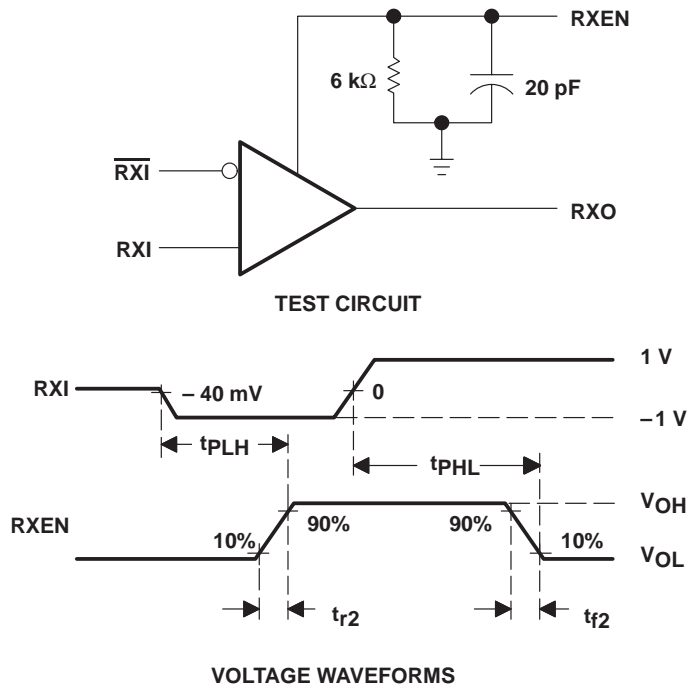
Figure 10. Test Circuit and Voltage Waveforms

## PARAMETER MEASUREMENT INFORMATION



NOTE: Input  $t_r \leq 5$  ns;  $t_f \leq 5$  ns

**Figure 11. Test Circuit and Voltage Waveforms**



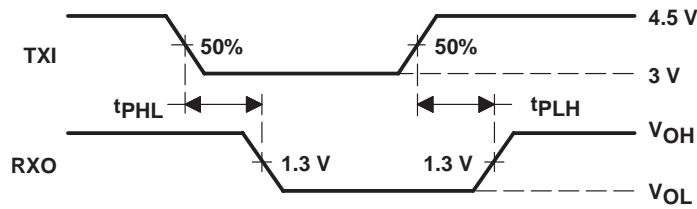
NOTE: Input  $t_r \leq 5$  ns;  $t_f \leq 5$  ns

**Figure 12. Test Circuit and Voltage Waveforms**

SN75ALS085  
LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

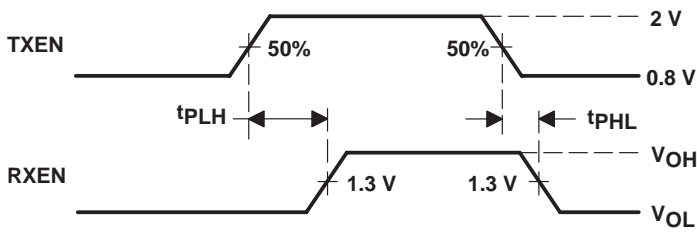
SLLS054B – APRIL 1989 – REVISED MAY 1995

PARAMETER MEASUREMENT INFORMATION



NOTE: Input  $t_r \leq 5$  ns;  $t_f \leq 5$  ns

Figure 13



NOTE: Input  $t_r \leq 5$  ns;  $t_f \leq 5$  ns

Figure 14



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