Data sheet acquired from Harris Semiconductor
SCHS271A

January 1997 - Revised October 1999

CD54FCT245, CD74FCT245

BiCMOS FCT Interface Logic, Octal-Bus Tranceivers, Three-State

Features

- **Buffered Inputs**
- **Typical Propagation Delay: 5.0ns at V_{CC} = 5V, T_A = 25^oC**
- **Noninverting**
- **SCR Latchup Resistant BiCMOS Process and Circuit Design**
- **Speed of Bipolar FAST™/AS/S**
- **64mA Output Sink Current (74 Series)**
- **48mA Output Sink Current (54 Series)**
- **Output Voltage Swing Limited to 3.7V at V_{CC} = 5V**
- **Controlled Output Edge Rates**
- **Input/Output Isolation to V_{CC}**
- **BiCMOS Technology with Low Quiescent Power**

Description

The CD54/74FCT245 octal bus transceiver uses a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48mA to 64mA.

The CD54/74FCT245 is a noninverting, three-state, bidirectional transceiver/buffer intended for two-way transmission from"A" bus to "B" bus or "B" bus to "A" bus. The logic level present on the Direction Input (DIR) determines the data direction. When the Output Enable input is HIGH, the outputs are in the high impedance state.

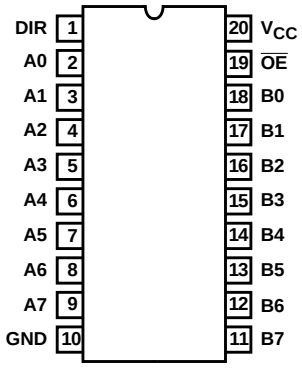
Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CD74FCT245E	0 to 70	20 Ld PDIP	E20.3
CD74FCT245M	0 to 70	20 Ld SOIC	M20.3
CD54FCT245E	-55 to 125	20 Ld PDIP	E20.3

NOTE: When ordering the suffix M and SM packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD54FCT245, CD74FCT245
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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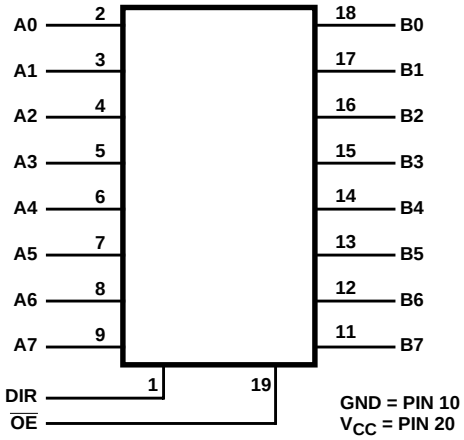
Functional Diagram



TRUTH TABLE (NOTE 1)

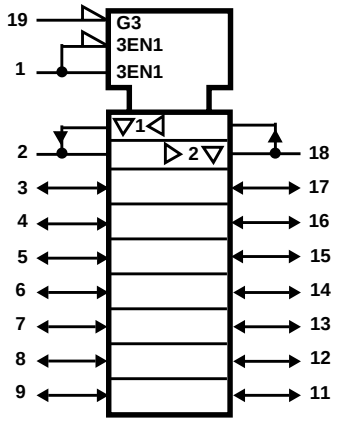
CONTROL INPUTS		
$\overline{OE}$	DIR	OPERATION
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

NOTES:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Irrelevant
2. To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1 MΩ resistors.

IEC Logic Symbol

CD74FCT245, CD54FCT245



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) . . . . . -0.5V to 6.0V
DC Input Diode Current, I_{IK} (for V_I < -0.5V) . . . . . -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) . . . . . -50mA
DC Output Sink Current per Output Pin, I_O 70mA
DC Output Source Current per Output Pin, I_O . . . . . -30mA
DC V_{CC} Current (I_{CC}) 140mA
DC Ground Current (I_{GND}) 528mA

Operating Conditions

Operating Temperature Range (T_A) . . . . . -55^oC to 125^oC
Supply Voltage Range, V_{CC}
CD74 Series, $T_A = 0^oC$ to 70^oC . . . . . 4.75V to 5.25V
CD54 Series, $T_A = -55^oC$ to 125^oC . . . . . 4.5V to 5.5V
DC Input Voltage, V_I . . . . . 0 to V_{CC}
DC Output Voltage, V_O . . . . . 0 to $\leq V_{CC}$
Input Rise and Fall Slew Rate, dt/dv . . . . . 0 to 10ns/V

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} ($^oC/W$)
PDIP Package	69
SOIC Package	58

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is calculated in accordance with JESD 51.

Electrical Specifications

74FCT Commercial Temperature Range 0^oC to 70^oC, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V
54FCT Extended Industrial Temperature Range -55^oC to 125^oC; V_{CC} Max = 5.5V, V_{CC} Min = 4.5V

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A)						UNITS
					25^oC		0^oC TO 70^oC		-55^oC TO 125^oC		
		V_I	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.5 to 5.5	2	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or	-15	Min	2.4	-	2.4	-	-	-	V
		V_{IL}	-12	Min	2.4	-	-	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or	64	Min	-	0.55	-	0.55	-	-	V
		V_{IL}	48	Min	-	0.55	-	-	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	-	-1	µA
Three-State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	-	-10	µA
Short Circuit Output Current (Note 4)	I_{OS}	V_{CC} or GND $V_O = 0$		Max	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 5)		Max	-	1.6	-	1.6	-	2	mA

NOTES:

4. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
5. Inputs that are not measured are at V_{CC} or GND.
6. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA Max at 70^oC.

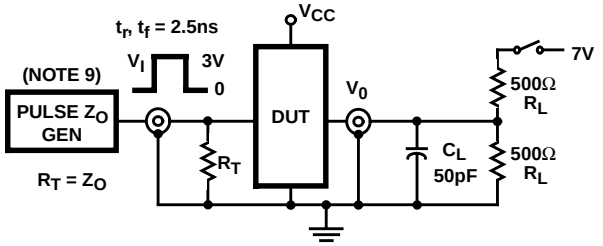
Switching Specifications t_r, t_f = 2.5ns, C_L = 50pF, R_L - See Figure 3

PARAMETER	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A)							UNITS
			25°C	0°C TO 70°C			-55°C TO 125°C			
			TYP	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delays Data to Outputs)	t_{PLH}, t_{PHL}	5	5	1.5	-	7	1.5	-	7.5	ns
Output Enable to Output	t_{PZL}, t_{PZH}	5	6	1.5	-	9.5	1.5	-	10	ns
Output Disable to Output	t_{PLZ}, t_{PHZ}	5	6	1.5	-	7.5	1.5	-	10	ns
Power Dissipation Capacitance	C_{PD}	-	49	-	49	-	-	49	-	pF
Min (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV}	5	0.5	-	-	-	-	-	-	V
Max (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP}	5	1	-	-	-	-	-	-	V
Input Capacitance	C_I	-	-	-	-	10	-	-	10	pF
Input/Output Capacitance	$C_{I/O}$	-	-	-	-	15	-	-	15	pF

NOTES:

7. 5V: Min is at 5.5V, Max is at 4.5V.
   5V: Min is at 5.25V for 0°C to 70°C, Max is at 4.75V for 0°C to 70°C, Typ is at 5V.
8. C_{PD}, measured per function, is used to determine the dynamic power consumption.
   P_D (per package) = V_{CC} I_{CC} + Σ (V_{CC}^2 f_I C_{PD} + V_O^2 f_O C_L + V_{CC} ΔI_{CC} D) where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_I = input frequency

Test Circuits and Waveforms



NOTE:

9. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

Input: $t_r = t_f$ = 2.5ns (10% to 90%), unless otherwise specified

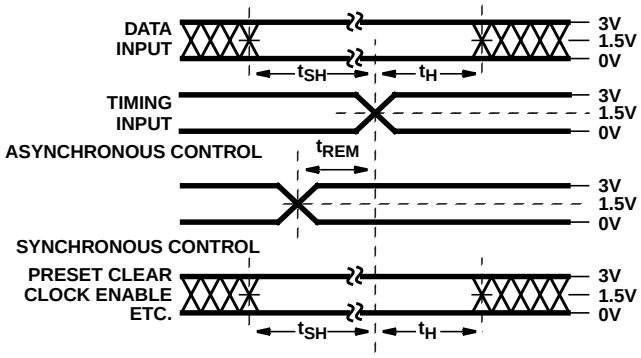


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

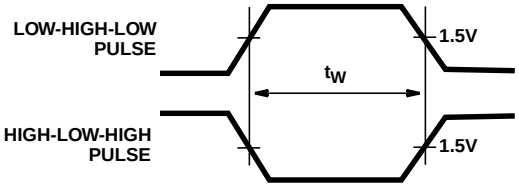


FIGURE 3. PULSE WIDTH

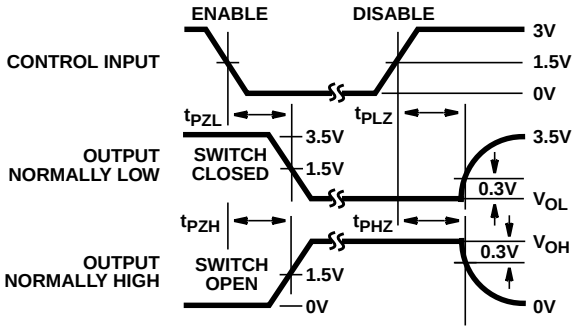


FIGURE 4. ENABLE AND DISABLE TIMING

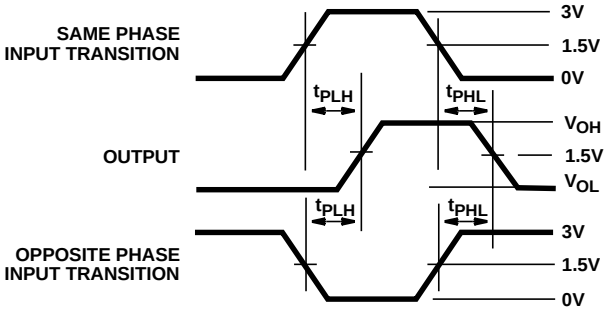
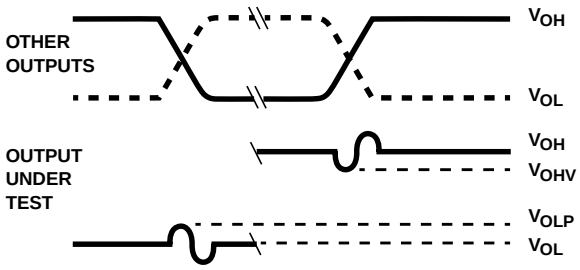


FIGURE 5. PROPAGATION DELAY

Test Circuits and Waveforms (Continued)



NOTES:

10. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
11. Input pulses have the following characteristics:
    $P_{RR} \leq 1MHz$, $t_r = 2.5ns$, $t_f = 2.5ns$, skew 1ns.
12. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

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