(1) 215201 links to page 210, offset is 161

(2)
   a) $2^{21}/2^{11}$ = 1024 entries
   b) $2^{16}/2^{11}$ = 32 entries

(3)
   a) $256 * 2^{12}$ = 1048576 bits for the logical address
   b) $64 * 2^{12}$ = 262144 bits for the physical address

(4)
   a) 430 + 219 = 649
   b) 10+2300 = 2310
   c) Bad Reference
   d) 1327+400=1727
   e) Bad Reference

(5)
   a) 0xE12C → x312C, (page 14, frame 3, rf bit 1)
      0x3A9D → xAA9d, (page 3, frame 10, rf bit 1)
      0xA9D9 → x59D9, (page 10, frame 5, rf bit 1)
      0x7001 → xF001, (page 7, frame 15, rf bit 1)
   b) 0xA9D9→x59D9, (page 10, frame 5, rf bit 1)
   c) LRU will choose any frame with reference bit 0, in other words, the least recently used bit.
      It can also select an unused frame that is free.

(6)

(7)
   a) FIFO
      A, b, g, a, d, e(page fault, a OUT, e IN)
      a (b OUT, a IN)
      b(g OUT, b IN)
      a, d, e, g(d OUT, g IN)
      d (e OUT, d IN)
      e (a OUT, e IN)
      10 page faults
   b) Second-chance FIFO (clock method)
      A, b, g, a, d, e(page fault, a OUT, e IN)
      a (b OUT, a IN)
      b(g OUT, b IN)
      a, d, e, g(d OUT, g IN)
      d(e OUT, d IN)
      e (a OUT, e IN)
      10 page faults
   c) LRU
      a, b, g, a, d, e(page fault, b OUT, e IN)
      a, b(page fault, g OUT, b IN)

a, d, e, g(page fault, b OUT, g IN)
d e
7 page faults
d) WS with τ = 2
A, b, g, a, d(b OUT, d IN)
e(g OUT, e IN)
a, b(d OUT, b IN)
a, d(e OUT, dIN)
e(b OUT e IN)
g(a OUT, g IN)
d, e
9 page faults