



# Extremely Accurate I<sup>2</sup>C-Integrated RTC/TCXO/Crystal

## ABSOLUTE MAXIMUM RATINGS

Voltage Range on V<sub>CC</sub>, V<sub>BAT</sub>, 32kHz, SCL, SDA,  $\overline{\text{RST}}$ ,  
 $\overline{\text{INT}}$ /SQW Relative to Ground .....-0.3V to +6.0V  
 Operating Temperature Range  
 (noncondensing) .....-40°C to +85°C  
 Junction Temperature .....+125°C

Storage Temperature Range .....-40°C to +85°C  
 Lead Temperature  
 (Soldering, 10s).....+260°C/10s  
 Soldering Temperature.....See the *Handling, PC Board Layout, and Assembly* section.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## RECOMMENDED DC OPERATING CONDITIONS

(T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V <sub>CC</sub>		2.3	3.3	5.5	V
	V <sub>BAT</sub>		2.3	3.0	5.5	V
Logic 1 Input SDA, SCL	V <sub>IH</sub>		0.7 x V <sub>CC</sub>		V <sub>CC</sub> + 0.3	V
Logic 0 Input SDA, SCL	V <sub>IL</sub>		-0.3		+0.3 x V <sub>CC</sub>	V
Pullup Voltage (SDA, SCL, 32kHz, $\overline{\text{INT}}$ /SQW)	V <sub>PU</sub>	V <sub>CC</sub> = 0V			5.5V	V

## ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 2.3V to 5.5V, V<sub>CC</sub> > V<sub>BAT</sub>, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.) (Typical values are at V<sub>CC</sub> = 3.3V, V<sub>BAT</sub> = 3.0V, and T<sub>A</sub> = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Active Supply Current	I <sub>CCA</sub>	(Notes 3, 4)	V <sub>CC</sub> = 3.63V			200	μA
			V <sub>CC</sub> = 5.5V			300	
Standby Supply Current	I <sub>CCS</sub>	I <sup>2</sup> C bus inactive, 32kHz output on, SQW output off (Note 4)	V <sub>CC</sub> = 3.63V			110	μA
			V <sub>CC</sub> = 5.5V			170	
Temperature Conversion Current	I <sub>CCSCONV</sub>	I <sup>2</sup> C bus inactive, 32kHz output on, SQW output off	V <sub>CC</sub> = 3.63V			575	μA
			V <sub>CC</sub> = 5.5V			650	
Power-Fail Voltage	V <sub>PF</sub>		2.45	2.575	2.70		V
Logic 0 Output, 32kHz, $\overline{\text{INT}}$ /SQW, SDA	V <sub>OL</sub>	I <sub>OL</sub> = 3mA			0.4		V
Logic 0 Output, $\overline{\text{RST}}$	V <sub>OL</sub>	I <sub>OL</sub> = 1mA			0.4		V
Output Leakage Current 32kHz, $\overline{\text{INT}}$ /SQW, SDA	I <sub>LO</sub>	Output high impedance	-1	0	+1		μA
Input Leakage SCL	I <sub>LI</sub>		-1		+1		μA
$\overline{\text{RST}}$ Pin I/O Leakage	I <sub>OL</sub>	$\overline{\text{RST}}$ high impedance (Note 5)	-200		+10		μA
V <sub>BAT</sub> Leakage Current (V <sub>CC</sub> Active)	I <sub>BATLKG</sub>			25	100		nA

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## ELECTRICAL CHARACTERISTICS (continued)

(V<sub>CC</sub> = 2.3V to 5.5V, V<sub>CC</sub> > V<sub>BAT</sub>, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.) (Typical values are at V<sub>CC</sub> = 3.3V, V<sub>BAT</sub> = 3.0V, and T<sub>A</sub> = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Frequency	f <sub>OUT</sub>	V <sub>CC</sub> = 3.3V or V <sub>BAT</sub> = 3.3V		32.768			kHz
Frequency Stability vs. Temperature (Commercial)	Δf/f <sub>OUT</sub>	V <sub>CC</sub> = 3.3V or V <sub>BAT</sub> = 3.3V, aging offset = 00h	0°C to +40°C		±2		ppm
			>40°C to +70°C		±3.5		
Frequency Stability vs. Temperature (Industrial)	Δf/f <sub>OUT</sub>	V <sub>CC</sub> = 3.3V or V <sub>BAT</sub> = 3.3V, aging offset = 00h	-40°C to <0°C		±3.5		ppm
			0°C to +40°C		±2		
			>40°C to +85°C		±3.5		
Frequency Stability vs. Voltage	Δf/V				1		ppm/V
Trim Register Frequency Sensitivity per LSB	Δf/LSB	Specified at:	-40°C		0.7		ppm
			+25°C		0.1		
			+70°C		0.4		
			+85°C		0.8		
Temperature Accuracy	Temp	V <sub>CC</sub> = 3.3V or V <sub>BAT</sub> = 3.3V		-3		+3	°C
Crystal Aging	Δf/f <sub>0</sub>	After reflow, not production tested	First year		±1.0		ppm
			0–10 years		±5.0		

## ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 0V, V<sub>BAT</sub> = 2.3V to 5.5V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Active Battery Current	I <sub>BATA</sub>	E <sub>OSC</sub> = 0, BBSQW = 0, SCL = 400kHz (Note 4)	V <sub>BAT</sub> = 3.63V			70	μA
			V <sub>BAT</sub> = 5.5V			150	
Timekeeping Battery Current	I <sub>BATT</sub>	E <sub>OSC</sub> = 0, BBSQW = 0, EN32kHz = 1, SCL = SDA = 0V or SCL = SDA = V <sub>BAT</sub> (Note 4)	V <sub>BAT</sub> = 3.63V		0.84	3.0	μA
			V <sub>BAT</sub> = 5.5V		1.0	3.5	
Temperature Conversion Current	I <sub>BATTC</sub>	E <sub>OSC</sub> = 0, BBSQW = 0, SCL = SDA = 0V or SCL = SDA = V <sub>BAT</sub>	V <sub>BAT</sub> = 3.63V			575	μA
			V <sub>BAT</sub> = 5.5V			650	
Data-Retention Current	I <sub>BATTDR</sub>	E <sub>OSC</sub> = 1, SCL = SDA = 0V, +25°C				100	nA

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## AC ELECTRICAL CHARACTERISTICS

(VCC = VCC(MIN) to VCC(MAX) or VBAT = VBAT(MIN) to VBAT(MAX), VBAT > VCC, TA = TMIN to TMAX, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	fSCL	Fast mode	100		400	kHz
		Standard mode	0		100	
Bus Free Time Between STOP and START Conditions	tBUF	Fast mode	1.3			μs
		Standard mode	4.7			
Hold Time (Repeated) START Condition (Note 6)	tHD:STA	Fast mode	0.6			μs
		Standard mode	4.0			
Low Period of SCL Clock	tLOW	Fast mode	1.3			μs
		Standard mode	4.7			
High Period of SCL Clock	tHIGH	Fast mode	0.6			μs
		Standard mode	4.0			
Data Hold Time (Notes 7, 8)	tHD:DAT	Fast mode	0		0.9	μs
		Standard mode	0		0.9	
Data Setup Time (Note 9)	tSU:DAT	Fast mode	100			ns
		Standard mode	250			
Start Setup Time	tSU:STA	Fast mode	0.6			μs
		Standard mode	4.7			
Rise Time of Both SDA and SCL Signals (Note 10)	tR	Fast mode	20 + $\frac{300}{0.1C_B}$		300	ns
		Standard mode	0.1C <sub>B</sub>		1000	
Fall Time of Both SDA and SCL Signals (Note 10)	tF	Fast mode	20 + $\frac{300}{0.1C_B}$		300	ns
		Standard mode	0.1C <sub>B</sub>		300	
Setup Time for STOP Condition	tSU:STO	Fast mode	0.6			μs
		Standard mode	4.7			
Capacitive Load for Each Bus Line (Note 10)	C <sub>B</sub>				400	pF
Capacitance for SDA, SCL	C <sub>I/O</sub>			10		pF
Pulse Width of Spikes That Must Be Suppressed by the Input Filter	tSP			30		ns
Pushbutton Debounce	PB <sub>DB</sub>			250		ms
Reset Active Time	tRST			250		ms
Oscillator Stop Flag (OSF) Delay	tOSF	(Note 11)		100		ms
Temperature Conversion Time	tCONV			125	200	ms

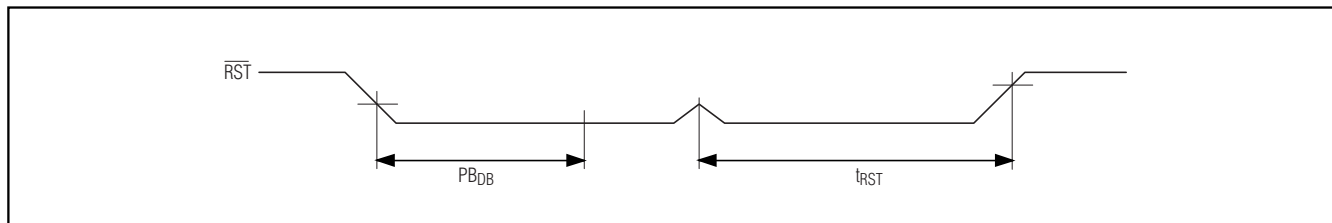
## POWER-SWITCH CHARACTERISTICS

(TA = TMIN to TMAX)

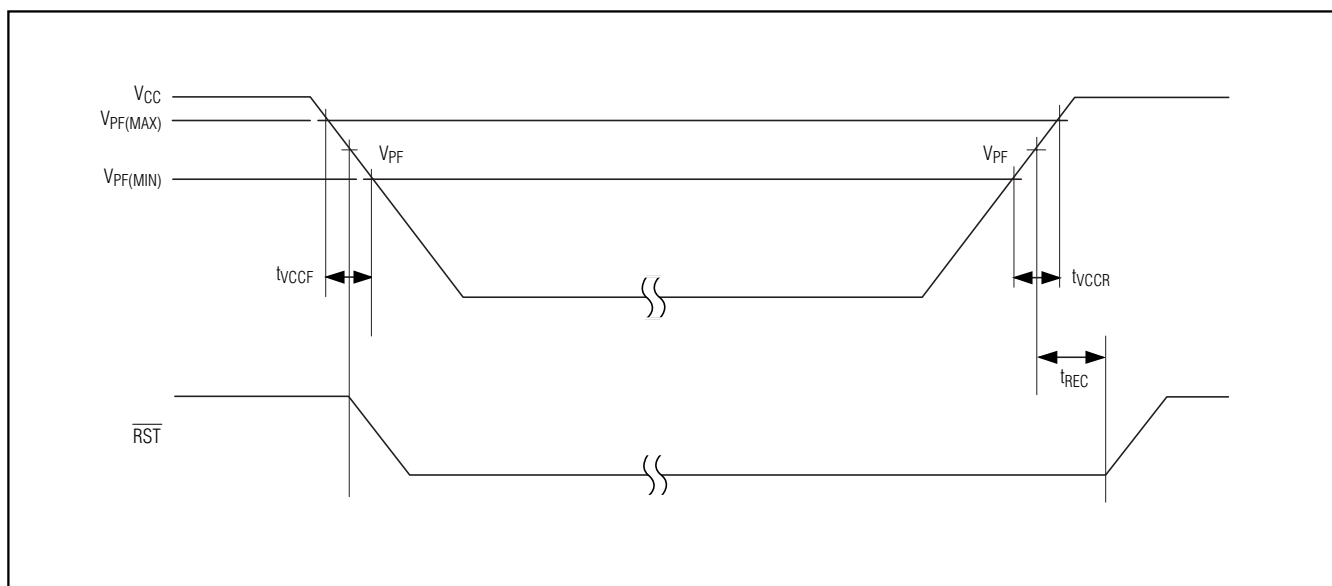
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VCC Fall Time; VPF(MAX) to VPF(MIN)	tVCCF		300			μs
VCC Rise Time; VPF(MIN) to VPF(MAX)	tVCCR		0			μs
Recovery at Power-Up	tREC	(Note 12)		250	300	ms

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## Pushbutton Reset Timing



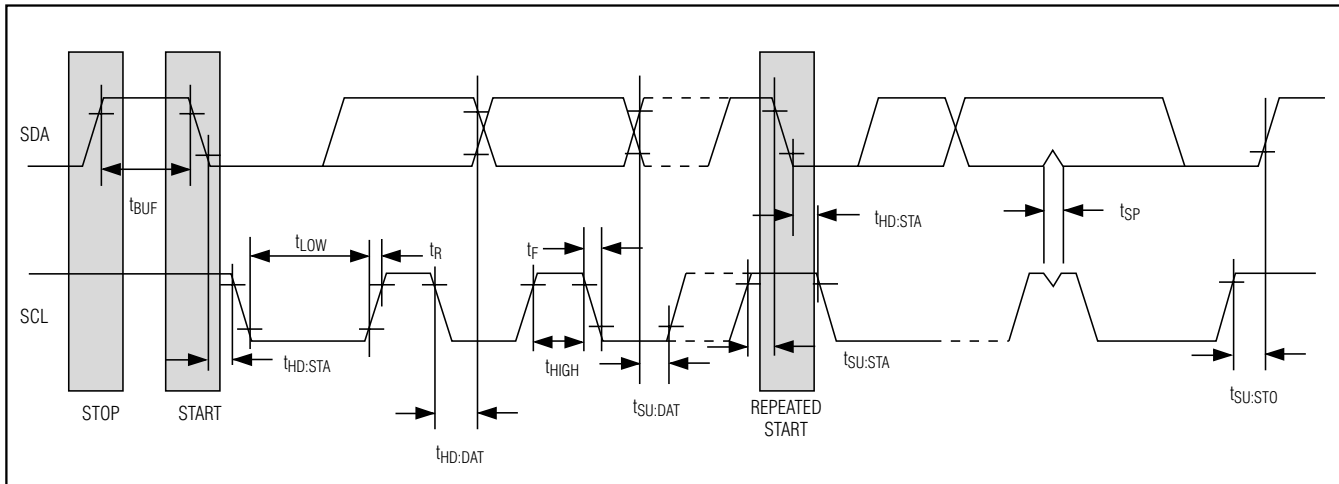
## Power-Switch Timing



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## Data Transfer on I<sup>2</sup>C Serial Bus



**Note 1:** Limits at -40°C are guaranteed by design and not production tested.

**Note 2:** All voltages are referenced to ground.

**Note 3:**  $I_{CCA}$ —SCL clocking at max frequency = 400kHz.

**Note 4:** Current is the averaged input current, which includes the temperature conversion current.

**Note 5:** The  $\overline{RST}$  pin has an internal 50k $\Omega$  (nominal) pullup resistor to  $V_{CC}$ .

**Note 6:** After this period, the first clock pulse is generated.

**Note 7:** A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the  $V_{IH(MIN)}$  of the SCL signal) to bridge the undefined region of the falling edge of SCL.

**Note 8:** The maximum  $t_{HD:DAT}$  needs only to be met if the device does not stretch the low period ( $t_{LOW}$ ) of the SCL signal.

**Note 9:** A fast-mode device can be used in a standard-mode system, but the requirement  $t_{SU:DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line  $t_R(MAX) + t_{SU:DAT} = 1000 + 250 = 1250$ ns before the SCL line is released.

**Note 10:**  $C_B$ —total capacitance of one bus line in pF.

**Note 11:** The parameter  $t_{OSF}$  is the period of time the oscillator must be stopped for the OSF flag to be set over the voltage range of  $0.0V \leq V_{CC} \leq V_{CC(MAX)}$  and  $2.3V \leq V_{BAT} \leq 3.4V$ .

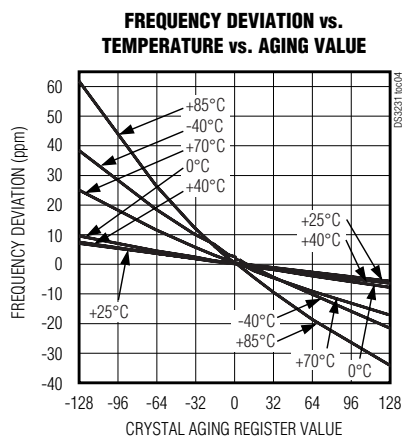
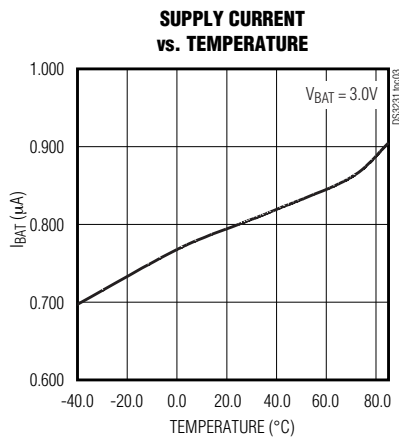
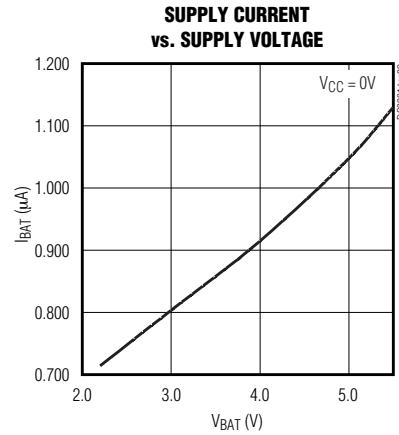
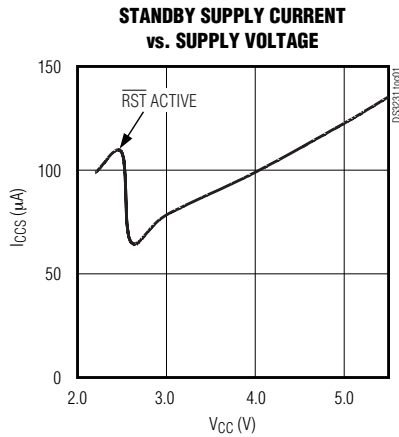
**Note 12:** This delay applies only if the oscillator is enabled and running. If the  $\overline{EOSC}$  bit is a 1, the startup time of the oscillator is added to this delay.

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## Typical Operating Characteristics

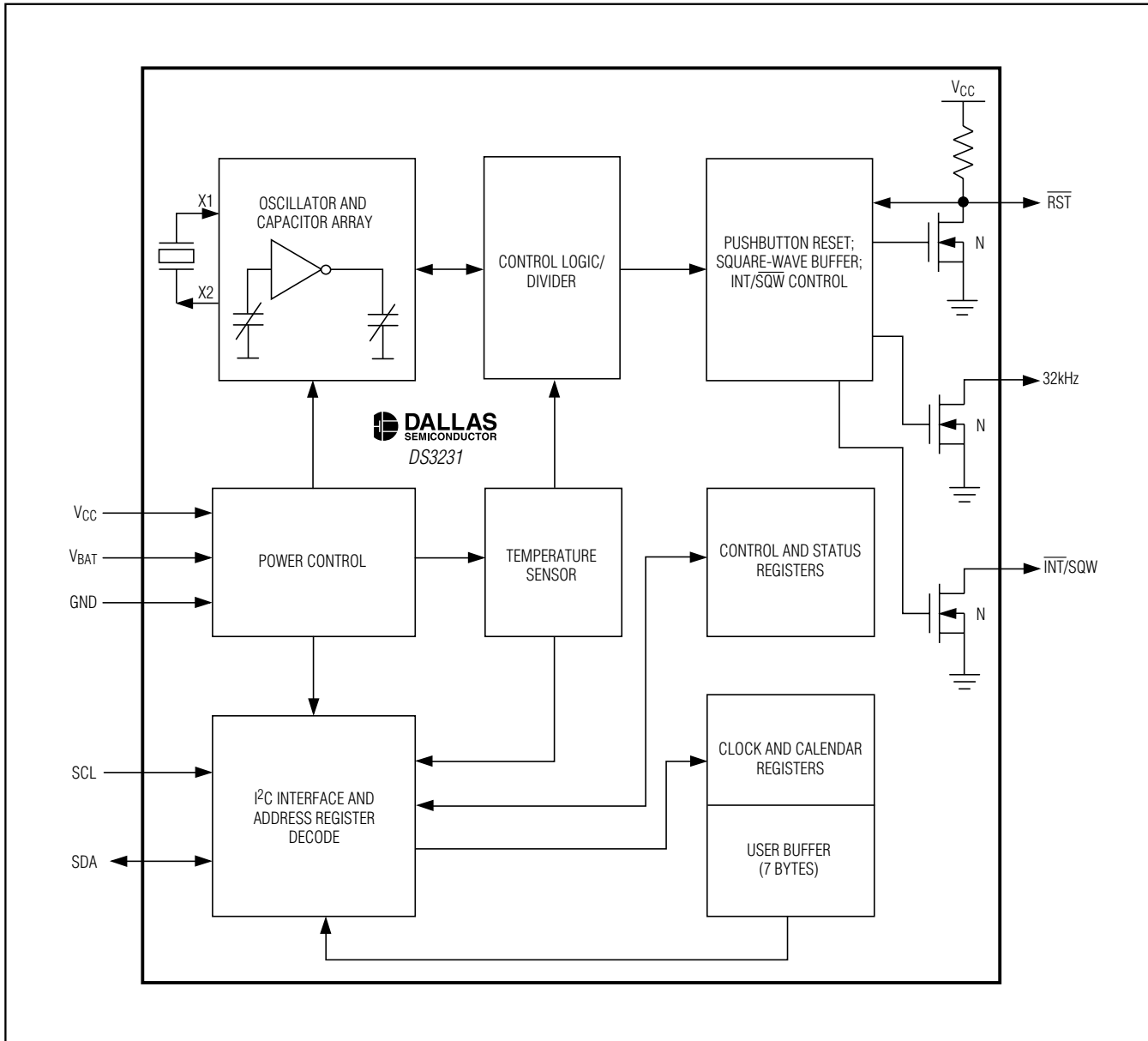
(V<sub>CC</sub> = +3.3V, T<sub>A</sub> = +25°C, unless otherwise noted.)

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## Block Diagram





# Extremely Accurate I<sup>2</sup>C-Integrated RTC/TCXO/Crystal

## Pin Description

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PIN	NAME	FUNCTION
1	32kHz	32kHz Output. This open-drain pin requires an external pullup resistor. It may be left open if not used.
2	V <sub>CC</sub>	DC Power Pin for Primary Power Supply. This pin should be decoupled using a 0.1μF to 1.0μF capacitor. If not used, connect to ground.
3	$\overline{\text{INT}}/\text{SQW}$	Active-Low Interrupt or Square-Wave Output. This open-drain pin requires an external pullup resistor. It may be left open if not used. This multifunction pin is determined by the state of the INTCN bit in the Control Register (0Eh). When INTCN is set to logic 0, this pin outputs a square wave and its frequency is determined by RS2 and RS1 bits. When INTCN is set to logic 1, then a match between the timekeeping registers and either of the alarm registers activates the $\overline{\text{INT}}/\text{SQW}$ pin (if the alarm is enabled). Because the INTCN bit is set to logic 1 when power is first applied, the pin defaults to an interrupt output with alarms disabled.
4	$\overline{\text{RST}}$	Active-Low Reset. This pin is an open-drain input/output. It indicates the status of V <sub>CC</sub> relative to the V <sub>PF</sub> specification. As V <sub>CC</sub> falls below V <sub>PF</sub> , the $\overline{\text{RST}}$ pin is driven low. When V <sub>CC</sub> exceeds V <sub>PF</sub> , for t <sub>RST</sub> , the $\overline{\text{RST}}$ pin is driven high impedance. The active-low, open-drain output is combined with a debounced pushbutton input function. This pin can be activated by a pushbutton reset request. It has an internal 50kΩ nominal value pullup resistor to V <sub>CC</sub> . No external pullup resistors should be connected. If the crystal oscillator is disabled, the startup time of the oscillator is added to the t <sub>RST</sub> delay.
5–12	N.C.	No Connection. Must be connected to ground.
13	GND	Ground
14	V <sub>BAT</sub>	Backup Power-Supply Input. This pin should be decoupled using a 0.1μF to 1.0μF low-leakage capacitor. If the I <sup>2</sup> C interface is inactive whenever the device is powered by the V <sub>BAT</sub> input, the decoupling capacitor is not required. If V <sub>BAT</sub> is not used, connect to ground. UL recognized to ensure against reverse charging when used with a lithium battery. Go to <a href="http://www.maxim-ic.com/qa/info/ul">www.maxim-ic.com/qa/info/ul</a> .
15	SDA	Serial Data Input/Output. This pin is the data input/output for the I <sup>2</sup> C serial interface. This open-drain pin requires an external pullup resistor.
16	SCL	Serial Clock Input. This pin is the clock input for the I <sup>2</sup> C serial interface and is used to synchronize data movement on the serial interface.

## Detailed Description

The DS3231 is a serial RTC driven by a temperature-compensated 32kHz crystal oscillator. The TCXO provides a stable and accurate reference clock, and maintains the RTC to within ±2 minutes per year accuracy from -40°C to +85°C. The TCXO frequency output is available at the 32kHz pin. The RTC is a low-power clock/calendar with two programmable time-of-day alarms and a programmable square-wave output. The  $\overline{\text{INT}}/\text{SQW}$  provides either an interrupt signal due to alarm conditions or a square-wave output. The clock/calendar provides seconds, minutes, hours, day, date,

month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. The internal registers are accessible through an I<sup>2</sup>C bus interface.

A temperature-compensated voltage reference and comparator circuit monitors the level of V<sub>CC</sub> to detect power failures and to automatically switch to the back-up supply when necessary. The  $\overline{\text{RST}}$  pin provides an external pushbutton function and acts as an indicator of a power-fail event.

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## Operation

The block diagram shows the main elements of the DS3231. The eight blocks can be grouped into four functional groups: TCXO, power control, pushbutton function, and RTC. Their operations are described separately in the following sections.

### 32kHz TCXO

The temperature sensor, oscillator, and control logic form the TCXO. The controller reads the output of the on-chip temperature sensor and uses a lookup table to determine the capacitance required, adds the aging correction in AGE register, and then sets the capacitance selection registers. New values, including changes to the AGE register, are loaded only when a change in the temperature value occurs, or when a user-initiated temperature conversion is completed. The temperature is read on initial application of VCC and once every 64 seconds afterwards.

### Power Control

This function is provided by a temperature-compensated voltage reference and a comparator circuit that monitors the VCC level. When VCC is greater than VPF, the part is powered by VCC. When VCC is less than VPF but greater than VBAT, the DS3231 is powered by VCC. If VCC is less than VPF and is less than VBAT, the device is powered by VBAT. See Table 1.

**Table 1. Power Control**

SUPPLY CONDITION	POWERED BY
$V_{CC} < V_{PF}$ , $V_{CC} < V_{BAT}$	VBAT
$V_{CC} < V_{PF}$ , $V_{CC} > V_{BAT}$	VCC
$V_{CC} > V_{PF}$ , $V_{CC} < V_{BAT}$	VCC
$V_{CC} > V_{PF}$ , $V_{CC} > V_{BAT}$	VCC

To preserve the battery, the first time VBAT is applied to the device, the oscillator will not start up until VCC is applied, or until a valid I<sup>2</sup>C address is written to the part. Typical oscillator startup time is less than one second. Approximately 2 seconds after VCC is applied, or a valid I<sup>2</sup>C address is written, the device makes a temperature measurement and applies the calculated correction to the oscillator. Once the oscillator is running, it continues to run as long as a valid power source is available (VCC or VBAT), and the device continues to measure the temperature and correct the oscillator frequency every 64 seconds.

## Pushbutton Reset Function

The DS3231 provides for a pushbutton switch to be connected to the  $\overline{RST}$  output pin. When the DS3231 is not in a reset cycle, it continuously monitors the  $\overline{RST}$  signal for a low going edge. If an edge transition is detected, the DS3231 debounces the switch by pulling the  $\overline{RST}$  low. After the internal timer has expired (PBDB), the DS3231 continues to monitor the  $\overline{RST}$  line. If the line is still low, the DS3231 continuously monitors the line looking for a rising edge. Upon detecting release, the DS3231 forces the  $\overline{RST}$  pin low and holds it low for  $t_{RST}$ .

The same pin,  $\overline{RST}$ , is used to indicate a power-fail condition. When VCC is lower than VPF, an internal power-fail signal is generated, which forces the  $\overline{RST}$  pin low. When VCC returns to a level above VPF, the  $\overline{RST}$  pin is held low for approximately 250ms ( $t_{REC}$ ) to allow the power supply to stabilize. If the oscillator is not running (see the *Power Control* section) when VCC is applied,  $t_{REC}$  is bypassed and  $\overline{RST}$  immediately goes high.

## Real-Time Clock

With the clock source from the TCXO, the RTC provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator.

The clock provides two programmable time-of-day alarms and a programmable square-wave output. The INT/SQW pin either generates an interrupt due to alarm condition or outputs a square-wave signal and the selection is controlled by the bit INTCN.

## Address Map

Figure 1 shows the address map for the DS3231 time-keeping registers. During a multibyte access, when the address pointer reaches the end of the register space (12h), it wraps around to location 00h. On an I<sup>2</sup>C START or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to reread the registers in case the main registers update during a read.

## I<sup>2</sup>C Interface

The I<sup>2</sup>C interface is accessible whenever either VCC or VBAT is at a valid level. If a microcontroller connected to the DS3231 resets because of a loss of VCC or other event, it is possible that the microcontroller and DS3231 I<sup>2</sup>C communications could become unsynchronized, e.g., the microcontroller resets while reading data from the DS3231. When the microcontroller resets, the

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Figure 1. Timekeeping Registers

ADDRESS	BIT 7 MSB	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 LSB	FUNCTION	RANGE
00H	0	10 Seconds			Seconds				Seconds	00–59
01H	0	10 Minutes			Minutes				Minutes	00–59
02H	0	12/24	AM/PM 10 Hour	10 Hour	Hour				Hours	1–12 + AM/PM 00–23
03H	0	0	0	0	0	Day			Day	1–7
04H	0	0	10 Date		Date				Date	00–31
05H	Century	0	0	10 Month	Month				Month/ Century	01–12 + Century
06H	10 Year				Year				Year	00–99
07H	A1M1	10 Seconds			Seconds				Alarm 1 Seconds	00–59
08H	A1M2	10 Minutes			Minutes				Alarm 1 Minutes	00–59
09H	A1M3	12/24	AM/PM 10 Hour	10 Hour	Hour				Alarm 1 Hours	1–12 + AM/PM 00–23
0AH	A1M4	DY/DT	10 Date		Day				Alarm 1 Day	1–7
					Date				Alarm 1 Date	1–31
0BH	A2M2	10 Minutes			Minutes				Alarm 2 Minutes	00–59
0CH	A2M3	12/24	AM/PM 10 Hour	10 Hour	Hour				Alarm 2 Hours	1–12 + AM/PM 00–23
0DH	A2M4	DY/DT	10 Date		Day				Alarm 2 Day	1–7
					Date				Alarm 2 Date	1–31
0EH	EOSC	BBSQW	CONV	RS2	RS1	INTCN	A2IE	A1IE	Control	—
0FH	OSF	0	0	0	EN32kHz	BSY	A2F	A1F	Control/Status	—
10H	SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA	Aging Offset	—
11H	SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA	MSB of Temp	—
12H	DATA	DATA	0	0	0	0	0	0	LSB of Temp	—

**Note:** Unless otherwise specified, the registers' state is not defined when power is first applied.

DS3231 I<sup>2</sup>C interface may be placed into a known state by toggling SCL until SDA is observed to be at a high level. At that point the microcontroller should pull SDA low while SCL is high, generating a START condition.

## Clock and Calendar

The time and calendar information is obtained by reading the appropriate register bytes. Figure 1 illustrates the RTC registers. The time and calendar data are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format. The DS3231 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic-high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23

hours). The century bit (bit 7 of the month register) is toggled when the years register overflows from 99 to 00.

The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any START and when the register pointer rolls over to zero. The time information is read from these secondary registers, while the clock continues to run. This eliminates the need to reread the registers in case the main registers update during a read.

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The countdown chain is reset whenever the seconds register is written. Write transfers occur on the acknowledge from the DS3231. Once the countdown chain is reset, to avoid rollover issues the remaining time and date registers must be written within 1 second. The 1Hz square-wave output, if enabled, transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

## Alarms

The DS3231 contains two time-of-day/date alarms. Alarm 1 can be set by writing to registers 07h to 0Ah. Alarm 2 can be set by writing to registers 0Bh to 0Dh. The alarms can be programmed (by the alarm enable and INTCN bits of the control register) to activate the INT/SQW output on an alarm match condition. Bit 7 of each of the time-of-day/date alarm registers are mask bits (Table 2). When all the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers match the corresponding values

stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 2 shows the possible settings. Configurations not listed in the table will result in illogical operation.

The DY/DT̄ bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0 to 5 of that register reflects the day of the week or the date of the month. If DY/DT̄ is written to logic 0, the alarm will be the result of a match with date of the month. If DY/DT̄ is written to logic 1, the alarm will be the result of a match with day of the week.

When the RTC register values match alarm register settings, the corresponding Alarm Flag 'A1F' or 'A2F' bit is set to logic 1. If the corresponding Alarm Interrupt Enable 'A1IE' or 'A2IE' is also set to logic 1 and the INTCN bit is set to logic 1, the alarm condition will activate the INT/SQW signal. The match is tested on the once-per-second update of the time and date registers.

**Table 2. Alarm Mask Bits**

DY/DT̄	ALARM 1 REGISTER MASK BITS (BIT 7)				ALARM RATE
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match
DY/DT̄	ALARM 2 REGISTER MASK BITS (BIT 7)			ALARM RATE	
	A2M4	A2M3	A2M2		
X	1	1	1	Alarm once per minute (00 seconds of every minute)	
X	1	1	0	Alarm when minutes match	
X	1	0	0	Alarm when hours and minutes match	
0	0	0	0	Alarm when date, hours, and minutes match	
1	0	0	0	Alarm when day, hours, and minutes match	

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## Control Register (0Eh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{\text{EOSC}}$	BBSQW	CONV	RS2	RS1	INTCN	A2IE	A1IE

## Special-Purpose Registers

The DS3231 has two additional registers (control and status) that control the real-time clock, alarms, and square-wave output.

### Control Register (0Eh)

**Bit 7: Enable Oscillator ( $\overline{\text{EOSC}}$ ).** When set to logic 0, the oscillator is started. When set to logic 1, the oscillator is stopped when the DS3231 switches to V<sub>BAT</sub>. This bit is clear (logic 0) when power is first applied. When the DS3231 is powered by V<sub>CC</sub>, the oscillator is always on regardless of the status of the  $\overline{\text{EOSC}}$  bit.

**Bit 6: Battery-Backed Square-Wave Enable (BBSQW).** When set to logic 1 and the DS3231 is being powered by the V<sub>BAT</sub> pin, this bit enables the square-wave output when V<sub>CC</sub> is absent. When BBSQW is logic 0, the  $\overline{\text{INT/SQW}}$  pin goes high impedance when V<sub>CC</sub> falls below the power-fail trip point. This bit is disabled (logic 0) when power is first applied.

**Bit 5: Convert Temperature (CONV).** Setting this bit to 1 forces the temperature sensor to convert the temperature into digital code and execute the TCXO algorithm to update the capacitance array to the oscillator. This can only happen during the idle period. The status bit, BSY, prevents the bit from being set when BSY = 1. The user should check the status bit BSY before forcing the controller to start a new TCXO execution. A user-initiated temperature conversion does not affect the internal 64-second update cycle.

A user-initiated temperature conversion does not affect the BSY bit for approximately 2ms. The CONV bit remains at a 1 from the time it is written until the conversion is finished, at which time both CONV and BSY go to 0. The CONV bit should be used when monitoring the status of a user-initiated conversion.

**Bits 4 and 3: Rate Select (RS2 and RS1).** These bits control the frequency of the square-wave output when the square wave has been enabled. The following table shows the square-wave frequencies that can be selected with the RS bits. These bits are both set to logic 1 (8.192kHz) when power is first applied.

### SQUARE-WAVE OUTPUT FREQUENCY

RS2	RS1	SQUARE-WAVE OUTPUT FREQUENCY
0	0	1Hz
0	1	1.024kHz
1	0	4.096kHz
1	1	8.192kHz

**Bit 2: Interrupt Control (INTCN).** This bit controls the  $\overline{\text{INT/SQW}}$  signal. When the INTCN bit is set to logic 0, a square wave is output on the  $\overline{\text{INT/SQW}}$  pin. When the INTCN bit is set to logic 1, then a match between the timekeeping registers and either of the alarm registers activates the  $\overline{\text{INT/SQW}}$  (if the alarm is also enabled). The corresponding alarm flag is always set regardless of the state of the INTCN bit. The INTCN bit is set to logic 1 when power is first applied.

**Bit 1: Alarm 2 Interrupt Enable (A2IE).** When set to logic 1, this bit permits the alarm 2 flag (A2F) bit in the status register to assert  $\overline{\text{INT/SQW}}$  (when INTCN = 1). When the A2IE bit is set to logic 0 or INTCN is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

**Bit 0: Alarm 1 Interrupt Enable (A1IE).** When set to logic 1, this bit permits the alarm 1 flag (A1F) bit in the status register to assert  $\overline{\text{INT/SQW}}$  (when INTCN = 1). When the A1IE bit is set to logic 0 or INTCN is set to logic 0, the A1F bit does not initiate the  $\overline{\text{INT/SQW}}$  signal. The A1IE bit is disabled (logic 0) when power is first applied.

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## Status Register (0Fh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OSF	0	0	0	EN32kHz	BSY	A2F	A1F

### Status Register (0Fh)

**Bit 7: Oscillator Stop Flag (OSF).** A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period and may be used to judge the validity of the timekeeping data. This bit is set to logic 1 any time that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

- 1) The first time power is applied.
- 2) The voltages present on both VCC and VBAT are insufficient to support oscillation.
- 3) The E<sub>OSC</sub> bit is turned off in battery-backed mode.
- 4) External influences on the crystal (i.e., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0.

**Bit 3: Enable 32kHz Output (EN32kHz).** This bit indicates the status of the 32kHz pin. When set to logic 1, the 32kHz pin is enabled and outputs a 32.768kHz square-wave signal. When set to logic 0, the 32kHz pin goes to a high-impedance state. The initial power-up state of this bit is logic 1, and a 32.768kHz square-wave signal appears at the 32kHz pin after a power source is applied to the DS3231 (if the oscillator is running).

**Bit 2: Busy (BSY).** This bit indicates the device is busy executing TCXO functions. It goes to logic 1 when the conversion signal to the temperature sensor is asserted and then is cleared when the device is in the 1-minute idle state.

**Bit 1: Alarm 2 Flag (A2F).** A logic 1 in the alarm 2 flag bit indicates that the time matched the alarm 2 registers. If the A2IE bit is logic 1 and the INTCN bit is set to logic 1, the INT/SQW pin is also asserted. A2F is

cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

**Bit 0: Alarm 1 Flag (A1F).** A logic 1 in the alarm 1 flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit is logic 1 and the INTCN bit is set to logic 1, the INT/SQW pin is also asserted. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

## Crystal Aging

The crystal aging offset register provides an 8-bit code to add to the codes in the capacitance array registers. The code is encoded in two's complement. One LSB represents one small capacitor to be switched in or out of the capacitance array at the crystal pins. The offset register is added to the capacitance array register under the following conditions: during a normal temperature conversion, if the temperature changes from the previous conversion, or during a manual user conversion (setting the CONV bit). To see the effects of the aging register on the 32kHz output frequency immediately, a manual conversion should be started after each aging register change.

Positive aging values add capacitance to the array, slowing the oscillator frequency. Negative values remove capacitance from the array, increasing the oscillator frequency.

The change in ppm per LSB is different at different temperatures. The frequency vs. temperature curve is shifted by the values used in this register. At +25°C, one LSB typically provides about 0.1ppm change in frequency.

## Crystal Aging Offset (10h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Sign	Data	Data	Data	Data	Data	Data	Data

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## Temperature Register (Upper Byte) (11h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Sign	Data	Data	Data	Data	Data	Data	Data

## Temperature Register (Lower Byte) (12h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Data	Data	0	0	0	0	0	0

### Temperature Registers (11h–12h)

Temperature is represented as a 10-bit code with a resolution of +0.25°C and is accessible at location 11h and 12h. The temperature is encoded in two's complement format. The upper 8 bits are at location 11h and the lower 2 bits are in the upper nibble at location 12h. Upon power reset, the registers are set to a default temperature of 0°C and the controller starts a temperature conversion. New temperature readings are stored in this register.

### I<sup>2</sup>C Serial Data Bus

The DS3231 supports a bidirectional I<sup>2</sup>C bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data is defined as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS3231 operates as a slave on the I<sup>2</sup>C bus. Connections to the bus are made through the SCL input and open-drain SDA I/O lines. Within the bus specifications, a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The DS3231 works in both modes.

The following bus protocol has been defined (Figure 2):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

**Bus not busy:** Both data and clock lines remain high.

**Start data transfer:** A change in the state of the data line from high to low, while the clock line is high, defines a START condition.

**Stop data transfer:** A change in the state of the data line from low to high, while the clock line is high, defines a STOP condition.

**Data valid:** The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and the STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

**Acknowledge:** Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition.

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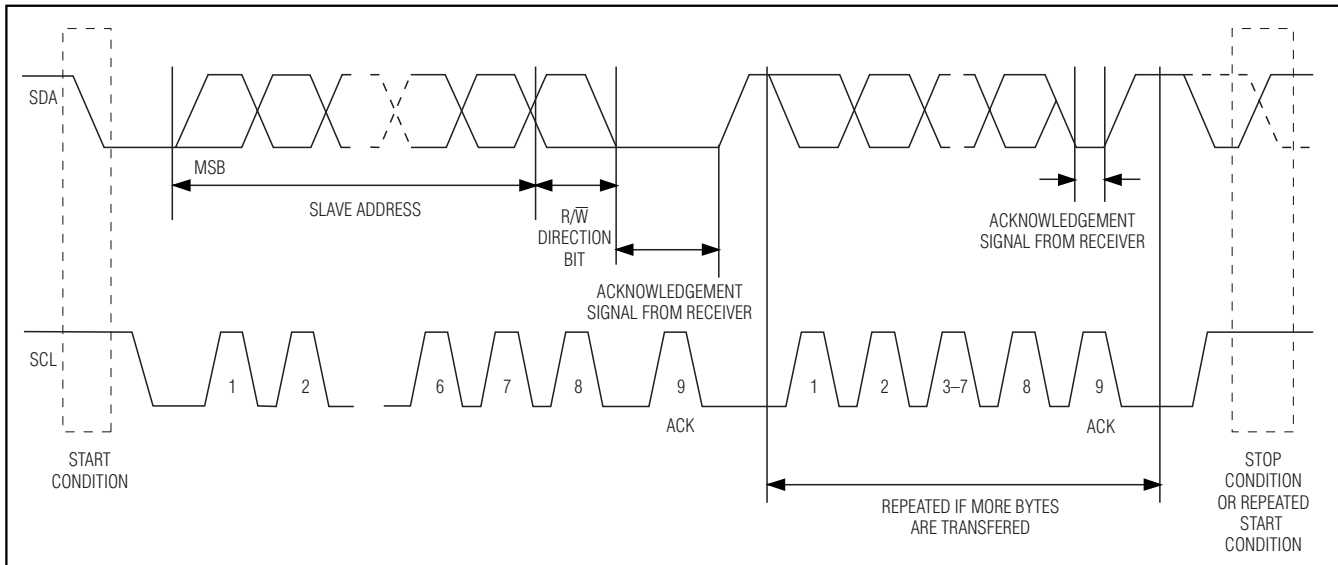


Figure 2. I<sup>2</sup>C Data Transfer Overview

Figures 3 and 4 detail how data transfer is accomplished on the I<sup>2</sup>C bus. Depending upon the state of the R/W bit, two types of data transfer are possible:

**Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

**Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not acknowledge is returned.

The master device generates all the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released. Data is transferred with the most significant bit (MSB) first.

The DS3231 can operate in the following two modes:

**Slave receiver mode (DS3231 write mode):** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer.

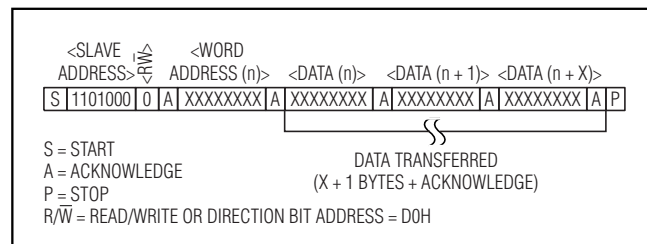


Figure 3. Slave Receiver Mode (Write Mode)

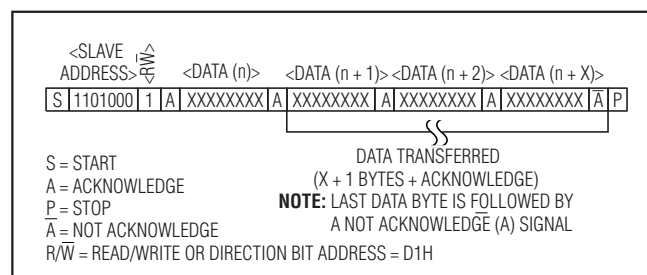


Figure 4. Slave Transmitter Mode (Read Mode)

Address recognition is performed by hardware after reception of the slave address and direction bit. The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit DS3231 address, which is 1101000, followed by the direction bit (R/W), which is 0 for a write. After receiving and decoding the slave address byte, the DS3231 outputs an



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acknowledge on SDA. After the DS3231 acknowledges the slave address + write bit, the master transmits a word address to the DS3231. This sets the register pointer on the DS3231, with the DS3231 acknowledging the transfer. The master may then transmit zero or more bytes of data, with the DS3231 acknowledging each byte received. The register pointer increments after each data byte is transferred. The master generates a STOP condition to terminate the data write.

**Slave transmitter mode (DS3231 read mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DS3231 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit. The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit DS3231 address, which is 1101000, followed by the direction bit ( $R/\overline{W}$ ), which is 1 for a read. After receiving and decoding the slave address byte, the DS3231 outputs an acknowledge on SDA. The DS3231 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode, the first address that is read is the last one stored in the register pointer. The DS3231 must receive a not acknowledge to end a read.

## **Handling, PC Board Layout, and Assembly**

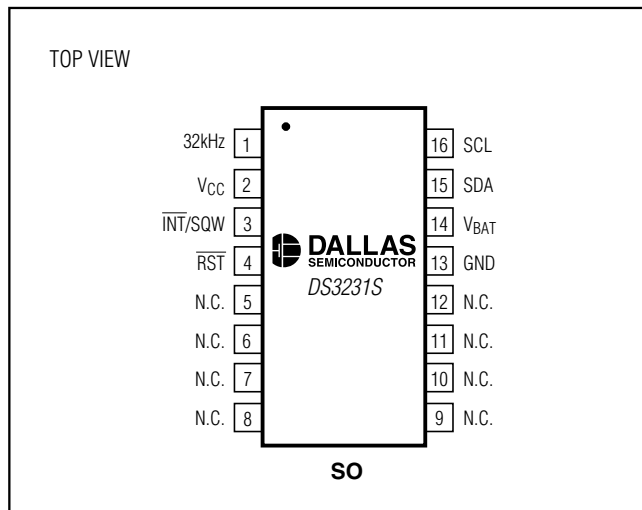
The DS3231 package contains a quartz tuning-fork crystal. Pick-and-place equipment can be used, but precautions should be taken to ensure that excessive shocks are avoided. Ultrasonic cleaning should be avoided to prevent damage to the crystal.

Avoid running signal traces under the package, unless a ground plane is placed between the package and the signal line. All N.C. (no connect) pins must be connected to ground.

Moisture-sensitive packages are shipped from the factory dry packed. Handling instructions listed on the package label must be followed to prevent damage during reflow. See IPC/JEDEC J-STD-020 standard for moisture-sensitive device (MSD) classifications and reflow profiles. Exposure to reflow is limited to 2 times maximum.

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## Pin Configuration



## Chip Information

TRANSISTOR COUNT: 33,000

SUBSTRATE CONNECTED TO GROUND

PROCESS: CMOS

## Thermal Information

Theta-JA: +73°C/W

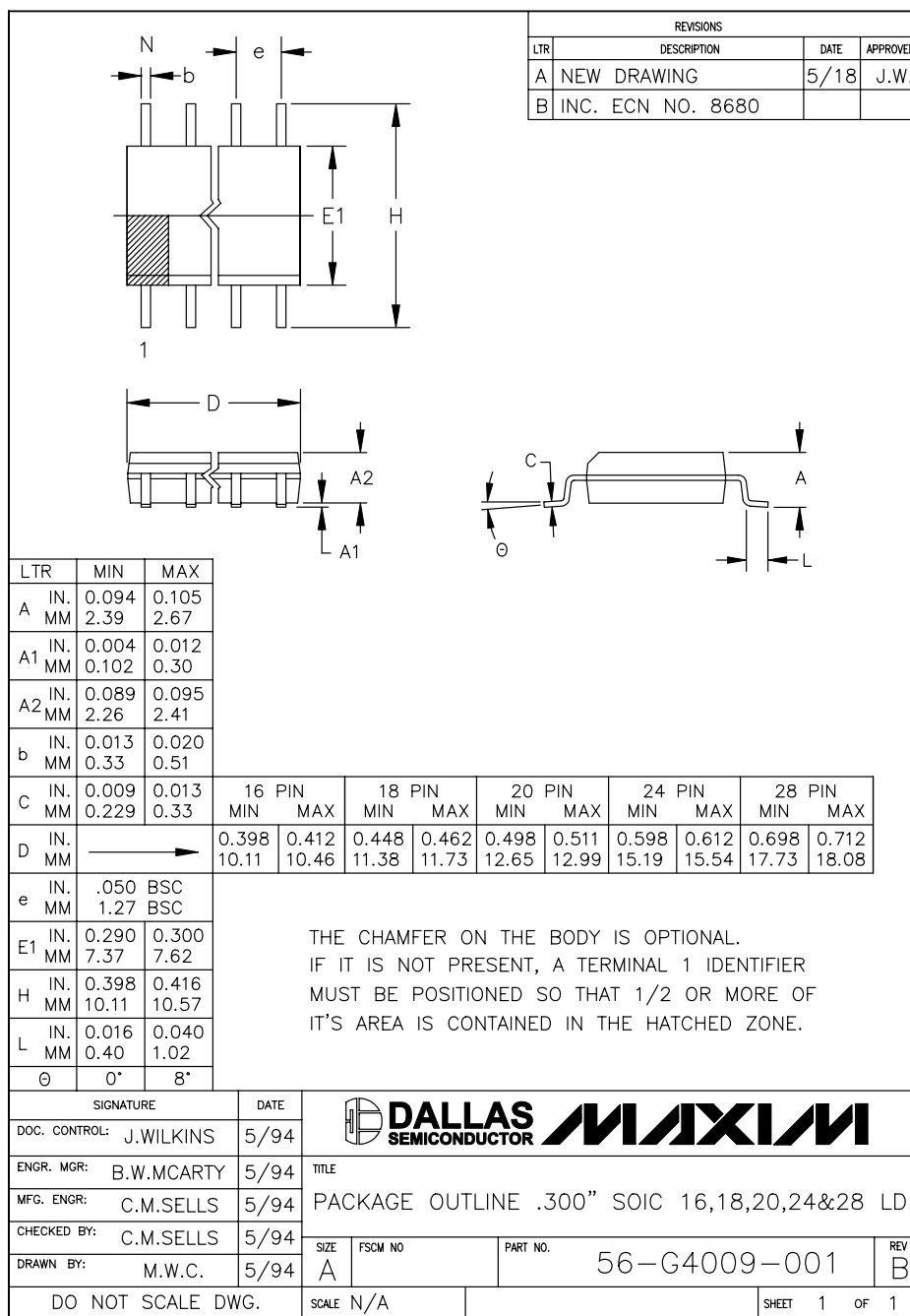
Theta-JC: +23°C/W

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## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/DallasPackInfo](http://www.maxim-ic.com/DallasPackInfo)).

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