Lantao Wang

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Education

2015/10-Present   Technical University of Munich   Electrical Engineering and Information Technology

- Candidate for Master of Science, 3rd semester
- GPA: Overall GPA of 1.5
- Courses relevant to this internship:

  System on Chip Technologies, System on Chip Platforms, SystemC Laboratory, VHDL System Design Laboratory, Project Laboratory IC Design, HW/SW Codesign

2015/07-2010/09   Tongji University, Shanghai, China   Electronic Science and Technology

- Received Bachelor degree
- GPA: Overall GPA of 4.2/5.0, corresponding to 1.8 in German grade system.

Skills

- Technologies: VHDL, C/C++, SystemC, Matlab, Cadence Virtuoso, Python
- Language: Fluent in English and German, basic Japanese, native Mandarin
- Others: LaTeX, Microsoft office

Relevant Projects

- **2016 SystemC Laboratory**

  Modeling communication on signal level, via sc_interface and eventually in the TLM 2.0 standard

  Exploration of a Network Processor Architecture

- **2016 Project Laboratory IC Design (Teamwork)**

  Implementation of a Clock by using Zynq-7000 FPGA with variable functions

  In charge of the design of Alarm clock module

- **2016 HW/SW Codesign (Course Project)**

  Sobel Edge Detection using C and VHDL on Zedboard

  Comparison between hardware and software implementations

- **2015 VDHL System Design Laboratory**

  Implementation of IDEA Algorithm

Awards

- **2014/10** Study scholarship of Tongji University (First Class)
- **2014/10** Volkswagen scholarship
- **2012/10** Study scholarship of Tongji University (Second Class)