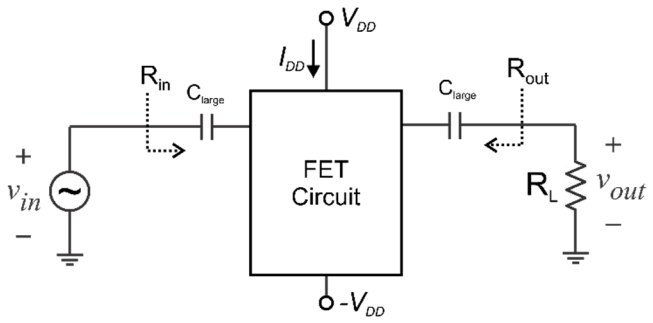
ECE3114 E.C. Design Project 4: FET Common Gate Amplifier Spring 2025

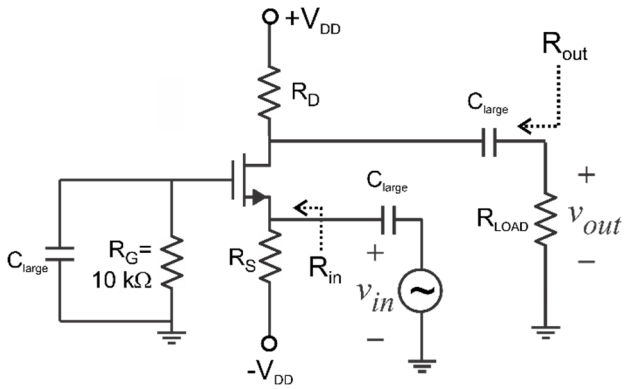
Design a single stage FET small signal amplifier that is connected in a **Common-Gate** configuration. The amplifier must meet the following specifications. ***This is an individual effort; similar designs will not be graded.*** Submit one complete document (PDF), points will be deducted if multiple files are submitted.

SPECIFICATIONS:

- Transistor: IRF840 NMOS FET, kn **= 6.5 A/V^2**, V_{TN} **= +3.85 V**, r_0 **= large**.
- **Dual** DC voltage supply, $|V_{DD}| \leq$ **+50 V** (you choose the +/- voltage)
- Load Resistor, R_L **= last two digits** of your student ID (N#). If this resistor is less than 20 ohms, add 20 ohms to your number. Your load resistor will fall in the range of $20\ \Omega \leq R_L \leq 119\ \Omega$.
- Resistor-only DC biasing (no DC current sources allowed)
- All coupling and bypass capacitors = Large
- All resistors <= 500kΩ
- Small signal voltage gain (magnitude), $|A_V| = \left|\frac{v_{out}}{v_{in}}\right| = \mathbf{10\ \pm 10\%}$.
- Design for a DC Power Dissipation for transistor to be below P_D **< 12.5 Watt (10% of maximum rated specification)**



Below is a typical Common Gate circuit. Note that there are two DC power supplies, $+V_{DD}$ and $-V_{DD}$. The input sinusoidal generator is connected to the source and the output load is connected to the drain.



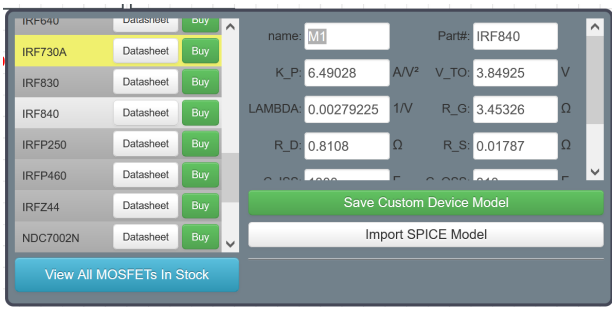
1. **HAND CALCULATIONS:** Design a single stage NMOS FET amplifier to achieve the above specifications. Note: this design requires two power supplies (+/- V_{DD}). As this is an amplifier circuit, you should design for a FET operating in saturation mode.

a. This is a design project; show all steps for selection of resistors, two DC power supplies and bias Q-point ($\boldsymbol{I_D}$, $\boldsymbol{V_{DS}}$). Submit all hand calculations for voltage gain (A_v), input resistance (R_{in}) and output resistance (R_{out} - not including R_L). Show the test schematic for calculating the output resistance. Confirm that your transistor is saturated.
b. **Submit** your complete schematic and label all resistor values.
c. On a **table**, list the following selected/calculated parameters
   i. Load Resistance, $\boldsymbol{R_L}$
   ii. DC Power Supply Voltages, +/-$\boldsymbol{V_{DD}}$
   iii. Total DC Power Supply Current, $\boldsymbol{I_{DD}}$
   iv. Calculated voltage gain, $\boldsymbol{A_V}$
   v. Calculated Input Resistance, $\boldsymbol{R_{in}}$
   vi. Calculated Output Resistance $\boldsymbol{R_{out}}$ (not including R_L)
   vii. Transistor power dissipation, $\boldsymbol{P_D}$

d. Calculate the amplitude of the sinusoidal input source, v_{in}, to have the transistor just operating at the small signal condition. What is this **amplitude for $\boldsymbol{v_{in}}$**?
e. Provide a brief statement on your design philosophy. This statement is approximately one paragraph and includes why/how you chose the values for resistors and DC bias. In your statement, also discuss if you designed for DC and AC stability.

2. **PSPICE:** Simulate your design and answer the following. <u>NOTE: You may find that your PSpice results (DC and gain) are slightly different than your hand calculations. In this case, you are allowed to slightly modify the resistor values in your simulation to improve the PSpice performance to the required amplifier specifications.</u>

- If using **CircuitLab**, select the PSpice FET model for the IRF840 found in the "MOSFETs" library (select the N-Channel device). Open the model parameters and confirm the value of K_P (transconductance parameter, k_N) equal to 6.49 A/V^2. Also confirm the value of the V_TO is equal to 3.85 V (Threshold Voltage, V_{TN}). The parameter settings should appears as this.



- For **large capacitors**, use a value of "1", meaning 1 FARAD.

<u>Answer the following:</u>

a. Show the complete PSpice schematic including v_{in} (Voltage Function Generator (CircuitLab), R_L and capacitors. All component values must be clearly shown.

b. Set the peak amplitude of your PSpice function generator to the 1/10 the calculated amplitude for v_{in} found in **1d** above. Set the sinusoidal frequency to 1 kHz (default).

c. Using your PSpice simulator, simulate the DC performance of your design. Submit your PSpice **schematic** showing values for DC voltage and DC current for the FET and bias resistors. (left column using CircuitLab). Your submission must clearly show a table for the DC voltages and currents.

d. What are the simulated DC bias parameters? **Submit a table showing the simulated values for I_{DD}, I_D, V_{GS}, V_{DS}, and $P_D=(V_{DS})(I_D)$**? Is your circuit operating the "**saturated**" region? Is your transistor **power dissipation less than the target $P_D < 12.5\ W$**?

e. **Simulated Gain:** Simulate a Transient analysis (time domain simulation). **Submit** a plot showing v_{in} versus time. **Submit** a plot showing and v_{out} versus time. These two plots should be on separate axis. The time scale is 0 to 3 msec, adjust the "max. time step" for a smooth sinusoidal curve (0.01 msec).

Answer the following:
e.1) Are your waveforms *in-phase* or *out-of-phase*?
e.2) Is there any observable distortion in the output sinusoidal waveform, v_{out}? If you observe distortion (something other than a sinewave), you may need to adjust the DC bias point (Q point) or reduce the amplitude of the input generator or both. Make a note of any changes and continue using the new values.

e.3) What is the simulated voltage gain, $A_v = v_{out}/v_{in}$? Use cursors to measure the peak amplitudes of each voltage waveform and calculate the small signal gain by taking the ratio.

e.4) Compare the simulated gain to your calculated gain, what is the percent difference between the two $\left(\frac{simulated-calculated}{calculated} x100\%\right)$? Is your simulated gain within +/10 % of $A_V = 10$?

f. **Simulated Input Resistance**: Simulate a Transient analysis, **submit** a plot of v_{in} versus time and a separate plot for i_{in} versus time under small signal conditions. The measurement point should be on the left of the input capacitor (no DC here). Using a cursor, measure the peak amplitudes of the input voltage and input current. Calculate the input resistance, $R_{in} = v_{in}/i_{in}$?. **Compare** the simulated value to your calculated value. What is the percent difference $\left(\frac{simulated-calculated}{calculated} x100\%\right)$?.

g. **Simulated Output Resistance**: Remove the input function generator and place a short across this location (***$v_{in} = 0$***). Remove the load resistor, R_L, and replace it with a function generator (test source). **Submit** a copy of this schematic. Simulate a Transient analysis under small signal conditions. **Submit** a plot of v_x versus time and a separate plot of i_x versus time. What is the simulated output resistance, $R_{out} = {v_x}/{i_x}$? Use cursors to measure the peak amplitudes of each waveform and calculate the ratio. **Compare** the simulated value to your calculated value and calculate the percent difference $\left(\frac{simulated-calculated}{calculated} x100\%\right)$?