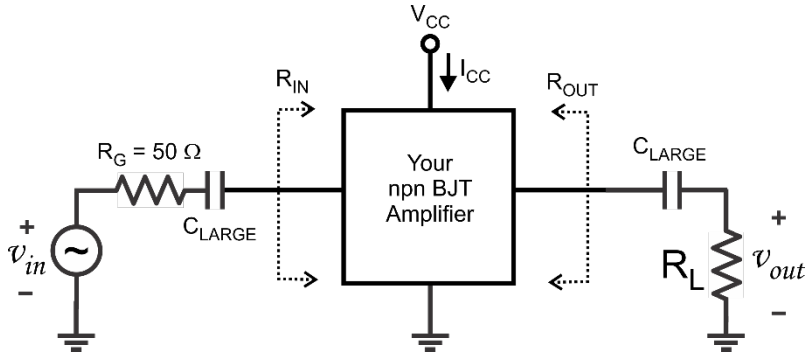
Design a single stage BJT small signal amplifier to the following specifications. ***This is an individual effort; similar designs will not be graded.*** Submit one complete document (PDF), 10 points will be deducted if multiple files are submitted.

SPECIFICATIONS:

- Transistors: type 2N3904
  $\beta_{nominal}$ =150
  V_A = infinite (hand calculations)
  $v_{CE,\,SAT}$ = 0.3V
- Single DC voltage supply, $V_{CC} \leq$ **+50 V** (you choose the voltage)
- Resistor-only DC biasing (no DC current sources allowed)
- All resistors <= 500kΩ (resistors can have any value)
- Load Resistor, R_L **= 800 Ω + last two digits** of your student ID (N#). Your load resistor will fall in the range of $800\ \Omega \leq R_L \leq 899\ \Omega$.
- All coupling and bypass capacitors = Large (1 F in PSpice)
- Inductors are not allowed
- Maximum DC Power Dissipation for transistor: $P_{D,max} = (V_{CEQ})(I_{CQ})$ **<= 200mWatt**

- Target Voltage Gain, $\left|A_{V,\beta=150}\right| = \left|\frac{v_{out}}{v_{in}}\right| = 15 \pm 5\%$ **(gain when** $\beta = 150$**)**
- Voltage Gain variation $= \left|A_{V,\beta=150}\right| \pm 7.5\%$ over $75 \leq \beta \leq 300$ (in PSpice)



1) **HAND CALCULATIONS:** Design a single stage BJT amplifier to achieve the above specifications. Show all steps for selection of resistors and bias (Q) point. As this is an amplifier circuit, you should design for a BJT operating in forward-active mode.
   If you make any guesses, assumptions, and/or approximations, briefly state the reason. For the hand calculations, use $\beta_{nominal}$ =150, **you must design for DC and AC stability.** Show the equations how you circuit achieves both DC and AC stability.

   A. This is a design project; show all steps for selection of resistors, DC power supply and bias Q-point (I_C, V_{CE}). Submit all hand calculations for voltage gain (A_v), input resistance (R_{in} - not including R_G) and output resistance (R_{out} - not including R_L). Show the test schematic for calculating the output resistance. Confirm that your transistor is forward-active. **Extra points** for neatness.
   B. **Submit** your complete schematic and label all resistor values.
   C. On a **table**, list the following selected/calculated parameters

i. Your N# and associated load resistance, R_L
ii. DC Power Supply Voltage, V_{CC}
iii. Total DC Power Supply Current, I_{CC}
iv. Calculated voltage gain, A_V, when $\beta = \beta_{nominal} = 150$
v. Calculated Input Resistance, R_{in} (not including R_G), when $\beta = \beta_{nominal} = 150$
vi. Calculated Output Resistance R_{out} (not including R_L), when $\beta = \beta_{nominal} = 150$
vii. Calculated transistor Power Dissipation, P_D. Did you exceed the maximum power dissipation rating for the transistor?

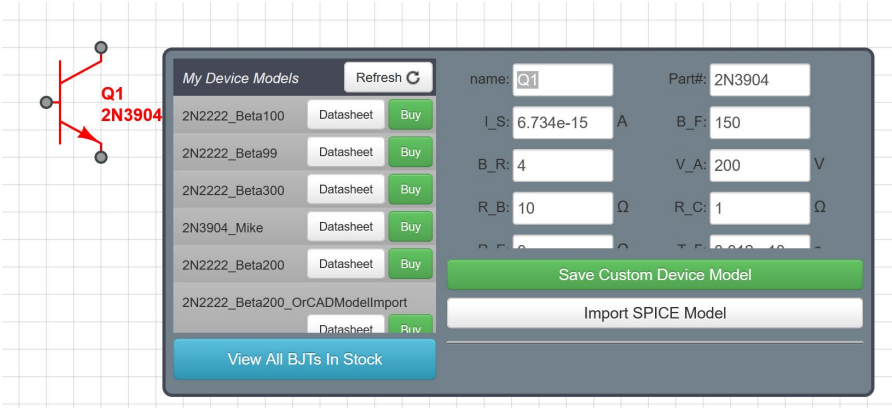
D. Discuss how you achieved DC and AC stability. Provide the equations that support your amplifier stability at $\beta = \beta_{nominal} = 150$

E. Calculate the amplitude of the sinusoidal input source, v_{in}, to have the transistor just operating at the small signal condition. What is this **amplitude for v_{in}**?

F. Provide a brief statement on your design philosophy. This statement is approximately one paragraph and includes why/how you chose the values for resistors and DC bias.

2) **PSPICE:** Simulate your design and answer the following. NOTE: You may find that your PSpice results (DC and gain) are slightly different than your hand calculations. In this case, you are allowed to slightly modify the resistor values in your simulation to improve the PSpice performance to the required amplifier specifications.

- If using **CircuitLab**, select the PSpice BJT model for the 2N3904 found in the "BJT-NPN" library. Open the model parameters and change the value of B_F (forward current gain Beta, β) to 150 (nominal value of $\beta = 150$). Increase the Early Voltage (V_A) to 200 V. You may leave the other parameters as their default values. The parameter settings should appears as this.



You can "Save Custom Device Model" to be used again.

- For **large capacitors**, use a value of "1", meaning 1 FARAD

Answer the following:

A. Show the complete PSpice schematic including v_{in} (Voltage Function Generator (CircuitLab), R_L and capacitors. All component values must be clearly shown.

B. Set the peak amplitude of your PSpice function generator to the 1/10 the calculated amplitude for v_{in} found in **1E** above. Set the sinusoidal frequency to 1 kHz (default).

C. Using your PSpice simulator, simulate the DC performance of your design. Submit your PSpice **schematic** showing values for DC voltage and DC current for the BJT and bias resistors (left column using CircuitLab). Your submission must clearly show a table for the DC voltages and currents.

D. What are the simulated DC bias parameters? **Submit a table showing the simulated values for** V_{CC}, I_{CC}, V_B, V_C, V_E, I_C, V_{CE}, V_{BE} and $P_D=(V_{CE})(I_C)$? Is your transistor biased in the **forward active** region? Is your transistor **power rating <= *200mW***?

E. **Simulated Gain with $\beta = 150$:** Simulate a Transient analysis (time domain simulation). **Submit** a plot showing v_{in} versus time. **Submit** a plot showing and v_{out} versus time. These two plots should be on separate axis. The time scale is 0 to 3 msec, adjust the "max. time step" for a smooth sinusoidal curve (0.01 msec).

Answer the following:
e.1) Are your waveforms *in-phase* or *out-of-phase*?
e.2) Is there any observable distortion in the output sinusoidal waveform, v_{out}? If you observe distortion (something other than a sinewave), you may need to adjust the DC bias point (Q point) or reduce the amplitude of the input generator or both. Make a note of any changes and continue using the new values.
e.3) What is the simulated voltage gain, $A_v = v_{out}/v_{in}$ when $\beta = 150$? Use cursors to measure the peak amplitudes of each voltage waveform and calculate the small signal gain by taking the ratio.
e.4) Compare the simulated gain to your calculated gain, what is the percent difference between the two $\left(\frac{simulated-target}{target} x100\%\right)$? Is your simulated gain within +/5.0 % of $A_V = 10$?

F. **Simulated Gain Variation with $\beta = 75$:** Edit the 2N3904 model and change B_F=75 ($\beta = 75$).

What is the simulated voltage gain, $A_v = v_{out}/v_{in}$ when $\beta = 75$? **Compare** the simulated gain at $\beta = 75$ to the gain found when $\beta = 150$. What is the percent difference $\left(\frac{A_{V,\beta=75}-A_{V,\beta=150}}{A_{V,\beta=150}} x100\%\right)$? Did you gain variation fall within $\pm 7.5\%$?

G. **Simulated Gain Variation with $\beta = 300$:** Edit the 2N3904 model and change B_F=300 ($\beta = 300$).

What is the simulated voltage gain, $A_v = v_{out}/v_{in}$ when $\beta = 300$? **Compare** the simulated gain at $\beta = 300$ to the gain found when $\beta = 150$. What is the percent difference $\left(\frac{A_{V,\beta=300}-A_{V,\beta=150}}{A_{V,\beta=150}} x100\%\right)$? Did you gain variation fall within $\pm 7.5\%$?

H. Simulated Input Resistance: Return the transistor $\boldsymbol{\beta}$ back to 150 ($\boldsymbol{\beta = 150}$). Simulate a Transient analysis, **submit** a plot of $\boldsymbol{v_{in}}$ versus time and a separate plot for $\boldsymbol{i_{in}}$ versus time under small signal conditions. The measurement point should be on the left of the input capacitor (no DC here). Using a cursor, measure the peak amplitudes of the input voltage and input current. Calculate the input resistance, $R_{in} = {}^{v_{in}}\!/_{i_{in}}$?. **Compare** the simulated value to your calculated value. What is the percent difference $\left(\frac{simulated-calculated}{calculated} x100\%\right)$?.

I. Simulated Output Resistance: Remove the input function generator and place a short across this location ($\boldsymbol{v_{in} = 0}$). Remove the load resistor, R_L, and replace it with a function generator (test source). **Submit** a copy of this schematic. Simulate a Transient analysis under small signal conditions. **Submit** a plot of v_x versus time and a separate plot of i_x versus time. What is the simulated output resistance, $R_{out} = {}^{v_x}\!/_{i_x}$? Use cursors to measure the peak amplitudes of each waveform and calculate the ratio. **Compare** the simulated value to your calculated value and calculate the percent difference $\left(\frac{simulated-calculated}{calculated} x100\%\right)$?