Isaac Liu

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Education

M.S. / Ph.D Electrical Engineering and Computer Science
University of California, Berkeley (2007 – Present)

- Graduate Researcher in CHESS (Center for Hybrid and Embedded Software Systems) with Professor Edward Lee
- Focus on Embedded Systems, Computer Architecture, Models of Computation, Precision Timed Machines, Real-Time Systems, Parallel Processors

B.S Computer Engineering
University of California, Santa Barbara (2003 – 2007)

- Valedictorian of the Computer Engineering class of 2007 with highest honors
- Received IEC William L. Everitt Student Awards of Excellence
- 3.91 overall GPA, 3.97 Major GPA

Experience/ Projects

- **Software Design Engineer – Microsoft**, Seattle, WA (Summer 2006)
  Worked in Microsoft Windows core deployment team. Read through windows kernel code base, understand data structures and design project to analyze Windows Imaging file format for Windows Vista. Develop tool to interact with file format and improve windows setup performance.
- **Projects** –
  - **Real Time Processor** – Research in developing processors with timing predictability and repeatability. Modified open source SPARC core implementation in VHDL (leon3) to add interleaved threading and a new instruction specifying timing properties of processor to use for research.
  - **Processor Modeling** – Created a cycle accurate leon3 SPARC core model in SystemC to aid in better architectural exploration, and simulation, to observe effects of non-functional properties.
  - **POV wand** – Persistence of Vision wand. Interfaced digital sensors and actuators with an 8 bit microprocessor to create a wand that shows words in the air when waved using persistence of vision. Also created light saber like sounds when waved.
  - **BIAS** – Basic Integrated Audio System. Mp3 player integrating FM transmitter, voice recorder, and storage on Compact Flash with FAT file system. Designed and built the complete system, including choose components, drawing layout, coding firmware, integration and testing.
  - **BURP** – Basic Undergrad RISC Processor. Using Verilog to write controller, modelsim to simulate processor, then loading controller onto FPGA, interfacing with ALU, RAM, and EEPROM to run RISC instructions.

Skills

Systems and hardware

- Labview, Matlab, ModelSim, VHDL, Verilog, SystemC, TTA, CAN, FlexRay, RTOS, Models of Computation, multi-core architectures, parallel processing, Real-Time systems.

Programming and software

- Languages: Java, C, C++, C#, SQL, UNIX shell scripting, PHP, Perl, XML, XHTML, AJAX, OpenGL, assembly, HTML, LateX, Network programming
- Sample programs: www.isaacliu.info/projects.html

Bilingual

- Fluent in Mandarin, Chinese, able to read and write newspaper and articles.

Interests/ activities

- Secretary of Tau Beta Pi Engineering honor society Cal Sigma Chapter (2003)
- Member Eta Kappa Nu Engineering honor society Epsilon Tau Chapter (2002-2003)