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Задача 1:

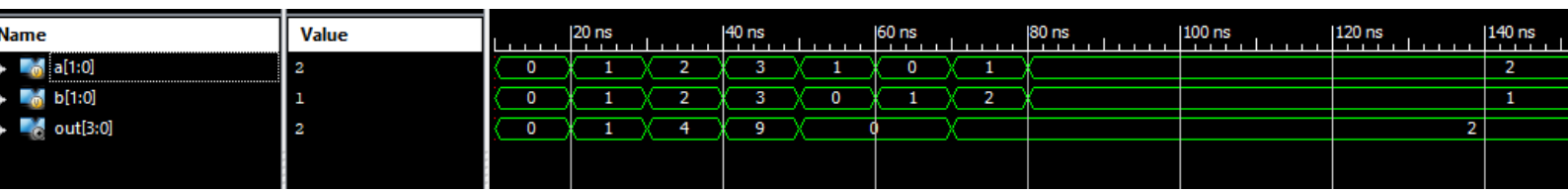
Модул:

```
1  module multiply (out, a, b);
2  output [3:0] out;
3     input  [1:0] a;
4     input  [1:0] b;
5
6     assign out = a * b;
7
8  endmodule
```

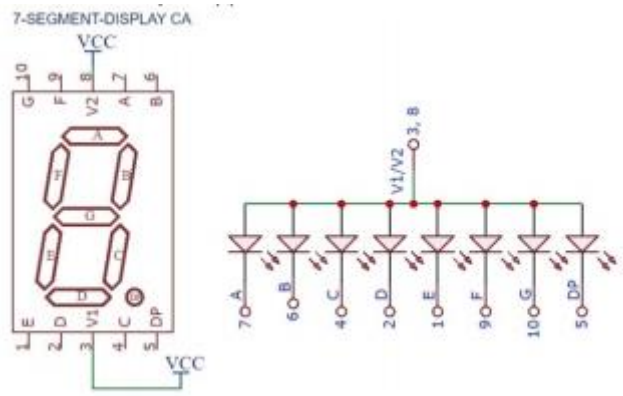
Тестбенч:

```
3  module multiply_TB();
4  wire [3:0] out;
5  reg [1:0] a;
6  reg [1:0] b;
7
8  multiply dut (.out(out),
9                .a(a),
10               .b(b));
11  initial
12    begin
13  #10 a = 0;
14      b = 0;
15  #10 a = 1;
16      b = 1;
17  #10 a = 2;
18      b = 2;
19  #10 a = 3;
20      b = 3;
21  #10 a = 1;
22      b = 0;
23  #10 a = 0;
24      b = 1;
25  #10 a = 1;
26      b = 2;
27  #10 a = 2;
28      b = 1;
29   #200
30   $finish;
31 end
32 endmodule
```

Симулация:



Задача 2:



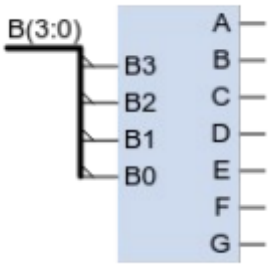


Таблица на истинност:

b3	b2	b1	b0	a	b	c	d	e	f	g	
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	2
0	0	1	1	0	0	0	0	1	1	0	3
0	1	0	0	1	0	0	1	1	0	0	4
0	1	0	1	0	1	0	0	1	0	0	5
0	1	1	0	0	1	0	0	0	0	0	6
0	1	1	1	0	0	0	1	1	1	1	7
1	0	0	0	0	0	0	0	0	0	0	8
1	0	0	1	0	0	0	0	1	0	0	9
1	0	1	0	0	0	0	1	0	0	0	A
1	0	1	1	0	0	0	0	0	0	0	B
1	1	0	0	0	1	1	0	0	0	1	C
1	1	0	1	0	0	0	0	0	0	1	D
1	1	1	0	0	1	1	0	0	0	0	E
1	1	1	1	0	1	1	1	0	0	0	F

(!a*!b*!c*!d) + (!a*!b*!c*d) + (!a*!b*c*!d) + (!a*!b*c*d) + (!a*b*!c*!d) + (!a*b*!c*d) + (!a*b*c*!d) + (!a*b*c*d) + (a*!b*!c*!d) + (a*!b*!c*d) + (a*!b*c*!d) + (a*!b*c*d) + (a*b*!c*!d) + (a*b*!c*d) + (a*b*c*!d) + (a*b*c*d)

a = b3 + (b2 * b0) + (! b2 * ! b0) + b1 bout = (b3 * ! b1 * b0) + (! b3 * b1 * b0) + (! b3 * ! b1 * ! b0) + ! b2 c = (b3 * ! b2) + (! b3 * b2) + (! b3 * ! b1) + (! b3 * b0) + (! b1 * b0) d = (b3 * ! b1) + (! b3 * ! b2 * ! b0) + (b2 * b1 * ! b0) + (b2 * ! b1 * b0) + (! b2 * b1 * b0) e = (b3 * b2) + (b3 * b1) + (! b2 * ! b0) + (b1 * ! b0) f = (b3 * ! b2) + (b3 * b1) + (! b3 * b2 * ! b1) + (b2 * ! b0) + (! b1 * ! b0) g = (b3 * ! b2) + (b3 * b1) + (! b3 * b2 * ! b1) + (! b2 * b1) + (b1 * ! b0)

Модул:

```
module seven_segment_dec(a, bout, c, d, e, f, g, dot, b);

 input [3:0] b;

 output reg a, bout, c, d, e, f, g, dot;

 assign a = ~(b[3] || (b[2] && b[0]) || (! b[2] && ! b[0]) || b[1]);

 assign bout = ~((b[3] && ! b[1] && b[0]) || (! b[3] && b[1] && b[0]) || (! b[3] && ! b[1] && ! b[0]) || ! b[2]);

 assign c = ~((b[3] && ! b[2]) || (! b[3] && b[2]) || (! b[3] && ! b[1]) || (! b[3] && b[0]) || (! b[1] && b[0]));

 assign d = ~((b[3] && ! b[1]) || (! b[3] && ! b[2] && ! b[0]) || (b[2] && b[1] && ! b[0]) || (b[2] && ! b[1] && b[0]) || (!b[2] && b[1] && b[0]));

 assign e = ~((b[3] && b[2]) || (b[3] && b[1]) || (! b[2] && ! b[0]) || (b[1] && ! b[0]));

 assign f = ~((b[3] && ! b[2]) || (b[3] && b[1]) || (! b[3] && b[2] && ! b[1]) || (b[2] && ! b[0]) || (! b[1] && ! b[0]));

 assign g = ~((b[3] && ! b[2]) || (b[3] && b[1]) || (! b[3] && b[2] && ! b[1]) || (! b[2] && b[1]) || (b[1] && ! b[0]));

 assign dot = ~(! b[3] || (! b[2] && ! b[1]));
```

Тестбенч:

```
endmodule

module seven_segment_dec_TB();

 reg [3:0] b;

 wire a, bout, c, d, e, f, g, dot;

 seven_segment_dec ist_1(a, bout, c, d, e, f, g, dot, b);

 initial begin

  $dumpfile("out.vcd");

  $dumpvars(1, seven_segment_dec_TB);

  b = 4'b0000;

 end

 initial begin

  #40;

  while(b!=4'b1111) begin

   b = b + 4'b0001;

   #40;
```

```
    end
  end
endmodule
```