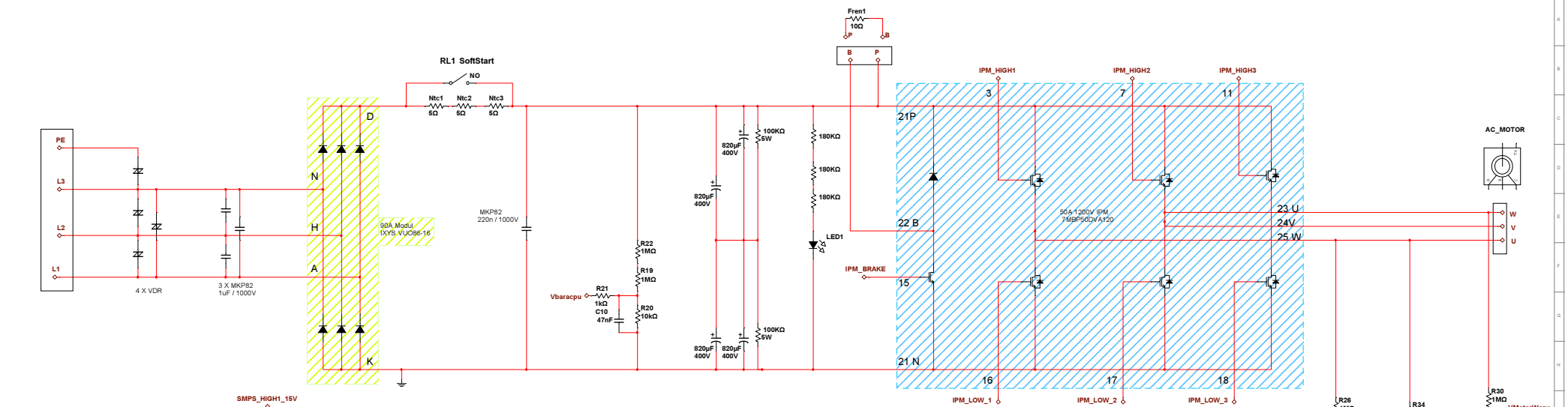

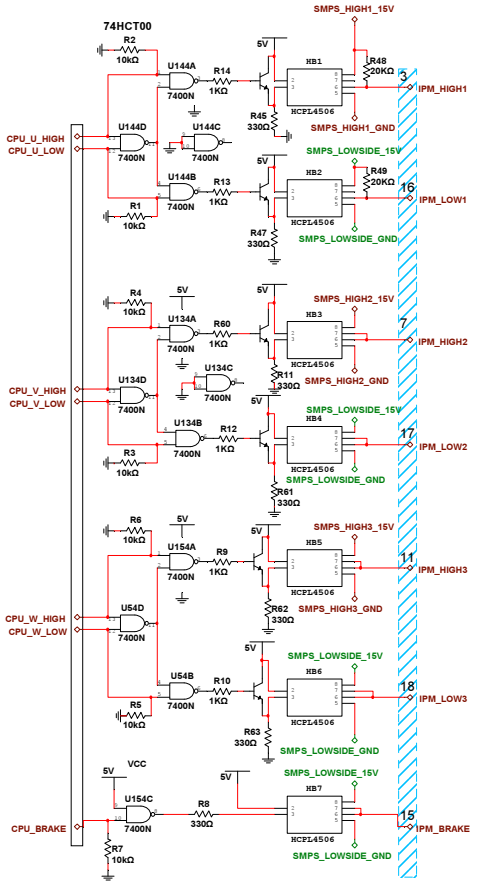

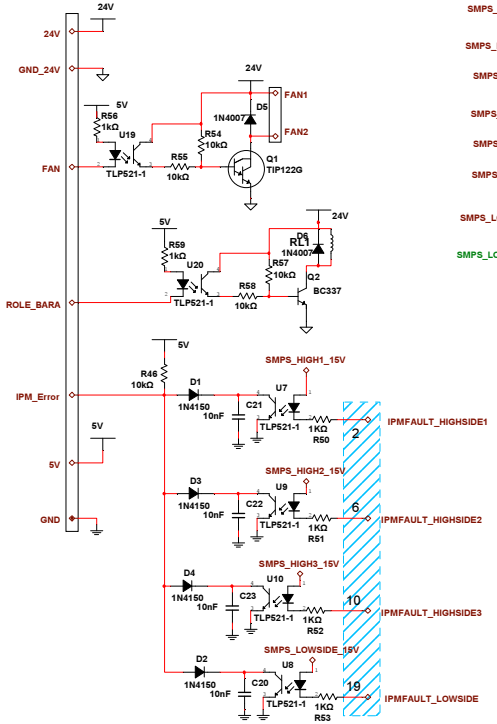

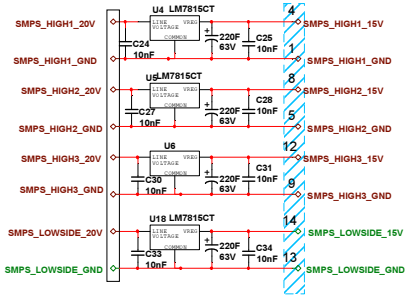

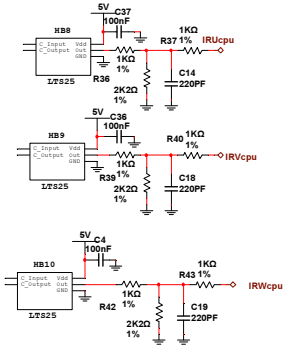

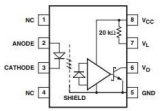

PWM LOJIC TABLE npn transistor

```
cpu g1  g2      tr      opt     out
        0|-> 1  on -> off -> 1 off
 0 |->1 1|
 0 |     1|-> 1  on -> off -> 1 off
        0|

cpu g1  g2      tr      opt     out
        1|-> 0 off -> on -> 0 on
 1 |->1 1|
 0 |     1|-> 1  on -> off -> 1 off
        0|

cpu g1  g2      tr      opt     out
        0|->1  on -> off -> 1 off
 0 |->1 1|
 1 |     1|-> 0 off -> on -> 0 on
        1|

cpu g1  g2      tr      opt     out
        1|-> 1  on -> off -> 1 off
 1 |->0 0|
 1 |     0|-> 1  on -> off -> 1 off
        1|
```

BREAKE LOJIC

```
cpu  g1 opt out
     1 |-> 0 -> 1
     1 |

cpu  g1 opt out
     1 |-> 1 -> 0
     0 |
```

3 X BYPASS 7400

5V C1 100nF, 5V C3 100nF, 5V C2 100nF

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