Transistor Worksheet

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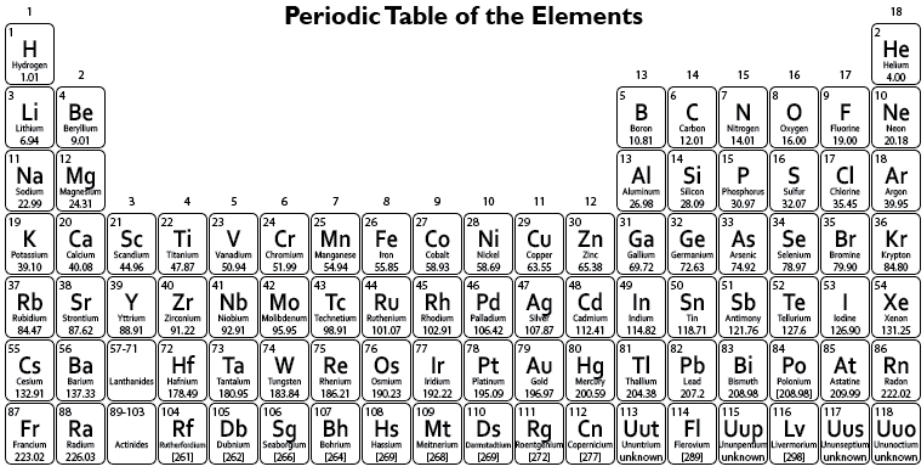
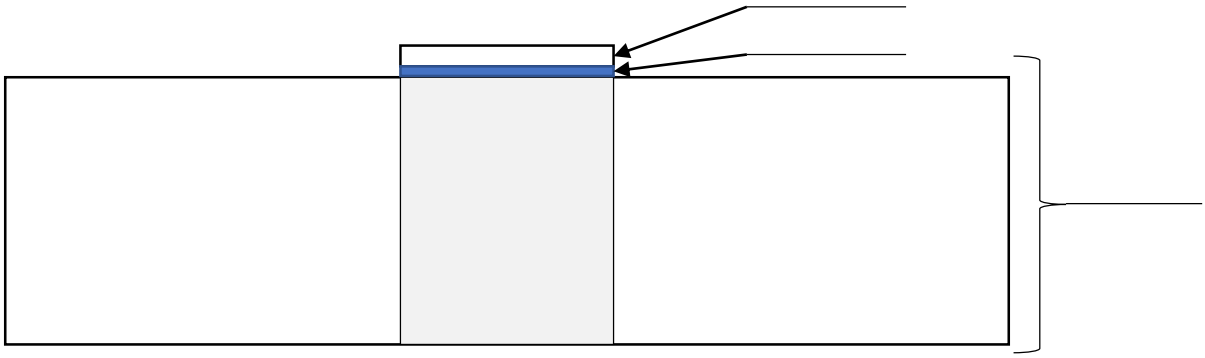
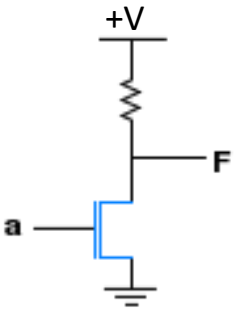


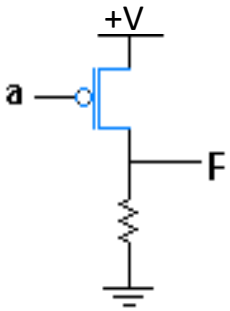
Transistor – NPN FET



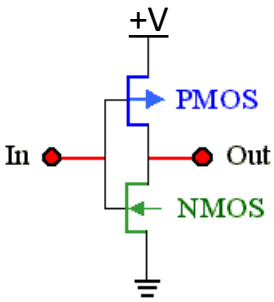
Logic – NMOS/PMOS Inverter vs CMOS Inverter



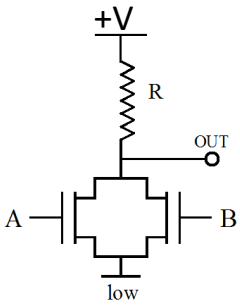
NMOS Not



PMOS Not



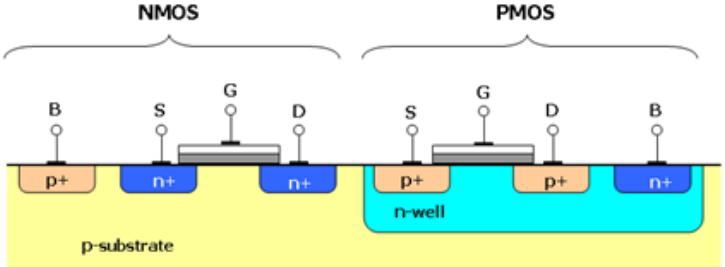
CMOS Not



What is this?

_____

Fabrication – The CMOS ***process***

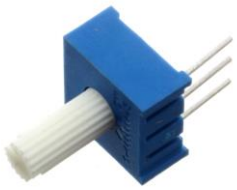


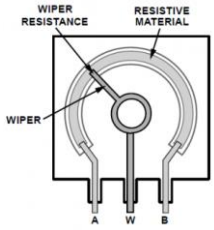
Draw the P doping mask(s)

Transistor Lab

Passive Electronic Circuit

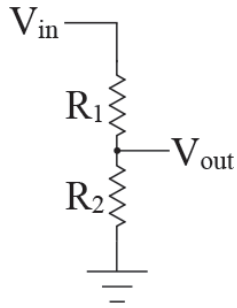
Build a voltage divider using a potentiometer.





Test the circuit.

$$V_{out} = V_{in} * \frac{R2}{(R1 + R2)}$$



Transistor Circuit – NPN FET

Use the voltage divider you designed above to measure the *Gate Threshold* voltage for an NPN MOSEFT (IRF510).

Draw test circuit here

Plot I_{DS} vs. V_{GS} here

G D S

Challenge

Build the circuit below. Use an audio signal as input.

What value for R1?
(LED current limit = 25 mA)

Why use the input capacitor?

Replace R4/R3 with your voltage divider.