# RTL8316B

## 16-PORT 10/100M ETHERNET SWITCH CONTROLLER WITH EMBEDDED MEMORY

## DATASHEET

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## REVISION HISTORY

| Revision | Release Date | Summary |
|----------|--------------|---------|
| 1.0 | 2005/03/21 | First release. |

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# 1. General Description

The RTL8316B  is a layer-2 switch controller that integrates 1.25Mbits of high-speed SSRAM, an 8K-entry MAC address lookup table, 16 Ethernet/Fast Ethernet MACs, and a switch engine into one chip.

The Remote Management Tool (RMT) software package is bundled with the RTL8316B. The RMT is a Windows-based tool developed to enhance the functionality of Realtek's dumb layer 2 switches via software. The RMT gives network administrators the ability to remotely configure and monitor dumb layer 2 switches as though they were intelligent switches. With QoS, Trunking, VLAN, bandwidth control, remote control, and an 0.18μm process, the RTL8316B is a cost effective switch controller for a 16-port 10/100 dumb or smart switch application.

Port trunking is supported on all ports to increase bandwidth. Load balancing and fault tolerance provide top performance and reliability. The RTL8316B provides 2-level priority queues for multimedia or real-time network applications. The CoS (Class of Service) can be port-based, IEEE 802.1p tag-based, and/or TCP/IP header TOS/DS field-based. The RTL8316B supports up to 32 VLAN groups that may be configured as port-based VLANs and/or IEEE 802.1Q tagged VLANs. ARP broadcast and Leaky VLAN are also supported.

The RTL8316B supports diagnostics and analysis. Counters are included for: RX byte count, RX packet count, TX byte count, TX packet count, CRC error packet count, collision packet count, dropped packet count, and dropped byte count. The RTL8316B supports TX and RX bandwidth control on each port; 128Kbps, 256Kbps, 512kbps, 1Mbps, 2Mbps, 4Mbps, or 8Mbps may be selected in each direction.

The RTL8316B provides for a Scan LED Group to display each port's status, without extra component cost. A loop-detection function is provided to notify whether a network loop exists, either via a visual LED, or via a register flag for smart applications. LED displays for broadcast storm, trunking status, flow control, and traffic utilization are also provided.

Maximum packet length can be up to 1552 bytes. The RTL8316B supports the ability to drop 802.1D specified reserved group MAC addresses: (01-80-C2-00-00-04 to 01-80-C2-00-00-0F) according to pin strapping upon reset, or register setting. The RTL8316B default setting enables dropping of these reserved group MAC address control frames. Frames with group MAC address 01-80-C2-00-00-01 (802.3x Pause), 01-80-C2-00-00-02 (802.3ad LACP) will always be filtered.

The RTL8316B supports IEEE 802.3x full duplex flow control and back pressure half duplex flow control. Full duplex flow control can be disabled both manually or automatically to ensure QoS control or

bandwidth control operates correctly. Broadcast storm filtering prevents network crashes caused by abnormal broadcast activity.

As well as supporting IEEE 802.3u auto-negotiation, the RTL8316B supports PHY Read/Write registers to access PHY registers through an MDC/MDIO interface. This expands system configuration options. In-band management of the functions provided by the RTL8316B may be implemented using a simple 8051 microprocessor, or via the RTL8316B's RRCP® protocol based Remote Management Tool (RMT).

The RTL8316B is designed with a link-list buffer management architecture and provides 4.8Gbps of bandwidth to achieve wire-speed performance. It also has an intelligent switching engine to prevent Head-of-Line blocking. Only a single 25MHz crystal is required for clock generation.

# 2.    Features

- 16-port 10/100Mbps layer-2 Ethernet switch controller with embedded lookup table and packet buffer
- Supports SMII on all ports
- Built-in 8K entry MAC address lookup table plus 64-entry CAM to eliminate hash collision problems
- Built-in 1.25Mbit SSRAM packet buffer
- Non-blocking wire-speed forwarding and filtering (3.2Gbps throughput)
- Store and forward architecture and head-of-line blocking prevention
- All ports support Speed, Duplex, and 802.3x flow-control ability auto-negotiation
- Supports broadcast storm filtering control
- Supports Trunking function with load balancing and fault tolerance
- Supports up to 32 VLAN groups for port-based VLAN and 802.1Q tag VLAN
- Supports Leaky VLAN
- Two priority queues for three types of Class of Service (CoS)
  - ◆ Port-based
  - ◆ IEEE 802.1p priority tag
  - ◆ TCP/IP header's TOS/DS classifier
- Weighted round robin queue scheduling
- Priority tag insert and remove function
- Supports ASIC based IGMPv1 and IGMPv2 snooping function

- Supports pin strapping, EEPROM, or serial CPU configuration interface
- Supports PHY register read/write access
- Supports Realtek Management Tool (RMT®) for in-band configuration and management
- Supports simple MIB counters
- TX/RX packet/byte, CRC error, and collision counter for diagnostics/statistics
- Supports per-port bandwidth control
- Supports loop detection and indication function
- Provides Scan LED, serial LED, and parallel LED interface for port properties and diagnostic display
- Provides Write EEPROM function via software (RMT® or MPU) for Smart Switch application.
- Provides configurable Port Mirror function.
- Needs only one low cost 25MHz crystal or OSC input
- 0.18μm, 128-pin PQFP, 3.3V single power, 5V I/O tolerance

# 3.    System Applications

10/100Mbps switch controller for a 16-port 10/100 dumb or smart switch application.

In-band management of the functions provided by the RTL8316B may be implemented using a simple 8051 microprocessor, or via the RTL8316B's RRCP® protocol based Remote Management Tool (RMT)

# 4.    Block Diagram

**Dumb/Smart**
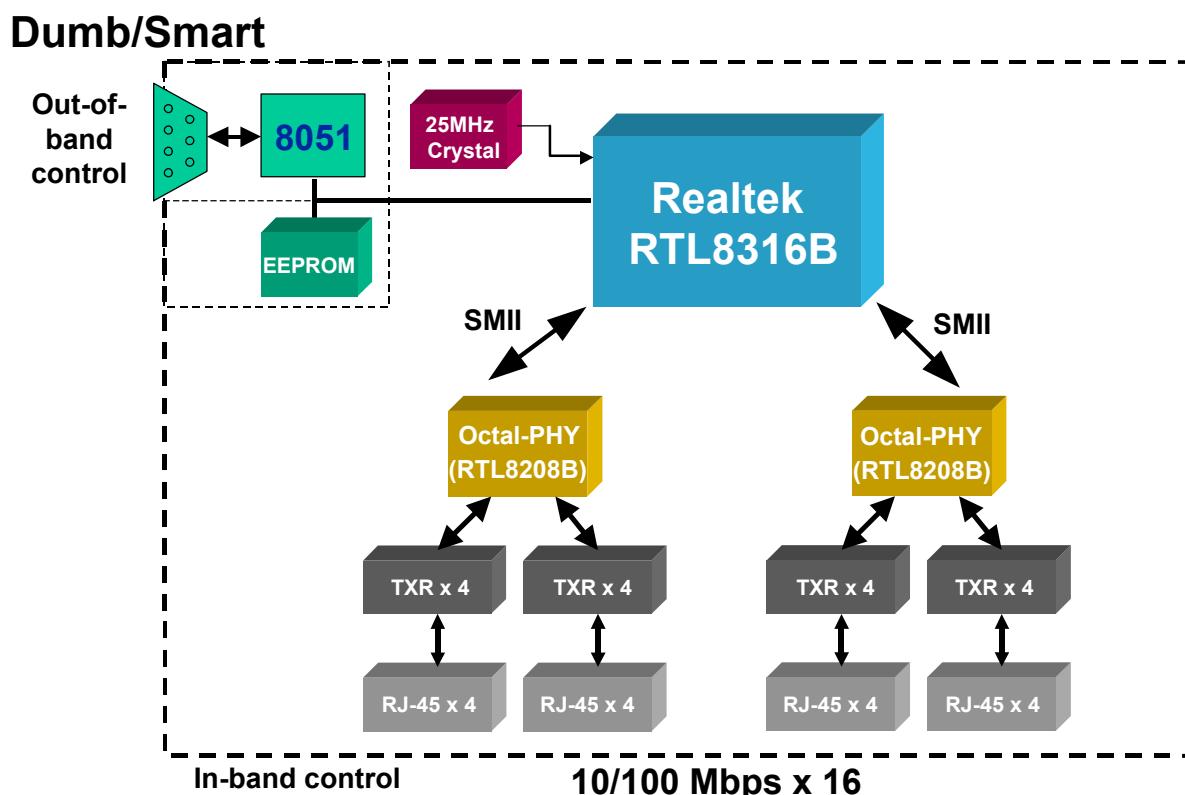


**Figure 1.   Block Diagram**

# 5.    Functional Block Diagram
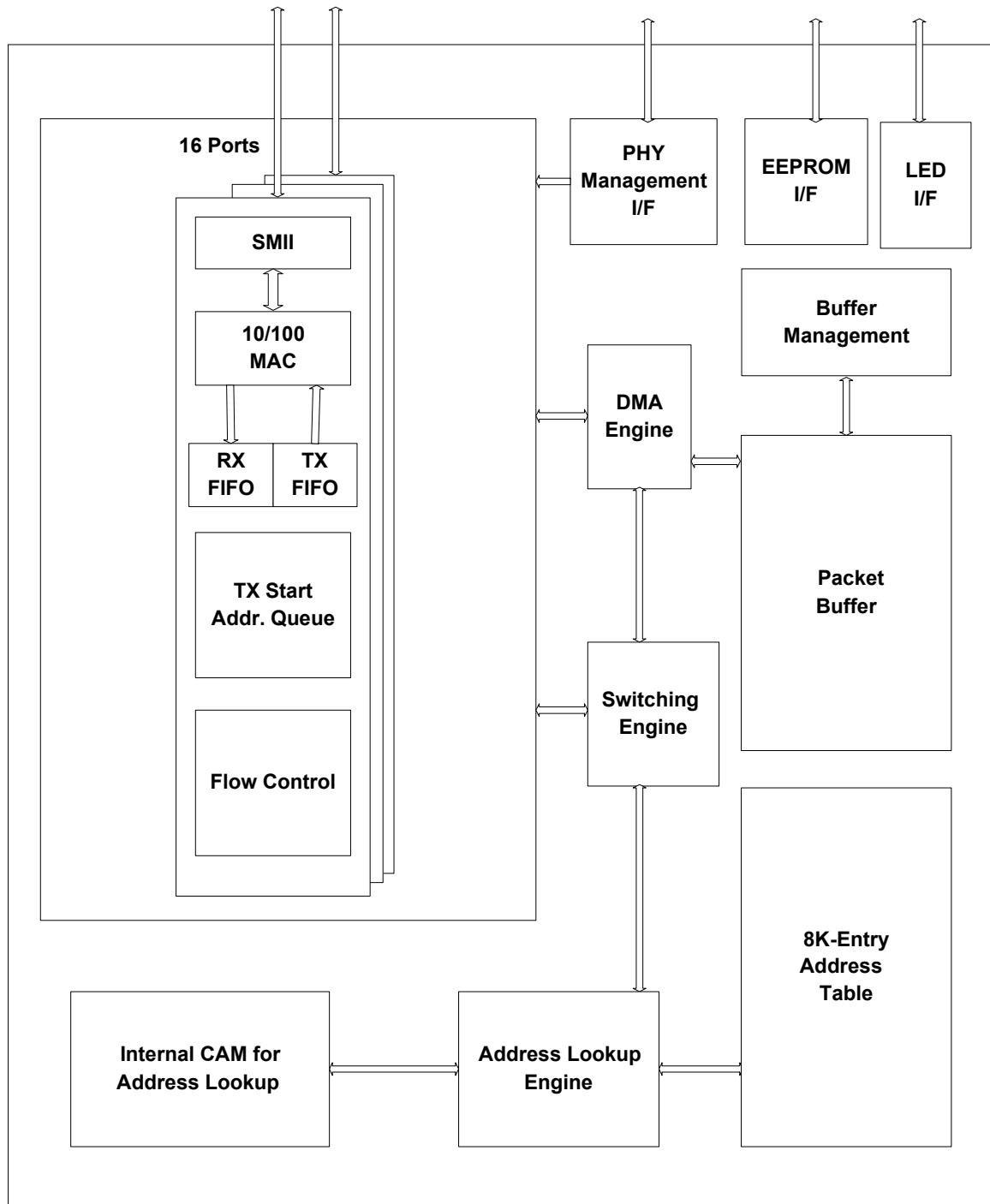


**Figure 2.   Functional Block Diagram**

# 6. Pin Assignments

## 6.1. Pin Assignment Figure
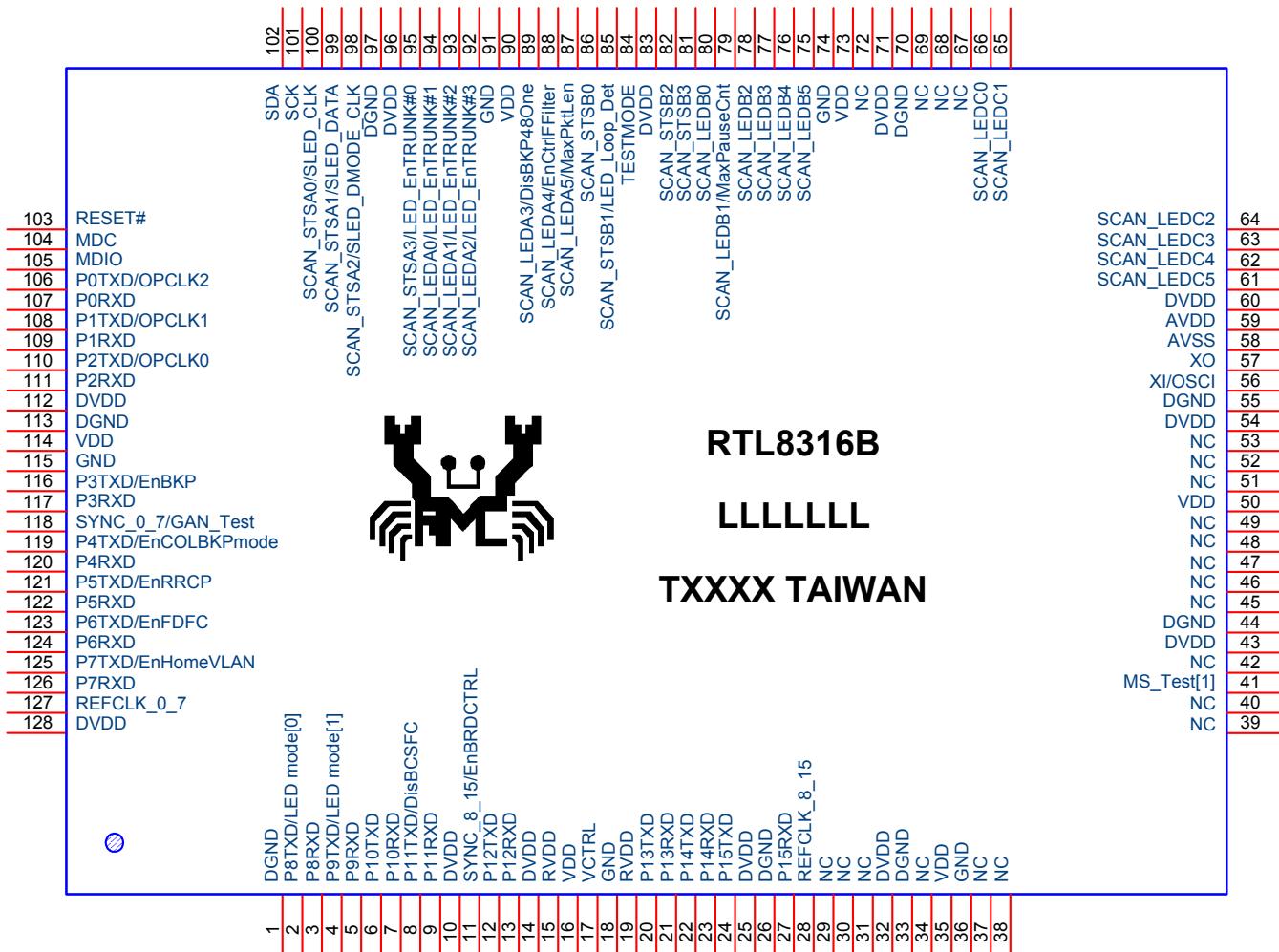


**Figure 3.   Pin Assignments**

## 6.2. Lead (Pb)-Free Package Identification

Lead (Pb)-free package is indicated by an 'L' in the location marked 'T' in Figure 3.

## 6.3. Pin Assignment Table (128-Pin PQFP)

Type codes used: P = Power; G = Ground, I = Input, O = Output.

**Table 1. Pin Assignment Table (PQFP-128)**

| Pin No. | Type | Pin Name | Pin No. | Type | Pin Name |
|---|---|---|---|---|---|
| 1 | G | DGND | 39 | O | NC |
| 2 | O | P8TXD/LED mode[0] | 40 | I | NC |
| 3 | I | P8RXD | 41 | O | MS_Test[1] |
| 4 | O | P9TXD/LED mode[1] | 42 | O | NC |
| 5 | I | P9RXD | 43 | P | DVDD |
| 6 | O | P10TXD | 44 | G | DGND |
| 7 | I | P10RXD | 45 | I | NC |
| 8 | O | P11TXD/DisBCSFC | 46 | O | NC |
| 9 | I | P11RXD | 47 | I | NC |
| 10 | P | DVDD | 48 | O | NC |
| 11 | O | SYNC_8_15/EnBRDCTRL | 49 | I | NC |
| 12 | O | P12TXD | 50 | P | VDD |
| 13 | I | P12RXD | 51 | O | NC |
| 14 | P | DVDD | 52 | I | NC |
| 15 | P | RVDD | 53 | O | NC |
| 16 | P | VDD | 54 | P | DVDD |
| 17 | O | VCTRL | 55 | G | DGND |
| 18 | G | GND | 56 | I | XI/OSCI |
| 19 | P | RVDD | 57 | O | XO |
| 20 | O | P13TXD | 58 | G | AVSS |
| 21 | I | P13RXD | 59 | P | AVDD |
| 22 | O | P14TXD | 60 | P | DVDD |
| 23 | I | P14RXD | 61 | O | SCAN_LEDC5 |
| 24 | O | P15TXD | 62 | O | SCAN_LEDC4 |
| 25 | P | DVDD | 63 | O | SCAN_LEDC3 |
| 26 | G | DGND | 64 | O | SCAN_LEDC2 |
| 27 | I | P15RXD | 65 | O | SCAN_LEDC1 |
| 28 | O | REFCLK_8_15 | 66 | O | SCAN_LEDC0 |
| 29 | O | NC | 67 | O | NC |
| 30 | I | NC | 68 | O | NC |
| 31 | O | NC | 69 | O | NC |
| 32 | P | DVDD | 70 | G | DGND |
| 33 | G | DGND | 71 | P | DVDD |
| 34 | I | NC | 72 | O | NC |
| 35 | P | VDD | 73 | P | VDD |
| 36 | G | GND | 74 | G | GND |
| 37 | O | NC | 75 | O | SCAN_LEDB5 |
| 38 | I | NC | 76 | O | SCAN_LEDB4 |

| Pin No. | Type | Pin Name |
|---|---|---|
| 77 | O | SCAN_LEDB3 |
| 78 | O | SCAN_LEDB2 |
| 79 | O | SCAN_LEDB1/MaxPauseCnt |
| 80 | O | SCAN_LEDB0 |
| 81 | O | SCAN_STSB3 |
| 82 | O | SCAN_STSB2 |
| 83 | G | DVDD |
| 84 | O | TESTMODE |
| 85 | O | SCAN_STSB1/LED_Loop_Det |
| 86 | O | SCAN_STSB0 |
| 87 | O | SCAN_LEDA5/MaxPktLen |
| 88 | O | SCAN_LEDA4/EnCtrlFFilter |
| 89 | O | SCAN_LEDA3/DisBKP48One |
| 90 | P | VDD |
| 91 | G | GND |
| 92 | O | SCAN_LEDA2/LED_EnTRUNK#3 |
| 93 | O | SCAN_LEDA1/LED_EnTRUNK#2 |
| 94 | O | SCAN_LEDA0/LED_EnTRUNK#1 |
| 95 | O | SCAN_STSA3/LED_EnTRUNK#0 |
| 96 | P | DVDD |
| 97 | G | DGND |
| 98 | O | SCAN_STSA2/SLED_DMODE _CLK |
| 99 | O | SCAN_STSA1/SLED_DATA |
| 100 | O | SCAN_STSA0/SLED_CLK |
| 101 | I/O | SCK |
| 102 | I/O | SDA |
| 103 | I | RESET# |
| 104 | O | MDC |
| 105 | I/O | MDIO |
| 106 | O | P0TXD/OPCLK2 |
| 107 | I | P0RXD |
| 108 | O | P1TXD/OPCLK1 |
| 109 | I | P1RXD |
| 110 | O | P2TXD/OPCLK0 |
| 111 | I | P2RXD |
| 112 | P | DVDD |
| 113 | G | DGND |
| 114 | P | VDD |
| 115 | G | GND |
| 116 | O | P3TXD/EnBKP |
| 117 | I | P3RXD |
| 118 | O | SYNC_0_7/GAN_Test |
| 119 | O | P4TXD/EnCOLBKPmode |

| Pin No. | Type | Pin Name |
|---|---|---|
| 120 | I | P4RXD |
| 121 | O | P5TXD/EnRRCP |
| 122 | I | P5RXD |
| 123 | O | P6TXD/EnFDFC |
| 124 | I | P6RXD |
| 125 | O | P7TXD/EnHomeVLAN |
| 126 | I | P7RXD |
| 127 | O | REFCLK_0_7 |
| 128 | P | DVDD |

# 7. Pin Descriptions

Type codes used: P = Power; G = Ground, I = Input, O = Output, Pu = Internal pull up (75K ohm), Pd = Internal pull down (75K ohm).

## 7.1. SMII Interface

**Table 2. SMII Interface**

| Pin Name | Type | Pin No. | Description |
|---|---|---|---|
| P0TXD | O | 106 | SMII Transmit Data Output: |
| P1TXD | | 108 | SMII transmit data is formed in 10-bit serial words. Each word contains one |
| P2TXD | | 110 | data byte (two nibbles of 4B coded data) and two |
| P3TXD | | 116 | status bits. |
| P4TXD | | 119 | The SMII operates at 125MHz using a global reference clock |
| P5TXD | | 121 | (REFCLK) and frame synchronization signal (SYNC). |
| P6TXD | | 123 | |
| P7TXD | | 125 | SMII transmit data is input on these pins, where: |
| P8TXD | | 2 | Ports 0~7 transmit data is sent synchronously to SYNC_0_7 |
| P9TXD | | 4 | and REFCLK_0_7. |
| P10TXD | | 6 | |
| P11TXD | | 8 | Ports 8~15 transmit data is sent synchronously to SYNC_8_15 |
| P12TXD | | 12 | and REFCLK_8_15. |
| P13TXD | | 20 | |
| P14TXD | | 22 | |
| P15TXD | | 24 | |
| P0RXD | I | 107 | SMII Receive Data Input: |
| P1RXD | | 109 | SMII receive data is input on these pins. Where: |
| P2RXD | | 111 | |
| P3RXD | | 117 | Ports 0~7 receive data is received synchronously to SYNC_0_7 and |
| P4RXD | | 120 | REFCLK_0_7. |
| P5RXD | | 122 | |
| P6RXD | | 124 | Ports 8~15 receive data is received synchronously to SYNC_8_15 and |
| P7RXD | | 126 | REFCLK_8_15. |
| P8RXD | | 3 | |
| P9RXD | | 5 | |
| P10RXD | | 7 | |
| P11RXD | | 9 | |
| P12RXD | | 13 | |
| P13RXD | | 21 | |
| P14RXD | | 23 | |
| P15RXD | | 27 | |
| SYNC_0_7 | O | 118 | SMII Synchronization Output. |
| SYNC_8_15 | | 11 | SMII transmit/receive data 10-bit word frame synchronization. Where: |
| | | | SYNC_0_7 synchronizes data for ports 0~7. |
| | | | SYNC_8_15 synchronizes data for ports 8~15. |

| Pin Name | Type | Pin No. | Description |
|---|---|---|---|
| REFCLK_0_7 | O | 127 | SMII Reference Clock Output. |
| REFCLK_8_15 | | 28 | The SMII reference clock output is a 125MHz +- 50ppm clock used to synchronize the SMII data. |
| | | | Ports 0~7 data is sent or received synchronously to SYNC_0_3. |
| | | | Ports 8~15 data is sent or received synchronously to SYNC_8_15. |

# 7.2. *Serial Management Interface (SMI)*

**Table 3. Serial Management Interface (SMI)**

| Pin Name | Type | Pin No | Description |
|---|---|---|---|
| MDC | O (Pu) | 104 | Serial Management Data Clock (MDC). MDC operates at 1MHz. MDC is in tri-state when RST# is active low. |
| MDIO | IO (Pu) | 105 | Serial Management Data Input/Output. MDIO is in tri-state when RST# is active low. |

# 7.3. *Serial EEPROM Interface*

**Table 4. Serial EEPROM Interface**

| Pin Name | Type | Pin No | Description |
|---|---|---|---|
| SCK | IO (Pu) | 101 | Serial EEPROM Interface Clock Output/ Serial CPU Access Clock Input. SCLK acts as an output pin after hardware reset for EEPROM read access. When the configuration download from EEPROM is finished, or if the EEPROM does not exist, then the SCLK will act as an input pin driven by an external CPU to access the RTL8316B internal registers. SCLK Frequency: Output: Operates at 100KHz Input: Max limit: 10MHz |
| SDA | IO (Pu) | 102 | Serial EEPROM Data Input/Output/Serial CPU Access Data Input/Output. After power on, this pin is EEPROM serial data IO. When the configuration download from EEPROM is finished, or if the EEPROM does not exist, then this pin acts as a serial CPU data IO. |

## 7.4. System Pins

**Table 5. System Pins**

| Pin Name | Type | Pin No | Description |
|---|---|---|---|
| RESET# | I<br>(Pu) | 103 | System Reset.<br>Active low to reset the system to a known state. After power-on reset (low to high), the configuration modes from Mode Control Pins (page 11) are strapped and determined. |
| XI/OSCI | I | 56 | Crystal Input/Oscillator Input.<br>This is a 25Mhz +-50 ppm crystal input or oscillator input.<br>When crystal is used, a capacitor connected from this pin to ground is recommended. |
| XO | O | 57 | Crystal Output.<br>When crystal is used, a capacitor connected from this pin to ground is recommended. When an oscillator is used, keep this pin floating. |

## 7.5. Mode Control Pins

The Mode Control pin values are strapped on power on reset. The strapped values may be updated via EEPROM configuration if it exists. They can also be modified by internal register access from the CPU interface.

**Table 6. Mode Control Pins**

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| MaxPktLen<br>(SCAN_LEDA5) | 87 | I/O<br>(P-down) | Max. Valid Packet Length Control.<br>0: 1536 bytes (Default)<br>1: 1552 bytes |
| MaxPauseCnt<br>(SCAN_LEDB1) | 79 | I/O<br>(P-down) | Max Pause frame Count for Congestion Control.<br>0: 128 (Default)<br>1: Continuous |
| EnCOLBKPmode<br>(P4TXD) | 119 | I/O<br>(P-down) | Enable Carrier-Based Back Pressure Mode.<br>Half duplex back pressure flow control algorithm selection.<br>0: Carrier-based back pressure mode (Default)<br>1: Collision-based back pressure mode |
| EnRRCP<br>(P5TXD) | 121 | I/O<br>(P-down) | Disable Realtek Remote Control Protocol Function.<br>0: Disable RRCP (Default)<br>1: Enable RRCP |
| EnCtrlFFilter/<br>(SCAN_LEDA4) | 88 | I/O<br>(P-down) | Enable 802.1D Specified Reserved Control Frame Filtering.<br>When network control frames are received with the destination MAC address as the group MAC address: (01-80-C2-00-00-04 ~ 01-80-C2-00-00-0F), the switch will drop the frames if the EnCtrlFilter=1. If EnCtrlFilter=0 the frames will be flooded.<br>0: Disable Filtering (Default)<br>1: Enable Filtering |

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| EnHomeVLAN (P7TXD) | 125 | I/O (P-down) | Enable Home-VLAN Configuration. When enabled, the switch will be configured in Home-VLAN mode. The "Home-VLan topology" is shown below: 0: Disable Home-VLAN Function (Default) 1: Enable (set VLAN as 14 VLANs with 2 overlapping port). |
| EnFDFC (P6TXD) | 123 | I/O (P-up) | Global Disable Full Duplex 802.3x Pause Flow Control Ability. Globally disables the 802.3x Pause ability flow control of all ports. 1: Enable 802.3x Pause flow control ability (Default) 0: Disable 802.3x Pause flow control ability |
| EnBKP (P3TXD) | 116 | I/O (P-up) | Global Disable Half Duplex Back Pressure Flow Control Ability. Globally disables the back pressure flow control ability of all ports. 1: Enable back pressure flow control ability (Default) 0: Disable back pressure flow control ability |
| EnBKP48One (SCAN_LEDA3) | 89 | I/O (P-up) | Enable Back Pressure 48 Pass One Algorithm. When the 48 Pass One algorithm is enabled, the switch will pass one incoming packet for every 48 collisions. 0: Disable 48 Pass One algorithm 1: Enable 48 Pass One algorithm (Default) |
| DisBCSFC (P11TXD) | 8 | I/O (P-down) | Disable Broadcast Packet Strict Flood Control. Set to disable broadcast packet (DA: 'FF-FF-FF-FF-FF-FF') strict flood mode and configure to loose flood mode. Strict flood mode will drop all broadcast packets if any one destination port is congested. Loose flood mode allows broadcast packets to be flooded to all non-congested ports. 0: Enable Broadcast Packet Strict Flood (Strict flood mode) (default) 1: Disable Broadcast Packet Strict Flood (Loose flood mode) |
| EnBRDCTRL (SYNC_8_15) | 11 | I/O (P-down) | Broadcast Storm Filtering Control. Disables broadcast storm filtering control. 0: Disable Broadcast storm filtering control (Default) 1: Enable Broadcast storm filtering control |
| LED mode[1:0] P9TXD P8TXD | 4 2 | I/O (P-down, P-up) | 00: Scan LED mode. 01: Serial LED mode (single color) (default) 10: Serial LED mode (bi-color) 11: Reserved |

## 7.6. *LED Pins*

## 7.6.1. Scan LED Pins

**Table 7. Scan LED Pins**

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| Port 0_7 | | I/O | Scan LED pins display for port0~port7 link status. |
| Scan_LED Group | | | In Scan LED mode, this LED group display each port's (1)Speed (2) Link/Active (3) Collision/Duplex status without external TTL. |
| SCAN_LEDA5 | 87 | | |
| SCAN_LEDA4 | 88 | | |
| SCAN_LEDA3 | 89 | | |
| SCAN_LEDA2 | 92 | | |
| SCAN_LEDA1 | 93 | | |
| SCAN_LEDA0 | 94 | | |
| SCAN_STSA3 | 95 | | |
| SCAN_STSA2 | 98 | | |
| SCAN_STSA1 | 99 | | |
| SCAN_STSA0 | 100 | | |
| Port 8_15 | | I/O | Scan LED pins display for port8~port15 link status. |
| Scan_LED Group | | | In Scan LED mode, this LED group display each port's (1) Speed (2) Link/Active (3) Collision/Duplex status without external TTL. |
| SCAN_LEDB5 | 75 | | |
| SCAN_LEDB4 | 76 | | |
| SCAN_LEDB3 | 77 | | |
| SCAN_LEDB2 | 78 | | |
| SCAN_LEDB1 | 79 | | |
| SCAN_LEDB0 | 80 | | |
| SCAN_STSB3 | 81 | | |
| SCAN_STSB2 | 82 | | |
| SCAN_STSB1 | 85 | | |
| SCAN_STSB0 | 86 | | |
| Scan_LED Group | | I/O | Pins used for Scan LED application. |
| SCAN_LEDC5 | 61 | | |
| SCAN_LEDC4 | 62 | | |
| SCAN_LEDC3 | 63 | | |
| SCAN_LEDC2 | 64 | | |
| SCAN_LEDC1 | 65 | | |
| SCAN_LEDC0 | 66 | | |

## 7.6.2.  Serial LED Pins

**Table 8.  Serial LED Pins**

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| SLED_CLK (SCAN_STSA0) | 100 | O | Serial LED Shift Clock. In Serial LED mode, when Serial LED mode is enabled, periodically active to enable SLED_DATA to shift into the external shift register. |
| SLED_DATA (SCAN_STSA1) | 99 | O | Serial LED Data Output. In Serial LED mode, when Serial LED mode is enabled, serial LED data is shifted out when SLED_CLK is active. |
| SLED_DMODE _CLK (SCAN_STSA2) | 98 | I | Serial LED Diagnostic Mode Item Select Control Pulse Input. This is an external signal pulse input signal for diagnostic item selection. The diagnostic LED display item will change whenever there is a signal pulse clock input on this pin. The diagnostic items list and its display sequence is as follows: (1) DisablePort/RxError (active low)     On: Port disabled     Blinking: Error Packet Received (includes dropped     packets) (2) FlowControl/FCActive (active low)     On: Flow control ability enabled     Blinking: Congestion flow control active (3) TrunkPort/TKFault (active low)     On: Trunk Port     Blinking: Trunk link fault port (4) HighPriorityPort (active low)     On: High priority port (5) LoopDetectPort (active low)     On: Loop event detected. (6) BroadcastStormAlarmPort (active low)     On: Broadcast Storm detected (7) Reserved (8) Reserved |
| LED_EnTRUNK#0 (SCAN_STSA3) LED_EnTRUNK#1 (SCAN_LEDA0) LED_EnTRUNK#2 (SCAN_LEDA1) LED_EnTRUNK#3 (SCAN_LEDA2) | 95 94 93 92 | O | Trunk Port Enabled LED output. 0 (On): Trunk Enabled 1 (Off): Trunk Disabled. The LED blinks to indicate that there is a trunk member port link down. For Serial LED Mode: act as Trunk 0 (port 0~3) Enable LED. For Serial LED Mode: act as Trunk 1 (port 4~7) Enable LED. For Serial LED Mode: act as Trunk 2 (port 8~11) Enable LED. For Serial LED Mode: act as Trunk 3 (port 12~15) Enable LED. |
| LED_Loop_Det (SCAN_LEDA5) | 87 | O | For Serial LED mode: act as Loop detect for global port. Loop Detect LED output. 0: Loop detected 1: Loop not detected |

# 7.7. Power/Ground Pins

**Table 9.   Power/Ground Pins**

| Pin Name | Type | Pin No | Description |
|---|---|---|---|
| DVDD | 3.3V(I) | 10, 14 25, 32 43, 54 60, 71 83, 96, 112, 128 | 3.3V for I/O digital power. |
| DGND | GND | 1, 26 33, 44 55, 70 97, 113 | GND for I/O. |
| RVDD | 3.3V(I) | 15 19 | 3.3V for internal 3.3V to 1.8V regular power input. |
| VDD | 1.8V(I) | 16, 35 50, 73 90, 114 | 1.8V input for internal test used. Do not supply 1.8V if RVDD is used. |
| GND | GND | 18, 36 74, 91 115 | GND for Core power. |
| VCTRL | 1.8V(o) | 17 | Voltage control: This pin controls a PNP transistor to generate the 1.8V power supply for VDD pins. Normally keep this pin floating. |
| AVDD | 3.3V(I) | 59 | 3.3V for PLL power. |
| AVSS | GND | 58 | GND for PLL. |

# 7.8. Test Pins

**Table 10. Test Pins**

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| TESTMODE | 84 | I/O (Pd) | Test pin. Normally not pulled up or down. |
| MS_Test[1] | 41 | I/O (P-down) | Must use 4.7K resistor to pull down to ground. |
| GAN_Test (SYNC_0_7) | 118 | I/O | Must use 1K resistor to pull up to 3.3V. |
| NC Pins | 29, 30, 32, 34, 37, 38, 39, 40, 42, 45, 46, 47, 48, 49, 51, 52, 53, 67, 68, 69 | | Keep NC pins floating. |
| OPCLK2 (P0TXD) | 106 | I/O (P-down) | Test pin. Normally not pulled up or down. |
| OPCLK1 (P1TXD) | 108 | I/O (P-down) | Test pin. Normally not pulled up or down. |
| OPCLK0 (P2TXD) | 110 | I/O (P-down) | Test pin. Normally not pulled up or down. |

# 8. Functional Description

## 8.1. Reset

### 8.1.1. Hardware Reset

In a power-on reset, an internal power-on reset pulse (44ms) will be generated and the RTL8316B will start the reset initialization procedures. These are:

1. Determine various default settings via the hardware strap pins at the end of the RST# signal

2. Auto load the configuration from EEPROM if EEPROM is detected (approx. 10ms)

3. Complete the embedded SSRAM BIST process (approx. 24 ms)

4. Initialize the packet buffer descriptor allocation

5. Initialize the internal registers and prepare them to be accessed by the serial CPU interface

6. Start MDC/MDIO configuration and polling

*Note 1: To guarantee register access is valid and correct, the RTL8316B registers should not be accessed before the reset initialization process is finished.*

*Note 2: The connected PHY should have completed the reset process before the RTL8316B starts the MDC/MDIO configuration and polling process.*

### 8.1.2. Software Reset

The software reset command resets the system control circuit and restarts auto-negotiation. It keeps the user configured settings. Hardware pin strapping, EEPROM auto load, and SSRAM BIST are NOT done when using the software reset command.

## 8.2. MAC to PHY Interface

The MAC to PHY interface supports SMII for all ports.

## 8.3. Fast Ethernet Port (SMII Interface)

Ports 0~15 are 10/100M Fast Ethernet ports supporting a Serial Media Independent Interface (SMII). The RTL8316B provides three SMII synchronous 125MHz clock outputs for three octal PHYs.

## 8.4. MAC Address Table Search and Learning

The RTL8316B MAC address lookup table consists of an 8K-entry hash table and 64-entry Content Addressable Memory (CAM). The RTL8316B uses the last 13 bits of the MAC address to index the 8K-entry lookup table for address searching and learning. If the mapped location in the 8K entries is occupied, then the RTL8316B will compare the destination MAC address with the contents of the CAM for address searching, and store the source MAC address in the CAM for address learning. The 128-entry CAM helps avoid address hash collisions and improves switch performance.

## 8.5. MAC Table Aging Function

In a dynamic network topology, address aging allows the contents of the address table to always be the most recent and correct. A learned source address entry will be cleared (aged out) if it is not updated by the address learning process within a set aging time period. The default aging timer of the MAC address lookup table is between 200 ~ 300 seconds.

## 8.6. Illegal Frame Filtering

Illegal frames such as CRC error packets, runt packets (length < 64 bytes) and oversize packets (length > maximum length) will be discarded. The maximum packet length may be 1536 or 1552 bytes.

This function is controlled by register 0x0001 [1:0].

Hardware Strapping Pin: MaxPKLen (87).

## 8.7. IEEE 802.1D Reserved Group Addresses Filtering Control

The RTL8316B supports the ability to drop 802.1D specified reserved group MAC addresses: 01-80-C2-00-00-04 to 01-80-C2-00-00-0F. The default setting disables dropping of these reserved group MAC address control frames. Frames with group MAC address 01-80-C2-00-00-01 (802.3x Pause), 01-80-c2-00-00-02 (802.3ad LACP) will always be filtered. MAC address 01-80-C2-00-00-03 is not filtered.

This function is controlled by register 0x0300 [2].

Hardware Strapping Pin: EnCtrlFFilter (88).

## 8.8. Backoff Algorithm

The RTL8316B implements the truncated exponential backoff algorithm compliant with the IEEE 802.3 standard. The collision counter is restarted after 16 consecutive collisions.

## 8.9. Inter-Packet Gap

The Inter-Packet Gap is 9.6μs for 10Mbps Ethernet, 960ns for 100Mbps Fast Ethernet.

The RTL8316B supports Transmit Inter-Packet Gap compensation for the frequency shift tolerance of the on-board oscillator.

This function is controlled by register 0x0001 [2].

## 8.10. Buffer Management

An embedded 1.25Mbit SSRAM is built-in as a packet storage buffer. To efficiently utilize the packet buffer, the RTL8316B divides the SSRAM into 1280 x 128-byte page-based buffers that are linked by a descriptor link list. For an Ethernet packet, a minimum of one, and maximum of 12 pages can be used. The system supports non-blocking wire-speed switching via 16 10/100M ports.

## 8.11. Flow Control

The RTL8316B supports IEEE 802.3x full-duplex flow control, and half-duplex back pressure congestion control.

### 8.11.1. IEEE 802.3x Pause Flow Control

IEEE 802.3x flow control is auto-negotiated between the remote device and the RTL8316B by writing the flow control ability, via MDIO, to an external connected PHY.

If a good PAUSE frame is received from any PAUSE flow-control-enabled port with DA=0180C2000001, the corresponding port of the RTL8316B will stop its packet transmission until a PAUSE timer timeout, or another PAUSE frame with zero PAUSE time is received.

The maximum transmitted Pause frame count during a congestion event is controllable. (1) limited to a 128 count (2) unlimited count. The limited count is used to avoid unexpectedly long pause time locks for some network topology traffic.

This function is controlled by register 0x0001 [3].

Hardware Strapping Pin: MaxPauseCnt (79).

### 8.11.2. Half Duplex Back Pressure Flow Control

The RTL8316B supports two back pressure flow control schemes to force incoming packet backoff when the switch destination port is congested. This back pressure mode is controlled by register 0x0001 [7] and Hardware Strapping Pin: EnCOLBKPMode (119).

**Collision-based back pressure:** Uses a 4-byte jam pattern to force collisions with each incoming packet to force the link partner to back off transmissions according to CSMA/CD until the destination port congestion event is cleared. The RTL8316B uses a special half-duplex back pressure design; after 48 forced collisions it unconditionally receives and forwards one packet successfully. This prevents the connected repeater from being partitioned due to excessive collisions.

**Carrier-sense-based back pressure:** When a congested event is asserted, the RTL8316B continuously sends 4k jam packets with a minimum Inter-Packet Gap to prevent the link partner from transmitting more packets.

# 8.12. Broadcast Storm Filtering Control

The Broadcast Storm Filtering Control function enables each port to drop broadcast packets (Destination MAC ID is 'ff ff ff ff ff ff') after a ***continuous received broadcast packets counter*** count of 64. The counter is reset to 0 every 800ms or when receiving non-broadcast packets (Destination MAC ID is not 'ff ff ff ff ff ff').

This Broadcast Storm Filtering Control function is controlled by register 0x0607 [4].

Hardware Strapping Pin: EnBRDCTRL (11).

# 8.13. Head-Of-Line Blocking Prevention

The RTL8316B incorporates a simple mechanism to prevent Head-Of-Line blocking problems when flow control is disabled. When the flow control function is disabled, the RTL8316B first checks the destination address of an incoming packet. If the destination port is congested, then the RTL8316B discards this packet to avoid blocking following packets destined for a non-congested port.

# 8.14. Port Trunking and Fault Recovery Support

Port Trunking is the ability to aggregate several 10/100Mbps ports into a single logical link. There are 6 trunk groups supported by the RTL8316B. They are identified as:

Trunk 0: (Port 0, 1, 2, 3)

Trunk 1: (Port 4, 5, 6, 7)

Trunk 2: (Port 8, 9, 10, 11)

Trunk 3: (Port 12, 13, 14, 15)

They are individually enabled by Register 0x0307[4:1], EnTrunk[3:0] during hardware reset. Each trunk supports a trunking port status LED. The LED will be active low when the trunking function is enabled.

The RTL8316B trunking port always sends packets over the same link path in the trunk with a given source and destination MAC address to prevent frames from getting out of order, but the reverse path may follow a different link.

## 8.14.1. Load Balancing

The load balancing scheme between links in a trunk group is determined by an Index[2:0] value that is calculated by a DA and SA hash algorithm.

Mapping algorithm. Given a number between 8 values of Index[2:0]:

If link up port is 4. Index value {(7, 6), (5, 4), (3, 2), (1, 0)} maps to LinkUpPort[3:0]

If link up port is 3. Index value {(7, 6, 5), (4, 3, 2), (1, 0)} maps to LinkUpPort[2:0]

If link up port is 2. Index value {(7, 6, 5, 4), (3, 2, 1, 0)} maps to LinkUpPort[1:0]

If link up port is 1. Index value {(7, 6, 5, 4, 3, 2, 1, 0)} maps to LinkUpPort[0]

## 8.14.2. Trunk Fault Auto Recovery

If a physical port of a trunk group is link down, then the EnTrunkLED will blink to warn of a link-down fault event. The Fault flag will be reported on register 0x0102 (System Fault Indication Register).

The RTL8316B will auto-start the Auto Fault Recovery scheme to distribute the trunk load to the remaining link up ports.

# 8.15. IGMP Snooping Support

The RTL8316B supports ASIC-based IGMP (Internet Group Management Protocol) snooping. This can be enabled via register 0x0308[0]. No other external CPU handling is required. It supports the ability to parse the IGMP control protocol packets and IP multicast data packets and learn the multicast router port and group address member ports into the multicast address table.

The RTL8316B differentiates between IGMP control protocol packets according to the message type:

- Router protocol packets (IGMP query packets and multicast routing protocol packets) are broadcast to all ports

- Group member protocol packets (IGMP v1, v2, Report and Leave packets) are sent directly to multicast router ports

IP multicast data packets involve multicast group table lookup and forwarding operations. If the table lookup returns a hit, the data packet is forwarded to all member ports and router ports. If the multicast address is not stored in the address table (i.e. lookup miss), the packet is broadcast to all ports of the broadcast domain.

The multicast table is combined with a L2 MAC table with a maximum of 8k entries. For a given multicast entry, the valid port member bit will auto age out after about 5 minutes if the port does not receive a corresponding group address IGMP report packet.

# 8.16. VLAN Function

The RTL8316B supports a VLAN function to segregate the switch into 32 VLANs. Each VLAN is a broadcast domain and each VLAN may be flexibly configured from 0 to 16 port members. Both port-based and tag-based VLAN functions are supported. The PVID, Tagging Control, and Ingress/Egress rules are manually configured on the VLAN Table at registers 0x030B~0x037C. The VLAN table format is shown as follows:

**Table 11. VLAN Table Format**

| VLAN Entry Index | VID (12-Bit) | Port Member Set (26-bit Bitmap) |
|---|---|---|
| 0 | | |
| 1 | | |
| 2 | | |
| : | | |
| 31 | | |

'VID' defines the 802.1Q VLAN ID. The value of 'VID' may NOT be '0x000' or '0xfff'.

A VLAN is used to divide the broadcast domain to cut broadcast scope. The VLAN Frame Forwarding Rules are defined as follows:

- A received broadcast/multicast frame will be flood forwarded to VLAN member ports only ('Port Member Set' in the VLAN table) of the VLAN except the source port.

- A received unicast frame will be forwarded to its destination port only if the destination port is in the same VLAN as the source port. If the destination port belongs to a different VLAN, the frame will be discarded unless Leaky VLAN control is enabled.

- All VLAN groups share the same layer-2 learned MAC address table (Shared Learning).

## 8.16.1. Port-Based VLAN

By setting the 0x030B register to disable the En8021Qaware control bit, port-based VLAN is enabled and 802.1Q VLAN tagging is ignored. All other VLAN table configurations are the same as tag-based VLAN functions. The VLAN classification of an incoming packet on a port-based VLAN is defined by the port PVID. The RTL8316B uses the Port VLAN Identifier (PVID) to search the VLAN table for the VLAN member.

## 8.16.2. IEEE 802.1Q Tag-Based VLAN

By setting the 0x030B register to enable the En8021Qaware control bit, 802.1Q tag-based VLAN is enabled.

VLAN classification is the first step before VLAN table lookup. The method of assigning a unique VID value to a received packet is as follows:

1. For a VLAN-tagged packet.

    If the tagged 12-bit VID != 0, then the tagged VID value is used.

    If the tagged VID = 0 (Null VID, priority tag), then the port's PVID value is used.

2. For a non-VLAN-tagged packet, the port's 12-bit PVID value is used.

*Note: The 'insert PVID' function for non-VLAN-tagged packets is controlled by registers 0x037D~0x037E).*

After a unique 12-bit VID is assigned, the RTL8316B checks the VLAN table ingress/egress rule, and then forwards the packet to valid destination ports.

## 8.16.3. Ingress/Egress Filtering Control Parameters

Two VLAN filtering rule control parameters are provided on register 0x030B:

- Acceptable frame type control: Admits all frames or admits only VLAN-tagged frames

- Ingress filtering control: Enables filtering of frames received from a port that is not in this port's VLAN group

## 8.16.4. Leaky VLAN

The Leaky VLAN feature enables specific frames to be forwarded between different VLANs.

For example, if the VLAN table entry is:

VLAN 1: Port members = {Port 1, 2, 3}

VLAN 2: Port members = {Port 4, 5, 6}

Normally, broadcast, multicast, and unicast packets are not allowed to be switched between these two VLANs. Port 1 broadcast packets will only flood to Port 2 and 3. A Port 1 unicast packet is not allowed to be forwarded to a member of VLAN 2.

If the Leaky VLAN function is enabled, three types of packets may be forwarded to destination ports outside the current VLAN.

1.    Unicast Packet: May be forwarded to a destination port (L2 table lookup hit) on a different VLAN

2.    ARP Broadcast Packet: May be broadcast to all ports on a switch

3.    IP Multicast Packet: May be flooded to all the multicast address group member set, ignoring the VLAN member set domain limitation

These types of leaky control are used when:

- A switch is divided into multiple VLANs and host to host communication is required between the different VLANs without using a router

- You want to improve router performance

## 8.16.5. Insert/Remove VLAN Priority Tag

The RTL8316B supports Output Priority tagging control via register set 0x0319~0x031B. There are four types of VLAN tagging:

1.    Remove the VLAN tag from all tagged packets

2.    Insert a priority tag into untagged high-priority packets (Set priority field: 7, VID field: 0 for high priority packets)

3.    Insert a priority tag into all untagged packets
      (Set priority field: 7, VID field: 0 for high priority packet. Set priority field: 0, VID field: 0 for low priority packets)

4.    Don't touch (No modification made to the packet)

*Note: This function may be enabled whether the VLAN function is enabled or not.*

# 8.17. QoS Function

The RTL8316B can recognize QoS priority information in an incoming packet and send the packet to different priority queues for different service priority. The RTL8316B identifies the packet's priority based on three types of QoS priority information:

1. Port-based priority

2. IEEE 802.1p/Q VLAN tag

3. TCP/IP TOS/DiffServ (DS) priority field

These three types of QoS can be configured via hardware pins, EEPROM, or Registers 0x0400 ~ 0x0402.

The RTL8316B supports two priority level queues. The queue service rate is based on the Weighted Round Robin algorithm. The packet-based service weight ratio of high-priority and low-priority queuing can be set to 4:1, 8:1, 16:1 or 'Always high priority first'.

## 8.17.1. Port-Based Priority

When port-based priority is applied, any packet received from a high priority port will be treated as a high priority packet.

## 8.17.2. IEEE 802.1p/Q Based Priority

When 802.1p tag priority is applied, the RTL8316B recognizes 802.1Q VLAN tagged packets and extracts the 3-bit User Priority information from the VLAN tag. The RTL8316B sets the User Priority threshold to 3. VLAN tagged packets with User Priority values 4~7 are treated as high priority packets, and other User Priority values (0~3) as low priority packets (follows the IEEE 802.1p standard).

## 8.17.3. Differentiated Services Based Priority

When TCP/IP's TOS/DiffServ (DS) based priority is applied, the RTL8316B recognizes TCP/IP Differentiated Services Codepoint (DSCP) priority information from the DS-field defined in RFC2474. The DS field byte for IPv4 is the Type-of-Service (TOS) octet. Recommended DiffServ Codepoints are defined in RFC2597 for classifying traffic into different service classes. The RTL8316B extracts the codepoint value of the DS field from IPv4 packets and identifies the priority of the incoming IP packet following the definitions listed below:

High Priority.  DS-field = 101110 (EF, Expected Forwarding)

001010; 010010; 011010; 100010 (AF, Assured Forwarding)

11x000 (Network Control)

Low Priority.  DS-field = Other values

VLAN tagged packet formats are shown below:

| 6 bytes | 6 bytes | 2 bytes | 3 bits | 5 bits | | 4 bytes |
|---------|---------|---------|--------|--------|------|---------|
| DA | SA | 81-00 | User Priority (0~3: Low-pri;   4~7: High-pri) | ---- | Data | CRC |

**Figure 4.   802.1Q VLAN Tag Frame Format**

| 6 bytes | 6 bytes | 4 bytes | 2 bytes | 4 bits | 4 bits | 6 bits | 2 bits | | 4 bytes |
|---------|---------|---------|---------|--------|--------|--------|--------|------|---------|
| DA | SA | 802.1Q Tag (Optional) | 08-00 | Version IPv4: 0100 | IHL | TOS[0:5]: DS-field | ---- | Data | CRC |

**Figure 5.   IPv4 Frame Format**

## 8.17.4. Flow Control Auto Turn Off

The RTL8316B can automatically turn off IEEE 802.3x flow control and back pressure flow control for 1~2 seconds whenever the port receives a high priority packet. Flow control is re-enabled when no priority packets are received for 1~2 seconds. This auto-turn off function is enabled via Register 0x0400[2].

## 8.18. Ingress and Egress Bandwidth Control

The RTL8316B supports bandwidth control on all ports. Each port's bandwidth is configurable on both ingress and egress traffic independently. Port bandwidth may be configured to 128kbps, 256kbps, 512kbps, 1Mbps, 2Mbps, 4Mbps, or 8Mbps.

When the ingress or egress traffic bandwidth exceeds the configured threshold, flow control is triggered to limit the throughput. The control description is shown in register 0x020A ~0x0215.

## 8.19. Simple MIB Counter Support

Three 32-bit MIB counters (Counter 1, Counter 2, and Counter 3) are implemented on each port for basic traffic management and diagnostic purposes.

The MIB object of each counter is configurable. The MIB object selection on each counter is shown in Table 12. A detailed description is given in 10.8 MIB Counter Registers, page 57.

**Table 12. MIB Object Selection**

| MIB Object | Counter 1 | Counter 2 | Counter 3 |
|---|---|---|---|
| RX Packet Count | V | - | - |
| RX Byte Count | V | - | - |
| TX Packet Count | - | V | - |
| TX Byte Count | - | V | - |
| Drop Packet Count | - | - | V |
| Drop Byte Count | - | - | V |
| CRC Error Packet Count | V | V | V |
| Collision Count | V | V | V |

## 8.20. *Realtek Remote Control Protocol*

The Realtek Remote Control Protocol (RRCP[®]) is a Realtek proprietary simple and easy device management program that is implemented for in-band remote control purposes.

The protocol is hardware ASIC-based and does not require an external CPU. It allows the system administrator to get/set the switch configuration, to read the statistic counters, and to find RRCP aware devices.

The Remote Management Tool (RMT) software package is bundled with the RTL8316B. The RMT is a Windows-based tool developed to enhance the functionality of Realtek's dumb layer 2 switches via software. The RMT gives network administrators the ability to remotely configure and monitor dumb layer 2 switches as though they were intelligent switches.
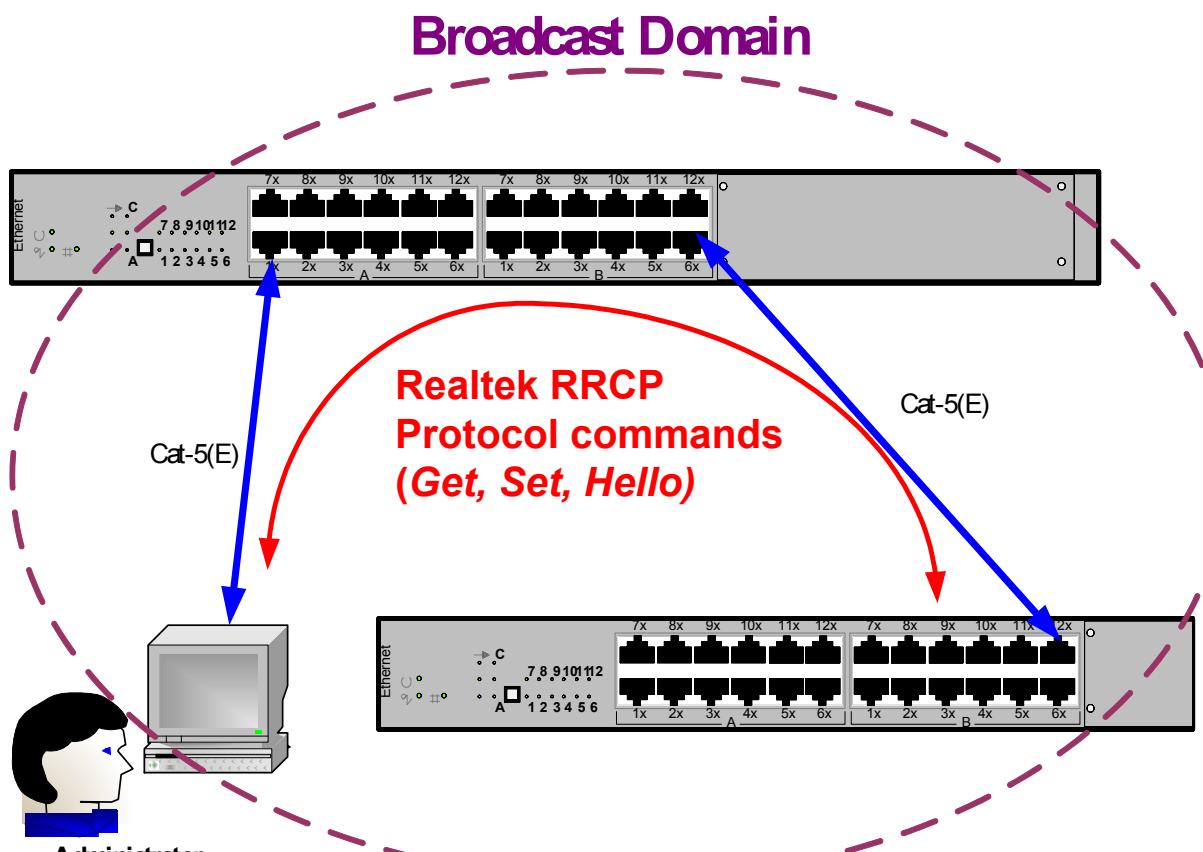
**Figure 6.   Realtek Remote Control Protocol**

# 8.20.1. RRCP® Capabilities

The RRCP is limited to the same network domain.

The RRCP supports the following:

1.    Network Topology Discovery

2.    Get/Set Configuration value of Register

3.    Security Management by an Authentication Key and management port setting

Operation commands are:

Management Operation          (1) register Get

                              (2) register Set

                              (3) Hello

Switch Operation              (1) register Get Reply

                              (2) Hello Reply

The Hello Reply packet reports the switch's link vector information back to the manager (Downlink MAC, Downlink Port), (Uplink MAC, Uplink Port). The link vector information enables discovery of the network topology.

# 8.20.2. Management Security Scheme

Two RRCP security schemes are implemented:

**RRCP Management Authorized Port Control**

An authorized port can be configured via registers 0x0201~0x0202. Only RRCP packets originating from an authorized port will be processed and responded to. Other RRCP with DA=switch's MAC address will be dropped.

**Protocol Authentication Key control**

Each RRCP packet must contain the Authentication Key defined in the register 0x0209. After powering on, the Authentication Key is reset to the default value (0x2379). It can be updated through a valid RRCP Set command or through a Serial CPU interface.

# 8.20.3.  RRCP® Protocol Packet Format

**Hello/Get/Set/Get_Reply Packet Format**

**Table 13. Hello/Get/Set/Get_Reply Packet Format**

| 0 | 8 | 16 | 24 | ~ | 32 |
|---|---|---|---|---|---|
| DA (6) | | | | | |
| DA | | SA (6) | | | |
| SA | | | | | |
| RealtekEtherType (2) | | Protocol (1) | r | OP Code (7bit) | |
| Authentication Key (2) | | Register Address (2) | | | |
| Register Data (4) | | | | | |
| Reserved (4) | | | | | |
| Reserved (4) | | | | | |
| Pad 00 | | | | | |
| : | | | | | |
| : | | | | | |
| CRC (4) | | | | | |

**Hello/Get/Set/Get_Reply Packet Format Description**

**Table 14. Hello/Get/Set/Get_Reply Packet Format Description**

| Field | Length | Description | Value |
|---|---|---|---|
| DA | 6B | Destination MAC Address.<br>-For a Get, Set packet, this is the unicast address of a switch.<br>-For a Get_Reply packet, this is the unicast address of the management station.<br>-For a Hello packet, this can be the unicast address of a switch or a broadcast address to all RRCP aware switches.<br>*Note: If the Authentication Key register has been updated after power on, the switch will only respond to a unicast Hello packet.* | -- |
| SA | 6B | Source MAC address. | -- |
| RealtekEtherType | 2B | Identifies the packet as a Realtek Remote Control packet. The EtherType value=0x8899. | 0x8899 |
| Protocol | 1B | Realtek Proprietary protocol type definition.<br>01: Realtek Remote Control Protocol<br>Others: Reserved | 01h |
| OP Code | 7bit | Operation Code (7bit).<br>Code definition:<br>00: Hello packet<br>01: Get configuration<br>02: Set configuration | -- |

| Field | Length | Description | Value |
|---|---|---|---|
| r | 1 bit | Reply flag.<br>On receiving a control packet reply from the switch to the management station, this flag will be set to 1. Otherwise, this bit should be 0. | Station to switch: 0<br>Switch to station: 1 |
| Authentication Key | 2B | Authentication Key.<br>Used for security of the management operation.<br>The Key value can be modified by the administrator via a remote control packet.<br>A received control packet with a valid Destination MAC address but with an unmatched authentication key will be dropped with no reply. If the DA is a broadcast address or is the address of another switch, it will still be relayed. | Default: 0x2379 |
| Register Address | 2B | Register address of the configuration. | -- |
| Register Data | 2B | Register data of the configuration. | -- |

## Hello_Reply Packet Format

**Table 15. Hello_Reply Packet Format**

| 0 | 8 | 16 | 24 ~ 32 | | |
|---|---|---|---|---|---|
| DA (6) | | | | | |
| DA | | SA (6) | | | |
| SA (=Downlink MAC) | | | | | |
| RealtekEtherType (2) | | Protocol (1) | r | OP Code (7bit) | |
| Authentication Key (2) | | Downlink Port (1) | Uplink Port (1) | | |
| Uplink MAC (6) | | | | | |
| Uplink MAC | | Chip ID (2) | | | |
| Vender ID (4) | | | | | |
| Pad 00 | | | | | |
| : | | | | | |
| : | | | | | |
| CRC (4) | | | | | |

## Hello_Reply Packet Format Description

**Table 16. Hello_Reply Packet Format Description**

| Field | Length | Description | Default |
|---|---|---|---|
| Downlink Port | 1B | Downlink Port number of the link vector.<br>Indicates the port number on the Hello Reply switch that is connected to the Uplink switch.<br>This is set by the Hello reply switch. | -- |
| Uplink Port | 1B | Uplink Port number of the link vector.<br>Indicates the port number of the Uplink switch that is connected to the Hello reply switch.<br>This is set by the Uplink switch. | 00h<br>Updated by the Uplink_MAC switch |
| Uplink MAC | 6B | The MAC address of the Uplink switch.<br>The default value is 000000000000h and is updated by the Uplink switch.<br>When a switch receives a Hello_Reply frame with zero UplinkMAC, then it will enter the SA MAC address here. | 0 |
| Chip ID | 2B | Realtek Chip ID.<br>This is set by the Hello_Reply switch.<br>Each Realtek switch controller that is aware of the RRCP has a unique Chip ID (see 11.3.6 0x0206H: Chip Model ID, page 67). | EEPROM |
| Vender ID | 4B | Vender ID.<br>This is set by the Hello_Reply switch.<br>The 4-byte vender ID is reserved for the system vender to configure its company name or the device model ID. | EEPROM |

# 8.21. *Network Loop Connection Fault Detection*

The RTL8316B periodically transmits a Realtek-EtherType (=0x8899) protocol frame to detect network loop faults.

- Normal transmission time interval is five minutes

- If a port detects a loop, the loop event flag will be set (register 0x0101) and the transmission time interval will change to one second to speed up the new topology change detection

- The loop event flag will be cleared and the transmission time interval will return to five minutes if the port does not receive a self-loop detect packet for 3 seconds

**Loop Detect Packet Format**

The Loop Detect Packet Format is shown below:

**Table 17. Loop Detect Packet Format**

| 0 | 8 | 16 | 24 | ~ | 32 |
|---|---|---|---|---|---|
| DA (6) [=0xffffffffffff] | | | | | |
| DA | | SA (6)[=Switch MAC] | | | |
| SA | | | | | |
| RealtekEtherType (2) [=0x8899] | | Protocol (1) [=03] | | Pad 0000 | |
| Pad 00000000 | | | | | |
| : | | | | | |
| : | | | | | |
| CRC (4) | | | | | |

# 8.22. Realtek Echo Protocol

The Realtek Echo Protocol (REP) supports the Layer 2 Echo test. It is easy for a host to do network connection diagnostics through a simple test packet, with or without other hosts on the network. No IP assignment is required.

When the RTL8316B receives a REP packet, it replies by sending the original REP frame to the source MAC address with the DA and SA exchanged.

**Realtek Echo Protocol Frame**

The REP frame format is shown below:

| 0 | 8 | 16 | 24 | ~ | 32 |
|---|---|---|---|---|---|
| DA (6) [=0xffffffffffff] | | | | | |
| DA | | SA (6)[=Switch MAC] | | | |
| SA | | | | | |
| RealtekEtherType (2) [=0x8899] | | Protocol (1) [=02] | | Pad 0000 | |
| Pad 00000000 | | | | | |
| : | | | | | |
| : | | | | | |
| CRC (4) | | | | | |

**Figure 7.   Realtek Echo Protocol Frame**

# 8.23. Port Security Control

The RTL8316B supports a scheme for port security control by per-port disabling of MAC address auto-learning (register 0x0301~0x0302) and enabling of dropping packets with an unknown destination MAC address (register 0x0300). This feature requires that the MAC table aging process is disabled (to keep the known MAC address table static). If port security control is enabled, all incoming packets with unknown destination MAC addresses will be dropped. A detected unknown source MAC address will be captured on register 0x0303~0x0306.

The RTL8316B also supports a fast aging time setting (12 seconds) to quickly refresh the MAC address table (register 0x0300). A detailed description is given in Table 68, page 72, register 0x0300 ~ 0x0306.

# 8.24. Disable Port

A port can be disabled via the Port Disable Control Register (register 0x0608~0x0609). When a port is disabled, the port will cease all packet transmission and reception except for Realtek Remote Control Protocol (RRCP) packets. The physical link status is not changed.

# 8.25. *Port Properties Configuration*

The RTL8316B supports a flexible method to configure port properties via the PHY MII registers. Configurable properties include Media Speed (10M/100M), Duplex Mode, and 802.3x PAUSE flow control. The properties of each can be configured by auto-negotiation or forced mode (auto negotiation disabled).

The port link state will be reported in the port Link Status registers. The configuration description is shown in registers 0x060A ~ 0x0624.

The following shows how to configure the Pause and Asymmetric Pause ability on port property registers (0x060A~0x0615) to get an expected negotiation result.

**Table 18. Configuring Pause and Asymmetric Pause**

| PAUSE | Asymmetric PAUSE | Expected PAUSE Result |
|---|---|---|
| 0 | 0 | Disable |
| 0 | 1 | Asymmetric to Link Partner |
| 1 | 0 | Symmetric |
| 1 | 1 | Asymmetric to Link Local or Symmetric |

When a port is configured to 'Forced Mode' (auto negotiation disabled), the following table shows how to configure flow control ability (TX pause/RX pause) on port property registers (0x060A~0x0615) to get an expected negotiation result.

**Table 19. TX/RX Pause Ability in Forced Mode**

| (0x060A~0x0615) bit[6] Asymmetric PAUSE | (0x060A~0x0615) bit[5] Asymmetric PAUSE | RTL8316B Flow Control Ability |
|---|---|---|
| 0 | 0 | RX pause ability only |
| 0 | 1 | No Flow Control ability |
| 1 | 0 | TX pause ability only |
| 1 | 1 | Both TX/RX pause ability |

# 8.26. Serial CPU Interface

The RTL8316B supports a serial CPU interface (Slave mode) that shares the same hardware pin (SCK, SDA) as the EEPROM interface (Master mode). The EEPROM and Serial interface can coexist by assigning a different device ID. Define EEPROM device ID=1010-000, RTL8316B device ID=1010-100. The interface is compatible with EEPROM 24LC024.
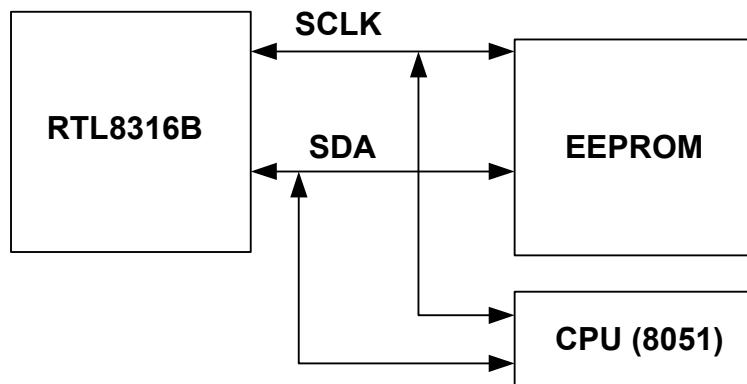


**Figure 8. Serial CPU Interface**

The serial CPU interface is enabled after the EEPROM download has finished. When operating in serial CPU mode the SCK is an input pin. The SDA is an IO pin with internal pull high.

## 8.26.1. Serial-CPU Access Format

In Serial CPU mode, 16-bit and 32-bit data access are both supported by the RTL8316B. The Serial Read Write access format is as follows.

- 16-bit Address (MSB first)
- 16/32-bit data Burst Read (Low byte (Byte0) first; MSB first)
- 16/32-bit data Burst Write (Low byte (Byte0) first; MSB first)

*Note: Each burst is one byte.*

**Start and Stop Definition (START; STOP)**

A high-to-low transition of SDA with SCLK high is a START condition and it must precede any other command.

A low-to-high transition of the SDA line while the clock (SCLK) is HIGH determines a STOP condition. All operations must end with a STOP.
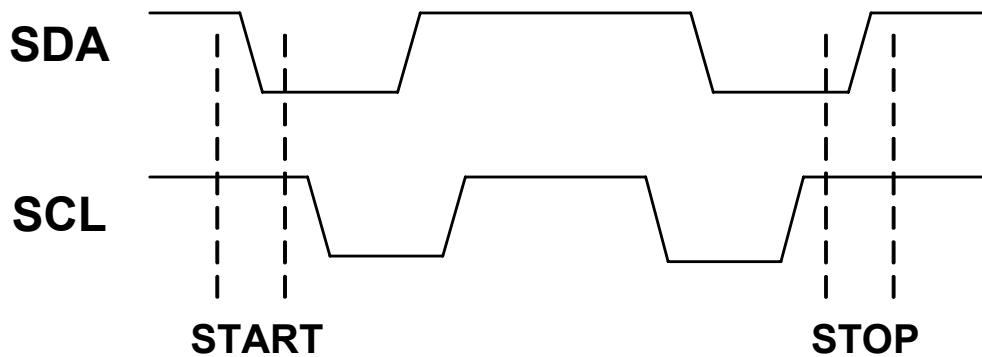
**Figure 9.   Start and Stop Definition**

### Output Acknowledge (ACK)

When addressed, each receiving device is obliged to generate an acknowledgment after reception of each byte.

The master device must generate an extra clock pulse that is associated with this acknowledgement bit.
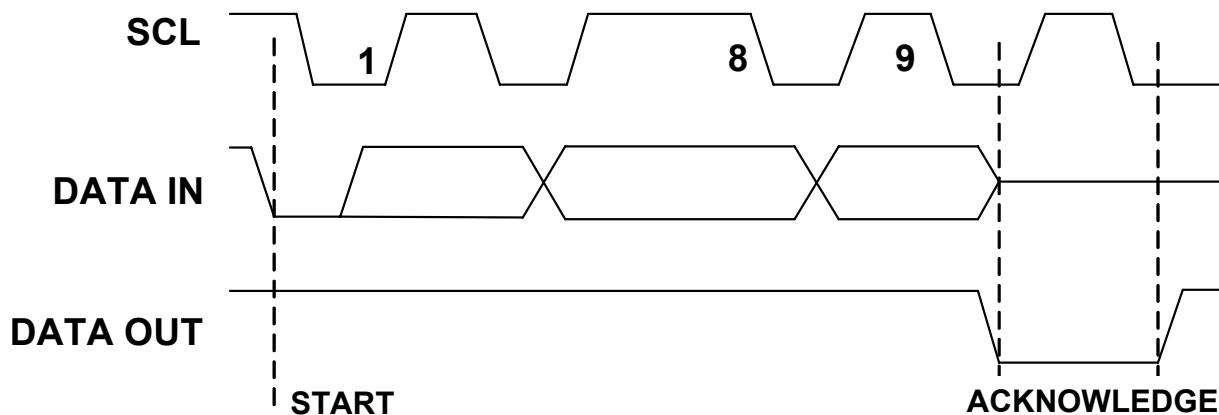


**Figure 10. Output Acknowledge (ACK)**

### Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

## Serial CPU 16-Bit Read/Write Format

**Table 20.  Serial CPU 16-Bit Read/Write Format**

| Bit Width | 1 | 4 | 3 | 1 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Operation | Start Bit | Control code | Chip Select | RW | Ack | Reg. Addr. [7:0] (MSB first) | Ack | Reg. Addr. [15:8] (MSB first) | Ack | Reg. Data. [7:0] (MSB first) | Ack | Reg. Data [15:8] (MSB first) | Ack | Stop Bit |
| 16-bit Read | Start | 1010 | 100 | 1 | 0 (*A) | Write Data | 0 (*A) | Write Data | 0 (*A) | Read Data | 0 (*B) | Read Data | 1 (*B) | Stop |
| 16-bit Write | Start | 1010 | 100 | 0 | 0 (*A) | Write Data | 0 (*A) | Write Data | 0 (*A) | Write Data | 0 (*A) | Write Data | 1 (*A) | Stop |

*Note: *A = ACK by RTL8316B.  *B = ACK by CPU*

## Serial CPU 32-Bit Read Format

**Table 21.  Serial CPU 32-Bit Read Format**

| Bit Width | 1 | 4 | 3 | 1 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Operation | Start Bit | Control code | Chip Select | RW | Ack | Reg. Addr. [7:0] (MSB first) | Ack | Reg. Addr. [15:8] (MSB first) | Ack | Reg. Data. [7:0] (MSB first) | Ack | Reg. Data. [15:8] (MSB first) | Ack | Reg. Data. [23:16] (MSB first) | Ack | Reg. Data [31:24] (MSB first) | Ack | Stop Bit |
| 32-bit Read | Start | 1010 | 100 | 1 | 0 (*A) | Write Data | 0 (*A) | Write Data | 0 (*A) | Read Data | 0 (*B) | Read Data | 0 (*B) | Read Data | 0 (*B) | Read Data | 1 (*B) | Stop |

*Note: *A = ACK by RTL8316B.  *B = ACK by CPU*

## 8.26.2. EEPROM RW Command Format

The RTL8316B provides a self-Read/Write EEPROM function, which can save and recall user configuration via the Realtek Remote Management Tool (RMT). Read/Write EEPROM function control is via register 0x0217~0x0218.

**Table 22. 0x0217H: EEPROM RW Command Register**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 7:0 | EEPROM Address | Assigns EEPROM address bits | RW | 0 |
| 10:8 | CHIP_SEL[2:0]] | Assigns chip selection bits | RW | 0 |
| 11 | Read/Write Operation | 0: Write Operation<br>1: Read Operation | RW | 0 |
| 12 | Status | 0: Idle<br>1: Busy | RW | 0 |
| 13 | Operation Success status | 0: Operation Succeeded<br>1: Operation Failed<br>(Read to Clear) | RW | 0 |
| 15:14 | Reserved | | | |

**Table 23. 0x0218H: EEPROM RW Data Register**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 7:0 | WdataEE[7:0] | Data to be written to EEPROM | RW | 0 |
| 15:8 | RdataEE[15:8] | Data Read from EEPROM | R | 0 |

**EEPROM Read/Write Procedure**
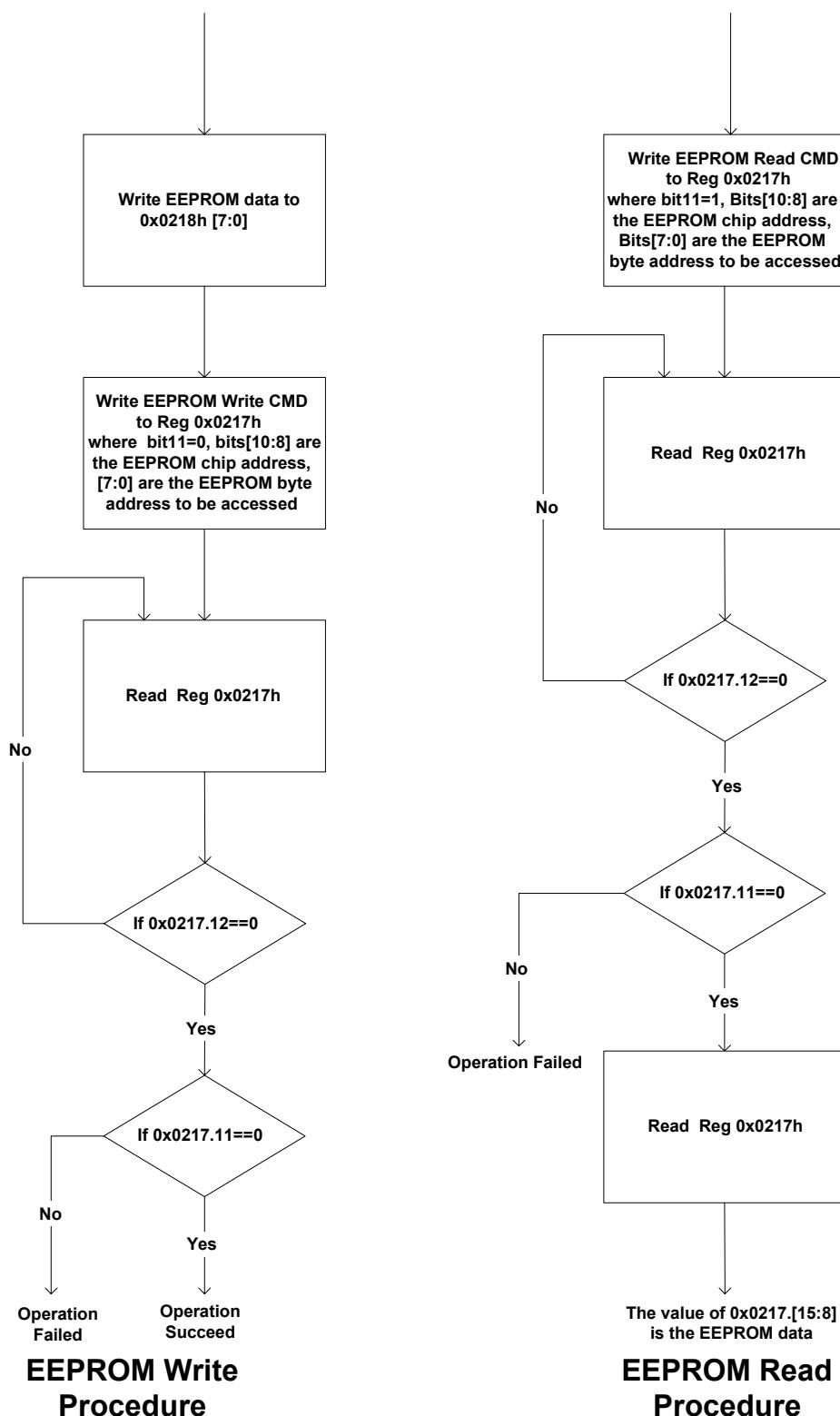


**Figure 11. EEPROM Read/Write Procedure**

# 8.27. *PHY Serial Management Interface*

The RTL8316B supports PHY management through the serial MDIO and MDC signal (SMI) to start the auto-negotiation process. After a power-on reset, the RTL8316B writes its abilities to the advertisement registers 0, 4, and 9 of the connected PHY and commands the PHY to restart the auto negotiation process. The PHY device address setting is defined as:

Address 16~31 for Fast Ethernet ports 0~15

After restarting auto-negotiation, the RTL8316B will continuously read the link status and abilities of local and link partners to determine the link state.

Port properties (speed, duplex, 802.3x flow control) can be configured via auto-negotiation or force mode. The configuration is described in register 0x060A ~ 0x0615. The final link status is reported in register 0x0619~0x0624.

## 8.27.1. SMI (MDC, MDIO) Interface

**SMI (MDC, MDIO) Management Packet Format**

**Table 24. SMI (MDC, MDIO) Management Packet Format**

| Management Frame Fields | | | | | | | |
|---|---|---|---|---|---|---|---|
| | PRE | ST | OP | PHYAD | REGAD | TA | DATA | IDLE |
| **Read** | 1…1 | 01 | 10 | AAAAA | RRRRR | Z0 | DDDDDDDDDDDDDDDD | Z |
| **Write** | 1…1 | 01 | 01 | AAAAA | RRRRR | 10 | DDDDDDDDDDDDDDDD | Z |

## 8.27.2. PHY Register Indirect Access

The RTL8316B supports the ability to randomly access PHY registers through a set of control registers at 0x0500~0x0502. Users need to define the PHY address ID, PHY Register ID, Data content of the write command, and operating command type (Read or Write) on the above registers. Then the RTL8316B will auto process the PHY Read/Write access through the MDC/MDIO interface.

**Read PHY Register Procedure**

Configure PHY Access Control Register (0x0500)

Read the result on PHY Access Read Data Register (0x0502)

**Write PHY Register Procedure**

Write the PHY Access Write Data Register (0x0501)

Configure the PHY Access Control Register (0x0500)

**PHY Address ID Definition**

The PHY address ID corresponds to the port location. The PHY address ID of Ports 0~15 are 0x10, 0x11, 0x12 …., 0x1F.

# 8.28. LED Interfaces

The RTL8316B provides a flexible per-port LED display to show the per-port link status and diagnostic information. Both a parallel and serial interface are provided to drive the LEDs.

During power on reset, the parallel LED signals are driven low and the serial interface shifts to a low value for about two seconds to turn on all the LEDs for testing purposes.

# 8.29. Parallel LED Interface

The parallel interface only provides a system status LED.

LED signals include: LED_loopDet, LED_EnTrunk[3:0].

# 8.30. Serial LED Interface

The serial interface, SLED_CLK, and SLED_DATA provide clock and data to enable the external shift registers 74164 to capture the per-port link status and diagnostic information.

Another pin, LED_DMODE_CLK, provides the diagnostic items selection control. Each pulse signal input from this pin changes the diagnostic item to be displayed on the diagnostic LED.

Each port provides three port-state LEDs (StateLED) and one diagnostic LED (DiagLED). The LED display type can be flexibly configured and can be enabled or disabled to achieve the optimal BOM cost.

The LED display configuration is controlled by register 0x0005h 'LED Display Configuration Register', and can also be configured via EEPROM.

The StateLED display is defined by StatLED_mode[2:0] on register 0x0005. The available display types are shown in the following table.

**Table 25. Serial LED Interface**

| StatLEDn_mode[2:0] | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
|---|---|---|---|---|---|---|---|---|
| StateLEDn Display Type | Link /Act | 100Spd | Duplex /Col | Link/Act /100Spd | Duplex | Act | Link | Col |

The display items of the diagnostic LED (DiagLED) are internally defined and are as follows:

**Table 26. Diagnostic LED Display**

| Item | Description |
|---|---|
| (DiagItem_0) DisablePort/RxError | ON: Disabled port<br>Blinking: RX CRC error |
| (DiagItem_1) FlowControl/FCActive | ON: Flow control enabled<br>Blinking: Flow control active |
| (DiagItem_2) TrunkPort/TKFault | ON: Trunking enabled port<br>Blinking: Trunk fault warning |
| (DiagItem_3) HighPriorityPort | ON: High priority port |
| (DiagItem_4) LoopDetectPort | ON: Network loop connection fault detect |
| (DiagItem_5) BroadcastStormAlarmPort | ON: Broadcast Storm Alarm port |
| (DiagItem_6) NULL | Reserved |
| (DiagItem_7) NULL | Reserved |

The DiagLED display item is changed by a trigger signal input from hardware pin 'LED_DMODE_CK'. The change sequence order of the DiagLED is:

DiagItem_0 → DiagItem_1→ DiagItem_2→ ……. → DiagItem_7→ Loop to DiagItem_0

## 8.30.1. Serial LED Display Panel Example (4 LEDs, Register 0x0005)

**Enable Serial LED Display Mode:**

➔ set EnSerialMode: 1

**Define Per-port 4 LED Display Mode:**

➔ Configuration. set EnLED[3:0]: 1111

**Define the statLED display type as: StatLED0=Link/Act, StatLED1=10/100M, StatLED2=Duplex/Collision:**

➔ Configuration. set StatLED0_mode[2:0]=000, StatLED1_mode[2:0]=001, StatLED2_mode[2:0]=010

Follow the same method to configure the per-port 1 LED, per-port 2 LED, and per-port 3 LED display mode, with or without enabling the diagnostic LED.

The LED panel is shown in Figure 12.
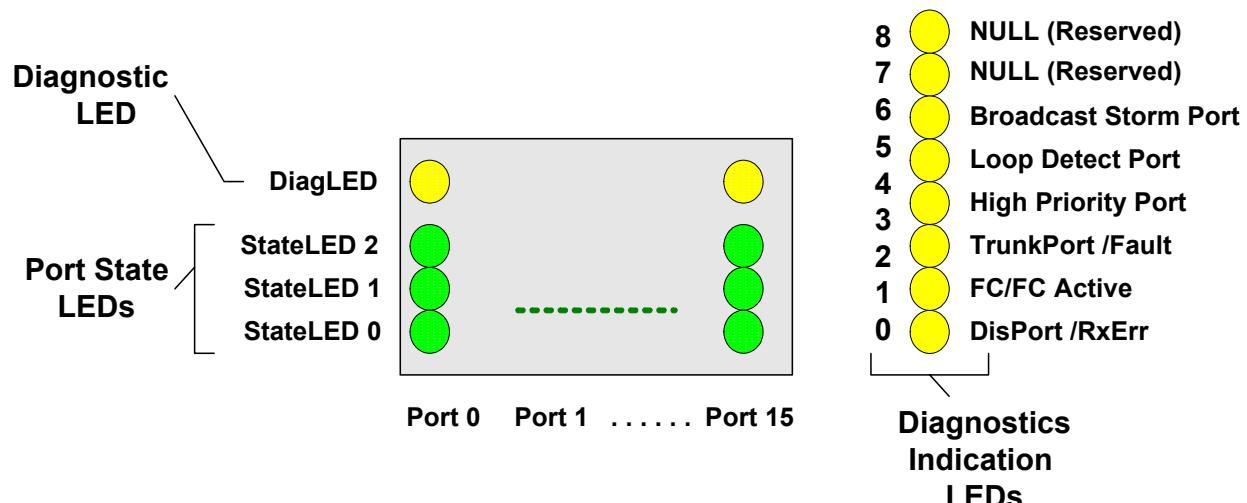


**Figure 12. Serial LED Display**

## 8.30.2. Serial LED Shift Out Sequence Order

The Serial LED output sequence is defined as follows: (first bit →….→ last bit).

Each port has four LEDs. There are eight diagnostic LEDs:

> → [P0 StateLED0] → [P0 StateLED1] → [P0 StateLED2] → [P0 DiagLED0]
> → [P1 StateLED0] → [P1 StateLED1] → [P1 StateLED2] → [P1 DiagLED0]
> →- - - - - - -- - - - →- - - - - -- - - - -→- - - - - -- - - - →- - - - - -- - - -
> → [P25 StateLED0]     → [P25 StateLED1]     →[P25 StateLED2]     → [P25 DiagLED0]
> → [Reserved_(DiagS0)] → [Reserved_(DiagS1)] → [Reserved_(DiagS2)] → [Reserved_(DiagS3)]
> → [Reserved_(DiagS4)] → [Reserved_(DiagS5)] → [Reserved_(DiagS6)] → [Reserved_(DiagS7)]

# 8.31.  SCAN LED Interface

The RTL8316B supports Scan LED display mode. The forms of LED status streams, as shown below, are controlled by HW pin LEDMODE[1:0] = 2b'00 , and are latched upon reset.

**Table 27. Scan LED Status**

| LED Status | Description |
|---|---|
| Spd | Speed Indicator |
| | High for 100Mbps and low for 10Mbps |
| Link/Act | Link, Activity Indicator |
| | High for link established |
| | Blinks when the corresponding port is transmitting or receiving |
| Col/Fulldup | Full duplex, Collision Indicator |
| | High for full duplex, and low for half duplex mode |
| | Blinks when there are collisions on the corresponding port |

The RTL8316B provides three Scan LED groups that display each port's status:

**Group A**
(Scan_LEDA[5:0], Scan_STSA[3:0]) displays status for port0~port7

**Group B**
(Scan_LEDB[5:0], Scan_STSB[3:0]) displays status for port8~port15

**Group C**
(Scan_LEDC[5:0], displays status for applications

Scan_LEDA[5:0], Scan_LEDB[5:0] and Scan_LEDC[5:0] operate with the same timing phase. The Scan LED timing diagram is shown in Figure 13, on page 46.

## Scan LED Timing Diagram
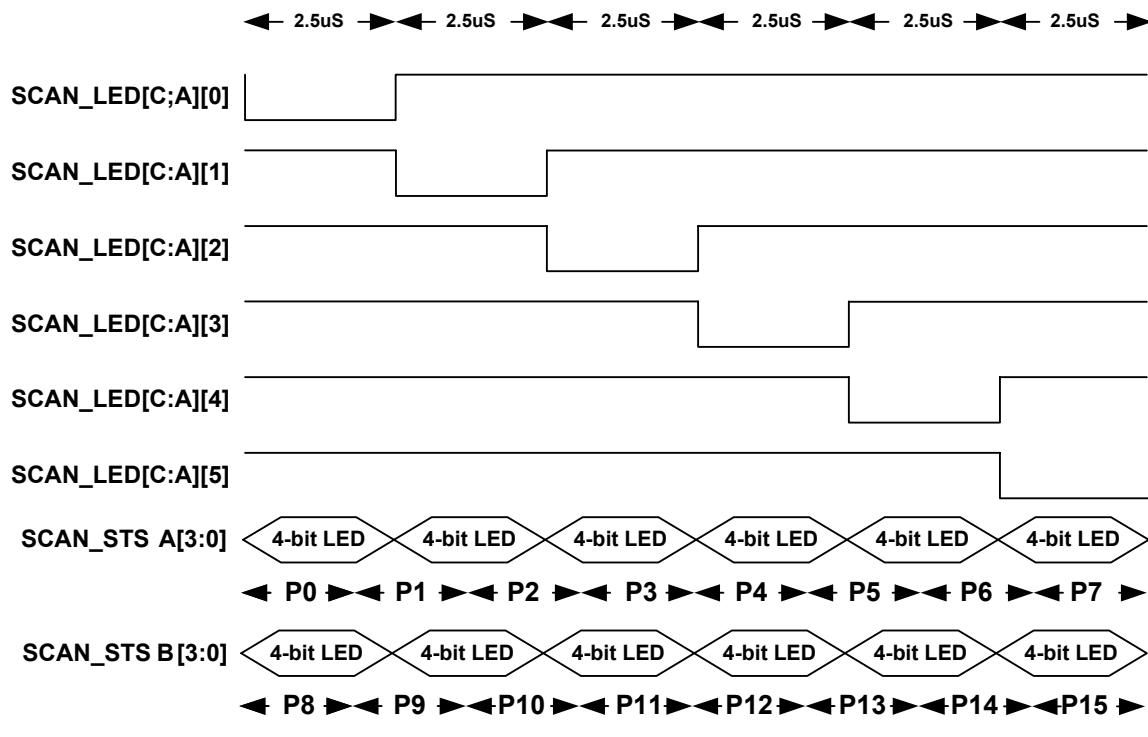


**Figure 13. Scan LED Timing Diagram**

**External circuit for Scan LED**

## RTL8316B
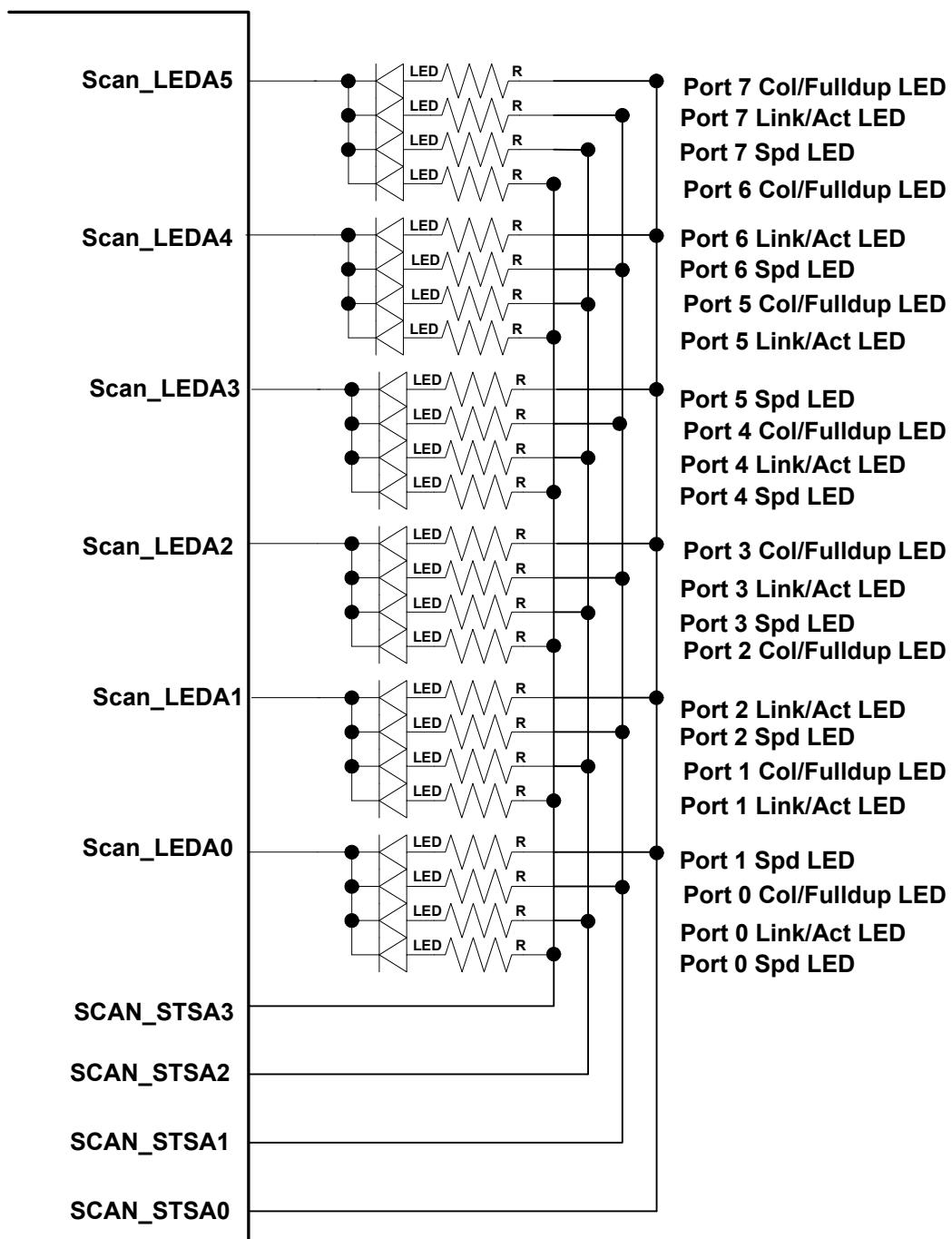


**Figure 14. External Circuit for Scan LED**

# 8.32. Port Mirroring

Port mirroring is used to forward traffic to a selected port based on one or more of the following:

- All traffic received from one or multi selected source ports (source mirroring)
- All traffic transmitted to one selected destination port (destination mirroring)

**Table 28. Port Mirror Control Register for P15-P0**

| Register | Bits | Name | Description | RW | Default |
|---|---|---|---|---|---|
| 0x0219 | 15:0 | EnPortMirror(0)[15:0] | Enables the port-based mirror function. Bit n corresponds to port n. Write '1' to enable a port's mirror function | RW | 0 |

**Table 29. RX Mirror Port Register  for P15-P0**

| Register | Bits | Name | Description | RW | Default |
|---|---|---|---|---|---|
| 0x021B | 15:0 | Mirror_RX(0)[15:0] | Bit n corresponds to port n. Write '1' to duplicate port n RX data to mirrored port. | RW | 0 |

**Table 30. TX Mirror Port Register for P15-P0**

| Register | Bits | Name | Description | RW | Default |
|---|---|---|---|---|---|
| 0x021D | 15:0 | Mirror_TX(0)[15:0] | Bit n corresponds to port n. Write '1' to duplicate port n TX data to mirrored port. | RW | 0 |

# 9.    Serial EEPROM Configuration (24LC024)

The EEPROM configuration bits are directly mapped to some of the internal registers. For example, EEPROM addresses 0x00h and 0x01h directly map to internal register 0x0002 'RX IO PAD Delay Configuration'.

The mapping rule is: EEPROM 0x00h: REG. 0x0002[7:0], EEPROM 0x01h: REG. 0x0002[15:8].

## 9.1.    EEPROM Configuration vs. Internal Register Mapping

**Table 31. EEPROM Configuration vs. Internal Register Mapping**

| EEPROM Physical Address (8-Bit Data Entry) (24LC02) | Description | Corresponding Internal Register Address Mapping | Internal Default |
|---|---|---|---|
| 01~00 | RX IO PAD Delay Configuration bit[5:0] value must be "000000" (bit 5 is used for BIST enable/disable of CP test) | 0x0002 | 0A80 |
| 03~02 | TX IO PAD Delay Configuration | 0x0003 | 0155 |
| 05~04 | LED Display Configuration 0 | 0x0005 | 0E88 |
| 07~06 | LED Display Configuration 1 | 0x0006 | -- |
| 09~08 | Reserved | | |
| 0B~0A | Reserved | | |
| 0D~0C | Realtek Protocol Control | 0x0200 | 0000 |
| 0F~0E | RRCP security Mask Configuration 0 | 0x0201 | 0000 |
| 11~10 | RRCP security Mask Configuration 1 | 0x0202 | 0000 |
| 13~12 | Switch MAC ID 0 | 0x0203 | 0000 |
| 15~14 | Switch MAC ID 1 | 0x0204 | 0000 |
| 17~16 | Switch MAC ID 2 | 0x0205 | 0000 |
| 19~18 | Chip ID 0 | 0x0206 | 0000 |
| 1B~1A | Vender ID 0 | 0x0207 | 0000 |
| 1D~1C | Vender ID 1 | 0x0208 | 0000 |
| 1F~1E | Reserved | | |
| 21~20 | Reserved | | |
| 23~22 | ALT Configuration | 0x0300 | 0004 |
| 25~24 | Port Trunking Configuration | 0x0307 | 0000 |
| 27~26 | IGMP Control Register | 0x0308 | 0000 |
| 29~28 | VLAN Control Register | 0x030B | 0000 |
| 2B~2A | Reserved | | |
| 2D~2C | Reserved | | |
| 2F~2E | QoS Control Register | 0x0400 | 0010 |
| 31~30 | Port Priority Configuration 0 | 0x0401 | 0000 |
| 33~32 | Port Priority Configuration 1 | 0x0402 | 0000 |
| 35~34 | Reserved | | |
| 37~36 | Reserved | | |
| 39~38 | Global Port Control Register | 0x0607 | 0010 |

| EEPROM Physical Address (8-Bit Data Entry) (24LC02) | Description | Corresponding Internal Register Address Mapping | Internal Default |
|---|---|---|---|
| 3B~3A | Port property Configuration 0 | 0x060A | AFAF |
| 3D~3C | Port property Configuration 1 | 0x060B | AFAF |
| 3F~3E | Port property Configuration 2 | 0x060C | AFAF |
| 41~40 | Port property Configuration 3 | 0x060D | AFAF |
| 43~42 | Port property Configuration 4 | 0x060E | AFAF |
| 45~44 | Port property Configuration 5 | 0x060F | AFAF |
| 47~46 | Port property Configuration 6 | 0x0610 | AFAF |
| 49~48 | Port property Configuration 7 | 0x0611 | AFAF |
| 4B~4A | Port property Configuration 8 | 0x0612 | AFAF |
| 4D~4C | Port property Configuration 9 | 0x0613 | AFAF |
| 4F~4E | Port property Configuration 10 | 0x0614 | AFAF |
| 51~50 | Port property Configuration 11 | 0x0615 | AFAF |
| 53~52 | Internal use | 0x0616 | -- |
| 55~54 | Reserved | | |
| 57~56 | Reserved | | |
| 59 ~~~ 5F | Reserved | | |
| 61~60 | Designer Diagnostic Configuration | 0xFFFF | 0000 |

# 10.    Internal Register Descriptions

Symbols:

R:      Read                          V:      Configurable

W:      Write                         P:      Partially Configurable

RW:     Read/Write                    X:      Not Configurable

## 10.1. System Configuration Registers

**Table 32. System Configuration Registers**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0000 | 0 | System Reset | RW | 0 | X | X |
| | 1 | Switch Parameter Register | R(W) | 0x84A0 | X | X |
| | 2 | EEPROM Check ID | R | 0 | X | V |
| | 3 | Reserved | | | | |
| | 4 | LED MODE | RW | 0001 | X | X |
| | 5 | LED Display Configuration 0 | RW | 1E88 | X | V |
| | 6 | LED Display Configuration 1 | RW | 0C00 | X | V |

## 10.2. System Status Registers

**Table 33. System Status Registers**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0100 | 0 | Board Trapping Status | R (/W) | 0C01 | X | X |
| | 1 | Loop Detect Status Register(32 bit Reg ) | R | 0 | X | X |
| | 2 | System Fault Flag Register | R | 0 | X | X |

## 10.3. Management Configuration Registers

**Table 34. Management Configuration Registers**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0200 | 0 | Realtek Protocol Control | RW | 0001 | X | V |
| | 1 | RRCP Security Mask Configuration (0) | RW | 0 | X | V |
| | 2 | RRCP Security Mask Configuration (1) | RW | 0 | X | V |
| | 3 | Switch MAC ID  (0) | R | 0 | X | V |
| | 4 | Switch MAC ID  (1) | R | 0 | X | V |

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| | 5 | Switch MAC ID (2) | R | 0 | X | V |
| | 6 | Chip ID (RO) | R | 0 | X | V |
| | 7 | Vender ID (0) (RO) | R | 0 | X | V |
| | 8 | Vender ID (1) (RO) | R | 0 | X | V |
| | 9 | RRCP Pass word | RW | 0x2379 | X | X |
| | 0A | Port Rate Control Register. | RW | 0 | X | X |
| | 0B | Port Rate Control Register. | RW | 0 | X | X |
| | 0C | Port Rate Control Register. | RW | 0 | X | X |
| | 0D | Port Rate Control Register. | RW | 0 | X | X |
| | 0E | Port Rate Control Register. | RW | 0 | X | X |
| | 0F | Port Rate Control Register. | RW | 0 | X | X |
| | 10 | Port Rate Control Register. | RW | 0 | X | X |
| | 11 | Port Rate Control Register. | RW | 0 | X | X |
| | 12 | Port Rate Control Register. | RW | 0 | X | X |
| | 13 | Port Rate Control Register. | RW | 0 | X | X |
| | 14 | Port Rate Control Register. | RW | 0 | X | X |
| | 15 | Port Rate Control Register. | RW | 0 | X | X |
| | 16 | Reserved | | | | |
| | 17 | EEPROM RW Command Register | RW | 0 | X | X |
| | 18 | EEPROM RW Data Register | R(/W) | 0 | X | X |
| | 19 | Port Mirror Control Register for P15-P0 | RW | 0 | X | X |
| | 1A | Port Mirror Control Register for P23-P16 | RW | 0 | X | X |
| | 1B | RX Mirror port mask for P15-P0 | RW | 0 | X | X |
| | 1C | RX Mirror port mask for P23-P16 | RW | 0 | X | X |
| | 1D | TX Mirror port mask for P15-P0 | RW | 0 | X | X |
| | 1E | TX Mirror port mask for P23-P16 | RW | 0 | X | X |

# 10.4. Address Lookup Table (ALT) Control Register

**Table 35. Address Lookup Table (ALT) Control Register**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0300 | 0 | ALT Configuration | RW | 0 | P | P |
| | 1 | Address Learning Control (0) | RW | 0 | X | X |
| | 2 | Address Learning Control (1) | RW | 0 | X | X |
| | 3 | Unknown SA Management 0 (RO) (0) | R | -- | X | X |
| | 4 | Unknown SA Management 0 (RO) (1) | R | -- | X | X |
| | 5 | Unknown SA Management 0 (RO) (2) | R | -- | X | X |
| | 6 | Unknown SA Management 1(RO) | R | -- | X | X |
| | 7 | Port Trunking Configuration | RW | 8200 | P | V |
| | 8 | IGMP Control Register | RW | 8200 | V | V |
| | 9 | IP Multicast Router Discovery | R | 0 | X | X |

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| | 0A | RSVD | | 0 | | |
| | 0B | VLAN Control Register | RW | 0 | P | V |
| | 0C | Port VLAN ID Assignment (0) | RW | 0100 | X | X |
| | 0D | Port VLAN ID Assignment (1) | RW | 0302 | X | X |
| | 0E | Port VLAN ID Assignment (2) | RW | 0504 | X | X |
| | 0F | Port VLAN ID Assignment (3) | RW | 0706 | X | X |
| | 10 | Port VLAN ID Assignment (4) | RW | 0908 | X | X |
| | 11 | Port VLAN ID Assignment (5) | RW | 0B0A | X | X |
| | 12 | Port VLAN ID Assignment (6) | RW | 0D0C | X | X |
| | 13 | Port VLAN ID Assignment (7) | RW | 0F0E | X | X |
| | 14 | Reserved | | | | |
| | 15 | Reserved | | | | |
| | 16 | Reserved | | | | |
| | 17 | Reserved | | | | |
| | 18 | Reserved | | | | |
| | 19 | VLAN TX Priority Tagging Control  (0) | RW | FFFF | X | X |
| | 1A | VLAN TX Priority Tagging Control  (1) | RW | FFFF | X | X |
| | 1B | Reserved | | | | |
| | 1C | Reserved | | | | |
| | | Port VLAN Configuration ( 32*[0,1,2]) | RW | | X | X |
| | 1D | VLAN_0_Entry_Configuration_0 (member[15:0]) | RW | 0001 | X | X |
| | 1E | Reserved | | | | |
| | 1F | VLAN_0_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 20 | VLAN_1_Entry_Configuration_0 (member[15:0]) | RW | 0002 | X | X |
| | 21 | Reserved | | | | |
| | 22 | VLAN_1_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 23 | VLAN_2_Entry_Configuration_0 (member[15:0]) | RW | 0004 | X | X |
| | 24 | Reserved | | | | |
| | 25 | VLAN_2_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 26 | VLAN_3_Entry_Configuration_0 (member[15:0]) | RW | 0008 | X | X |
| | 27 | Reserved | | | | |
| | 28 | VLAN_3_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 29 | VLAN_4_Entry_Configuration_0 (member[15:0]) | RW | 0010 | X | X |
| | 2A | Reserved | | | | |
| | 2B | VLAN_4_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 2C | VLAN_5_Entry_Configuration_0 (member[15:0]) | RW | 0020 | X | X |
| | 2D | Reserved | | | | |
| | 2E | VLAN_5_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 2F | VLAN_6_Entry_Configuration_0 (member[15:0]) | RW | 0040 | X | X |
| | 30 | Reserved | | | | |
| | 31 | VLAN_6_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 32 | VLAN_7_Entry_Configuration_0 (member[15:0]) | RW | 0080 | X | X |
| | 33 | Reserved | | | | |

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| | 34 | VLAN_7_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 35 | VLAN_8_Entry_Configuration_0 (member[15:0]) | RW | 0100 | X | X |
| | 36 | Reserved | | | | |
| | 37 | VLAN_8_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 38 | VLAN_9_Entry_Configuration_0 (member[15:0]) | RW | 0200 | X | X |
| | 39 | Reserved | | | | |
| | 3A | VLAN_9_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 3B | VLAN_10_Entry_Configuration_0 (member[15:0]) | RW | 0400 | X | X |
| | 3C | Reserved | | | | |
| | 3D | VLAN_10_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 3E | VLAN_11_Entry_Configuration_0 (member[15:0]) | RW | 0800 | X | X |
| | 3F | Reserved | | | | |
| | 40 | VLAN_11_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 41 | VLAN_12_Entry_Configuration_0 (member[15:0]) | RW | 1000 | X | X |
| | 42 | Reserved | | | | |
| | 43 | VLAN_12_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 44 | VLAN_13_Entry_Configuration_0 (member[15:0]) | RW | 2000 | X | X |
| | 45 | Reserved | | | | |
| | 46 | VLAN_13_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 47 | VLAN_14_Entry_Configuration_0 (member[15:0]) | RW | 4000 | X | X |
| | 48 | Reserved | | | | |
| | 49 | VLAN_14_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 4A | VLAN_15_Entry_Configuration_0 (member[15:0]) | RW | 8000 | X | X |
| | 4B | Reserved | | | | |
| | 4C | VLAN_15_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 4D | VLAN_16_Entry_Configuration_0 (member[15:0]) | RW | 0000 | X | X |
| | 4E | Reserved | | | | |
| | 4F | VLAN_16_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 50 | VLAN_17_Entry_Configuration_0 (member[15:0]) | RW | 0000 | X | X |
| | 51 | Reserved | | | | |
| | 52 | VLAN_17_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 53 | VLAN_18_Entry_Configuration_0 (member[15:0]) | RW | 0000 | X | X |
| | 54 | Reserved | | | | |
| | 55 | VLAN_18_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 56 | VLAN_19_Entry_Configuration_0 (member[15:0]) | RW | 0000 | X | X |
| | 57 | Reserved | | | | |
| | 58 | VLAN_19_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 59 | VLAN_20_Entry_Configuration_0 (member[15:0]) | RW | 0000 | X | X |
| | 5A | Reserved | | | | |
| | 5B | VLAN_20_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 5C | VLAN_21_Entry_Configuration_0 (member[15:0]) | RW | 0000 | X | X |
| | 5D | Reserved | | | | |
| | 5E | VLAN_21_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| | 5F | VLAN_22_Entry_Configuration_0 (member[15:0]) | RW | FFFF | X | X |
| | 60 | Reserved | | | | |
| | 61 | VLAN_22_Entry_Configuration_2 (VID[11:0]) | RW | F000 | X | X |
| | 62 | VLAN_23_Entry_Configuration_0 (member[15:0]) | RW | FFFF | X | X |
| | 63 | Reserved | | | | |
| | 64 | VLAN_23_Entry_Configuration_2 (VID[11:0]) | RW | F000 | X | X |
| | 65 | VLAN_24_Entry_Configuration_0 (member[15:0]) | RW | 0000 | X | X |
| | 66 | Reserved | | | | |
| | 67 | VLAN_24_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 68 | VLAN_25_Entry_Configuration_0 (member[15:0]) | RW | 0000 | X | X |
| | 69 | Reserved | | | | |
| | 6A | VLAN_25_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 6B | VLAN_26_Entry_Configuration_0 (member[15:0]) | RW | 0000 | X | X |
| | 6C | Reserved | | | | |
| | 6D | VLAN_26_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 6E | VLAN_27_Entry_Configuration_0 (member[15:0]) | RW | 0000 | X | X |
| | 6F | Reserved | | | | |
| | 70 | VLAN_27_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 71 | VLAN_28_Entry_Configuration_0 (member[15:0]) | RW | 0000 | X | X |
| | 72 | Reserved | | | | |
| | 73 | VLAN_28_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 74 | VLAN_29_Entry_Configuration_0 (member[15:0]) | RW | 0000 | X | X |
| | 75 | Reserved | | | | |
| | 76 | VLAN_29_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 77 | VLAN_30_Entry_Configuration_0 (member[15:0]) | RW | 0000 | X | X |
| | 78 | Reserved | | | | |
| | 79 | VLAN_30_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 7A | VLAN_31_Entry_Configuration_0 (member[15:0]) | RW | 0000 | X | X |
| | 7B | Reserved | | | | |
| | 7C | VLAN_31_Entry_Configuration_2 (VID[11:0]) | RW | 0000 | X | X |
| | 7D | Insert per-port VID enabling register | RW | 0 | X | V |
| | 7E | Reserved | | | | |

## 10.5. Queue Control Registers

**Table 36. Queue Control Registers**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0400 | 0 | QoS Control Register | RW | 0 | V | V |
| | 1 | Port Priority Configuration (0) | RW | 0 | V | V |
| | 2 | Port Priority Configuration (1) | RW | 0 | V | V |
| | 8 | Reserved (Used by RRCP software) | RW | 0 | V | V |

## 10.6. PHY Access Control Register

**Table 37. PHY Access Control Register**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0500 | 0 | PHY Access Addressing Control | R(/W) | 0 | X | X |
| | 1 | PHY Access Write Data | RW | -- | X | X |
| | 2 | PHY Access Read Data | R | -- | X | X |

## 10.7. Port Control Registers

**Table 38. Port Control Registers**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0600 | 0~6 | Reserved | | | | |
| | 7 | Global Port Control Register | RW | 0010 | V | V |
| | 8 | Port Access Authority Control (0) | RW | 0 | X | X |
| | 9 | Port Access Authority Control (1) | RW | 0 | X | X |
| | A | Port Property Configuration Register 0 (Port 0, 1) | RW | AFAF | X | V |
| | B | Port Property Configuration Register 1 (Port 2, 3) | RW | AFAF | X | V |
| | C | Port Property Configuration Register 2 (Port 4, 5) | RW | AFAF | X | V |
| | D | Port Property Configuration Register 3 (Port 6, 7) | RW | AFAF | X | V |
| | E | Port Property Configuration Register 4 (Port 8, 9) | RW | AFAF | X | V |
| | F | Port Property Configuration Register 5 (Port 10, 11) | RW | AFAF | X | V |
| | 10 | Port Property Configuration Register 6 (Port 12, 13) | RW | AFAF | X | V |
| | 11 | Port Property Configuration Register 7 (Port 14, 15) | RW | AFAF | X | V |
| | 12 | Reserved | | | | |
| | 13 | Reserved | | | | |
| | 14 | Reserved | | | | |
| | 15 | Reserved | | | | |
| | 16 | Reserved | | | | |
| | 17 | Reserved | | | | |
| | 18 | Reserved[15:2], SyncOk [1:0] | R | | X | X |
| | 19 | Port Link Status Register 0 (Port 0, 1) | R | 0 | X | X |

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| | 1A | Port Link Status Register 1 (Port 2, 3) | R | 0 | X | X |
| | 1B | Port Link Status Register 2 (Port 4, 5) | R | 0 | X | X |
| | 1C | Port Link Status Register 3 (Port 6, 7) | R | 0 | X | X |
| | 1D | Port Link Status Register 4 (Port 8, 9) | R | 0 | X | X |
| | 1E | Port Link Status Register 5 (Port 10, 11) | R | 0 | X | X |
| | 1F | Port Link Status Register 6 (Port 12, 13) | R | 0 | X | X |
| | 20 | Port Link Status Register 7 (Port 14, 15) | R | 0 | X | X |
| | 21 | Reserved | | | | |
| | 22 | Reserved | | | | |
| | 23 | Reserved | | | | |
| | 24 | Reserved | | | | |
| | 25 | Reserved | | | | |
| | 26 | Reserved | | | | |
| | 27 | Reserved | | | | |
| | 28 | Reserved | | | | |

## 10.8. MIB Counter Registers

**Table 39. MIB Counter Registers**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0700 | 0 | Port MIB Counter Object Selection Register 0 (Port 0, 1) | RW | 0555 | X | X |
| | 1 | Port MIB Counter Object Selection Register 1 (Port 2, 3) | RW | 0555 | X | X |
| | 2 | Port MIB Counter Object Selection Register 2 (Port 4, 5) | RW | 0555 | X | X |
| | 3 | Port MIB Counter Object Selection Register 3 (Port 6, 7) | RW | 0555 | X | X |
| | 4 | Port MIB Counter Object Selection Register 4 (Port 8, 9) | RW | 0555 | X | X |
| | 5 | Port MIB Counter Object Selection Register 5 (Port 10, 11) | RW | 0555 | X | X |
| | 6 | Port MIB Counter Object Selection Register 6 (Port 12, 13) | RW | 0555 | X | X |
| | 7 | Port MIB Counter Object Selection Register 7 (Port 14, 15) | RW | 0555 | X | X |
| | 8 | Reserved | | | | |
| | 9 | Reserved | | | | |
| | A | Reserved | | | | |
| | B | Reserved | | | | |
| | C | Reserved | | | | |

## 10.8.1. Port MIB Counter 1 Register (RX Counter) (32-bits)

**Table 40. Port MIB Counter 1 Register (RX Counter) (32-bits)**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0700 | D | Port 0 MIB Counter 1 Register (RX Counter) (32-bits) | R | 0 | X | X |
| | E | Port 1 MIB Counter 1 Register (RX Counter) (32-bits) | R | 0 | X | X |
| | F | Port 2 MIB Counter 1 Register (RX Counter) (32-bits) | R | 0 | X | X |
| | 10 | Port 3 MIB Counter 1 Register (RX Counter) (32-bits) | R | 0 | X | X |
| | 11 | Port 4 MIB Counter 1 Register (RX Counter) (32-bits) | R | 0 | X | X |
| | 12 | Port 5 MIB Counter 1 Register (RX Counter) (32-bits) | R | 0 | X | X |
| | 13 | Port 6 MIB Counter 1 Register (RX Counter) (32-bits) | R | 0 | X | X |
| | 14 | Port 7 MIB Counter 1 Register (RX Counter) (32-bits) | R | 0 | X | X |
| | 15 | Port 8 MIB Counter 1 Register (RX Counter) (32-bits) | R | 0 | X | X |
| | 16 | Port 9 MIB Counter 1 Register (RX Counter) (32-bits) | R | 0 | X | X |
| | 17 | Port 10 MIB Counter 1 Register (RX Counter) (32-bits) | R | 0 | X | X |
| | 18 | Port 11 MIB Counter 1 Register (RX Counter) (32-bits) | R | 0 | X | X |
| | 19 | Port 12 MIB Counter 1 Register (RX Counter) (32-bits) | R | 0 | X | X |
| | 1A | Port 13 MIB Counter 1 Register (RX Counter) (32-bits) | R | 0 | X | X |
| | 1B | Port 14 MIB Counter 1 Register (RX Counter) (32-bits) | R | 0 | X | X |
| | 1C | Port 15 MIB Counter 1 Register (RX Counter) (32-bits) | R | 0 | X | X |
| | 1D | Reserved | | | | |
| | 1E | Reserved | | | | |
| | 1F | Reserved | | | | |
| | 20 | Reserved | | | | |
| | 21 | Reserved | | | | |
| | 22 | Reserved | | | | |
| | 23 | Reserved | | | | |
| | 24 | Reserved | | | | |
| | 25 | Reserved | | | | |
| | 26 | Reserved | | | | |

**Table 41. Port MIB Counter 2 Register (TX Counter) (32-bits)**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0700 | 27 | Port 0 MIB Counter 2 Register (TX Counter) (32-bits) | R | 0 | X | X |
| | 28 | Port 1 MIB Counter 2 Register (TX Counter) (32-bits) | R | 0 | X | X |
| | 29 | Port 2 MIB Counter 2 Register (TX Counter) (32-bits) | R | 0 | X | X |
| | 2A | Port 3 MIB Counter 2 Register (TX Counter) (32-bits) | R | 0 | X | X |
| | 2B | Port 4 MIB Counter 2 Register (TX Counter) (32-bits) | R | 0 | X | X |
| | 2C | Port 5 MIB Counter 2 Register (TX Counter) (32-bits) | R | 0 | X | X |
| | 2D | Port 6 MIB Counter 2 Register (TX Counter) (32-bits) | R | 0 | X | X |
| | 2E | Port 7 MIB Counter 2 Register (TX Counter) (32-bits) | R | 0 | X | X |
| | 2F | Port 8 MIB Counter 2 Register (TX Counter) (32-bits) | R | 0 | X | X |
| | 30 | Port 9 MIB Counter 2 Register (TX Counter) (32-bits) | R | 0 | X | X |
| | 31 | Port 10 MIB Counter 2 Register (TX Counter) (32-bits) | R | 0 | X | X |
| | 32 | Port 11 MIB Counter 2 Register (TX Counter) (32-bits) | R | 0 | X | X |
| | 33 | Port 12 MIB Counter 2 Register (TX Counter) (32-bits) | R | 0 | X | X |
| | 34 | Port 13 MIB Counter 2 Register (TX Counter) (32-bits) | R | 0 | X | X |
| | 35 | Port 14 MIB Counter 2 Register (TX Counter) (32-bits) | R | 0 | X | X |
| | 36 | Port 15 MIB Counter 2 Register (TX Counter) (32-bits) | R | 0 | X | X |
| | 37 | Reserved | | | | |
| | 38 | Reserved | | | | |
| | 39 | Reserved | | | | |
| | 3A | Reserved | | | | |
| | 3B | Reserved | | | | |
| | 3C | Reserved | | | | |
| | 3D | Reserved | | | | |
| | 3E | Reserved | | | | |
| | 3F | Reserved | | | | |
| | 40 | Reserved | | | | |

## 10.8.2. Port MIB Counter 3 Register (Diagnostic Counter) (32-bits)

**Table 42. Port MIB Counter 3 Register (Diagnostic Counter) (32-bits)**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0700 | 41 | Port 0 MIB Counter 3 Register (Diagnostic Counter)(32-bits) | R | 0 | X | X |
| | 42 | Port 1 MIB Counter 3 Register (Diagnostic Counter)(32-bits) | R | 0 | X | X |
| | 43 | Port 2 MIB Counter 3 Register (Diagnostic Counter)(32-bits) | R | 0 | X | X |
| | 44 | Port 3 MIB Counter 3 Register (Diagnostic Counter)(32-bits) | R | 0 | X | X |
| | 45 | Port 4 MIB Counter 3 Register (Diagnostic Counter)(32-bits) | R | 0 | X | X |
| | 46 | Port 5 MIB Counter 3 Register (Diagnostic Counter)(32-bits) | R | 0 | X | X |
| | 47 | Port 6 MIB Counter 3 Register (Diagnostic Counter)(32-bits) | R | 0 | X | X |
| | 48 | Port 7 MIB Counter 3 Register (Diagnostic Counter)(32-bits) | R | 0 | X | X |
| | 49 | Port 8 MIB Counter 3 Register (Diagnostic Counter)(32-bits) | R | 0 | X | X |
| | 4A | Port 9 MIB Counter 3 Register (Diagnostic Counter)(32-bits) | R | 0 | X | X |
| | 4B | Port 10 MIB Counter 3 Register (Diagnostic Counter)(32-bits) | R | 0 | X | X |
| | 4C | Port 11 MIB Counter 3 Register (Diagnostic Counter)(32-bits) | R | 0 | X | X |
| | 4D | Port 12 MIB Counter 3 Register (Diagnostic Counter)(32-bits) | R | 0 | X | X |
| | 4E | Port 13 MIB Counter 3 Register (Diagnostic Counter)(32-bits) | R | 0 | X | X |
| | 4F | Port 14 MIB Counter 3 Register (Diagnostic Counter)(32-bits) | R | 0 | X | X |
| | 50 | Port 15 MIB Counter 3 Register (Diagnostic Counter)(32-bits) | R | 0 | X | X |
| | 51 | Reserved | | | | |
| | 52 | Reserved | | | | |
| | 53 | Reserved | | | | |
| | 54 | Reserved | | | | |
| | 55 | Reserved | | | | |
| | 56 | Reserved | | | | |
| | 57 | Reserved | | | | |
| | 58 | Reserved | | | | |
| | 59 | Reserved | | | | |
| | 5A | Reserved | | | | |

## 10.9. System Parameter Register (Reserved)

**Table 43. System Parameter Register (Reserved)**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0xFFFF | -- | System Parameter Register (Reserved). | RW | 0 | V | V |

# 11. Internal Register Settings

Register Symbols:

| | | | |
|---|---|---|---|
| R: | Read | LL: | Latch Low until cleared |
| W: | Write | LH: | Latch High until cleared |
| RW: | Read/Write | SC: | Self Clearing |
| (W: EEPROM. Permit writing by EEPROM) | | RC: | Read to Clear |

## *11.1. System Configuration Register*

### 11.1.1.  0x0000H: System Reset Control Register

**Table 44. 0x0000H: System Reset Control Register**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 0 | SRST | Soft Reset.<br>A soft reset will reset the system similar to a power on reset except that the user configuration will not be cleared:<br>1. The MAC table and VLAN table data are kept.<br>2. All current user configured internal register values are kept.<br>3. The EEPROM download is not done again.<br>4. The system restarts the auto-negotiation process.<br><br>0: Normal (Default)<br>1: Soft reset | W/SC | 0 |
| 1 | HRST | Hardware Reset.<br>Resets the system to the power on initial state:<br>1. Downloads configuration from strap pin and EEPROM.<br>2. Starts internal Memory self test.<br>3. Clears all the MAC, VLAN tables.<br>4. Resets all registers to default values.<br>5. Restarts auto-negotiation.<br><br>0: Normal (Default)<br>1: Hardware reset | W/SC | 0 |
| 15:2 | Reserved | | | |

## 11.1.2. 0x0001H: Switch Parameter Register

*Note: The Write operation is reserved for IC testing mode. Do NOT write this register.*

**Table 45. 0x0001H: Switch Parameter Register**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 1:0 | MaxPktLen[1:0] | System Valid Max Packet Length.<br>The minimum packet length is 64 bytes. The maximum packet length is controlled by MaxPktLen[1:0]:<br>00: 1536 bytes (Default)<br>01: 1552 byte<br>1x: Reserved. | RW | 00<br>HW pin<br>MaxPktLen |
| 2 | TXIPG_Comp | Transmit IPG Compensation.<br>Used to compensate the oscillator frequency or incoming packet Inter-Packet Gap (IPG) tolerance.<br>0: Give +65 ppm TXIPG compensation (Default)<br>1: Give +90 ppm TXIPG compensation | RW | 0 |
| 3 | MaxPauseCnt | Max Pause Count for Congestion Control.<br>0: Supports a maximum of 128 Pause frames during congestion control (Default)<br>1: Continue Pause mode. Do not limit the Pause frame count during congestion control. | RW | 0<br>HW pin<br>MaxPauseCnt |
| 4 | DisBKP48One<br>($\overline{\text{EnBKP48One}}$) | Disable Back pressure 48 Pass One Algorithm.<br>When the 48One algorithm is enabled, the switch will pass one incoming packet after every 48 collisions.<br>0: Enable 48 Pass One algorithm (Default)<br>1: Disable 48 Pass One algorithm | RW | 0<br>HW pin<br>EnBKP48One |
| 6:5 | Reserved | Internal test bit. | | |
| 7 | DisCRSBKPMode<br>($\overline{\text{EnCOLBKPMode}}$) | Disable Carrier Based Back Pressure Mode.<br>Half duplex back pressure algorithm selection.<br>0: Select Collision-based back pressure mode<br>1: Select Carrier-based back pressure mode (Default) | RW | 1<br>HW pin<br>EnCOLBKPmode |
| 15:8 | Reserved | Internal test bit. | | |

## 11.1.3. 0x0002H: EEPROM Check ID

**Table 46. 0x0002H: EEPROM Check ID**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 5:0 | Reserved<br>(EEPROM Check ID) | Reserved bits.<br>Used for EEPROM existence checking.<br>Keep the value at 000000. | | |
| 15:6 | Reserved | Internal test bit. | | |

## 11.1.4. 0x0004H: General Purpose User Defined I/O Data Register

**Table 47. 0x0004H: General Purpose User Defined I/O Data Register**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 1:0 | LED MODE | 00: Scan Led<br>01: Single-color serial (default)<br>10: Bi-color serial<br>11: RSVD | RW | 01<br>HW pin<br>P9TXD<br>P8TXD |
| 15:2 | Reserved | | | |

## 11.1.5. 0x0005H: LED Display Configuration

**Table 48. 0x0005H: LED Display Configuration**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 2:0 | StatLED0_mode[2:0] | Mode Selection for State LED0.<br>This state LED mode selection register controls the status type of the State LED0. The Status type is defined as follows:<br>000: Link/Act (Default)<br>001: 100Spd<br>010: Duplex/Col<br>011: Link/Act/100Spd<br>100: Duplex<br>101: Act<br>110: Link<br>111: Col | RW | 000 |
| 5:3 | StatLED1_mode[2:0] | Mode Selection for State LED1.<br>000: Link/Act<br>001: 100Spd (Default)<br>010: Duplex/Col<br>011: Link/Act/100Spd<br>100: Duplex<br>101: Act<br>110: Link<br>111: Col | RW | 001 |
| 8:6 | StatLED2_mode[2:0] | Mode Selection for State LED2.<br>000: Link/Act<br>001: 100Spd<br>010: Duplex/Col (Default)<br>011: Link/Act/100Spd<br>100: Duplex<br>101: Act<br>110: Link<br>111: Col | RW | 010 |

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 12:9 | EnLED[3:0] | State LED 0, 1, 2 and Diagnostic LED Enable/Disable Control.<br>EnLED[3:0] controls enabling/disabling of DiagLED, StatLED2, StatLED1, StatLED0.<br>0: Disable<br>1: Enable<br>If an LED is disabled, the corresponding serial clock will be masked. | RW | 0111 |
| 14:13 | Diagnostic mode | | RW | 00 |
| 15 | Reserved | | | |

## 11.2. System Status Register

### 11.2.1. 0x0100H: Board Trapping Status Register

**Table 49. 0x0100H: Board Trapping Status Register**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 0 | EEPROM_detect_ status | EEPROM Existence Status.<br>0: Exists (Default)<br>1: Does not Exist | R | 0 |
| 15:2 | Reserved | | | |

### 11.2.2. 0x0101H: Loop Detect Status Register (32-Bit Register)

**Table 50. 0x0101H: Loop Detect Status Register (32-Bit Register)**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 23:0 | LoopDetPort[23:0] | Network Loop event Detect Port Status.<br>If the loop detect function is enabled, the corresponding bit of LoopDetPort[23:0] will be set whenever a loop event is detected on the corresponding switch port. The set bit is cleared only when the loop event has disappeared on that port.<br><br>When the loop detect function is enabled, the switch will periodically transmit one loop detect diagnostic frame. The normal interval time is approx. five minutes. When a loop event is detected, the interval time will be changed to fast mode. In fast mode the interval time is about 1 second in order to accelerate detection and diagnostic. The loop event will be reported in this Loop Detect Status Register.<br>0: No Loop detected on this port (Default)<br>1: Loop detected on this port | R | 0 |
| 31:24 | Reserved | | | |

## 11.2.3.  0x0102H: System Fault Indication Register

**Table 51. 0x0102H: System Fault Indication Register**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 0 | Reserved | | | |
| 1 | TrunkFault | Trunk Fault event flag.<br><br>The flag indicates that there is a trunk port member link down. The trunk will still continue to operate due to the trunk auto fault recovery algorithm.<br><br>0: No trunk fault detected (Default)<br>1: Trunk fault detected | R | 0 |
| 2 | LoopFault | Network Loop Fault Indication.<br><br>When the Loop Fault indication is set, a loop detected port will be reported on the Loop Detect Port Register.<br><br>0: Network Loop not detected (Default)<br>1: Network Loop detected | R | 0 |
| 5:3 | Reserved | | | |
| 11:6 | FaultTkGroup[3:0] | The Fault Trunk Group Indicator.<br><br>Indicates a Link Fault in the trunk group.<br><br>A physical link failure of an enabled trunk group will cause the corresponding bit to be set in the FaultTkGroup[5:0]. This is a real time fault status report.<br><br>Even though the Trunk Group's fault occurred and the fault bit is set, the corresponding trunk can still work properly as fault recovery will be auto applied.<br><br>FaultTkGroup[0] indicator for Trunk 1: (port 0, 1, 2, 3)<br>FaultTkGroup[1] indicator for Trunk 2: (port 4, 5, 6, 7)<br>FaultTkGroup[2] indicator for Trunk 3: (port 8, 9, 10, 11)<br>FaultTkGroup[3] indicator for Trunk 4: (port 12, 13, 14, 15)<br><br>0: Trunk OK<br>1: Trunk Fault detected | R | 000000 |
| 15:12 | Reserved | | | |

# 11.3. Management Configuration Register

## 11.3.1. 0x0200H: Realtek Protocol Control Register

**Table 52. 0x0200H: Realtek Protocol Control Register**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 0 | DisRRCP (EnRRCP) | Disable Realtek Remote Control Protocol (RRCP).<br>0: Enable RRCP<br>1: Disable RRCP (Default) | RW | 1<br>HW pin: EnRRCP |
| 1 | DisREcho | Disable Realtek Remote Echo Protocol.<br>0: Enable REcho protocol<br>1: Disable REcho protocol(Default) | RW | 1 |
| 2 | EnLoopDet | Enable Loop Detect Function.<br>When enabled, the loop detect status will be reported in register 0x0101 (Loop Detect Status Register).<br>0: Disable(Default)<br>1: Enable | RW | 0 |
| 15:3 | Reserved | | | |

## 11.3.2. 0x0201H: RRCP Security Mask Configuration Register 0

**Table 53. 0x0201H: RRCP Security Mask Configuration Register 0**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 15:0 | RRCP_SMask[15:0] | RRCP Management Security Mask Configuration.<br>Configuration for ports 0 to 15.<br>Specifies which port's incoming RRCP access commands will be responded to.<br>0: RRCP Access enabled port (Default)<br>1: RRCP Access disabled port<br>*Note: Ports 0~15 RRCP security mask will be set if the hardware strap pin EnHomeVlan is pulled high during power on reset. This can be over written by EEPROM or registers access.* | RW | 0 |

## 11.3.3. 0x0203H: Switch MAC ID Register 0

**Table 54. 0x0203H: Switch MAC ID Register 0**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 15:0 | MACID[15:0] | Switch Physical MAC Address bit[15:0].<br>E.g., For the 48-bit MAC address '52-54-4C-01-02-03', then MACID[15:0]=54-52. | R<br>(W: EEPROM) | 0 |

## 11.3.4. 0x0204H: Switch MAC ID Register 1

**Table 55. 0x0204H: Switch MAC ID Register 1**

| Bits | Name | Description | RW | Default |
|------|------|-------------|----|---------|
| 15:0 | MACID[31:16] | Switch Physical MAC Address bit[31:16] <br><br> E.g., For the 48-bit MAC address '52-54-4C-01-02-03', then MACID[15:0]=54-52. | R <br> (W: EEPROM) | 0 |

## 11.3.5. 0x0205H: Switch MAC ID Register 2

**Table 56. 0x0205H: Switch MAC ID Register 2**

| Bits | Name | Description | RW | Default |
|------|------|-------------|----|---------|
| 15:0 | MACID[47:32] | Switch Physical MAC Address bit[47:32]. <br><br> E.g., For the 48-bit MAC address '52-54-4C-01-02-03', then MACID[15:0]=54-52. | R <br> (W: EEPROM) | 0 |

## 11.3.6. 0x0206H: Chip Model ID

**Table 57. 0x0206H: Chip Model ID**

| Bits | Name | Description | RW | Default |
|------|------|-------------|----|---------|
| 7:0 | ChipID[7:0] | Chip ID. <br><br> Identifies the chip version for programmer version control. | R <br> (W: EEPROM) | 0 |
| 15:8 | Reserved | | | |

# 11.4. 0x0207H: System Vender ID Register 0

**Table 58. 0x0207H: System Vender ID Register 0**

| Bits | Name | Description | RW | Default |
|------|------|-------------|----|---------|
| 15:0 | VenderID[15:0] | System Vender Identity Stream [15:0]. <br><br> Used for the system vender to fill a code or name stream for switch device model number or vender name identification. | R <br> (W: EEPROM) | 0 |

# 11.5. 0x0208H: System Vender ID Register 1

**Table 59. 0x0208H: System Vender ID Register 1**

| Bits | Name | Description | RW | Default |
|------|------|-------------|----|---------|
| 15:0 | VenderID[31:16] | System Vender Identity Stream [31:16]. <br><br> Used for system vender to fill a code or name stream for switch device model number or vender name identification. | R <br> (W: EEPROM) | 0 |

## 11.6. 0x0209H: RRCP Authentication Key Configuration Register

**Table 60. 0x0209H: RRCP Authentication Key Configuration Register**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 15:0 | RRCP_KEY[15:0] | RRCP Access Authentication Key Configuration. After power on reset, the RRCP Authentication Key is set to the default value '0x2379'. It can be updated via the CPU interface or by an RRCP control frame with a correct current authentication key value in the frame. The Authentication Key checking rule for RRCP frames is defined as follows: 1. For the Hello command frame: -- Broadcast Hello frame: Do not check Auth. Key. -- Unicast Hello frame: Auth. Key = RRCP_KEY[15:0] Note: When the RRCP_KEY[15:0] is updated by the user, only unicast Hello frames are valid. 2. For a Get/Set command frame: Always uses the current key value defined by RRCP_KEY[15:0] | RW | 0x2379 |

## 11.7. 0x020AH: Port 0, 1 Bandwidth Control Register

**Table 61. 0x020AH: Port 0, 1 Bandwidth Control Register**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 3:0 | P0RXRate[3:0] | Port 0 RX Bandwidth Control. Configures the maximum output bandwidth of the port. Bit 3 is a reserved bit. Bit[2:0] controls the maximum RX rate of the port. 000: Disables rate control (Default) 001: 128Kbps 010: 256Kbps 011: 512Kbps 100: 1Mbps 101: 2Mbps 110: 4Mbps 111: 8Mbps | RW | 0000 |

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 7:4 | P0TXRate[3:0] | Port 0 TX Bandwidth Control.<br>Configures the maximum input bandwidth of the port.<br>Bit 3 is a reserved bit.<br>Bit[2:0] controls the maximum TX rate of the port.<br>000: Disables rate control (Default)<br>001: 128Kbps<br>010: 256Kbps<br>011: 512Kbps<br>100: 1Mbps<br>101: 2Mbps<br>110: 4Mbps<br>111: 8Mbps | RW | 0000 |
| 11:8 | P1RXRate[3:0] | Port 1 RX Bandwidth Control.<br>Configures the maximum output bandwidth of the port.<br>Bit 3 is a reserved bit.<br>Bit[2:0] controls the maximum RX rate of the port.<br>000: Disables rate control (Default)<br>001: 128Kbps<br>010: 256Kbps<br>011: 512Kbps<br>100: 1Mbps<br>101: 2Mbps<br>110: 4Mbps<br>111: 8Mbps | RW | 0000 |
| 15:12 | P1TXRate[3:0] | Port 1 TX Bandwidth Control.<br>Configures the maximum input bandwidth of the port.<br>Bit 3 is a reserved bit.<br>Bit[2:0] controls the maximum TX rate of the port.<br>000: Disables rate control (Default)<br>001: 128Kbps<br>010: 256Kbps<br>011: 512Kbps<br>100: 1Mbps<br>101: 2Mbps<br>110: 4Mbps<br>111: 8Mbps | RW | 0000 |

## 11.7.1.  0x020BH~0x0211H: Port 2~15 Bandwidth Control Register

Refer to Table 61, for Configuration description of n: 1 ~ 11.

**Table 62. 0x020BH~0x0215H: Port 2~15 Bandwidth Control Register**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 3:0 | P2nRXRate[3:0] | Port 2n RX Bandwidth Control | RW | 0000 |
| 7:4 | P2nTXRate[3:0] | Port 2n TX Bandwidth Control | RW | 0000 |
| 11:8 | P2n+1RXRate[3:0] | Port 2n+1 RX Bandwidth Control. | RW | 0000 |
| 15:12 | P2n+1TXRate[3:0] | Port 2n+1 TX Bandwidth Control. | RW | 0000 |

# *11.8.  0x0217H~0x0218: EEPROM RW Control Register*

## 11.8.1.  0x0217H: EEPROM RW Command Register

**Table 63. 0x0217H: EEPROM RW Command Register**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 7:0 | EEPROM address | Assigns EEPROM address bits. | RW | 0 |
| 10:8 | CHIP_SEL[2:0]] | Assigns chip selection bits. | RW | 0 |
| 11 | Read/Write Operation | 0: Write Operation<br>1: Read Operation | RW | 0 |
| 12 | Status | 0: Idle<br>1: Busy | RW | 0 |
| 13 | Operation Succeeded status | 0: Operation Succeeded<br>1: Operation Fail<br>(Read Clear) | RW | 0 |
| 15:14 | Reserved | | | |

## 11.8.2.  0x0218H: EEPROM RW Data Register

**Table 64. 0x0218H: EEPROM RW Data Register**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 7:0 | WdataEE[7:0] | Data to be written to EEPROM. | RW | 0 |
| 15:8 | RdataEE[15:8] | Data Read from EEPROM. | R | 0 |

# 11.9. 0x0219H~0x021EH: Port Mirror Control Register

## 11.9.1. 0x0219H: Port Mirror Control Register 0 for P15-P0

**Table 65. Port Mirror Control Register for P15-P0**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 15:0 | EnPortMirror(0)[15:0] | Enables the port based mirror function.<br>Bit n corresponds to port n.<br>Write '1' to enable a port's mirror function. | RW | 0 |

## 11.9.2. 0x021BH: RX Mirror Port Register 0 for P15-P0

**Table 66. RX Mirror Port Register 0 for P15-P0**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 15:0 | Mirror_RX(0)[15:0] | Bit n corresponds to port n.<br>Write '1' to duplicate port n RX data to mirrored port. | RW | 0 |

## 11.9.3. 0x021DH: TX Mirror Port Register 0 for P15-P0

**Table 67. TX Mirror Port Register 0 for P15-P0**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 15:0 | Mirror_TX(0)[15:0] | Bit n corresponds to port n.<br>Write '1' to duplicate port n TX data to mirrored port. | RW | 0 |

# 11.10. Address Lookup Table (ALT) Control Register

## 11.10.1. 0x0300H: ALT Configuration Register

**Table 68. 0x0300H: ALT Configuration Register**

| Bits | Name | Description | RW | Default |
|------|------|-------------|----|---------|
| 0 | DisMacAging | Global Disable Mac Table Aging Function.<br>0: Enable Aging function (Default)<br>1: Disable Aging function | RW | 0 |
| 1 | EnFastAgeTime | Enable Fast Aging Time Mode.<br>0: Disable Fast Aging time; Aging set to 300 seconds (Default)<br>1: Enable Fast Aging time; Aging set to 12 seconds | RW | 0 |
| 2 | EnCtrlFFilter | Global Enable 802.1D Specified Reserved Control Frame Filtering.<br>When network control packets are received with a destination MAC address as the group MAC address: (01-80-C2-00-00-04 ~ 01-80-C2-00-00-0F), the switch will drop the packets if the bit EnCtrlFilter=1. Otherwise (EnCtrlFilter=0) they will be flooded.<br>1: Enable Filtering (Default)<br>0: Disable Filtering | RW | 1<br>HW pin.<br>EnCtrlFFilter |
| 3 | EnDropUknDA | Internal test bit. | RW | 0 |
| 15:4 | Reserved | | | |

## 11.10.2. 0x0301H: Address Learning Control Register 0

**Table 69. 0x0301H: Address Learning Control Register 0**

| Bits | Name | Description | RW | Default |
|------|------|-------------|----|---------|
| 15:0 | DisMacLearn[15:0] | Per-Port Disable Mac Address Learning Function (Ports 0~15).<br>DisMacLearn[15:0] control port[15:0].<br>The Layer 2 MAC address learning function can be per-port disabled for security management purposes.<br>Generally this register is used with the ALT Configuration Register (0x0300) bits 'DisMacAging'.<br>0: Enable learning (Default)<br>1: Disable learning | RW | 0 |

## 11.10.3. 0x0307H: Port Trunking Configuration Register

**Table 70. 0x0307H: Port Trunking Configuration Register**

| Bits | Name | Description | RW | Default |
|------|------|-------------|----|---------|
| 0 | Reserved | | | |
| 4:1 | EnTrunk[3:0] | Trunk Group Enable/Disable Control. Enables trunk groups. EnTrunk[0] control for Trunk 1: (port 0, 1, 2, 3). EnTrunk[1] control for Trunk 2: (port 4, 5, 6, 7). EnTrunk[2] control for Trunk 3: (port 8, 9, 10, 11). EnTrunk[3] control for Trunk 4: (port 12, 13, 14, 15). 0: Disable Trunking (Default) 1: Enable Trunking | RW | 0x00 |
| 15:7 | Reserved | | | |

## 11.10.4. 0x0308H: IGMP Snooping Control Register

**Table 71. 0x0308H: IGMP Snooping Control Register**

| Bits | Name | Description | RW | Default |
|------|------|-------------|----|---------|
| 0 | EnIGMPsnooping | Enable IGMP Snooping. The switch controller features an ASIC-based auto IGMP v1 snooping function. No software support is required. When enabled, the switch can automatically snoop IGMP packets and build up an IP multicast address table. The discovered IP multicast Router port will be indicated in the 'IP Multicast Router Port Discovery Register'. 0: Disable IGMP snooping (Default) 1: Enable IGMP snooping | RW | 0 |
| 15:1 | Reserved | | | |

## 11.10.5. 0x0309H: IP Multicast Router Port Discovery Register (32 bits)

**Table 72. 0x0309H: IP Multicast Router Port Discovery Register (32 bits)**

| Bits | Name | Description | RW | Default |
|------|------|-------------|----|---------|
| 23:0 | IPMRouterDISC[23:0] | IP Multicast Router Ports Discovery Result. This is a bit map that indicates which port is an IP Multicast Router port. IPMRouterDISC[23:0] maps to port 15 ~ 0 0: Normal port (Default) 1: IP multicast Router port | R | 0 |
| 31:24 | Reserved | | | |

# 11.10.6. 0x030BH: VLAN Control Register

**Table 73. 0x030BH: VLAN Control Register**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 0 | EnHomeVlan | Enable VLAN Function.<br><br>When the VLAN function is enabled, the power on default VLAN topology is 16 Home VLANs for non-EEPROM environments. The VLAN topology can be configured by Port VLAN Configuration Registers.<br>0: Disable VLAN (Default)<br>1: Enable VLAN | RW | 0<br>HW pin.<br>EnHomeVLAN |
| 1 | EnUCleaky | Unicast Packet Inter-VLAN Leaky Control.<br><br>Enables inter-VLAN communication for unicast forwarding packets.<br>Normally, inter-VLAN packet switching is not valid. The RTL8316B supports a control bit to enable inter-VLAN communication in the switch without an external router.<br>0: Disable (Default)<br>1: Enable | RW | 0 |
| 2 | EnARPleaky | ARP broadcast Packet Inter-VLAN Leaky Control.<br><br>Enables inter-VLAN communication for ARP broadcast packet forwarding.<br>0: Disable (Default)<br>1: Enable | RW | 0 |
| 3 | EnIPMleaky | IP Multicast Packet Inter-VLAN Leaky Control.<br><br>Enables inter-VLAN communication for ARP broadcast packet forwarding.<br>0: Disable (Default)<br>1: Enable | RW | 0 |
| 4 | En8021Qaware | Enable 802.1Q VLAN tag aware.<br><br>If 802.1Q VLAN aware, the switch supports the ability to identify the VLAN ID from the VLAN tag. Reset to force the switch to ignore the VLAN tag header and classify the VLAN only by the PVID.<br>0: Disable 802.1Q VLAN aware (Default)<br>1: Enable 802.1Q VLAN aware | RW | 0 |
| 5 | EnIR_TagAdmit | Ingress Rule for Acceptable frame types control.<br><br>If this parameter is set to 'Admit only VLAN-Tagged Frames', any frames received on that port that carry no VID (i.e., Untagged Frames or Priority-Tagged Frames) are discarded.<br>If this parameter is set to 'Admit all Frames', all incoming Priority-Tagged and Untagged Frames are associated with a VLAN by the ingress rule on the receiving port.<br>0: Admit all Frames (Default)<br>1: Admit only VLAN-Tagged Frames | RW | 0 |

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 6 | EnIR_MembSet | Ingress Rule for Ingress Filtering control.<br><br>If the Enable Ingress Filtering parameter 'EnIR_MembSet' is set, then all frames received on a port whose VLAN classification does not include that port in its member set shall be discarded.<br>0: Disable ingress member set Filtering (Default)<br>1: Enable ingress member set filtering | RW | 0 |
| 15:7 | Reserved | | | |

## 11.10.7. 0x030C~0x0313H: Port VLAN ID Assignment Index Register 0~7

For Port(2n), and Port(2n+1) the register is defined as follows: where n=0, 1, 2, … 6, 7
(Addr: 0x030CH + n).

**Table 74. 0x030C~0x0317H: Port VLAN ID Assignment Index Register 0~7**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 7:0 | P(2n)_VIDIndex[7:0] | Port(2n) VID assignment Index.<br>Bit[4:0]: Port VID assignment index. Use the index value as the offset to map to the VLAN configuration table to get a 12-bit Port VLAN ID.<br>Bit[7:5]: Reserved | RW | n |
| 15:8 | P(2n+1)_VIDIndex[7:0] | Port(2n+1) VID assignment Index.<br>Bit[4:0]: Port VID assignment index. Use the index value as the offset to map to the VLAN configuration table to get a 12-bit Port VLAN ID.<br>Bit[7:5]: Reserved | RW | 2n+1 |

# 11.10.8. 0x0319~0x031AH: VLAN Output Port Priority-Tagging Control Register 0, 1

For Port(8n), Port(8n+1), …. ~ Port(8n+7) the register is defined as follows: n=0, 1

**Table 75. 0x0319~0x031AH: VLAN Output Port Priority-Tagging Control Register 0, 1**

| Bits | Name | Description | RW | Default |
|------|------|-------------|----|---------|
| 1:0 | P(8n)_PriTagCtl[1:0] | Port(8n) VLAN Output priority Tag/Untag Control. 00: Remove the VLAN tag from a tagged frame 01: Insert priority tag into an untagged high-priority frame (set priority field: 7, VID field: 0 for high priority frame) 10: Insert priority tag into all untagged frames. (set priority field: 7, VID field: 0 for high priority frame; set priority field: 0, VID field: 0 for low priority frame) 11: Don't touch (Don't modify the packet) (Default) | RW | 11 |
| 3:2 | P(8n+1)_PriTagCtl[1:0] | Port(8n+1) VLAN Output priority Tag/Untag Control. | RW | 11 |
| 5:4 | P(8n+2)_PriTagCtl[1:0] | Port(8n+2) VLAN Output priority Tag/Untag Control. | RW | 11 |
| 7:6 | P(8n+3)_PriTagCtl[1:0] | Port(8n+3) VLAN Output priority Tag/Untag Control. | RW | 11 |
| 9:8 | P(8n+4)_PriTagCtl[1:0] | Port(8n+4) VLAN Output priority Tag/Untag Control. | RW | 11 |
| 11:10 | P(8n+5)_PriTagCtl[1:0] | Port(8n+5) VLAN Output priority Tag/Untag Control. | RW | 11 |
| 13:12 | P(8n+6)_PriTagCtl[1:0] | Port(8n+6) VLAN Output priority Tag/Untag Control. | RW | 11 |
| 15:14 | P(8n+7)_PriTagCtl[1:0] | Port(8n+7) VLAN Output priority Tag/Untag Control. | RW | 11 |

# 11.11. 0x031D~0x037CH: VLAN Table Configuration Registers

Each VLAN configuration entry requires three 16-bit registers. There are 32 VLAN configuration entries in the VLAN table. The VLAN configuration entry is combined with three registers: VLAN_Entry_Configuration_0, 1, 2. For VLAN m, its format is defined as follows: m=0, 1, 2, …. 31.

## 11.11.1. Register VLAN(m)_Entry_Configuration_0 (Addr: (0x031DH+3m))

Table 76. Register VLAN(m)_Entry_Configuration_0 (Addr: (0x031DH+3m))

| Bits | Name | Description | RW | Default |
|------|------|-------------|----|---------|
| 15:0 | VLAN(m)_PM[15:0] | VLAN (entry m) Port Member, 24-bit map (bit 0~15). Bit value 0: Port is not a member of the VLAN Bit value 1: Port is a member of the VLAN | RW | |

## 11.11.2. Register VLAN(m)_Entry_Configuration_2 (Addr: (0x031DH+3m+2))

Table 77. Register VLAN(m)_Entry_Configuration_2 (Addr: (0x031DH+3m+2))

| Bits | Name | Description | RW | Default |
|------|------|-------------|----|---------|
| 11:0 | VLAN(m)_VID[11:0] | VLAN(m) VID[11:0] bit 11~0. Each VLAN must be assigned a 12-bit VID. | RW | 0 |
| 15:12 | Reserved | | | |

# 11.12. 0x037D~0x037EH: Insert Per-Port VID (PVID) Enabling Register

## 11.12.1. 0x037D: Insert per-port VID (PVID) Enabling Register 0 (P15~P0)

Table 78. Insert Per-Port VID (PVID) Enabling Register 0

| Bits | Name | Description | RW | Default |
|------|------|-------------|----|---------|
| 15:0 | InsPVID_0[15:0] | To enable per-port insert PVID function (P15-P0). 0: Disable (default) 1: Enable | RW | 0 |

# 11.13.    *QoS Configuration Register*

## 11.13.1. 0x0400H: QoS Control Register

**Table 79. 0x0400H: QoS Control Register**

| Bits | Name | Description | RW | Default |
|------|------|-------------|----|---------|
| 0 | EnDSPri | Enable TCP/IP TOS/DS (DiffServ) based Priority QoS.<br>0: Disabled (Default)<br>1: Enabled<br>When enabled, the priority definition is defined as follows:<br>High Priority: If TOS/DS[0:5]:<br>                 (EF) '101110';<br>                 (AF) '001010', '010010',<br>                         '011010', '100010';<br>                 (Network Control) "11x000'<br>Low Priority: TOS/DS = Other codepoint values<br>*Note 1: The DS[0:5] bit location is equal to the mapping of TOS[0:5] ={precedence[2:0], Delay, Throughput, Reliability}.*<br>*Note 2: DS=Differentiated Services, EF= Expected Forwarding, AF= Assured Forwarding.* | RW | 0 |
| 1 | En8021pPri | Enable 802.1p VLAN Tag Based Priority QoS Function.<br>0: Disable (Default)<br>1: Enable | RW | 0 |
| 2 | EnFCAutoOff | Enable Flow Control Ability Auto Turn Off for QoS.<br>Enabled: Enables auto turn off of a port's queue flow control ability for 1~2 seconds whenever the port receives a high priority frame. The flow control ability of this port is re-enabled when no high priority frames are received at this port during a 1~2 second period.<br>Disabled: When EnFCAutoOff is disabled, the flow control ability of this port for any packet will be enabled as it was set.<br>0: Disabled (Default)<br>1: Enabled | RW | 0 |
| 4:3 | QWEIGHT[1:0] | Weighted round robin ratio setting of priority queue.<br>The frame service rate of High-pri queue to Low-pri queue is:<br>00: 4:1<br>01: 8:1<br>10: 16:1 (Default)<br>11: High priority queue first always | RW | 10 |
| 15:5 | Reserved | | | |

## 11.13.2. 0x0401: Port Priority Configuration Registers 0

**Table 80. 0x0401: Port Priority Configuration Registers 0**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 15:0 | PortPriCfg[15:0] | Port-based Priority setting (Port0 ~ Port15). Sets the priority QoS based on the physical port. If a port is set as a high priority port, all packets received from that port will be treated as high priority packets. Bit value 1: Sets that port as a high priority port Bit value 0: Sets that port as a low priority port *Note: Ports 0~15 map to bits 0~15.* | RW | 0 |

# 11.14.    *PHY Access Control Register*

## 11.14.1. 0x0500H: PHY Access Control Register

**Table 81. 0x0500H: PHY Access Control Register**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 4:0 | REG_addr | PHY Register address setting for the PHY Access command. | RW | 0 |
| 9:5 | PHY_ID[4:0] | PHY ID (PHY address) setting for the PHY Access command. RTL8316B connected PHY ID is fixed as: Fast Ethernet Port0 ~ 15. PHY ID: 16,17, …, 30, 31. | RW | 0 |
| 13:10 | Reserved | | | 0 |
| 14 | PHY_RW | PHY Access Command. 0: PHY Access Read command (Default) 1: PHY Access Write command | RW | 0 |
| 15 | PHYCmdExeSta | PHY Access Command Execution Status. 0: Idle (Default) 1: Busy | R | 0 |

## 11.14.2. 0x0501H: PHY Access Write Data Register

**Table 82. 0x0501H: PHY Access Write Data Register**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 15:0 | PHY_WD[15:0] | PHY Access Write Out Data (16 bits). | RW | 0 |

## 11.14.3. 0x0502H: PHY Access Read Data Register

**Table 83. 0x0502H: PHY Access Read Data Register**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 15:0 | PHY_RD[15:0] | PHY Access Read In Data (16 bits). | R | 0 |

# 11.15. Port Control Register

## 11.15.1. 0x0607H: Global Port Control Register

**Table 84. 0x0607H: Global Port Control Register**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 0 | DisFDFC ($\overline{\text{EnFDFC}}$) | Disable Full Duplex Flow Control (802.3x PAUSE ability). This control bit will be applied to the switch only when a software reset is sent to the switch. This function can also be directly controlled by PHY register access through the PHY Access Control Register 0: Enable 802.3x Pause ability (Default) 1: Disable 802.3x Pause ability | RW | 0 HW pin: EnFDFC |
| 1 | DisBKP ($\overline{\text{EnBKP}}$) | Globally Disable Half Duplex Back Pressure Flow Control Ability. Set to globally disable the back pressure flow control ability of all ports. 0: Enable back pressure flow control ability (Default) 1: Disable back pressure flow control ability | RW | 0 HW pin. EnBKP |
| 2 | DisBCSFC | Disable Broadcast Packet Strict Flood Control. This control function is used under 802.3x flow control mode. Strict flood mode will drop broadcast packets (DA: FF-FF-FF-FF-FF-FF) if any destination port member is congested. Loose flood mode allows broadcast packets to be flooded to all non-congested ports. 0: Disable Broadcast Packet Strict Flood (Loose flood mode) (default) 1: Enable Broadcast Packet Strict Flood (Strict flood mode) | RW | 0 HW pin. DisBCSFC |
| 3 | DisIPMCFC | Disable IP Multicast Packet Strict Flood Control. This control function is used under 802.3x flow control mode. Strict flood mode will drop IP Multicast packets (DA: 01-00-5E-XX-XX-XX) if any destination port member is congested. Loose flood mode allows IP multicast packets to be flooded to all non-congested ports. 0: Disable IP Multicast Packet Strict Flood (Loose flood mode) (default) 1: Enable IP Multicast Packet Strict Flood (Strict flood mode) | RW | 0 |
| 4 | DisBRDCTRL ($\overline{\text{EnBRDCTRL}}$) | Disable Broadcast Storm Filtering Control. Set to disable the broadcast storm filtering control function. 1: Disable Broadcast storm filtering control (Default) 0: Enable Broadcast storm filtering control | RW | 0 HW pin: EnBRDCTRL |
| 15:5 | Reserved | | | |

## 11.15.2. 0x0608H: Port Disable Control Register 0

**Table 85. 0x0608H: Port Disable Control Register 0**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 15:0 | PortDisable[15:0] | Port Enable/Disable Control for ports 0~15.<br>Bit value 0: Port enable<br>Bit value 1: Port disable<br>When disabled, the port will disable packet transmission and reception except for Realtek Remote Control Packets.<br>*Note: Ports 0~15 map to bits 0~15.* | RW | 0 |

## 11.15.3. 0x060AH~0x0615. Port Property Configuration Register 0 ~ 7

For Port(2n) and Port(2n+1) the Port Property is defined as follows: n = 0, 1, 2,. …, 7 (Addr: 0x060AH +n); where n=0~7 for Fast Ethernet ports.

**Table 86. 0x060AH~0x0615. Port Property Configuration Register 0 ~ 7**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 7:0 | P(2n)_Property[7:0] | Port(2n) Port Property configuration.<br>Bit [4:0]: Media Capability[4:0]= (1000F, 100F, 100H, 10F, 10H).<br>Bit [5]: Pause ability (1: Enable).<br>Bit [6]: AsyPause ability (Asynchronous Pause) (1. enable)<br>Bit [7]: Enable Auto Negotiation (1: Enable). | RW | 100M. 0xAF |
| 15:8 | P(2n+1)_Property[7:0] | Port(2n+1) Port property configuration.<br>Bit [4:0]: Media Capability[4:0]=<br>{1000F, 100F, 100H, 10F, 10H}.<br>Bit [5]: Pause ability (1: Enable).<br>Bit [6]: AsyPause ability ( Asynchronous Pause)<br>(1: Enable).<br>Bit [7]: Enable Auto Negotiation (1: Enable). | RW | 100M. 0xAF |

*Note: A configuration update of these registers requires a software reset (via write Reg. 0x0000 bit 0 =1) to force the configuration to be written to the PHY register and restart the auto-negotiation process.*

## 11.15.4. 0x0619H~0x0624. Port Link Status Register 0 ~ 7

For Port(2n) and Port(2n+1) the Port Properties are defined as follows:
(n: 0,1,2,. …, 7) (Addr: 0x060AH +n).

**Table 87. 0x0619H~0x0625. Port Link Status Register 0 ~ 7**

| Bits | Name | Description | RW | Default |
|------|------|-------------|----|----|
| 7:0 | P(2n)_LinkStatus[7:0] | Port (2n) Port Link Status.<br><br>Bit [1:0]: Link speed[1:0]:<br>00: 10Mbps<br>01: 100Mbps<br>10: 1000Mbps<br>11: NA.<br><br>Bit [2]: Full duplex:<br>0: Half duplex<br>1: Full duplex<br>Bit[3]: Reserved.<br><br>Bit [4]: Link up:<br>0: Link down<br>1: Link up<br><br>Bit [5]: Flow control (back pressure or 802.3x):<br>For ports 0~15 (Fast Ethernet ports). Defined as Pause ability.<br>In half duplex mode. Defined as back pressure ability.<br>0: Flow control disabled<br>1: Flow control enabled<br><br>Bit [6]: AsyPause ability (Asymmetric Pause):<br>For ports 0~16 (Fast Ethernet ports) Don't Care.<br><br>Bit [7]: Enable Auto Negotiation (AN):<br>0: Disable AN<br>1: Enable AN | R | 0 |

| Bits | Name | Description | RW | Default |
|------|------|-------------|----|---------|
| 15:8 | P(2n+1)_LinkStatus[7:0] | Port(2n+1) Port Link Status.<br><br>Bit [1:0]: Link speed[1:0]:<br>00: 10Mbps<br>01: 100Mbps<br>10: 1000Mbps<br>11: NA.<br><br>Bit [2]: Full duplex:<br>0: Half duplex<br>1: Full duplex<br><br>Bit[3]: Reserved.<br><br>Bit [4]: Link up:<br>0: Link down<br>1: Link up<br><br>Bit [5]: Flow Control (back pressure or 802.3x):<br>For ports 0~15 (Fast Ethernet ports). Defined as Pause ability.<br>In half duplex mode. Defined as back pressure ability.<br>0: Flow control disabled<br>1: Flow control enabled<br><br>Bit [6]: AsyPause ability (Asymmetric Pause):<br>For ports 0~15 (Fast Ethernet ports) Don't Care.<br>In half duplex mode. Don't Care.<br>0: Flow control disabled<br>1: Flow control enabled<br><br>Bit [7]: Enable Auto Negotiation (AN):<br>0: Disable AN<br>1: Enable AN | R | 0 |

# 12.   MIB Counter Registers

## 12.1. *0x0700H~0x0707H: Port MIB Counter Object Selection Register 0~7*

For Port(2n), Port(2n+1), the Port MIB Counter Object Selection Register is defined as follows: n = 0, 1, 2, …, 7) (Addr=0x0700H +n).

**Table 88. 0x0700H~0x0707H: Port MIB Counter Object Selection Register 0~7**

| Bits | Name | Description | RW | Default |
|------|------|-------------|----|---------|
| 1:0 | P(2n)CNT1_MIBS [1:0] | Port(2n) Counter_1 MIB Object Selection.<br>P(2n)CNT_1_MIBS [1:0]<br>00: MIB object: RX byte count<br>01: MIB object: RX packet count (Default)<br>10: MIB object: CRC error packet count<br>11: MIB object: Collision packet count<br><br>RX byte count. This counter is incremented once for every data byte of a received and forwarded packet (includes both good and bad packets).<br>RX packet count. This counter is incremented once for every received and forwarded packet (includes both good and bad packets). | RW | 01 |
| 3:2 | P(2n)CNT2_MIBS [1:0] | Port(2n) Counter_2 MIB Object Selection.<br>P(2n)CNT_2_MIBS [1:0]<br>00: MIB object: TX byte count<br>01: MIB object: TX packet count (Default)<br>10: MIB object: CRC error packet count<br>11: MIB object: Collision packet count<br><br>TX byte count. This counter is incremented once for every data byte of a transmitted packet (includes both good and bad packets).<br>TX packet count. This counter is incremented once for every transmitted packet (includes both good and bad packets). | RW | 01 |

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 5:4 | P(2n)CNT3_MIBS [1:0] | Port(2n) Counter_3 MIB Object Selection<br>P(2n)CNT_3_MIBS [1:0]<br>00: MIB object: Drop byte count<br>01: MIB object: Drop packet count (Default)<br>10: MIB object: CRC error packet count<br>11: MIB object: Collision packet count<br><br>Drop packet count. This counter is incremented once for every drop of a received packet. Packet drop events could be due to undersize, oversize, CRC error, lack of resources, local packet, point-to-point control packet (ex. Pause packet, LACP packet, including RRCP® packets).<br>CRC error packet count. This counter is incremented once for every received packet with a valid length but with a CRC error.<br>Collision packet counter. This counter is incremented once for every collision event detected. | RW | 01 |
| 7:6 | P(2n+1)CNT1_MIBS [1:0] | Port(2n+1) Counter_1 MIB Object Selection. | RW | 01 |
| 9:8 | P(2n+1)CNT2_MIBS [1:0] | Port(2n+1) Counter_2 MIB Object Selection. | RW | 01 |
| 11:10 | P(2n+1)CNT3_MIBS [1:0] | Port(2n+1) Counter_3 MIB Object Selection. | RW | 01 |

# 12.2. 0x070DH ~071CH: Port MIB Counter 1 Register (RX Counter) (32 bits)

The MIB counters are 32-bit counters. After power on reset, the counters are all reset to 0. A read access of the MIB counter will NOT reset the counter to 0. When a MIB counter MIB object is changed, then the counter will be reset to 0 and the count will restart.

The time before the next read of the same counter should not be longer than the counter's timeout. The timeout of the 32-bit MIB counter depends on the object type and the port speed, and is calculated as follows:

Packet counter timeout is calculated based on 64-byte packets and byte counter timeout is calculated based on 1518 byte packets).

**Table 89. MIB Counter Timeout**

| Port Speed | MIB Object Type | MIB Counter Timeout (Sec.) |
|-----------|-----------------|----------------------------|
| 100Mbps | Packet count | 28862 |
| | Byte count | 348 |
| 10Mbps | Packet count | 288621 |
| | Byte count | 3481 |

## 12.2.1. For Port(n) MIB Counter 1 Register (32-bit). n=0, 1, 2, … 15 (Addr: 0x070DH+n)

**Table 90. 0x070DH ~0724H: Port MIB Counter 1 Register (RX Counter) (32 bits)**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 31:0 | Port(n)_MIB_CNT_1[31:0] | Port(n) MIB Counter_1[31:0] | R | 0 |

## 12.2.2. 0x0727~0736H: Port MIB Counter 2 Register (TX Counter) (32-bits)

For Port(n) MIB Counter 2 Register (32-bit): n = 0, 1, 2, … 15 (Addr: 0x0727H+n).

**Table 91. 0x0727~0736H: Port MIB Counter 2 Register (TX Counter) (32 bits)**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 31:0 | Port(n)_MIB_CNT_2[31:0] | Port(n) MIB Counter_2[31:0] | R | 0 |

## 12.2.3. 0x0741~0750H: Port MIB Counter 3 Register (Diagnostic Counter) (32-bits)

For Port(n) MIB Counter 3 Register (32-bit): n = 0, 1, 2, … 15 (Addr: 0x0741H+n).

**Table 92. 0x0741~0750H: Port MIB Counter 3 Register (Diagnostic Counter) (32 bits)**

| Bits | Name | Description | RW | Default |
|------|------|-------------|-----|---------|
| 31:0 | Port(n)_MIB_CNT_3[31:0] | Port(n) MIB Counter_3[31:0] | R | 0 |

# 13. Characteristics

## 13.1. DC Characteristics

Supply Voltage VDD: 3.3V ± 5%.

**Table 93. DC Characteristics**

| Parameter | Symbol | Conditions | Min | Typical | Max | Units |
|---|---|---|---|---|---|---|
| Power Supply Current | Icc | 16FE, wire-speed traffic load | | | 200 | mA |
| | | 16FE all idle | | | 140 | |
| Total Power Consumption | PS | 16FE, wire-speed traffic load | | | 660 | mW |
| | | 16FE all idle | | | 462 | |
| TTL Input High Voltage | $V_{ih}$ | | 2.0 | | | V |
| TTL Input Low Voltage | $V_{il}$ | | | | 0.8 | V |
| TTL Input Current | $I_{in}$ | | -10 | | 10 | uA |
| TTL Input Capacitance | $C_{in}$ | | | 2.9 | | pF |
| Output High Voltage | $V_{oh}$ | | 2.6 | | 3.6 | V |
| Output Low voltage | $V_{ol}$ | | 0 | | 0.4 | V |

# 13.2. AC Characteristics

## 13.2.1. PHY Management (SMI) Timing

**Table 94. PHY Management (SMI) Timing**

| Symbol | Description | Minimum | Typical | Maximum | Units |
|--------|-------------|---------|---------|---------|-------|
| t1 | MDC clock period | - | 1360 | - | ns |
| t2 | MDC high level width | - | 680 | - | ns |
| t3 | MDC low level width | - | 680 | - | ns |
| t4 | MDIO to MDC rising setup time (Write Bits) | | 680 | - | ns |
| t5 | MDIO to MDC rising hold time (Write Bits) | | 680 | - | ns |
| t6 | MDC to MDIO delay (Read Bits) | - | - | 20 | ns |
| t7 | MDC/MDIO actives from RST# deasserted | - | 45 | - | ms |
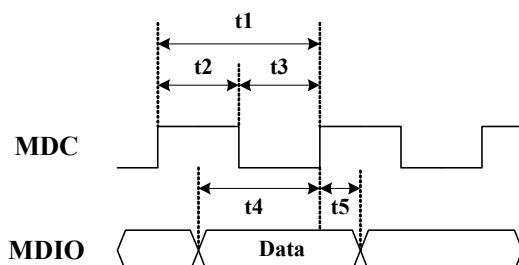


**Figure 15. MDC/MDIO Write Timing**
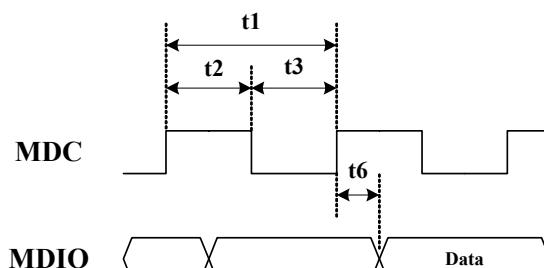


**Figure 16. MDC/MDIO Read Timing**
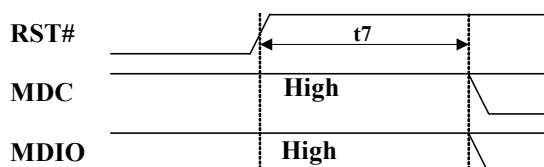


**Figure 17. MDC/MDIO Reset Timing**

## 13.2.2. SMII Transmit Timing

**Table 95. PHY Management (SMI) Timing**

| Symbol | Description | Minimum | Typical | Maximum | Units |
|--------|-------------|---------|---------|---------|-------|
| T_opd_txd_smii | REFCLK rising edge to TXD (SYNC) delay. | 2 | 4 | 5 | ns |
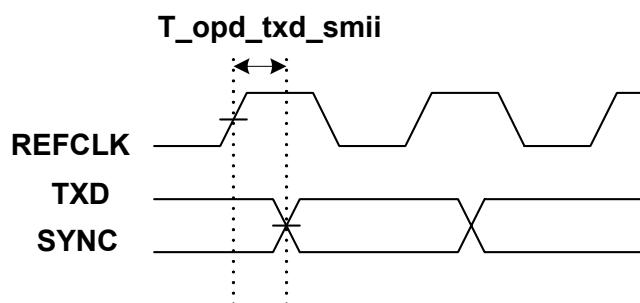
**Figure 18. SMII Transmit Timing**

## 13.2.3. SMII Receive Timing

**Table 96. SMII Receive Timing**

| Symbol | Description | Minimum | Typical | Maximum | Units |
|--------|-------------|---------|---------|---------|-------|
| T_ipsu_rxd_smii | RXD setup time to REFCLK. | 2 | | | ns |
| T_iphd_rxd_smii | RXD hold time from REFCLK. | 1.5 | | | ns |
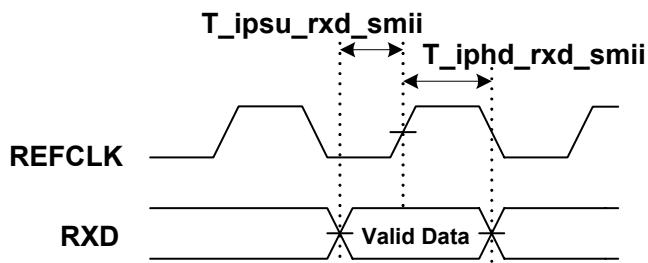
**Figure 19. SMII Receive Timing**

# 14.  Mechanical Information
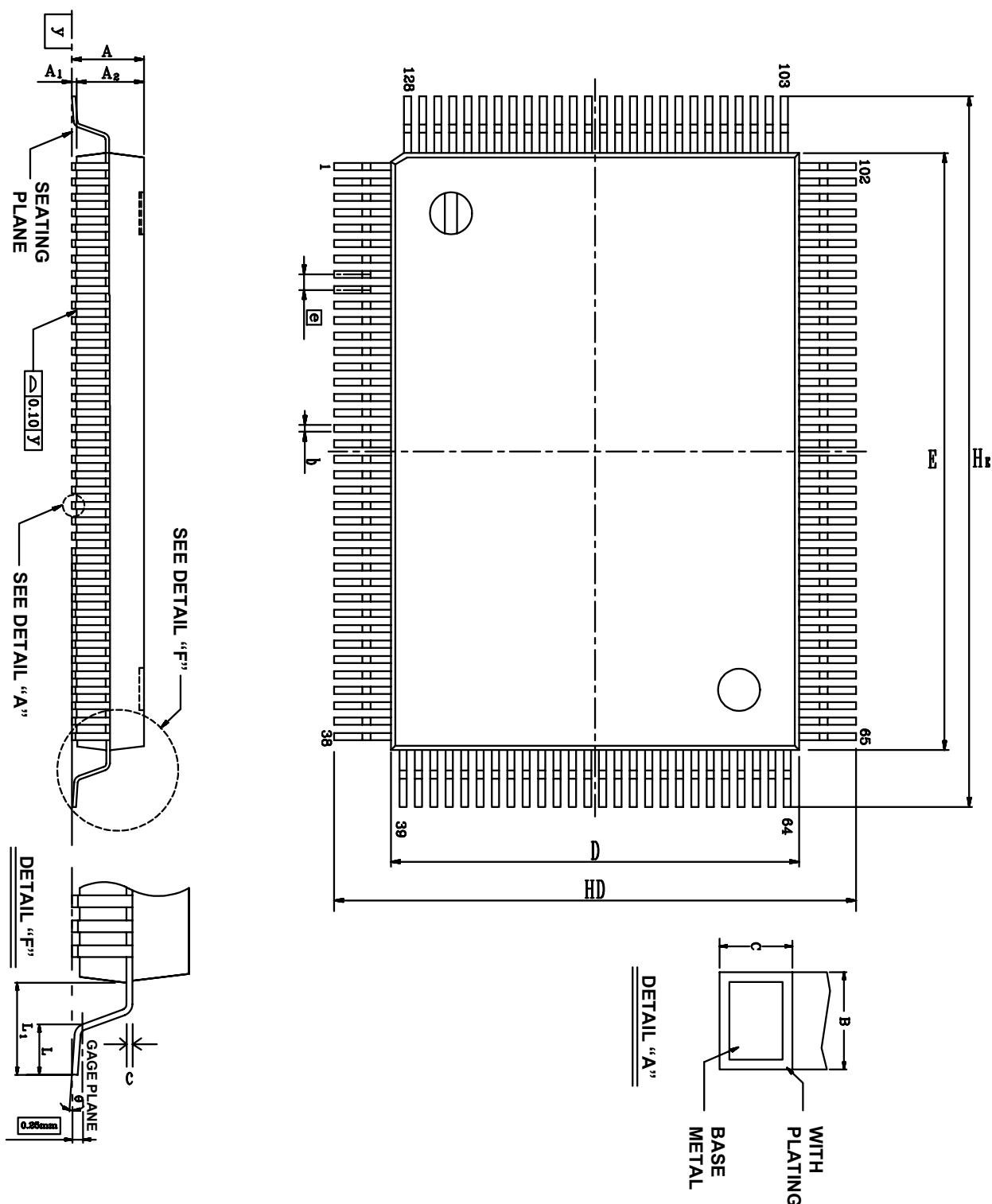


See the Mechanical Dimensions notes on the next page.

## 14.1. *Mechanical Dimensions Notes*

| Symbol | Dimensions in inches | | | Dimensions in mm | | |
|---|---|---|---|---|---|---|
| | Min | Typical | Max | Min | Typical | Max |
| **A** | - | - | 0.134 | - | - | 3.40 |
| **A1** | 0.004 | 0.010 | 0.036 | 0.10 | **0.25** | 0.91 |
| **A2** | 0.102 | 0.112 | 0.122 | 2.60 | **2.85** | 3.10 |
| **b** | 0.005 | 0.009 | 0.013 | 0.12 | **0.22** | 0.32 |
| **c** | 0.002 | 0.006 | 0.010 | 0.05 | **0.15** | 0.25 |
| **D** | 0.541 | 0.551 | 0.561 | 13.75 | **14.00** | 14.25 |
| **E** | 0.778 | 0.787 | 0.797 | 19.75 | **20.00** | 20.25 |
| **e** | 0.010 | 0.020 | 0.030 | 0.25 | **0.5** | 0.75 |
| **HD** | 0.665 | 0.677 | 0.689 | 16.90 | **17.20** | 17.50 |
| **HE** | 0.902 | 0.913 | 0.925 | 22.90 | **23.20** | 23.50 |
| **L** | 0.027 | 0.035 | 0.043 | 0.68 | **0.88** | 1.08 |
| **L1** | 0.053 | 0.063 | 0.073 | 1.35 | **1.60** | 1.85 |
| **y** | - | - | 0.004 | - | - | 0.10 |
| **θ** | 0° | - | 12° | 0° | - | 12° |

Notes:
1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar rotrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. Should be based on final visual inspection.

| TITLE: -CU L/F, PQFP FOOTPRINT 3.2 mm | | | |
|---|---|---|---|
| LEADFRAME MATERIAL: | | | |
| APPROVE | | DOC. NO. | |
| | | VERSION | 1.2 |
| | | PAGE | |
| CHECK | | DWG NO. | Q128 - 1 |
| | | DATE | |
| REALTEK SEMICONDUCTOR CORP. | | | |

# 15.   Ordering Information

**Table 97. Ordering Information**

| Part Number | Package | Status |
|---|---|---|
| RTL8316B | PQFP-128 | Available Now |
| RTL8316B-LF | RTL8316B with Lead (Pb)-Free package | Available Now |

*Note: See page 6 for lead (Pb)-free package identification.*

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