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SEL0621: Experiência 3

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Programa de Graduação

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1 Introdução

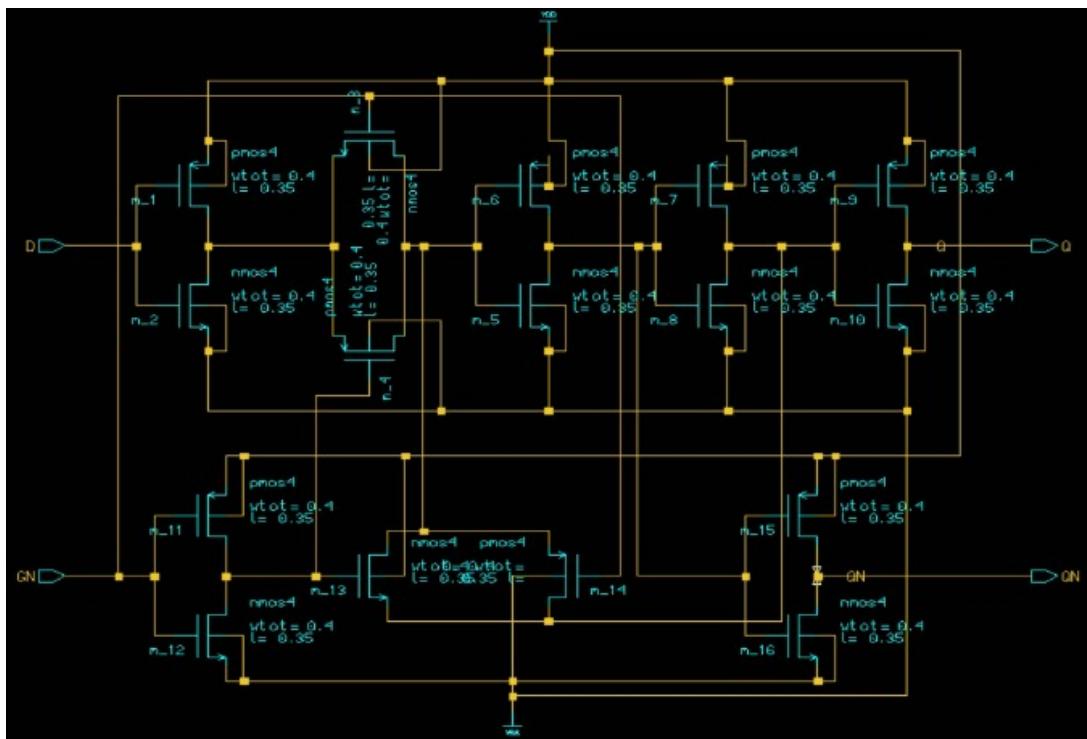
Neste experimento analisamos as principais diferenças entre as extrações do circuito (esquematico, *Layout* - C+CC e *Layout* - R+C+CC) contra o valor teórico, concluindo que conforme a complexidade da extração mais estruturas parasitas impactam em aspectos como frequência máxima de operação e consumo de potência. Para a análise de corrente foi explorado o conceito de tempos de *holding* e de *set-up* em *flip-flops*, ou seja, “margens” antes e após o pulso de *clock* para manter constante a retenção de dados em *flip-flops*.

2 Questões

Questão 2: Procure o layout da célula DL1 e o abra no IcStation. Levante e desenhe o circuito esquemático desta célula (não precisa determinar as dimensões dos transistores). Observe com cuidado o layout feito

Círcuito da célula DL1 presente na figura 1.

Figura 1 – Esquemático da célula DL1 presente na biblioteca CORELAB

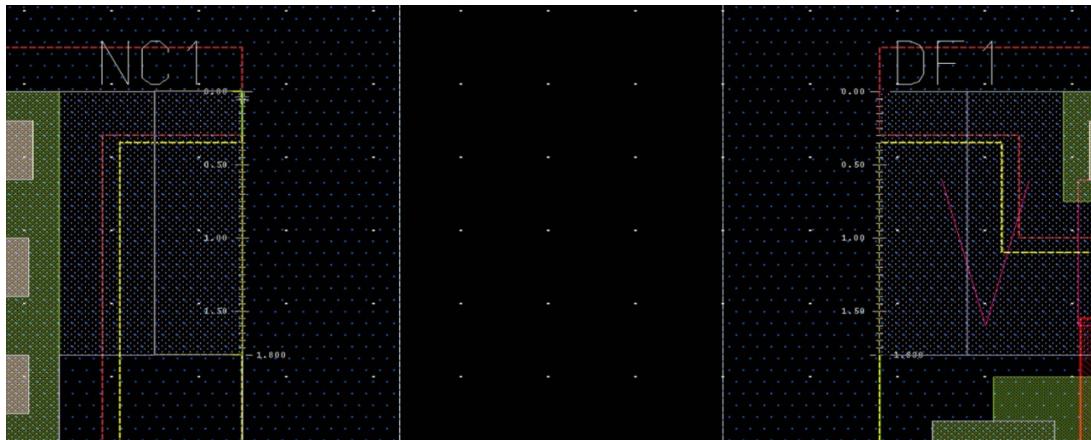


Fonte: Pelos próprios autores

Questão 3: Observe que na célula DL1 as linhas dos sinais de VDD e VSS correm nas extremidades superior e inferior. Qual é a dimensão vertical destas linhas e qual a distância entre elas. Abra outra célula da biblioteca e verifique as dimensões das linhas de VDD e VSS e a distância entre elas. São iguais em todas as células? Seria/é interessante que fossem/sejam iguais, por quê?

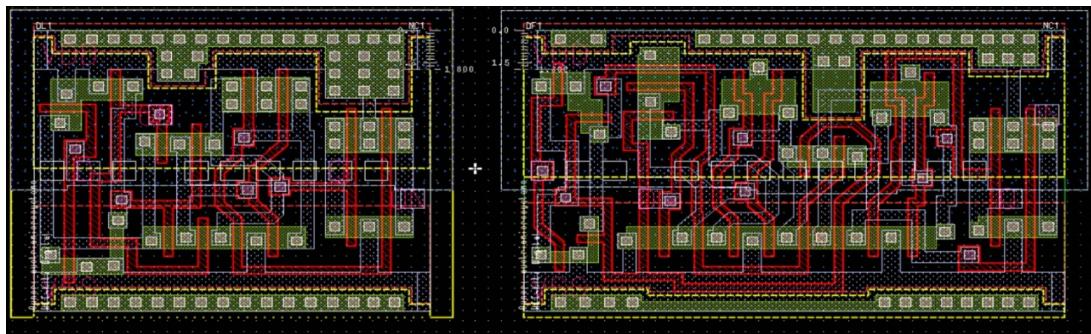
Como visto na figura 2 temos que os terminais de alimentação possuem $1,8\mu m$ e todos as células da biblioteca **CORELIB** também apresentam dimensão vertical entre terminais de $9,4\mu m$, esse padrão possibilita melhor alinhamento na utilizações desta biblioteca (como visto na figura 3), o que economiza área de projeto e uso de material.

Figura 2 – *Layout* com dimensão dos terminais de alimentação das células da biblioteca CORELAB DL1 e DF1



Fonte: Pelos próprios autores

Figura 3 – *Layout* células da biblioteca CORELAB DL1 e DF1



Fonte: Pelos próprios autores

Questão 4: Considere o circuito da Figura 2. Desenhe seu esquemático utilizando as células DF3, NAND22. Como sinal de entrada deve colocar o clock e D; como sinal de saída, Q. Gere o símbolo para a célula e faça todas as verificações necessárias. Certifique-se que não haja erros ou warnings.

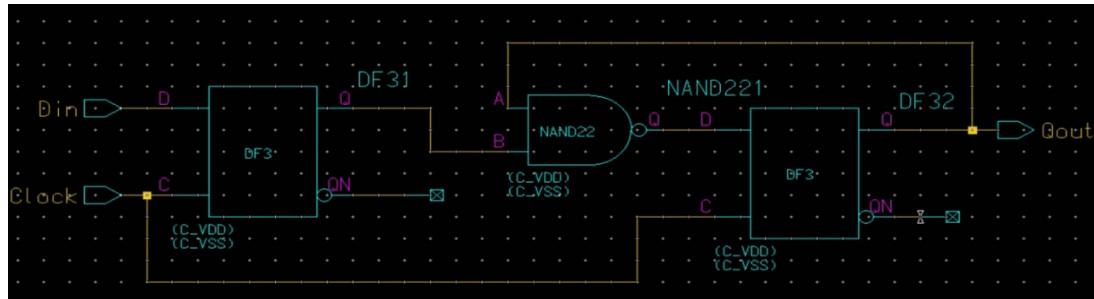
O esquemático solicitado e implementado e apresentado na figura 19.

Questão 5: A partir das informações dos blocos que compõe este circuito estime o valor máximo da frequência do *clock* que o circuito pode suportar (considere a entrada D = “1”, utilize o pior caso entre subida e descida das portas e considere que os sinais são rápidos). Apresente os cálculos.

Inicialmente, acessamos os *datasheets* na localidade /local/tools/dkit/ams_3.70_mgc/www/index.html temos algumas informações a cerca dos componentes utilizados (DF3 e NAND22) como visto nas figuras 5 e 6.

Considerando a entrada $D = 1$ temos que o pior caso é a descida, e considerando

Figura 4 – Esquemático do Latch



Fonte: Pelos próprios autores

Figura 5 – Datasheet DF3

DF3 is a static, master-slave D flip-flop with 3x drive strength.																																																																																												
Truth table	Symbol	Capacitance																																																																																										
<table border="1"> <tr> <th>C</th><th>D</th><th>Q</th><th>QN</th></tr> <tr> <td>R</td><td>0</td><td>0</td><td>1</td></tr> <tr> <td>R</td><td>1</td><td>1</td><td>0</td></tr> </table>	C	D	Q	QN	R	0	0	1	R	1	1	0	<p>DF3-Symbol</p>	<table border="1"> <tr> <th>Pin</th><th>Cap [pF]</th></tr> <tr> <td>C</td><td>0.004</td></tr> <tr> <td>D</td><td>0.005</td></tr> </table>	Pin	Cap [pF]	C	0.004	D	0.005																																																																								
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Fonte: Retirado de ([CORPORATION, 2005](#))

que o projeto trabalha a alta velocidade logo *slope* será de 0,05.

Com o exposto em aula a máxima frequência de *clock* depende do atraso total desempenhado pelo sistema:

$$T_{Total} = T_{setup} + T_{NAND22} + T_{DF3}$$

verificamos que tempo de atraso de propagação em descido ou subida depende da carga associada, logo para o componente **DF31** temos uma carga 0,013 pF correspon-

Figura 6 – Datasheet NAND22

NAND22 is a 2-input NAND gate with 2x drive strength.

Truth table			Symbol		Capacitance			
A	B	Q	NAND22-Symbol		Pin	Cap [pF]		
0	X	1			A	0.008		
X	0	1			B	0.013		
1	1	0						
Area			Power					
0.085 mil ²			0.70 µW/MHz					
55 µm ²								
AC Characteristics								
Delay[ns] = f(SL, L), Output Slope [ns] = f(SL, L) with SL = Input Slope [ns] and L = Output Load [pF]								
AC Characteristics: T _j = 25 °C VDD=3.3V Typical Process								
		Rise		Fall				
Slope [ns]	0.05	2	0.05	2				
Load [pF]	0.002	0.64	0.002	0.64	0.002	0.64		
Delay A => Q	0.05	1.62	0.35	2.00	0.03	0.83	-0.11	1.08
Delay B => Q	0.07	1.64	0.43	2.04	0.03	0.84	-0.15	0.93
Slew A => Q	0.08	4.08	0.32	4.10	0.04	1.96	0.34	2.12
Slew B => Q	0.13	4.14	0.36	4.13	0.04	1.96	0.37	2.06

Fonte: Retirado de ([CORPORATION, 2005](#))

dente ao pino B (NAND221), e para o componente **NAND221** temos carga de 0,005pF correspondente ao pino D do componente **DF32**, por fim, temos que utilizaremos uma interpolação linear considerando que a relação capacidade e *delay* é linear, além de considerar D = 1 , temos a tabela 1.

Tabela 1 – Tempo de atraso de propagação dos componentes

Componente	Carga [pF]	Atraso na descida [ns]	Atraso na subida [ns]
NAND22	0,002	0,07	0,03
NAND22	0,64	1,64	0,84
DF3	0,003	0,53	0,61
DF3	0,96	2,08	1,66

Fonte: Pelos próprios autores

$$\frac{0,013 - 0,003}{0,96 - 0,003} = \frac{x - 0,61}{1,66 - 0,61} \Rightarrow \frac{x - 0,61}{1,05} = \frac{0,01}{0,957} \Rightarrow x = t_{DF3} = 0,621\text{ns}$$

$$\frac{0,005 - 0,002}{0,64 - 0,002} = \frac{y - 0,07}{1,64 - 0,07} \Rightarrow \frac{y - 0,07}{1,57} = \frac{0,003}{0,638} \Rightarrow y = t_{NAND22} = 0,077\text{ns}$$

Com a expressão do período do circuito como um todo, temos a frequência máxima do *clock*:

$$T_{total} = 0 + 0,621 + 0,077 = 0,698\text{ns}$$

$$F_{máx} = \frac{1}{0,698 * 10^{-9}} \approx 1,4326648\text{GHz}$$

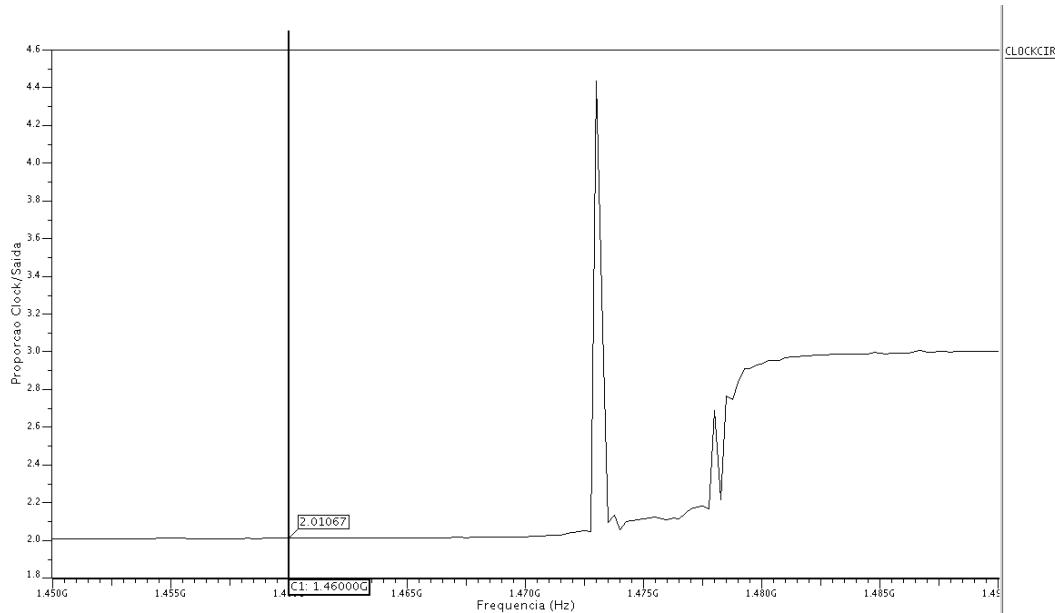
Questão 6: O que significam tempos de *holding* e de *set-up* em *flip-flops*. Qual seria o valor máximo do clock, do exercício acima, caso o tempo de *set-up* fosse de 0,1 ns.

A característica dos *flip-flops* em manter os dados constantes é necessário para exercer suas funcionalidades, para a metaestabilidade em *flip-flops* podemos contorná-lo através de “margens” para mate-lo constante, logo são estabelecidos tempo de *setup* e *hold* (antes e após o pulso de *clock*).

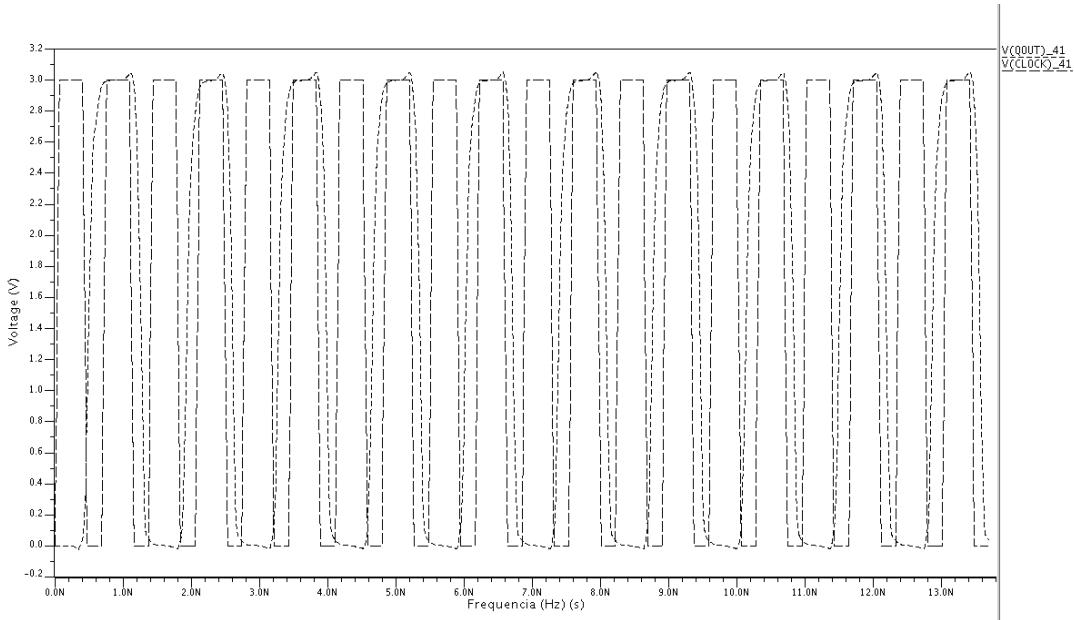
Questão 7: Gere, a partir do esquemático, um arquivo netlist para o ELD. Simule o circuito com os parâmetros típicos e determine a máxima velocidade (*clock*) do circuito.

Neste item temos a análise do circuito com células *flip-flop* e ***NAND***, realizamos o estudo para verificar o comportamento do circuito mediante excursionamento de frequência de operação e a proporção do período do *clock* com a saída vista na figura 7 e sinais tensões do *clock* e saída para as frequências marcadas na figura 8 (disposto na figura 7).

Figura 7 – Proporção entre o ciclo de *clock* e período de saída do circuito para excursionamento de frequência, marcado em 1,46GHz



Fonte: Pelos próprios autores

Figura 8 – Sinais de tensão de saída e *clock* para frequência de 1,46GHz

Fonte: Pelos próprios autores

Código completo da simulação:

```

.CONNECT GROUND 0
.global VDD VSS
.subckt INVBT_CORE_PARAM#6 Q A
    MN2 Q A VSS VSS MODN w=5.000000e-07 l=3.500000e-07 as=4.250000e-13
+ ad=4.250000e-13 ps=2.200000e-06 pd=2.200000e-06 nrs=8.500000e-01 nrd=8.500000e-01
    MP2 Q A VDD VDD MODP w=1.000000e-06 l=3.500000e-07 as=8.500000e-13
+ ad=8.500000e-13 ps=2.700000e-06 pd=2.700000e-06 nrs=4.250000e-01 nrd=4.250000e-01
.ends INVBT_CORE_PARAM#6
* Component pathname : $GATES/invb_core:param#5
.subckt INVBT_CORE_PARAM#5 Q A
    MN2 Q A VSS VSS MODN w=4.000000e-07 l=3.500000e-07 as=3.400000e-13
+ ad=3.400000e-13 ps=2.100000e-06 pd=2.100000e-06 nrs=1.062500e+00 nrd=1.062500e+00
    MP2 Q A VDD VDD MODP w=8.000000e-07 l=3.500000e-07 as=6.800000e-13
+ ad=6.800000e-13 ps=2.500000e-06 pd=2.500000e-06 nrs=5.312500e-01 nrd=5.312500e-01
.ends INVBT_CORE_PARAM#5
* Component pathname : $GATES/tgate_core
.subckt TGATE_CORE OUT EN EP IN
    MN1 OUT EN IN VSS MODN w=1.000000e-06 l=3.500000e-07 as=8.500000e-13
+ ad=8.500000e-13 ps=2.700000e-06 pd=2.700000e-06 nrs=4.250000e-01 nrd=4.250000e-01
    MP1 OUT EP IN VDD MODP w=1.000000e-06 l=3.500000e-07 as=8.500000e-13

```

```

+ ad=8.50000e-13 ps=2.70000e-06 pd=2.70000e-06 nrs=4.25000e-01 nrd=4.25000e-01
  .ends TGATE_CORE
* Component pathname : $GATES/inv_core:param#2
  .subckt INV_CORE_PARAM#2 OUT IN
    MP1 OUT IN VDD VDD MODP w=1.60000e-06 l=3.50000e-07 as=1.36000e-12
+ ad=1.36000e-12 ps=3.30000e-06 pd=3.30000e-06 nrs=2.656250e-01 nrd=2.656250e-01
    MN1 OUT IN VSS VSS MODN w=1.00000e-06 l=3.50000e-07 as=8.50000e-13
+ ad=8.50000e-13 ps=2.70000e-06 pd=2.70000e-06 nrs=4.25000e-01 nrd=4.25000e-01
  .ends INV_CORE_PARAM#2
* Component pathname : $GATES/inv_core:param#3
  .subckt INV_CORE_PARAM#3 OUT IN
    MP1 OUT IN VDD VDD MODP w=4.80000e-06 l=3.50000e-07 as=4.08000e-12
+ ad=4.08000e-12 ps=6.50000e-06 pd=6.50000e-06 nrs=8.854167e-02 nrd=8.854167e-02
    MN1 OUT IN VSS VSS MODN w=3.00000e-06 l=3.50000e-07 as=2.55000e-12
+ ad=2.55000e-12 ps=4.70000e-06 pd=4.70000e-06 nrs=1.416667e-01 nrd=1.416667e-01
  .ends INV_CORE_PARAM#3
* Component pathname : $GATES/clinva_core
  .subckt CLINVA_CORE Q A C CN
    MP1 NET10 CN VDD VDD MODP w=1.60000e-06 l=3.50000e-07 as=1.36000e-12
+ ad=1.36000e-12 ps=3.30000e-06 pd=3.30000e-06 nrs=2.656250e-01 nrd=2.656250e-01
    MPO Q A NET10 VDD MODP w=1.60000e-06 l=3.50000e-07 as=1.36000e-12
+ ad=1.36000e-12 ps=3.30000e-06 pd=3.30000e-06 nrs=2.656250e-01 nrd=2.656250e-01
    MN1 NET18 C VSS VSS MODN w=1.00000e-06 l=3.50000e-07 as=8.50000e-13
+ ad=8.50000e-13 ps=2.70000e-06 pd=2.70000e-06 nrs=4.25000e-01 nrd=4.25000e-01
    MNO Q A NET18 VSS MODN w=1.00000e-06 l=3.50000e-07 as=8.50000e-13
+ ad=8.50000e-13 ps=2.70000e-06 pd=2.70000e-06 nrs=4.25000e-01 nrd=4.25000e-01
  .ends CLINVA_CORE
* Component pathname : $CORELIB/DF3
  .subckt DF3 Q QN C D
    X_I54 CN C INV_B_CORE_PARAM#6
    X_I53 CI CN INV_B_CORE_PARAM#5
    X_I55 X CN CI NET55 TGATE_CORE
    X_I56 NET48 CI CN NET47 TGATE_CORE
    X_I57 X CI CN NET63 TGATE_CORE
    X_I58 NET63 NET48 INV_CORE_PARAM#2
    X_I59 Q NET57 INV_CORE_PARAM#3
    X_I60 QN NET55 INV_CORE_PARAM#3
    X_I61 NET47 NET63 INV_CORE_PARAM#2
    X_I62 NET55 NET57 INV_CORE_PARAM#2

```

```

        X_I63 NET57 X INV_CORE_PARAM#2
        X_I52 NET48 D CN CI CLINVA_CORE
.ends DF3
* Component pathname : $GATES/nand2_core
.subckt NAND2_CORE OUT A B
    MP1 OUT A VDD VDD MODP w=3.200000e-06 l=3.500000e-07 as=2.720000e-12
+ ad=2.720000e-12 ps=4.900000e-06 pd=4.900000e-06 nrs=1.328125e-01 nrd=1.328125e-01
    MP2 OUT B VDD VDD MODP w=3.200000e-06 l=3.500000e-07 as=2.720000e-12
+ ad=2.720000e-12 ps=4.900000e-06 pd=4.900000e-06 nrs=1.328125e-01 nrd=1.328125e-01
    MN1 OUT A NET13 VSS MODN w=4.000000e-06 l=3.500000e-07 as=3.400000e-12
+ ad=3.400000e-12 ps=5.700000e-06 pd=5.700000e-06 nrs=1.062500e-01 nrd=1.062500e-01
    MN2 NET13 B VSS VSS MODN w=4.000000e-06 l=3.500000e-07 as=3.400000e-12
+ ad=3.400000e-12 ps=5.700000e-06 pd=5.700000e-06 nrs=1.062500e-01 nrd=1.062500e-01
.ends NAND2_CORE
* Component pathname : $CORELIB/NAND22
.subckt NAND22 Q A B
    X_I1 Q A B NAND2_CORE
.ends NAND22
* MAIN CELL: Component pathname : $mydl/default.group/logic.views/dlclock
    X_DF32 QOUT N$9 CLOCK N$10 DF3
    X_NAND221 N$10 QOUT N$3 NAND22
    X_DF31 N$3 N$4 CLOCK DIN DF3
*** Parametros
.Param tensao=3v
.Param F=0.2G P='1/F'
*** Tensoes estabelecidas
Vdd VDD GROUND DC tensao
.CONNECT VSS 0
Vclock CLOCK GROUND PULSE(0 3.0 0 '0.1*P' '0.1*P' '0.49*P' P)
*** Conexao do circuito
.CONNECT DIN VDD

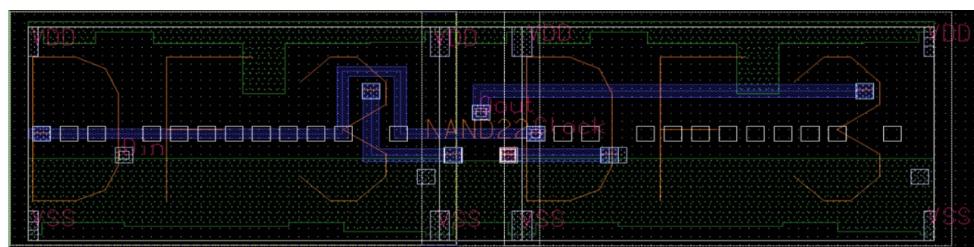
*** Tempo de propagacao de subida e descida
.meas tran Pout trig v(QOUT) val=tensao/2 rise=3
+ targ v(QOUT) val=tensao/2 rise=4
.meas tran PClock trig v(CLOCK) val=tensao/2 rise=3
+ targ v(CLOCK) val=tensao/2 rise=4
.meas tran clockCir PARAM='Pout/Pclock'

```

```
*** Escursionando frequencia em busca da maxima
.tran P '20*P' 0 'P/1000' sweep F INCR 0.00025G 1.45G 1.49G
*****
.probe tran ALL
.include Model135_Eldo
.end
```

Questão 8: Gere agora o layout para o circuito (use para isso o design *viewpoint* não o *schematic*).

Figura 9 – *Layout* do circuito DF3-NAND22-DF3

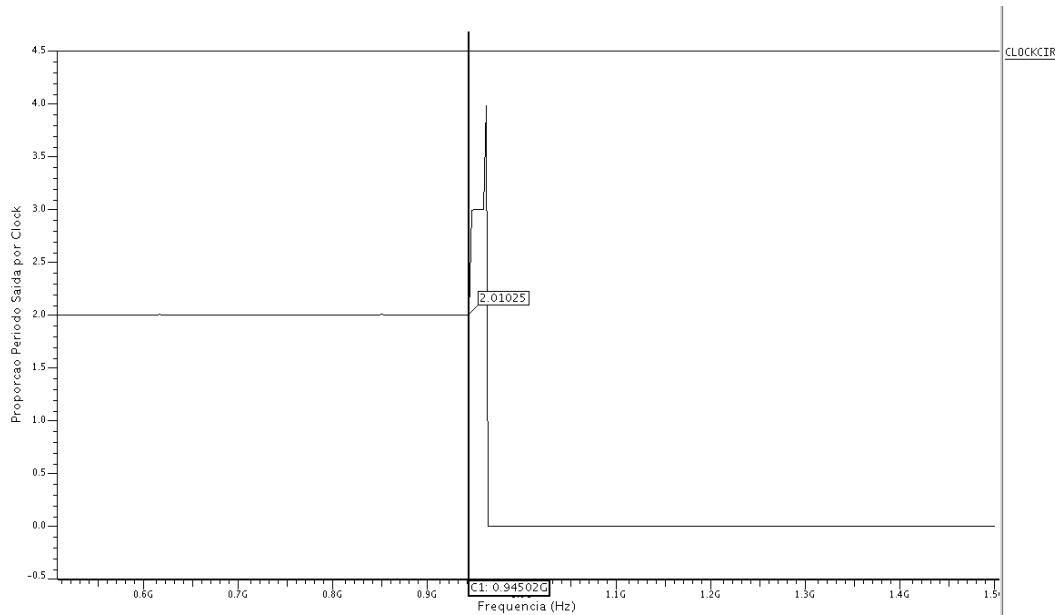


Fonte: Pelos próprios autores

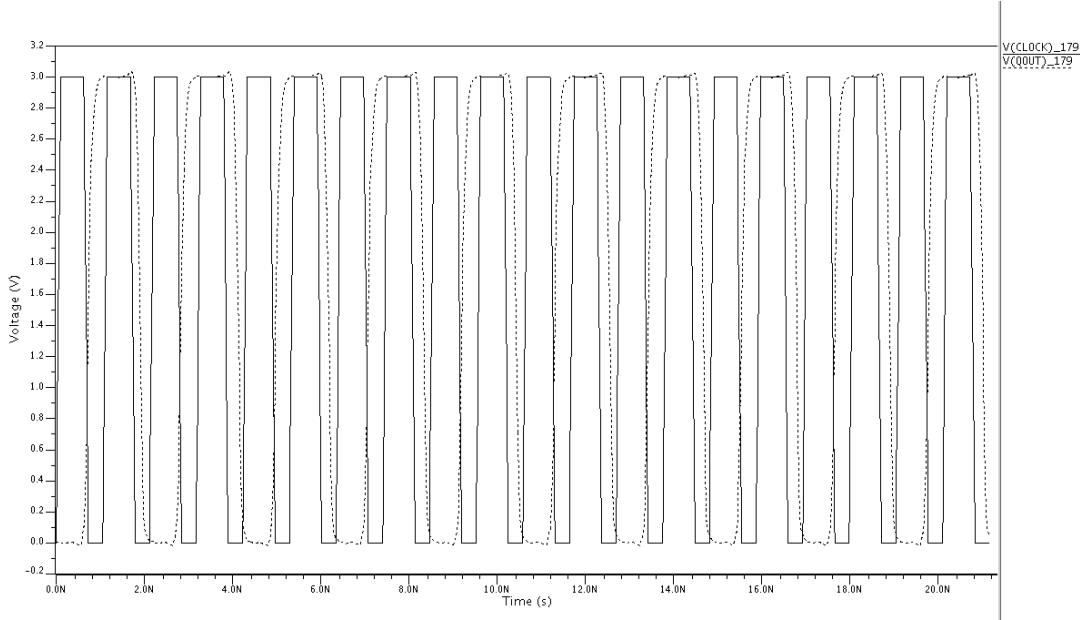
Questão 9: Faça a extração do circuito via o Calibre com a opção C+CC (deve ser usada uma configuração que garanta que o nome dos nós venha do schematic). Simule o circuito com parâmetros típicos e determine sua máxima velocidade. Utilize as mesmas condições do exercício 7

Neste item, com a extração C+CC, temos a análise do circuito com células *flip-flop* e **NAND**, realizamos o estudo para verificar o comportamento do circuito mediante excursionamento de frequência de operação e a proporção do período do *clock* com a saída vista na figura 10 e sinais tensões do *clock* e saída para as frequências marcadas na figura 10 (disposto na figura 11).

Figura 10 – Proporção entre o ciclo de *clock* e período de saída do circuito para excursionamento de frequência, marcado em 0,945GHz



Fonte: Pelos próprios autores

Figura 11 – Sinais de tensão de saída e *clock* para frequência de 0,945GHz

Fonte: Pelos próprios autores

Código completo da simulação:

```
mM0 8 1 VSS VSS MODN L=3.5e-07 W=4e-06 AD=9.7875e-13 AS=2.755e-12 PD=4.5e-07
+ PS=5.35e-06 NRD=0.0977011 NRS=0.0977011
mM1 3 QOUT 8 VSS MODN L=3.5e-07 W=4e-06 AD=2.6825e-12 AS=9.7875e-13
+ PD=5.35e-06 PS=4.5e-07 NRD=0.0977011 NRS=0.0977011
mM2 3 1 VDD VDD MODP L=3.5e-07 W=3.2e-06 AD=1.62625e-12 AS=2.52875e-12
+ PD=1.1e-06 PS=4.55e-06 NRD=0.119718 NRS=0.119718
mM3 VDD QOUT 3 VDD MODP L=3.5e-07 W=3.2e-06 AD=2.89375e-12 AS=1.62625e-12
+ PD=5.25e-06 PS=1.1e-06 NRD=0.119718 NRS=0.119718
mX4_M0 VSS CLOCK X4_2 VSS MODN L=3.5e-07 W=5e-07 AD=5.375e-13 AS=5.9e-13
+ PD=1.97222e-06 PS=2.7e-06 NRD=0.85 NRS=0.85
mX4_M1 X4_3 X4_2 VSS VSS MODN L=3.5e-07 W=4e-07 AD=5.7e-13 AS=4.3e-13
+ PD=2.8e-06 PS=1.57778e-06 NRD=1.0625 NRS=1.0625
mX4_M2 X4_15 X4_2 VSS VSS MODN L=3.5e-07 W=1e-06 AD=2.25e-13 AS=7.45e-13
+ PD=4.5e-07 PS=2.7e-06 NRD=0.425 NRS=0.425
mX4_M3 X4_5 DIN X4_15 VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=2.25e-13 PD=1e-06
+ PS=4.5e-07 NRD=0.425 NRS=0.425
mX4_M4 X4_6 X4_3 X4_5 VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13 PD=1e-06
+ PS=1e-06 NRD=0.425 NRS=0.425
mX4_M5 VSS X4_7 X4_6 VSS MODN L=3.5e-07 W=1e-06 AD=5.125e-13 AS=5e-13
+ PD=1.025e-06 PS=1e-06 NRD=0.425 NRS=0.425
```

mX4_M6 X4_7 X4_5 VSS VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5.125e-13 PD=1e-06
+ PS=1.025e-06 NRD=0.425 NRS=0.425
mX4_M7 X4_X X4_3 X4_7 VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13 PD=1e-06
+ PS=1e-06 NRD=0.425 NRS=0.425
mX4_M8 X4_9 X4_2 X4_X VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13 PD=1e-06
+ PS=1e-06 NRD=0.425 NRS=0.425
mX4_M9 VSS X4_10 X4_9 VSS MODN L=3.5e-07 W=1e-06 AD=5.875e-13 AS=5e-13
+ PD=1.175e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX4_M10 X4_10 X4_X VSS VSS MODN L=3.5e-07 W=1e-06 AD=1.325e-12 AS=5.875e-13
+ PD=4.25e-06 PS=1.175e-06 NRD=0.425 NRS=0.425
mX4_M11 VSS X4_10 1 VSS MODN L=3.5e-07 W=2.975e-06 AD=1.4875e-12 AS=2.0125e-12
+ PD=1e-06 PS=4.675e-06 NRD=0.142857 NRS=0.142857
mX4_M12 X4_QN X4_9 VSS VSS MODN L=3.5e-07 W=2.975e-06 AD=2.0125e-12
+ AS=1.4875e-12 PD=4.675e-06 PS=1e-06 NRD=0.142857 NRS=0.142857
mX4_M13 VDD CLOCK X4_2 VDD MODP L=3.5e-07 W=1e-06 AD=1.16944e-12 AS=7.45e-13
+ PD=2.86111e-06 PS=2.7e-06 NRD=0.425 NRS=0.425
mX4_M14 VDD X4_2 X4_3 VDD MODP L=3.5e-07 W=8e-07 AD=9.35556e-13 AS=7.55e-13
+ PD=2.28889e-06 PS=3.1e-06 NRD=0.53125 NRS=0.53125
mX4_M15 X4_5 X4_2 X4_6 VDD MODP L=3.5e-07 W=1e-06 AD=5e-13 AS=1.355e-12
+ PD=1e-06 PS=4.1e-06 NRD=0.425 NRS=0.425
mX4_M16 X4_16 DIN X4_5 VDD MODP L=3.5e-07 W=1.6e-06 AD=3.6e-13 AS=8e-13
+ PD=4.5e-07 PS=1.6e-06 NRD=0.265625 NRS=0.265625
mX4_M17 VDD X4_3 X4_16 VDD MODP L=3.5e-07 W=1.6e-06 AD=1.31625e-12 AS=3.6e-13
+ PD=3.3e-06 PS=4.5e-07 NRD=0.265625 NRS=0.265625
mX4_M18 VDD X4_7 X4_6 VDD MODP L=3.5e-07 W=1.6e-06 AD=9.1125e-13 AS=1.25e-12
+ PD=1.725e-06 PS=3.7e-06 NRD=0.217949 NRS=0.217949
mX4_M19 X4_7 X4_5 VDD VDD MODP L=3.5e-07 W=1.6e-06 AD=1.25e-12 AS=9.1125e-13
+ PD=3.7e-06 PS=1.725e-06 NRD=0.217949 NRS=0.217949
mX4_M20 X4_X X4_2 X4_7 VDD MODP L=3.5e-07 W=1e-06 AD=5e-13 AS=7.45e-13
+ PD=1e-06 PS=2.7e-06 NRD=0.425 NRS=0.425
mX4_M21 X4_9 X4_3 X4_X VDD MODP L=3.5e-07 W=1e-06 AD=8.5e-13 AS=5e-13
+ PD=2.7e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX4_M22 VDD X4_10 X4_9 VDD MODP L=3.5e-07 W=1.6e-06 AD=9.025e-13 AS=1.455e-12
+ PD=1.6e-06 PS=4e-06 NRD=0.217949 NRS=0.217949
mX4_M23 X4_10 X4_X VDD VDD MODP L=3.5e-07 W=1.6e-06 AD=1.335e-12 AS=9.025e-13
+ PD=3.85e-06 PS=1.6e-06 NRD=0.217949 NRS=0.217949
mX4_M24 VDD X4_10 1 VDD MODP L=3.5e-07 W=4.8e-06 AD=2.4e-12 AS=3.765e-12
+ PD=1e-06 PS=6.5e-06 NRD=0.0885417 NRS=0.0885417
mX4_M25 X4_QN X4_9 VDD VDD MODP L=3.5e-07 W=4.8e-06 AD=3.765e-12 AS=2.4e-12

+ PD=6.5e-06 PS=1e-06 NRD=0.0885417 NRS=0.0885417
mX5_M0 VSS CLOCK X5_2 VSS MODN L=3.5e-07 W=5e-07 AD=5.375e-13 AS=5.9e-13
+ PD=1.97222e-06 PS=2.7e-06 NRD=0.85 NRS=0.85
mX5_M1 X5_3 X5_2 VSS VSS MODN L=3.5e-07 W=4e-07 AD=5.7e-13 AS=4.3e-13
+ PD=2.8e-06 PS=1.57778e-06 NRD=1.0625 NRS=1.0625
mX5_M2 X5_15 X5_2 VSS VSS MODN L=3.5e-07 W=1e-06 AD=2.25e-13 AS=7.45e-13
+ PD=4.5e-07 PS=2.7e-06 NRD=0.425 NRS=0.425
mX5_M3 X5_5 3 X5_15 VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=2.25e-13 PD=1e-06
+ PS=4.5e-07 NRD=0.425 NRS=0.425
mX5_M4 X5_6 X5_3 X5_5 VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13 PD=1e-06
+ PS=1e-06 NRD=0.425 NRS=0.425
mX5_M5 VSS X5_7 X5_6 VSS MODN L=3.5e-07 W=1e-06 AD=5.125e-13 AS=5e-13
+ PD=1.025e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX5_M6 X5_7 X5_5 VSS VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5.125e-13 PD=1e-06
+ PS=1.025e-06 NRD=0.425 NRS=0.425
mX5_M7 X5_X X5_3 X5_7 VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13 PD=1e-06
+ PS=1e-06 NRD=0.425 NRS=0.425
mX5_M8 X5_9 X5_2 X5_X VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13 PD=1e-06
+ PS=1e-06 NRD=0.425 NRS=0.425
mX5_M9 VSS X5_10 X5_9 VSS MODN L=3.5e-07 W=1e-06 AD=5.875e-13 AS=5e-13
+ PD=1.175e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX5_M10 X5_10 X5_X VSS VSS MODN L=3.5e-07 W=1e-06 AD=1.325e-12 AS=5.875e-13
+ PD=4.25e-06 PS=1.175e-06 NRD=0.425 NRS=0.425
mX5_M11 VSS X5_10 QOUT VSS MODN L=3.5e-07 W=2.975e-06 AD=1.4875e-12
+ AS=2.0125e-12 PD=1e-06 PS=4.675e-06 NRD=0.142857 NRS=0.142857
mX5_M12 X5_QN X5_9 VSS VSS MODN L=3.5e-07 W=2.975e-06 AD=2.0125e-12
+ AS=1.4875e-12 PD=4.675e-06 PS=1e-06 NRD=0.142857 NRS=0.142857
mX5_M13 VDD CLOCK X5_2 VDD MODP L=3.5e-07 W=1e-06 AD=1.16944e-12 AS=7.45e-13
+ PD=2.86111e-06 PS=2.7e-06 NRD=0.425 NRS=0.425
mX5_M14 VDD X5_2 X5_3 VDD MODP L=3.5e-07 W=8e-07 AD=9.35556e-13 AS=7.55e-13
+ PD=2.28889e-06 PS=3.1e-06 NRD=0.53125 NRS=0.53125
mX5_M15 X5_5 X5_2 X5_6 VDD MODP L=3.5e-07 W=1e-06 AD=5e-13 AS=1.355e-12
+ PD=1e-06 PS=4.1e-06 NRD=0.425 NRS=0.425
mX5_M16 X5_16 3 X5_5 VDD MODP L=3.5e-07 W=1.6e-06 AD=3.6e-13 AS=8e-13
+ PD=4.5e-07 PS=1.6e-06 NRD=0.265625 NRS=0.265625
mX5_M17 VDD X5_3 X5_16 VDD MODP L=3.5e-07 W=1.6e-06 AD=1.31625e-12 AS=3.6e-13
+ PD=3.3e-06 PS=4.5e-07 NRD=0.265625 NRS=0.265625
mX5_M18 VDD X5_7 X5_6 VDD MODP L=3.5e-07 W=1.6e-06 AD=9.1125e-13 AS=1.25e-12
+ PD=1.725e-06 PS=3.7e-06 NRD=0.217949 NRS=0.217949

```
mX5_M19 X5_7 X5_5 VDD VDD MODP L=3.5e-07 W=1.6e-06 AD=1.25e-12 AS=9.1125e-13
+ PD=3.7e-06 PS=1.725e-06 NRD=0.217949 NRS=0.217949
mX5_M20 X5_X X5_2 X5_7 VDD MODP L=3.5e-07 W=1e-06 AD=5e-13 AS=7.45e-13
+ PD=1e-06 PS=2.7e-06 NRD=0.425 NRS=0.425
mX5_M21 X5_9 X5_3 X5_X VDD MODP L=3.5e-07 W=1e-06 AD=8.5e-13 AS=5e-13
+ PD=2.7e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX5_M22 VDD X5_10 X5_9 VDD MODP L=3.5e-07 W=1.6e-06 AD=9.025e-13 AS=1.455e-12
+ PD=1.6e-06 PS=4e-06 NRD=0.217949 NRS=0.217949
mX5_M23 X5_10 X5_X VDD VDD MODP L=3.5e-07 W=1.6e-06 AD=1.335e-12 AS=9.025e-13
+ PD=3.85e-06 PS=1.6e-06 NRD=0.217949 NRS=0.217949
mX5_M24 VDD X5_10 QOUT VDD MODP L=3.5e-07 W=4.8e-06 AD=2.4e-12 AS=3.765e-12
+ PD=1e-06 PS=6.5e-06 NRD=0.0885417 NRS=0.0885417
mX5_M25 X5_QN X5_9 VDD VDD MODP L=3.5e-07 W=4.8e-06 AD=3.765e-12 AS=2.4e-12
+ PD=6.5e-06 PS=1e-06 NRD=0.0885417 NRS=0.0885417
c_11 1 0 0.565776f
c_27 QOUT 0 0.325598f
c_39 3 0 0.928346f
c_58 CLOCK 0 0.966035f
c_84 VSS 0 6.00091f
c_93 DIN 0 0.423947f
c_118 VDD 0 104.076f
c_131 X4_2 0 2.93697f
c_142 X4_3 0 1.30519f
c_152 X4_5 0 0.483562f
c_162 X4_6 0 0.127323f
c_173 X4_7 0 0.333807f
c_185 X4_X 0 0.410331f
c_196 X4_9 0 1.31675f
c_205 X4_10 0 0.605375f
c_214 X4_QN 0 0.166836f
c_228 X5_2 0 2.89815f
c_240 X5_3 0 1.29727f
c_251 X5_5 0 0.483562f
c_261 X5_6 0 0.127323f
c_272 X5_7 0 0.333807f
c_283 X5_X 0 0.410331f
c_293 X5_9 0 1.33748f
c_301 X5_10 0 0.61737f
c_307 X5_QN 0 0.218863f
```

```

*
.include "dlclock.pex.netlist.DLCLOCK.pxi"
*
*** Parametros
.Param tensao=3v
.Param F=0.2G T='1/F'

*** Tensões estabelecidas
Vdd VDD VSS DC tensao
.CONNECT VSS 0
Vclock CLOCK 0 PULSE(0 3.0 0 '0.1*T' '0.1*T' '0.4*T' T)
*** Conexão do circuito
.CONNECT DIN VDD

*** Tempo de propagacão de subida e descida
.meas tran Pout trig v(QOUT) val=tensao/2 rise=4 targ v(QOUT) val=tensao/2 rise=5
.meas tran PClock trig v(CLOCK) val=tensao/2 rise=4 targ v(CLOCK) val=tensao/2 rise=5
.meas tran clockCir PARAM='Pout/Pclock'

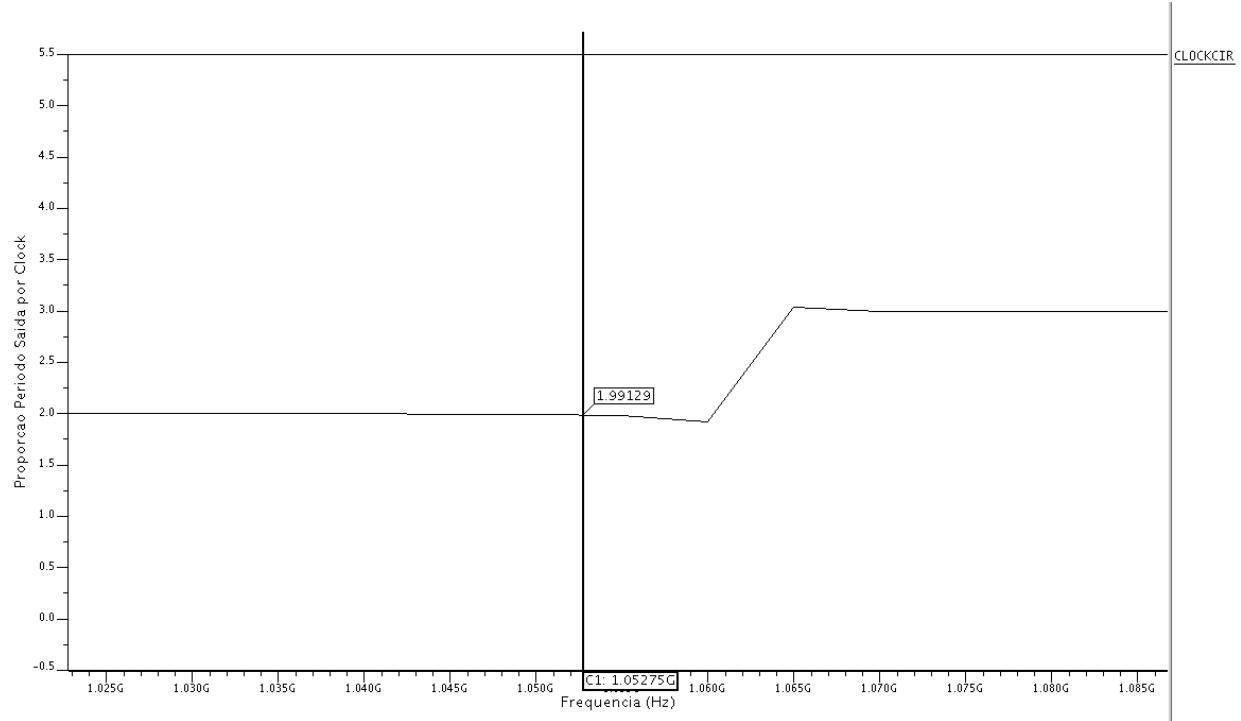
*** Escursionando frequencia em busca da maxima
*.tran 0.1p '20*T' 0 5p sweep F INCR 0.1G 0.5G 2.5G
.tran 0.1p '20*T' 0 5p sweep F INCR 0.005G 0.5G 1.4G
*****
.probe tran ALL
.include Model135_Eldo
.end

```

Questão 10: Extraia agora com a opção R+C+CC. Simule o circuito com parâmetros típicos e determine sua máxima velocidade. Utilize as mesmas condições do exercício 7.

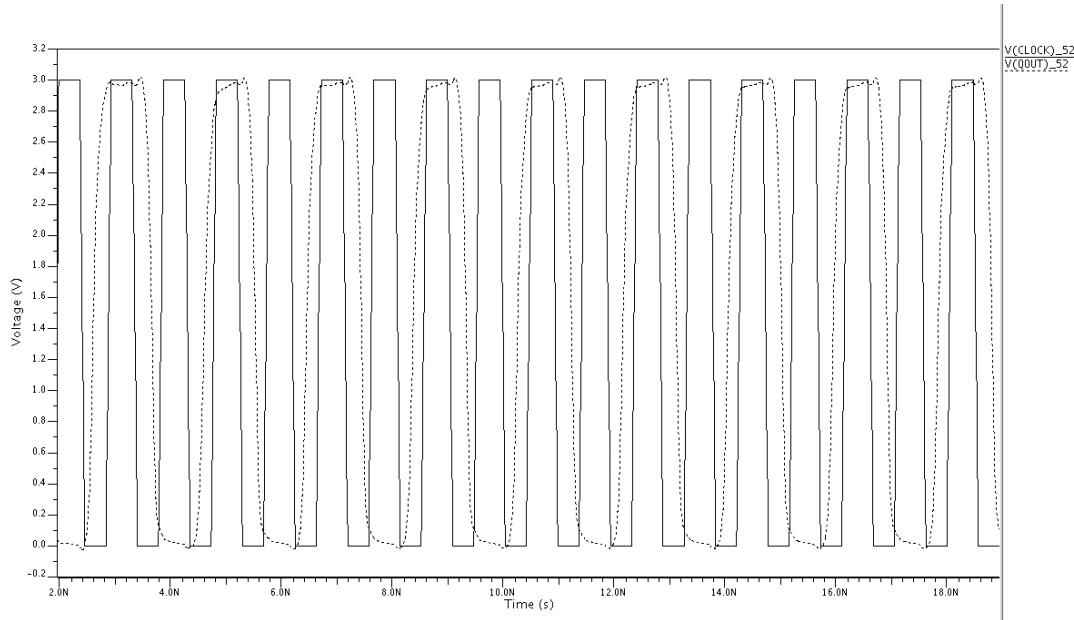
Neste item, através da extração R+C+CC, temos a análise do circuito com células *flip-flop* e ***NAND***, realizamos o estudo para verificar o comportamento do circuito mediante excursionamento de frequência de operação e a proporção do período do *clock* com a saída vista na figura 12 e sinais tensões do *clock* e saída para as frequências marcadas na figura 12 (disposto na figura 13).

Figura 12 – Proporção entre o ciclo de *clock* e período de saída do circuito para excursamento de frequência, marcado em 1,052GHz



Fonte: Pelos próprios autores

Figura 13 – Sinais de tensão de saída e *clock* para frequência de 1,052GHz



Fonte: Pelos próprios autores

Código completo da simulação:

*** Configuracao Simulacao

```

.option measDGT=8
.options ingold=1
*.option lis
.option hmax=0.01n

.include "dlclock.pex.netlist.pex"
.subckt DLCLK N_QOUT_X5_M24_s N_CLOCK_X5_M0_g N_DIN_X4_M3_g N_VDD_M3_d N_VSS_M0_
mM0 8 N_1_M0_g N_VSS_M0_s N_VSS_X4_M0_b MODN L=3.5e-07 W=4e-06 AD=9.7875e-13
+ AS=2.755e-12 PD=4.5e-07 PS=5.35e-06 NRD=0.0977011 NRS=0.0977011
mM1 N_3_M1_d N_QOUT_M1_g 8 N_VSS_X4_M0_b MODN L=3.5e-07 W=4e-06 AD=2.6825e-12
+ AS=9.7875e-13 PD=5.35e-06 PS=4.5e-07 NRD=0.0977011 NRS=0.0977011
mM2 N_3_M2_d N_1_M2_g N_VDD_M2_s N_VDD_X4_M13_b MODP L=3.5e-07 W=3.2e-06
+ AD=1.62625e-12 AS=2.52875e-12 PD=1.1e-06 PS=4.55e-06 NRD=0.119718 NRS=0.119718
mM3 N_VDD_M3_d N_QOUT_M3_g N_3_M2_d N_VDD_X4_M13_b MODP L=3.5e-07 W=3.2e-06
+ AD=2.89375e-12 AS=1.62625e-12 PD=5.25e-06 PS=1.1e-06 NRD=0.119718 NRS=0.119718
mX4_M0 N_VSS_X4_M0_d N_CLOCK_X4_M0_g N_X4_2_X4_M0_s N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=5e-07 AD=5.375e-13 AS=5.9e-13 PD=1.97222e-06 PS=2.7e-06 NRD=0.85
+ NRS=0.85
mX4_M1 N_X4_3_X4_M1_d N_X4_2_X4_M1_g N_VSS_X4_M0_d N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=4e-07 AD=5.7e-13 AS=4.3e-13 PD=2.8e-06 PS=1.57778e-06 NRD=1.0625
+ NRS=1.0625
mX4_M2 X4_15 N_X4_2_X4_M2_g N_VSS_X4_M2_s N_VSS_X4_M0_b MODN L=3.5e-07 W=1e-06
+ AD=2.25e-13 AS=7.45e-13 PD=4.5e-07 PS=2.7e-06 NRD=0.425 NRS=0.425
mX4_M3 N_X4_5_X4_M3_d N_DIN_X4_M3_g X4_15 N_VSS_X4_M0_b MODN L=3.5e-07 W=1e-06
+ AD=5e-13 AS=2.25e-13 PD=1e-06 PS=4.5e-07 NRD=0.425 NRS=0.425
mX4_M4 N_X4_6_X4_M4_d N_X4_3_X4_M4_g N_X4_5_X4_M3_d N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13 PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX4_M5 N_VSS_X4_M5_d N_X4_7_X4_M5_g N_X4_6_X4_M4_d N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5.125e-13 AS=5e-13 PD=1.025e-06 PS=1e-06 NRD=0.425
+ NRS=0.425
mX4_M6 N_X4_7_X4_M6_d N_X4_5_X4_M6_g N_VSS_X4_M5_d N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5e-13 AS=5.125e-13 PD=1e-06 PS=1.025e-06 NRD=0.425
+ NRS=0.425
mX4_M7 N_X4_X_X4_M7_d N_X4_3_X4_M7_g N_X4_7_X4_M6_d N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13 PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX4_M8 N_X4_9_X4_M8_d N_X4_2_X4_M8_g N_X4_X_X4_M7_d N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13 PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX4_M9 N_VSS_X4_M9_d N_X4_10_X4_M9_g N_X4_9_X4_M8_d N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5.875e-13 AS=5e-13 PD=1.175e-06 PS=1e-06 NRD=0.425

```

```

+ NRS=0.425
mX4_M10 N_X4_10_X4_M10_d N_X4_X_X4_M10_g N_VSS_X4_M9_d N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=1.325e-12 AS=5.875e-13 PD=4.25e-06 PS=1.175e-06 NRD=0.425
+ NRS=0.425
mX4_M11 N_VSS_X4_M11_d N_X4_10_X4_M11_g N_1_X4_M11_s N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=2.975e-06 AD=1.4875e-12 AS=2.0125e-12 PD=1e-06 PS=4.675e-06
+ NRD=0.142857 NRS=0.142857
mX4_M12 N_X4_QN_X4_M12_d N_X4_9_X4_M12_g N_VSS_X4_M11_d N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=2.975e-06 AD=2.0125e-12 AS=1.4875e-12 PD=4.675e-06 PS=1e-06
+ NRD=0.142857 NRS=0.142857
mX4_M13 N_VDD_X4_M13_d N_CLOCK_X4_M13_g N_X4_2_X4_M13_s N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=1e-06 AD=1.16944e-12 AS=7.45e-13 PD=2.86111e-06 PS=2.7e-06
+ NRD=0.425 NRS=0.425
mX4_M14 N_VDD_X4_M13_d N_X4_2_X4_M14_g N_X4_3_X4_M14_s N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=8e-07 AD=9.35556e-13 AS=7.55e-13 PD=2.28889e-06 PS=3.1e-06
+ NRD=0.53125 NRS=0.53125
mX4_M15 N_X4_5_X4_M15_d N_X4_2_X4_M15_g N_X4_6_X4_M15_s N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=1e-06 AD=5e-13 AS=1.355e-12 PD=1e-06 PS=4.1e-06 NRD=0.425 NRS=0.425
mX4_M16 X4_16 N_DIN_X4_M16_g N_X4_5_X4_M15_d N_VDD_X4_M13_b MODP L=3.5e-07
+ W=1.6e-06 AD=3.6e-13 AS=8e-13 PD=4.5e-07 PS=1.6e-06 NRD=0.265625 NRS=0.265625
mX4_M17 N_VDD_X4_M17_d N_X4_3_X4_M17_g X4_16 N_VDD_X4_M13_b MODP L=3.5e-07
+ W=1.6e-06 AD=1.31625e-12 AS=3.6e-13 PD=3.3e-06 PS=4.5e-07 NRD=0.265625
+ NRS=0.265625
mX4_M18 N_VDD_X4_M18_d N_X4_7_X4_M18_g N_X4_6_X4_M18_s N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=1.6e-06 AD=9.1125e-13 AS=1.25e-12 PD=1.725e-06 PS=3.7e-06
+ NRD=0.217949 NRS=0.217949
mX4_M19 N_X4_7_X4_M19_d N_X4_5_X4_M19_g N_VDD_X4_M18_d N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=1.6e-06 AD=1.25e-12 AS=9.1125e-13 PD=3.7e-06 PS=1.725e-06
+ NRD=0.217949 NRS=0.217949
mX4_M20 N_X4_X_X4_M20_d N_X4_2_X4_M20_g N_X4_7_X4_M20_s N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=1e-06 AD=5e-13 AS=7.45e-13 PD=1e-06 PS=2.7e-06 NRD=0.425 NRS=0.425
mX4_M21 N_X4_9_X4_M21_d N_X4_3_X4_M21_g N_X4_X_X4_M20_d N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=1e-06 AD=8.5e-13 AS=5e-13 PD=2.7e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX4_M22 N_VDD_X4_M22_d N_X4_10_X4_M22_g N_X4_9_X4_M22_s N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=1.6e-06 AD=9.025e-13 AS=1.455e-12 PD=1.6e-06 PS=4e-06 NRD=0.217949
+ NRS=0.217949
mX4_M23 N_X4_10_X4_M23_d N_X4_X_X4_M23_g N_VDD_X4_M22_d N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=1.6e-06 AD=1.335e-12 AS=9.025e-13 PD=3.85e-06 PS=1.6e-06
+ NRD=0.217949 NRS=0.217949

```

```

mX4_M24 N_VDD_X4_M24_d N_X4_10_X4_M24_g N_1_X4_M24_s N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=4.8e-06 AD=2.4e-12 AS=3.765e-12 PD=1e-06 PS=6.5e-06 NRD=0.0885417
+ NRS=0.0885417

mX4_M25 N_X4_QN_X4_M25_d N_X4_9_X4_M25_g N_VDD_X4_M24_d N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=4.8e-06 AD=3.765e-12 AS=2.4e-12 PD=6.5e-06 PS=1e-06 NRD=0.0885417
+ NRS=0.0885417

mX5_M0 N_VSS_X5_M0_d N_CLOCK_X5_M0_g N_X5_2_X5_M0_s N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=5e-07 AD=5.375e-13 AS=5.9e-13 PD=1.97222e-06 PS=2.7e-06 NRD=0.85
+ NRS=0.85

mX5_M1 N_X5_3_X5_M1_d N_X5_2_X5_M1_g N_VSS_X5_M0_d N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=4e-07 AD=5.7e-13 AS=4.3e-13 PD=2.8e-06 PS=1.57778e-06 NRD=1.0625
+ NRS=1.0625

mX5_M2 X5_15 N_X5_2_X5_M2_g N_VSS_X5_M2_s N_VSS_X4_M0_b MODN L=3.5e-07 W=1e-06
+ AD=2.25e-13 AS=7.45e-13 PD=4.5e-07 PS=2.7e-06 NRD=0.425 NRS=0.425

mX5_M3 N_X5_5_X5_M3_d N_3_X5_M3_g X5_15 N_VSS_X4_M0_b MODN L=3.5e-07 W=1e-06
+ AD=5e-13 AS=2.25e-13 PD=1e-06 PS=4.5e-07 NRD=0.425 NRS=0.425

mX5_M4 N_X5_6_X5_M4_d N_X5_3_X5_M4_g N_X5_5_X5_M3_d N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13 PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425

mX5_M5 N_VSS_X5_M5_d N_X5_7_X5_M5_g N_X5_6_X5_M4_d N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5.125e-13 AS=5e-13 PD=1.025e-06 PS=1e-06 NRD=0.425
+ NRS=0.425

mX5_M6 N_X5_7_X5_M6_d N_X5_5_X5_M6_g N_VSS_X5_M5_d N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5e-13 AS=5.125e-13 PD=1e-06 PS=1.025e-06 NRD=0.425
+ NRS=0.425

mX5_M7 N_X5_X_X5_M7_d N_X5_3_X5_M7_g N_X5_7_X5_M6_d N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13 PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425

mX5_M8 N_X5_9_X5_M8_d N_X5_2_X5_M8_g N_X5_X_X5_M7_d N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13 PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425

mX5_M9 N_VSS_X5_M9_d N_X5_10_X5_M9_g N_X5_9_X5_M8_d N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5.875e-13 AS=5e-13 PD=1.175e-06 PS=1e-06 NRD=0.425
+ NRS=0.425

mX5_M10 N_X5_10_X5_M10_d N_X5_X_X5_M10_g N_VSS_X5_M9_d N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=1.325e-12 AS=5.875e-13 PD=4.25e-06 PS=1.175e-06 NRD=0.425
+ NRS=0.425

mX5_M11 N_VSS_X5_M11_d N_X5_10_X5_M11_g N_QOUT_X5_M11_s N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=2.975e-06 AD=1.4875e-12 AS=2.0125e-12 PD=1e-06 PS=4.675e-06
+ NRD=0.142857 NRS=0.142857

mX5_M12 N_X5_QN_X5_M12_d N_X5_9_X5_M12_g N_VSS_X5_M11_d N_VSS_X4_M0_b MODN
+ L=3.5e-07 W=2.975e-06 AD=2.0125e-12 AS=1.4875e-12 PD=4.675e-06 PS=1e-06

```

```

+ NRD=0.142857 NRS=0.142857
mX5_M13 N_VDD_X5_M13_d N_CLOCK_X5_M13_g N_X5_2_X5_M13_s N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=1e-06 AD=1.16944e-12 AS=7.45e-13 PD=2.86111e-06 PS=2.7e-06
+ NRD=0.425 NRS=0.425
mX5_M14 N_VDD_X5_M13_d N_X5_2_X5_M14_g N_X5_3_X5_M14_s N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=8e-07 AD=9.35556e-13 AS=7.55e-13 PD=2.28889e-06 PS=3.1e-06
+ NRD=0.53125 NRS=0.53125
mX5_M15 N_X5_5_X5_M15_d N_X5_2_X5_M15_g N_X5_6_X5_M15_s N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=1e-06 AD=5e-13 AS=1.355e-12 PD=1e-06 PS=4.1e-06 NRD=0.425 NRS=0.425
mX5_M16 X5_16 N_3_X5_M16_g N_X5_5_X5_M15_d N_VDD_X4_M13_b MODP L=3.5e-07
+ W=1.6e-06 AD=3.6e-13 AS=8e-13 PD=4.5e-07 PS=1.6e-06 NRD=0.265625 NRS=0.265625
mX5_M17 N_VDD_X5_M17_d N_X5_3_X5_M17_g X5_16 N_VDD_X4_M13_b MODP L=3.5e-07
+ W=1.6e-06 AD=1.31625e-12 AS=3.6e-13 PD=3.3e-06 PS=4.5e-07 NRD=0.265625
+ NRS=0.265625
mX5_M18 N_VDD_X5_M18_d N_X5_7_X5_M18_g N_X5_6_X5_M18_s N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=1.6e-06 AD=9.1125e-13 AS=1.25e-12 PD=1.725e-06 PS=3.7e-06
+ NRD=0.217949 NRS=0.217949
mX5_M19 N_X5_7_X5_M19_d N_X5_5_X5_M19_g N_VDD_X5_M18_d N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=1.6e-06 AD=1.25e-12 AS=9.1125e-13 PD=3.7e-06 PS=1.725e-06
+ NRD=0.217949 NRS=0.217949
mX5_M20 N_X5_X_X5_M20_d N_X5_2_X5_M20_g N_X5_7_X5_M20_s N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=1e-06 AD=5e-13 AS=7.45e-13 PD=1e-06 PS=2.7e-06 NRD=0.425 NRS=0.425
mX5_M21 N_X5_9_X5_M21_d N_X5_3_X5_M21_g N_X5_X_X5_M20_d N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=1e-06 AD=8.5e-13 AS=5e-13 PD=2.7e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX5_M22 N_VDD_X5_M22_d N_X5_10_X5_M22_g N_X5_9_X5_M22_s N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=1.6e-06 AD=9.025e-13 AS=1.455e-12 PD=1.6e-06 PS=4e-06 NRD=0.217949
+ NRS=0.217949
mX5_M23 N_X5_10_X5_M23_d N_X5_X_X5_M23_g N_VDD_X5_M22_d N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=1.6e-06 AD=1.335e-12 AS=9.025e-13 PD=3.85e-06 PS=1.6e-06
+ NRD=0.217949 NRS=0.217949
mX5_M24 N_VDD_X5_M24_d N_X5_10_X5_M24_g N_QOUT_X5_M24_s N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=4.8e-06 AD=2.4e-12 AS=3.765e-12 PD=1e-06 PS=6.5e-06 NRD=0.0885417
+ NRS=0.0885417
mX5_M25 N_X5_QN_X5_M25_d N_X5_9_X5_M25_g N_VDD_X5_M24_d N_VDD_X4_M13_b MODP
+ L=3.5e-07 W=4.8e-06 AD=3.765e-12 AS=2.4e-12 PD=6.5e-06 PS=1e-06 NRD=0.0885417
+ NRS=0.0885417
*
.incluie "dlclock.pex.netlist.DLCLOCK.pkl"
*
```

```

.ends DLCLOCK
*
*** Conectando circuito
Xcir QOUT CLOCK DIN VDD VSS DLCLOCK

*** Parametros
.Param tensao=3v
.Param F=0.2G T='1/F'

*** Tensões estabelecidas
Vdd VDD VSS DC tensao
.CONNECT VSS 0
Vclock CLOCK 0 PULSE(0 3.0 0 '0.1*T' '0.1*T' '0.4*T' T)

*** Conexão do circuito
.CONNECT DIN VDD

*** Tempo de período
.meas tran Pout trig v(QOUT) val=tensao/2 rise=4
+ targ v(QOUT) val=tensao/2 rise=5
.meas tran PClock trig v(CLOCK) val=tensao/2 rise=4
+ targ v(CLOCK) val=tensao/2 rise=5
.meas tran clockCir PARAM='Pout/Pclock'

*** Escursionando frequência em busca da máxima
*.tran 0.1p '20*T' 0 5p sweep F INCR 0.1G 0.5G 2.5G
.tran 0.1p '20*T' 0 5p sweep F INCR 0.005G 0.8G 1.3G
*****
.probe tran ALL
.include Model135_Eldo
.end

```

Questão 11: Monte uma tabela com os resultados obtidos nos exercícios 5, 7, 9 e 10. Compare e comente os resultados.

Como solicitado apresenta-se a tabela 2 com o resultados para máxima frequência de operação.

Com os valores de frequência máxima de operação entre as distintas formas de projetar (manipular) o circuito, verifica-se que o esquemático se aproxima do valor teórico

Tabela 2 – Tabela com frequência máxima conforme extração

Tipo Extração	Frequência Máxima [GHz]
Teórico	1,432
Esquemático	1,460
R+C+CC	1,052
C+CC	0,945

Fonte: Pelos próprios autores

por desprezar os componentes parasitários provenientes das propriedades físicas do projeto, e, esta relação, é verificada também entre a extração C+CC e R+C+CC, pois a segunda apresenta mais componentes parasitários que a anterior.

Questão 12: Determine a área total do circuito que desenhou.

Assim como realizado anteriormente utilizando a ferramente “Report -> Windows” temos que o circuito possui $47,193\mu m$ de largura e $14,2\mu m$ de comprimento como visto na figura 14, logo o circuito possui área de $698,54\mu m^2$ aproximadamente.

Figura 14 – Captura de tela Report - Windows

```

Report Windows
Report Windows

Selectable Layers: 0-4097, 4101, 4104-4106, 4109-4112, 4117-4167, 4190-4224

IC Windows

Name   Snap   Minor   Major   Grid           Offset           Cull   Active   Iconified
      Snap (X, Y)   (X, Y)
*****
IC 0   On     1       10      0.050, 0.050  0.000, 0.000   5     Yes     Window
--- View Extent:  [[-27.743, -8.850], [73.537, 43.950]]
--- Cell Extent:  [[-1.700, 10.450], [47.493, 24.650]]
--- Top Cell:    $mydl/default.group/layout.views/dlclock/dlclock
--- Displayed Cell: $mydl/default.group/layout.views/dlclock/dlclock
--- Visible Layers: 0-4098, 4100-4102, 4104-4106, 4109-4132, 4158-4189, 4193-422

```

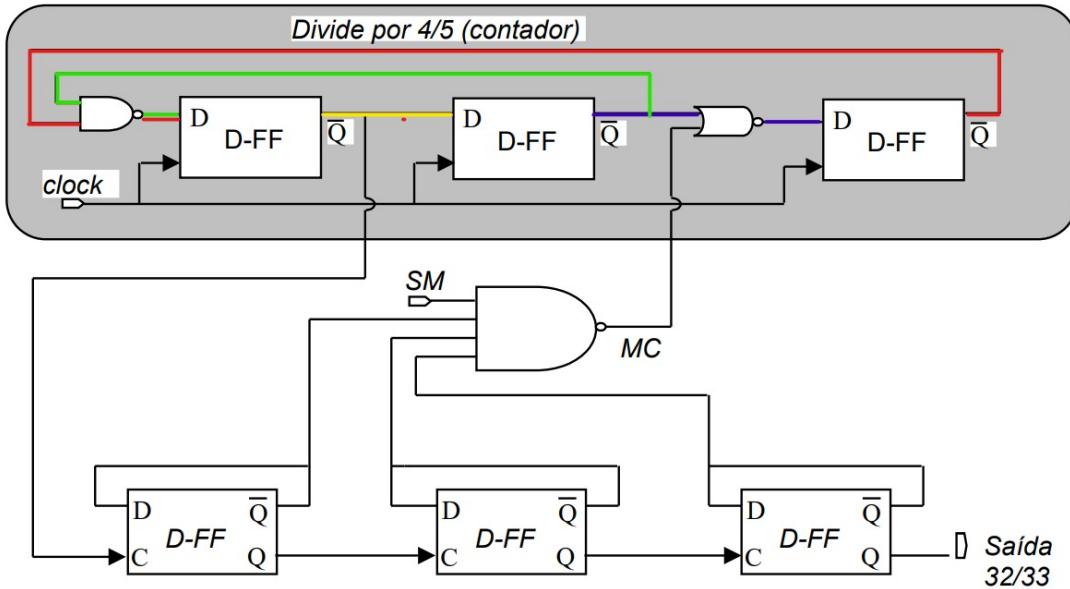
Fonte: Pelos próprios autores

Questão 14: A partir dos dados dos blocos que compõe o divisor 4/5 estime o máximo clock que o circuito pode suportar (considere que são usados na implementação os blocos DF1, 2 NAND23 e NOR23 e utilize o pior caso entre subida e descida das portas). Apresente os cálculos

Assim como realizado no item 5, analisaremos o tempo de atraso de propagação entre os componentes a fim de estudar a máxima frequência de operação do circuito. Neste item faremos uso do circuito presente na figura 15.

Novamente consideraremos o *slope* de 0,05 e o pior caso como sendo de subida. Logo resumiremos os tempos propagação de atraso de subida na tabela 3.

Figura 15 – Divisor 4/5 (contador) parte do circuito Prescaler 32/33



Fonte: Modificado do enunciado

Tabela 3 – Tabela tempo de atraso de propagação de subida para os componentes do circuito contador 4/5

Componente - Pino	Capacitância [pF]	Atraso de Subida [ns]
DF1 - D	0,001	0,66
DF1 - D	0,320	2,29
NOR23 - A,B	0,003	0,07
NOR23 - A,B	0,960	1,60
NAND23 - A	0,003	0,04
NAND23 - A	0,960	1,67
NAND23 - B	0,003	0,08
NAND23 - B	0,960	1,70

Fonte: Pelos próprios autores a partir de ([CORPORATION, 2005](#))

Com o caminho selecionado calculamos a aproximação linear considerando a capacidade de saída para seleção correta de tempo de atraso de propagação de subida para cada trecho. Em que os trechos *flip-flop1* (DF1) é conectado a DF2 (caminho Amarelo), DF2 conectado a DF1 (caminho Verde), DF3 conectado a DF1 (caminho Vermelho), e, por fim, o DF2 conectado ao DF3 (caminho Azul), respectivamente, T_{DF11_DF12} , T_{DF12_DF11} , T_{DF13_DF11} e T_{DF12_DF13} , ressalva-se que entre os *flip-flop* existe portas NOR e NAND que serão consideradas tempos invermediários para cada um dos quatro trechos.

Trecho 1: caminho Amarelo

$$T_{DF11_DF12} = \frac{x - 0,66}{2,29 - 0,66} = \frac{0,005 - 0,001}{0,32 - 0,001} \Rightarrow x = 0,680 \text{ ns}$$

Trecho 2: caminho Verde Este trecho é composto pela conexão *flip-flop* 2 com NAND e este com *flip-flop* 1, logo temos:

$$T_{DF12_DF11} = T_{DF12_NAND23} + T_{NAND23_DF11}$$

$$T_{DF12_NAND23} = \frac{x - 0,66}{2,29 - 0,66} = \frac{0,041 - 0,001}{0,32 - 0,001} \Rightarrow x = 0,864 \text{ ns}$$

$$T_{NAND23_DF11} = \frac{y - 0,08}{1,70 - 0,08} = \frac{0,005 - 0,003}{0,96 - 0,003} \Rightarrow y = 0,083 \text{ ns}$$

$$T_{DF12_DF11} = 0,864 + 0,083 = 0,947 \text{ ns}$$

Trecho 3: caminho Vermelho

Este trecho é composto pela conexão *flip-flop* 3 com NAND e este com *flip-flop* 1, logo temos:

$$T_{DF13_DF11} = T_{DF13_NAND23} + T_{NAND23_DF11}$$

$$T_{DF13_NAND23} = \frac{x - 0,66}{2,29 - 0,66} = \frac{0,020 - 0,001}{0,32 - 0,001} \Rightarrow x = 0,757 \text{ ns}$$

$$T_{NAND23_DF11} = \frac{y - 0,08}{1,70 - 0,08} = \frac{0,005 - 0,003}{0,96 - 0,003} \Rightarrow y = 0,083 \text{ ns}$$

$$T_{DF13_DF11} = 0,757 + 0,083 = 0,840 \text{ ns}$$

Trecho 4: caminho Azul

Este trecho é composto pela conexão *flip-flop* 2 com NOR e este com *flip-flop* 3, logo temos:

$$T_{DF12_DF13} = T_{DF12_NOR23} + T_{NOR23_DF13}$$

$$T_{DF12_NOR23} = \frac{x - 0,66}{2,29 - 0,66} = \frac{0,020 - 0,001}{0,32 - 0,001} \Rightarrow x = 0,762 \text{ ns}$$

$$T_{NOR23_DF13} = \frac{y - 0,08}{1,70 - 0,08} = \frac{0,005 - 0,003}{0,96 - 0,003} \Rightarrow y = 0,073 \text{ ns}$$

$$T_{DF12_DF11} = 0,757 + 0,083 = 0,835 \text{ ns}$$

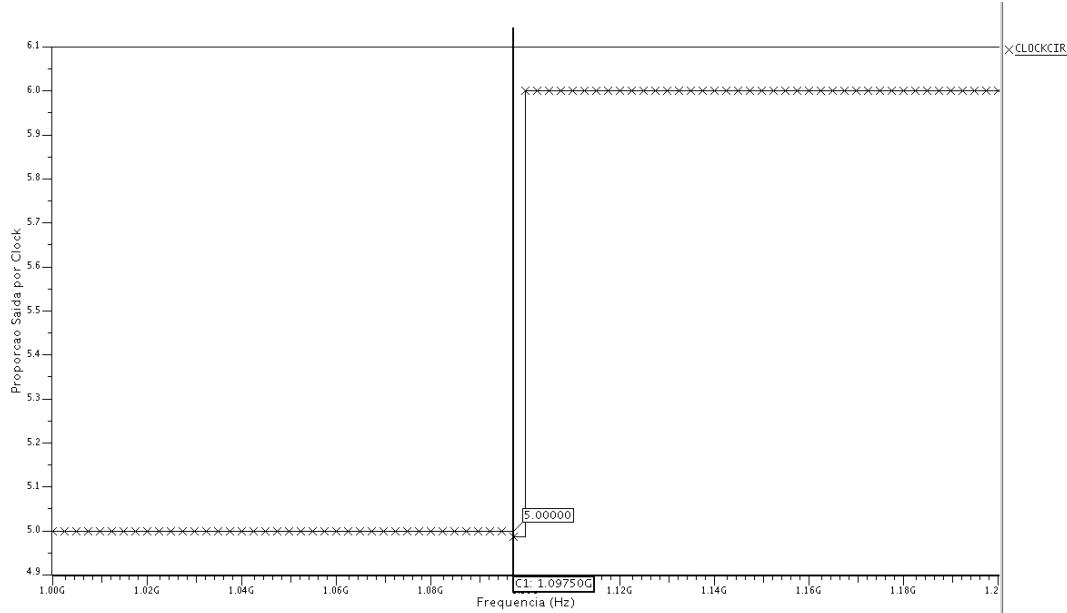
Logo, com a somatória dos atrasos de propagação na subida de todos os componentes para o pior dos casos temos:

$$F = \frac{1}{\max(\text{trecho1}, \text{trecho2}, \text{trecho3}, \text{trecho4})} = \frac{1}{T_{DF12_DF11}} = \frac{1}{0,947} \approx 1,056 \text{ GHz}$$

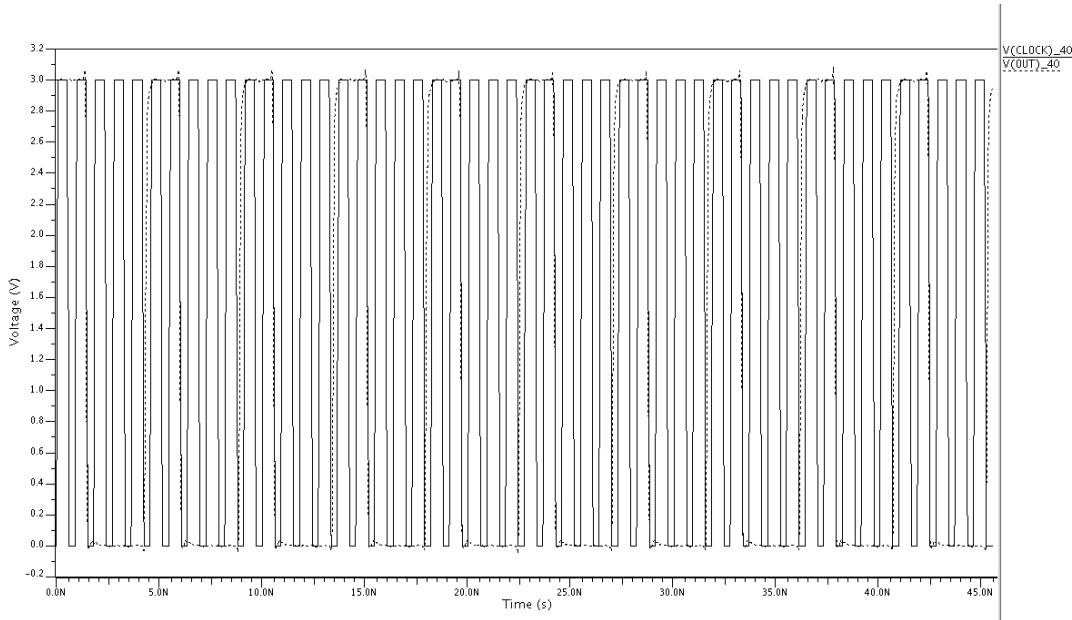
Questão 16: Gere, a partir do esquemático, um arquivo netlist para o ELD. Simule o circuito com parâmetros típicos e determine a máxima velocidade e consumo do circuito (consumo em mW/GHz)

Idem ao item 7, a partir do esquemático, temos a análise do circuito com células *flip-flop*, **NOR** e **NAND**, realizamos o estudo para verificar o comportamento do circuito mediante excursionamento de frequência de operação e a proporção do período do *clock* com a saída vista na figura 16 e sinais tensões do *clock* e saída para as frequências marcadas na figura 16 (disposto na figura 17), e por fim, o consumo e potência dispersada presente na figura 18.

Figura 16 – Proporção entre o ciclo de *clock* e período de saída do circuito para excursionamento de frequência, marcado em 1,098GHz

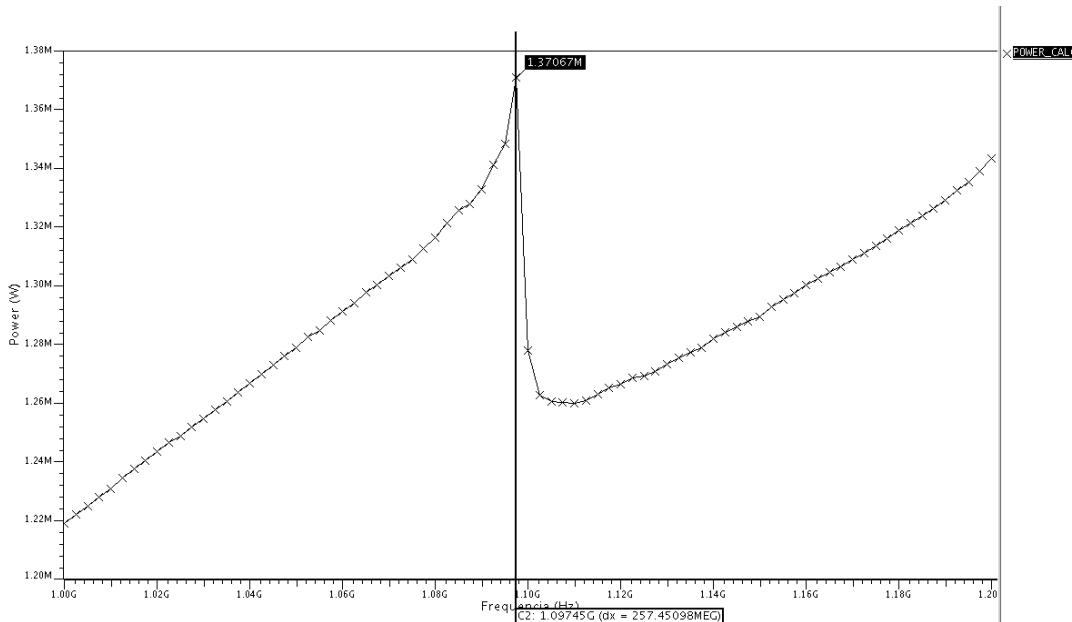


Fonte: Pelos próprios autores

Figura 17 – Sinais de tensão de saída e *clock* para frequência de 1,098GHz

Fonte: Pelos próprios autores

Figura 18 – Consumo de potência dispersada pelo divisor 4/5 para frequência de 1,098GHz



Fonte: Pelos próprios autores

Código completo da simulação:

```
.CONNECT GROUND 0
.global VDD VSS
.subckt INV_B_CORE_PARAM#5 Q A
MN2 Q A VSS VSS MODN w=5.000000e-07 l=3.500000e-07 as=4.250000e-13
```

```

+ ad=4.250000e-13 ps=2.200000e-06 pd=2.200000e-06 nrs=8.500000e-01 nrd=8.500000e-01
    MP2 Q A VDD VDD MODP w=1.000000e-06 l=3.500000e-07 as=8.500000e-13
+ ad=8.500000e-13 ps=2.700000e-06 pd=2.700000e-06 nrs=4.250000e-01 nrd=4.250000e-01
.ends INV_CORE_PARAM#5
.subckt INV_CORE_PARAM#4 Q A
    MN2 Q A VSS VSS MODN w=4.000000e-07 l=3.500000e-07 as=3.400000e-13
+ ad=3.400000e-13 ps=2.100000e-06 pd=2.100000e-06 nrs=1.062500e+00 nrd=1.062500e+00
    MP2 Q A VDD VDD MODP w=8.000000e-07 l=3.500000e-07 as=6.800000e-13
+ ad=6.800000e-13 ps=2.500000e-06 pd=2.500000e-06 nrs=5.312500e-01 nrd=5.312500e-01
.ends INV_CORE_PARAM#4
.subckt TGATE_CORE OUT EN EP IN
    MN1 OUT EN IN VSS MODN w=1.000000e-06 l=3.500000e-07 as=8.500000e-13
+ ad=8.500000e-13 ps=2.700000e-06 pd=2.700000e-06 nrs=4.250000e-01 nrd=4.250000e-01
    MP1 OUT EP IN VDD MODP w=1.000000e-06 l=3.500000e-07 as=8.500000e-13
+ ad=8.500000e-13 ps=2.700000e-06 pd=2.700000e-06 nrs=4.250000e-01 nrd=4.250000e-01
.ends TGATE_CORE
.subckt INV_CORE OUT IN
    MP1 OUT IN VDD VDD MODP w=1.600000e-06 l=3.500000e-07 as=1.360000e-12
+ ad=1.360000e-12 ps=3.300000e-06 pd=3.300000e-06 nrs=2.656250e-01 nrd=2.656250e-01
    MN1 OUT IN VSS VSS MODN w=1.000000e-06 l=3.500000e-07 as=8.500000e-13
+ ad=8.500000e-13 ps=2.700000e-06 pd=2.700000e-06 nrs=4.250000e-01 nrd=4.250000e-01
.ends INV_CORE
.subckt CLINVA_CORE Q A C CN
    MP1 NET10 CN VDD VDD MODP w=1.600000e-06 l=3.500000e-07 as=1.360000e-12
+ ad=1.360000e-12 ps=3.300000e-06 pd=3.300000e-06 nrs=2.656250e-01 nrd=2.656250e-01
    MPO Q A NET10 VDD MODP w=1.600000e-06 l=3.500000e-07 as=1.360000e-12
+ ad=1.360000e-12 ps=3.300000e-06 pd=3.300000e-06 nrs=2.656250e-01 nrd=2.656250e-01
    MN1 NET18 C VSS VSS MODN w=1.000000e-06 l=3.500000e-07 as=8.500000e-13
+ ad=8.500000e-13 ps=2.700000e-06 pd=2.700000e-06 nrs=4.250000e-01 nrd=4.250000e-01
    MNO Q A NET18 VSS MODN w=1.000000e-06 l=3.500000e-07 as=8.500000e-13
+ ad=8.500000e-13 ps=2.700000e-06 pd=2.700000e-06 nrs=4.250000e-01 nrd=4.250000e-01
.ends CLINVA_CORE
.subckt DF1 Q QN C D
    X_I54 CN C INV_CORE_PARAM#5
    X_I53 CI CN INV_CORE_PARAM#4
    X_I55 X CN CI NET55 TGATE_CORE
    X_I56 NET48 CI CN NET47 TGATE_CORE
    X_I57 X CI CN NET63 TGATE_CORE
    X_I58 NET63 NET48 INV_CORE

```

```

        X_I59 Q NET57 INV_CORE
        X_I60 QN NET55 INV_CORE
        X_I61 NET47 NET63 INV_CORE
        X_I62 NET55 NET57 INV_CORE
        X_I63 NET57 X INV_CORE
        X_I52 NET48 D CN CI CLINVA_CORE

.ends DF1

.subckt NOR2_CORE OUT A B

        MP1 OUT A NET17 VDD MODP w=9.600000e-06 l=3.500000e-07 as=8.160000e-12
+ ad=8.160000e-12 ps=1.130000e-05 pd=1.130000e-05 nrs=4.427083e-02 nrd=4.427083e-02
        MP2 NET17 B VDD VDD MODP w=9.600000e-06 l=3.500000e-07 as=8.160000e-12
+ ad=8.160000e-12 ps=1.130000e-05 pd=1.130000e-05 nrs=4.427083e-02 nrd=4.427083e-02
        MN1 OUT B VSS VSS MODN w=3.000000e-06 l=3.500000e-07 as=2.550000e-12
+ ad=2.550000e-12 ps=4.700000e-06 pd=4.700000e-06 nrs=1.416667e-01 nrd=1.416667e-01
        MN2 OUT A VSS VSS MODN w=3.000000e-06 l=3.500000e-07 as=2.550000e-12
+ ad=2.550000e-12 ps=4.700000e-06 pd=4.700000e-06 nrs=1.416667e-01 nrd=1.416667e-01
.ends NOR2_CORE

.subckt NOR23 Q A B

        X_I1 Q B A NOR2_CORE
.ends NOR23

.subckt NAND2_CORE OUT A B

        MP1 OUT A VDD VDD MODP w=4.800000e-06 l=3.500000e-07 as=4.080000e-12
+ ad=4.080000e-12 ps=6.500000e-06 pd=6.500000e-06 nrs=8.854167e-02 nrd=8.854167e-02
        MP2 OUT B VDD VDD MODP w=4.800000e-06 l=3.500000e-07 as=4.080000e-12
+ ad=4.080000e-12 ps=6.500000e-06 pd=6.500000e-06 nrs=8.854167e-02 nrd=8.854167e-02
        MN1 OUT A NET13 VSS MODN w=5.970000e-06 l=3.500000e-07 as=5.074500e-12
+ ad=5.074500e-12 ps=7.670000e-06 pd=7.670000e-06 nrs=7.118928e-02 nrd=7.118928e-02
        MN2 NET13 B VSS VSS MODN w=6.000000e-06 l=3.500000e-07 as=5.100000e-12
+ ad=5.100000e-12 ps=7.700000e-06 pd=7.700000e-06 nrs=7.083333e-02 nrd=7.083333e-02
.ends NAND2_CORE

.subckt NAND23 Q A B

        X_I1 Q A B NAND2_CORE
.ends NAND23

X_DF13 N$210 N$211 CLOCK N$208 DF1
X_DF12 N$209 N$1 CLOCK OUT DF1

```

```

X_NOR231 N$208 N$1 MC NOR23
X_NAND231 N$207 N$1 N$211 NAND23
X_DF11 N$206 OUT CLOCK N$207 DF1

*** Parametros
.Param tensao=3v
.Param F=0.2G P='1/F'

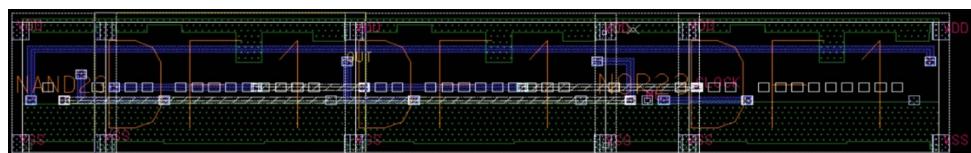
*** Tensoes estabelecidas
Vdd VDD GROUND DC tensao
.CONNECT VSS 0
Vclock CLOCK GROUND PULSE(0 3.0 0 '0.1*P' '0.1*P' '0.49*P' P)
*** Conexao do circuito
.CONNECT MC 0

*** Tempo de propagacao de subida e descida
.meas tran Pout trig v(OUT) val=tensao/2 rise=4 targ v(OUT) val=tensao/2 rise=5
.meas tran PClock trig v(CLOCK) val=tensao/2 rise=4 targ v(CLOCK) val=tensao/2 rise=5
.meas tran clockCir PARAM='Pout/Pclock'
*** Calculo Corrente media
.meas tran cor_avg AVG I(Vdd) FROM '5*P'
*** Calculo Consumo de potencia
.meas tran power_calc PARAM='-cor_avg*tensao'
*** Escursionando frequencia em busca da maxima
*.tran 0 '50*P' 0 '0.1*P' sweep F INCR 0.1G 0.8G 1.5G
.tran 0 '50*P' 0 '0.1*P' sweep F INCR 0.0025G 1G 1.2G
*****
.probe tran ALL
.include Model35_Eldo
.end

```

Questão 17: Gere agora o layout do circuito.

Figura 19 – *Layout* do circuito divisor 4/5 (contador)

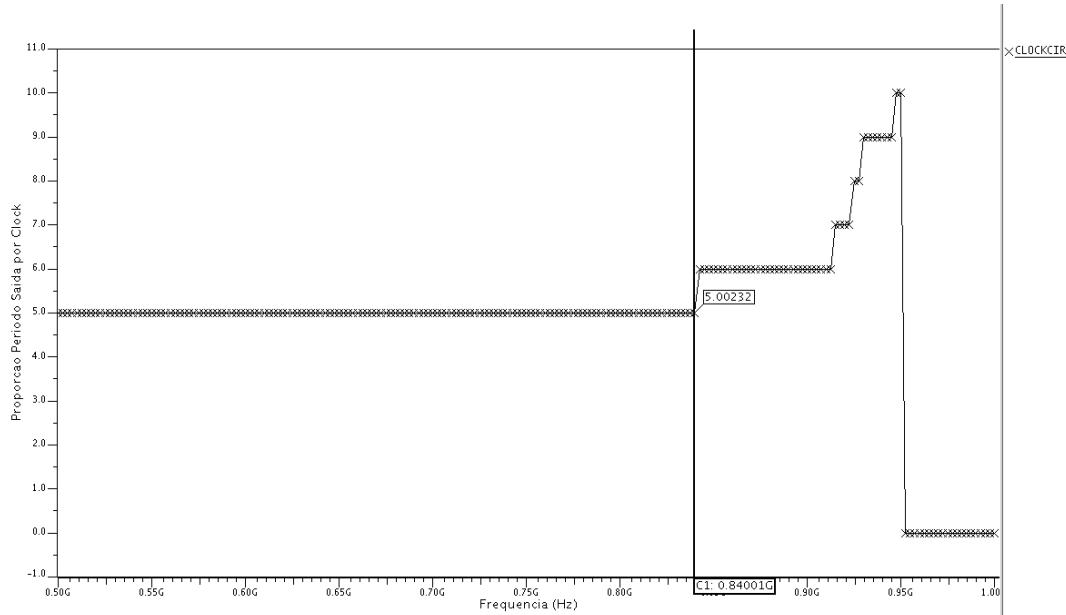


Fonte: Pelos próprios autores

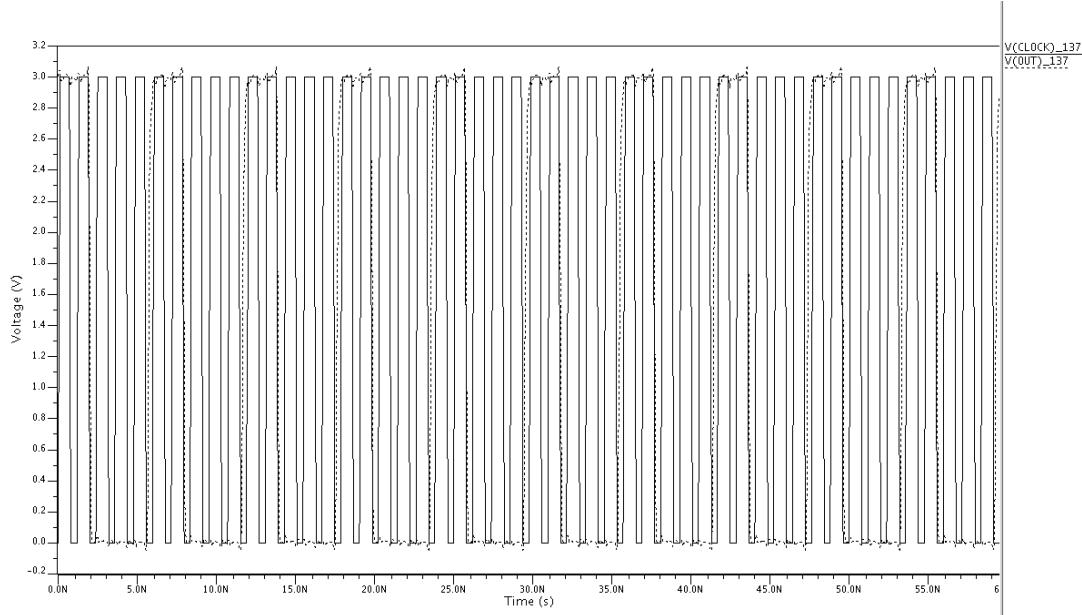
Questão 18: Faça a extração do circuito via o Calibre com a opção C+CC. Simule o circuito com parâmetros típicos e determine a máxima velocidade e consumo do circuito. Considere as mesmas condições do exercício 16

Idem ao item 9, a partir da extração C+CC do *layout*, temos a análise do circuito com células *flip-flop*, **NOR** e **NAND**, realizamos o estudo para verificar o comportamento do circuito mediante excursionamento de frequência de operação e a proporção do período do *clock* com a saída vista na figura 20 e sinais tensões do *clock* e saída para as frequências marcadas na figura 20 (disposto na figura 21), e por fim, o consumo e potência dispersada presente na figura 22.

Figura 20 – Proporção entre o ciclo de *clock* e período de saída do circuito para excursionamento de frequência, marcado em 0,84GHz

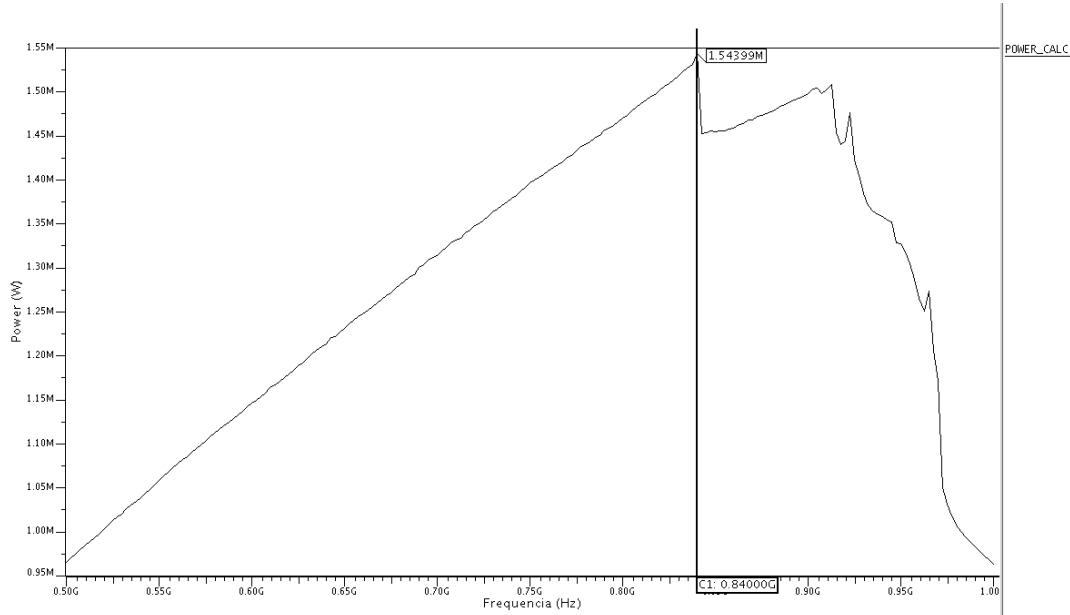


Fonte: Pelos próprios autores

Figura 21 – Sinais de tensão de saída e *clock* para frequência de 0,84GHz

Fonte: Pelos próprios autores

Figura 22 – Consumo de potência dispersada pelo divisor 4/5 para frequência de 0,84GHz



Fonte: Pelos próprios autores

Código completo da simulação:

```
mM0 VSS 6 8 VSS MODN L=3.5e-07 W=3e-06 AD=1.0225e-12 AS=2.69e-12 PD=5.5e-07
+ PS=5.05e-06 NRD=0.126866 NRS=0.126866
mM1 8 6 VSS VSS MODN L=3.5e-07 W=3e-06 AD=2.19946e-12 AS=1.0225e-12
+ PD=1.74401e-06 PS=5.5e-07 NRD=0.126866 NRS=0.126866
```

mM2 3 2 8 VSS MODN L=3.5e-07 W=2.975e-06 AD=1.03175e-12 AS=2.18304e-12
+ PD=5.60393e-07 PS=1.73099e-06 NRD=0.12782 NRS=0.12782

mM3 8 2 3 VSS MODN L=3.5e-07 W=3e-06 AD=2.69e-12 AS=1.0395e-12 PD=5.05e-06
+ PS=5.64607e-07 NRD=0.126866 NRS=0.126866

mM4 5 2 VSS VSS MODN L=3.5e-07 W=3e-06 AD=2.42375e-12 AS=2.93e-12 PD=1.8e-06
+ PS=5.05e-06 NRD=0.126866 NRS=0.126866

mM5 VSS MC 5 VSS MODN L=3.5e-07 W=3e-06 AD=4.4375e-12 AS=2.42375e-12
+ PD=5.95e-06 PS=1.8e-06 NRD=0.126866 NRS=0.126866

mM6 3 6 VDD VDD MODP L=3.5e-07 W=2.4e-06 AD=1.2e-12 AS=2.04e-12 PD=1e-06
+ PS=4.1e-06 NRD=0.177083 NRS=0.177083

mM7 VDD 6 3 VDD MODP L=3.5e-07 W=2.4e-06 AD=1.2e-12 AS=1.2e-12 PD=1e-06
+ PS=1e-06 NRD=0.177083 NRS=0.177083

mM8 3 2 VDD VDD MODP L=3.5e-07 W=2.4e-06 AD=1.2e-12 AS=1.2e-12 PD=1e-06
+ PS=1e-06 NRD=0.177083 NRS=0.177083

mM9 VDD 2 3 VDD MODP L=3.5e-07 W=2.4e-06 AD=2.04e-12 AS=1.2e-12 PD=4.1e-06
+ PS=1e-06 NRD=0.177083 NRS=0.177083

mM10 11 2 VDD VDD MODP L=3.5e-07 W=4.8e-06 AD=1.15875e-12 AS=3.685e-12
+ PD=4.5e-07 PS=6.15e-06 NRD=0.0825243 NRS=0.0825243

mM11 5 MC 11 VDD MODP L=3.5e-07 W=4.8e-06 AD=3.45687e-12 AS=1.15875e-12
+ PD=2.025e-06 PS=4.5e-07 NRD=0.0825243 NRS=0.0825243

mM12 12 MC 5 VDD MODP L=3.5e-07 W=4.8e-06 AD=1.15875e-12 AS=3.45687e-12
+ PD=4.5e-07 PS=2.025e-06 NRD=0.0825243 NRS=0.0825243

mM13 VDD 2 12 VDD MODP L=3.5e-07 W=4.8e-06 AD=3.9625e-12 AS=1.15875e-12
+ PD=6.15e-06 PS=4.5e-07 NRD=0.0825243 NRS=0.0825243

mX14_M0 VSS CLOCK X14_2 VSS MODN L=3.5e-07 W=5e-07 AD=5.375e-13 AS=5.9e-13
+ PD=1.97222e-06 PS=2.7e-06 NRD=0.85 NRS=0.85

mX14_M1 X14_3 X14_2 VSS VSS MODN L=3.5e-07 W=4e-07 AD=5.7e-13 AS=4.3e-13
+ PD=2.8e-06 PS=1.57778e-06 NRD=1.0625 NRS=1.0625

mX14_M2 X14_15 X14_2 VSS VSS MODN L=3.5e-07 W=1e-06 AD=2.25e-13 AS=7.45e-13
+ PD=4.5e-07 PS=2.7e-06 NRD=0.425 NRS=0.425

mX14_M3 X14_5 3 X14_15 VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=2.25e-13
+ PD=1e-06 PS=4.5e-07 NRD=0.425 NRS=0.425

mX14_M4 X14_6 X14_3 X14_5 VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13
+ PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425

mX14_M5 VSS X14_7 X14_6 VSS MODN L=3.5e-07 W=1e-06 AD=5.125e-13 AS=5e-13
+ PD=1.025e-06 PS=1e-06 NRD=0.425 NRS=0.425

mX14_M6 X14_7 X14_5 VSS VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5.125e-13
+ PD=1e-06 PS=1.025e-06 NRD=0.425 NRS=0.425

mX14_M7 X14_X X14_3 X14_7 VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13

+ PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX14_M8 X14_10 X14_2 X14_X VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13
+ PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX14_M9 VSS X14_9 X14_10 VSS MODN L=3.5e-07 W=1e-06 AD=5.875e-13 AS=5e-13
+ PD=1.175e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX14_M10 X14_9 X14_X VSS VSS MODN L=3.5e-07 W=1e-06 AD=1.215e-12 AS=5.875e-13
+ PD=4.1e-06 PS=1.175e-06 NRD=0.425 NRS=0.425
mX14_M11 VSS X14_9 X14_Q VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=7.45e-13
+ PD=1e-06 PS=2.7e-06 NRD=0.425 NRS=0.425
mX14_M12 OUT X14_10 VSS VSS MODN L=3.5e-07 W=1e-06 AD=8.5e-13 AS=5e-13
+ PD=2.7e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX14_M13 VDD CLOCK X14_2 VDD MODP L=3.5e-07 W=1e-06 AD=1.16944e-12 AS=7.45e-13
+ PD=2.86111e-06 PS=2.7e-06 NRD=0.425 NRS=0.425
mX14_M14 VDD X14_2 X14_3 VDD MODP L=3.5e-07 W=8e-07 AD=9.35556e-13 AS=7.55e-13
+ PD=2.28889e-06 PS=3.1e-06 NRD=0.53125 NRS=0.53125
mX14_M15 X14_5 X14_2 X14_6 VDD MODP L=3.5e-07 W=1e-06 AD=5e-13 AS=1.355e-12
+ PD=1e-06 PS=4.1e-06 NRD=0.425 NRS=0.425
mX14_M16 X14_16 3 X14_5 VDD MODP L=3.5e-07 W=1.6e-06 AD=3.6e-13 AS=8e-13
+ PD=4.5e-07 PS=1.6e-06 NRD=0.265625 NRS=0.265625
mX14_M17 VDD X14_3 X14_16 VDD MODP L=3.5e-07 W=1.6e-06 AD=1.31625e-12
+ AS=3.6e-13 PD=3.3e-06 PS=4.5e-07 NRD=0.265625 NRS=0.265625
mX14_M18 VDD X14_7 X14_6 VDD MODP L=3.5e-07 W=1.6e-06 AD=9.1125e-13
+ AS=1.25e-12 PD=1.725e-06 PS=3.7e-06 NRD=0.217949 NRS=0.217949
mX14_M19 X14_7 X14_5 VDD VDD MODP L=3.5e-07 W=1.6e-06 AD=1.25e-12
+ AS=9.1125e-13 PD=3.7e-06 PS=1.725e-06 NRD=0.217949 NRS=0.217949
mX14_M20 X14_X X14_2 X14_7 VDD MODP L=3.5e-07 W=1e-06 AD=5e-13 AS=7.45e-13
+ PD=1e-06 PS=2.7e-06 NRD=0.425 NRS=0.425
mX14_M21 X14_10 X14_3 X14_X VDD MODP L=3.5e-07 W=1e-06 AD=8.5e-13 AS=5e-13
+ PD=2.7e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX14_M22 VDD X14_9 X14_10 VDD MODP L=3.5e-07 W=1.6e-06 AD=9.025e-13
+ AS=1.455e-12 PD=1.6e-06 PS=4e-06 NRD=0.217949 NRS=0.217949
mX14_M23 X14_9 X14_X VDD VDD MODP L=3.5e-07 W=1.6e-06 AD=1.335e-12
+ AS=9.025e-13 PD=3.85e-06 PS=1.6e-06 NRD=0.217949 NRS=0.217949
mX14_M24 VDD X14_9 X14_Q VDD MODP L=3.5e-07 W=1.6e-06 AD=8e-13 AS=1.36e-12
+ PD=1e-06 PS=3.3e-06 NRD=0.265625 NRS=0.265625
mX14_M25 OUT X14_10 VDD VDD MODP L=3.5e-07 W=1.6e-06 AD=1.36e-12 AS=8e-13
+ PD=3.3e-06 PS=1e-06 NRD=0.265625 NRS=0.265625
mX15_M0 VSS CLOCK X15_2 VSS MODN L=3.5e-07 W=5e-07 AD=5.375e-13 AS=5.9e-13
+ PD=1.97222e-06 PS=2.7e-06 NRD=0.85 NRS=0.85

mX15_M1 X15_3 X15_2 VSS VSS MODN L=3.5e-07 W=4e-07 AD=5.7e-13 AS=4.3e-13
+ PD=2.8e-06 PS=1.57778e-06 NRD=1.0625 NRS=1.0625
mX15_M2 X15_15 X15_2 VSS VSS MODN L=3.5e-07 W=1e-06 AD=2.25e-13 AS=7.45e-13
+ PD=4.5e-07 PS=2.7e-06 NRD=0.425 NRS=0.425
mX15_M3 X15_5 OUT X15_15 VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=2.25e-13
+ PD=1e-06 PS=4.5e-07 NRD=0.425 NRS=0.425
mX15_M4 X15_6 X15_3 X15_5 VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13
+ PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX15_M5 VSS X15_7 X15_6 VSS MODN L=3.5e-07 W=1e-06 AD=5.125e-13 AS=5e-13
+ PD=1.025e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX15_M6 X15_7 X15_5 VSS VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5.125e-13
+ PD=1e-06 PS=1.025e-06 NRD=0.425 NRS=0.425
mX15_M7 X15_X X15_3 X15_7 VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13
+ PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX15_M8 X15_10 X15_2 X15_X VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13
+ PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX15_M9 VSS X15_9 X15_10 VSS MODN L=3.5e-07 W=1e-06 AD=5.875e-13 AS=5e-13
+ PD=1.175e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX15_M10 X15_9 X15_X VSS VSS MODN L=3.5e-07 W=1e-06 AD=1.215e-12 AS=5.875e-13
+ PD=4.1e-06 PS=1.175e-06 NRD=0.425 NRS=0.425
mX15_M11 VSS X15_9 X15_Q VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=7.45e-13
+ PD=1e-06 PS=2.7e-06 NRD=0.425 NRS=0.425
mX15_M12 2 X15_10 VSS VSS MODN L=3.5e-07 W=1e-06 AD=8.5e-13 AS=5e-13
+ PD=2.7e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX15_M13 VDD CLOCK X15_2 VDD MODP L=3.5e-07 W=1e-06 AD=1.16944e-12 AS=7.45e-13
+ PD=2.86111e-06 PS=2.7e-06 NRD=0.425 NRS=0.425
mX15_M14 VDD X15_2 X15_3 VDD MODP L=3.5e-07 W=8e-07 AD=9.35556e-13 AS=7.55e-13
+ PD=2.28889e-06 PS=3.1e-06 NRD=0.53125 NRS=0.53125
mX15_M15 X15_5 X15_2 X15_6 VDD MODP L=3.5e-07 W=1e-06 AD=5e-13 AS=1.355e-12
+ PD=1e-06 PS=4.1e-06 NRD=0.425 NRS=0.425
mX15_M16 X15_16 OUT X15_5 VDD MODP L=3.5e-07 W=1.6e-06 AD=3.6e-13 AS=8e-13
+ PD=4.5e-07 PS=1.6e-06 NRD=0.265625 NRS=0.265625
mX15_M17 VDD X15_3 X15_16 VDD MODP L=3.5e-07 W=1.6e-06 AD=1.31625e-12
+ AS=3.6e-13 PD=3.3e-06 PS=4.5e-07 NRD=0.265625 NRS=0.265625
mX15_M18 VDD X15_7 X15_6 VDD MODP L=3.5e-07 W=1.6e-06 AD=9.1125e-13
+ AS=1.25e-12 PD=1.725e-06 PS=3.7e-06 NRD=0.217949 NRS=0.217949
mX15_M19 X15_7 X15_5 VDD VDD MODP L=3.5e-07 W=1.6e-06 AD=1.25e-12
+ AS=9.1125e-13 PD=3.7e-06 PS=1.725e-06 NRD=0.217949 NRS=0.217949
mX15_M20 X15_X X15_2 X15_7 VDD MODP L=3.5e-07 W=1e-06 AD=5e-13 AS=7.45e-13

+ PD=1e-06 PS=2.7e-06 NRD=0.425 NRS=0.425
mX15_M21 X15_10 X15_3 X15_X VDD MODP L=3.5e-07 W=1e-06 AD=8.5e-13 AS=5e-13
+ PD=2.7e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX15_M22 VDD X15_9 X15_10 VDD MODP L=3.5e-07 W=1.6e-06 AD=9.025e-13
+ AS=1.455e-12 PD=1.6e-06 PS=4e-06 NRD=0.217949 NRS=0.217949
mX15_M23 X15_9 X15_X VDD VDD MODP L=3.5e-07 W=1.6e-06 AD=1.335e-12
+ AS=9.025e-13 PD=3.85e-06 PS=1.6e-06 NRD=0.217949 NRS=0.217949
mX15_M24 VDD X15_9 X15_Q VDD MODP L=3.5e-07 W=1.6e-06 AD=8e-13 AS=1.36e-12
+ PD=1e-06 PS=3.3e-06 NRD=0.265625 NRS=0.265625
mX15_M25 2 X15_10 VDD VDD MODP L=3.5e-07 W=1.6e-06 AD=1.36e-12 AS=8e-13
+ PD=3.3e-06 PS=1e-06 NRD=0.265625 NRS=0.265625
mX16_M0 VSS CLOCK X16_2 VSS MODN L=3.5e-07 W=5e-07 AD=5.375e-13 AS=5.9e-13
+ PD=1.97222e-06 PS=2.7e-06 NRD=0.85 NRS=0.85
mX16_M1 X16_3 X16_2 VSS VSS MODN L=3.5e-07 W=4e-07 AD=5.7e-13 AS=4.3e-13
+ PD=2.8e-06 PS=1.57778e-06 NRD=1.0625 NRS=1.0625
mX16_M2 X16_15 X16_2 VSS VSS MODN L=3.5e-07 W=1e-06 AD=2.25e-13 AS=7.45e-13
+ PD=4.5e-07 PS=2.7e-06 NRD=0.425 NRS=0.425
mX16_M3 X16_5 5 X16_15 VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=2.25e-13
+ PD=1e-06 PS=4.5e-07 NRD=0.425 NRS=0.425
mX16_M4 X16_6 X16_3 X16_5 VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13
+ PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX16_M5 VSS X16_7 X16_6 VSS MODN L=3.5e-07 W=1e-06 AD=5.125e-13 AS=5e-13
+ PD=1.025e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX16_M6 X16_7 X16_5 VSS VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5.125e-13
+ PD=1e-06 PS=1.025e-06 NRD=0.425 NRS=0.425
mX16_M7 X16_X X16_3 X16_7 VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13
+ PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX16_M8 X16_10 X16_2 X16_X VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13
+ PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX16_M9 VSS X16_9 X16_10 VSS MODN L=3.5e-07 W=1e-06 AD=5.875e-13 AS=5e-13
+ PD=1.175e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX16_M10 X16_9 X16_X VSS VSS MODN L=3.5e-07 W=1e-06 AD=1.215e-12 AS=5.875e-13
+ PD=4.1e-06 PS=1.175e-06 NRD=0.425 NRS=0.425
mX16_M11 VSS X16_9 X16_Q VSS MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=7.45e-13
+ PD=1e-06 PS=2.7e-06 NRD=0.425 NRS=0.425
mX16_M12 6 X16_10 VSS VSS MODN L=3.5e-07 W=1e-06 AD=8.5e-13 AS=5e-13
+ PD=2.7e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX16_M13 VDD CLOCK X16_2 VDD MODP L=3.5e-07 W=1e-06 AD=1.16944e-12 AS=7.45e-13
+ PD=2.86111e-06 PS=2.7e-06 NRD=0.425 NRS=0.425

mX16_M14 VDD X16_2 X16_3 VDD MODP L=3.5e-07 W=8e-07 AD=9.35556e-13 AS=7.55e-13
+ PD=2.28889e-06 PS=3.1e-06 NRD=0.53125 NRS=0.53125
mX16_M15 X16_5 X16_2 X16_6 VDD MODP L=3.5e-07 W=1e-06 AD=5e-13 AS=1.355e-12
+ PD=1e-06 PS=4.1e-06 NRD=0.425 NRS=0.425
mX16_M16 X16_16 5 X16_5 VDD MODP L=3.5e-07 W=1.6e-06 AD=3.6e-13 AS=8e-13
+ PD=4.5e-07 PS=1.6e-06 NRD=0.265625 NRS=0.265625
mX16_M17 VDD X16_3 X16_16 VDD MODP L=3.5e-07 W=1.6e-06 AD=1.31625e-12
+ AS=3.6e-13 PD=3.3e-06 PS=4.5e-07 NRD=0.265625 NRS=0.265625
mX16_M18 VDD X16_7 X16_6 VDD MODP L=3.5e-07 W=1.6e-06 AD=9.1125e-13
+ AS=1.25e-12 PD=1.725e-06 PS=3.7e-06 NRD=0.217949 NRS=0.217949
mX16_M19 X16_7 X16_5 VDD VDD MODP L=3.5e-07 W=1.6e-06 AD=1.25e-12
+ AS=9.1125e-13 PD=3.7e-06 PS=1.725e-06 NRD=0.217949 NRS=0.217949
mX16_M20 X16_X X16_2 X16_7 VDD MODP L=3.5e-07 W=1e-06 AD=5e-13 AS=7.45e-13
+ PD=1e-06 PS=2.7e-06 NRD=0.425 NRS=0.425
mX16_M21 X16_10 X16_3 X16_X VDD MODP L=3.5e-07 W=1e-06 AD=8.5e-13 AS=5e-13
+ PD=2.7e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX16_M22 VDD X16_9 X16_10 VDD MODP L=3.5e-07 W=1.6e-06 AD=9.025e-13
+ AS=1.455e-12 PD=1.6e-06 PS=4e-06 NRD=0.217949 NRS=0.217949
mX16_M23 X16_9 X16_X VDD VDD MODP L=3.5e-07 W=1.6e-06 AD=1.335e-12
+ AS=9.025e-13 PD=3.85e-06 PS=1.6e-06 NRD=0.217949 NRS=0.217949
mX16_M24 VDD X16_9 X16_Q VDD MODP L=3.5e-07 W=1.6e-06 AD=8e-13 AS=1.36e-12
+ PD=1e-06 PS=3.3e-06 NRD=0.265625 NRS=0.265625
mX16_M25 6 X16_10 VDD VDD MODP L=3.5e-07 W=1.6e-06 AD=1.36e-12 AS=8e-13
+ PD=3.3e-06 PS=1e-06 NRD=0.265625 NRS=0.265625
c_31 CLOCK 0 1.44146f
c_61 2 0 2.3146f
c_73 3 0 0.566562f
c_87 OUT 0 0.593016f
c_100 5 0 0.856052f
c_142 6 0 0.727463f
c_178 VSS 0 10.5137f
c_186 8 0 0.225096f
c_224 VDD 0 165.311f
c_232 MC 0 0.378762f
c_253 X14_2 0 2.87295f
c_266 X14_3 0 1.29562f
c_278 X14_5 0 0.471951f
c_290 X14_6 0 0.121883f
c_303 X14_7 0 0.330461f

```
c_317 X14_X 0 0.398805f
c_328 X14_9 0 0.613873f
c_342 X14_10 0 1.25606f
c_352 X14_Q 0 0.15992f
c_368 X15_2 0 2.87846f
c_381 X15_3 0 1.29562f
c_393 X15_5 0 0.471951f
c_405 X15_6 0 0.121883f
c_418 X15_7 0 0.330461f
c_432 X15_X 0 0.398805f
c_442 X15_9 0 0.613873f
c_454 X15_10 0 1.26564f
c_463 X15_Q 0 0.15992f
c_479 X16_2 0 2.87781f
c_491 X16_3 0 1.3015f
c_502 X16_5 0 0.48294f
c_512 X16_6 0 0.127323f
c_523 X16_7 0 0.333807f
c_535 X16_X 0 0.411526f
c_543 X16_9 0 0.626199f
c_553 X16_10 0 1.28431f
c_560 X16_Q 0 0.165263f
.include "divisorqq.pex.netlist.DIVISORQQ.pxi"
*** Parametros
.Param tensao=3v
.Param F=0.2G P='1/F'
*** Tensoes estabelecidas
Vdd VDD VSS DC tensao
.CONNECT VSS 0
Vclock CLOCK 0 PULSE(0 3.0 0 '0.1*P' '0.1*P' '0.49*P' P)
*** Conexao do circuito
.CONNECT MC 0
*** Tempo de propagacao de subida e descida
.meas tran Pout trig v(OUT) val=tensao/2 rise=4 targ v(OUT) val=tensao/2 rise=5
.meas tran PClock trig v(CLOCK) val=tensao/2 rise=4 targ v(CLOCK) val=tensao/2 rise=5
.meas tran clockCir PARAM='Pout/Pclock'
*** Calculo Corrente media
.meas tran cor_avg AVG I(Vdd) FROM '5*P'
*** Calculo Potencia Consumida
```

```

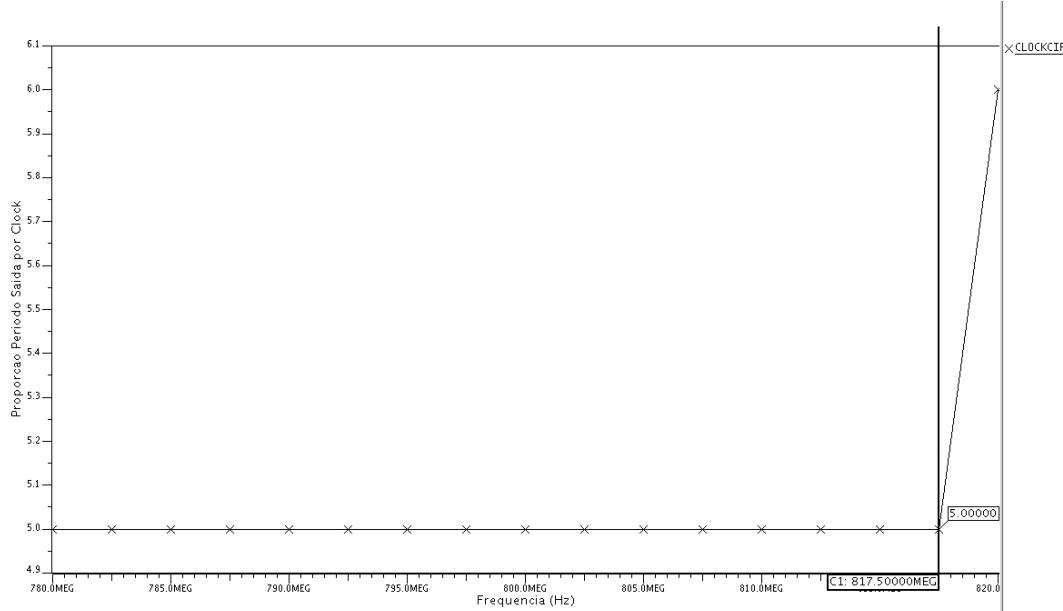
.meas tran power_calc PARAM='-cor_avg*tensao'
*** Escursionando frequencia em busca da maxima
*.tran 0 '50*P' 0 '0.1*P' sweep F INCR 0.1G 0.5G 1.5G
.tran 0 '50*P' 0 '0.1*P' sweep F INCR 0.0025G 0.5G 1.0G
*****
.probe tran ALL
.include Model135_Eldo
.end

```

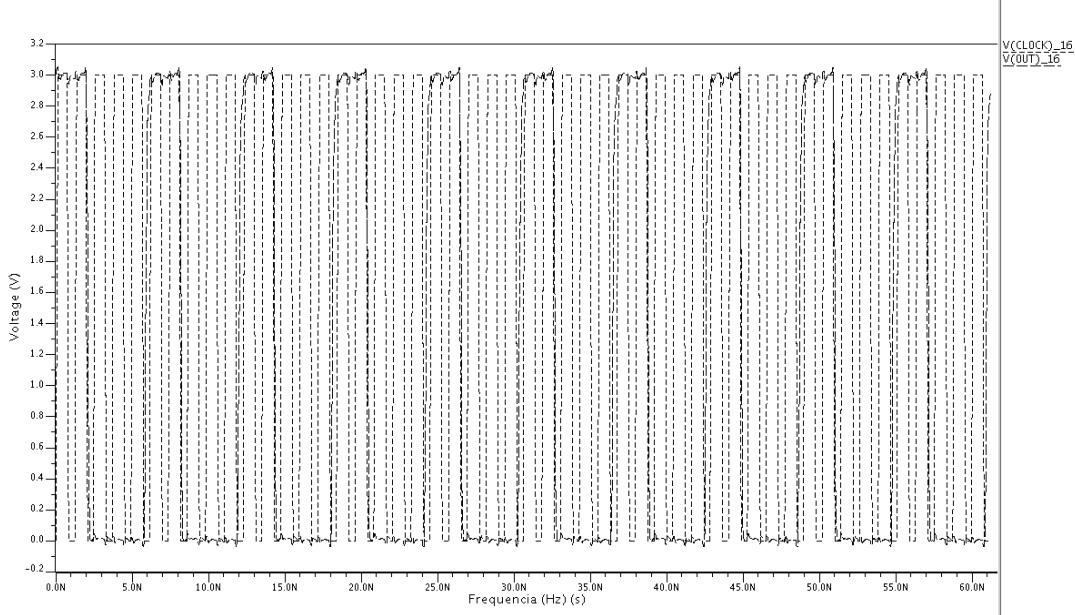
Questão 19: Extraia agora com a opção R+C+CC. Simule o circuito com parâmetros típicos e determine a máxima velocidade e consumo do circuito. Considere as mesmas condições do exercício 16.

Idem ao item 10, a partir da extração R+C+CC do *layout*, temos a análise do circuito com células *flip-flop*, **NOR** e **NAND**, realizamos o estudo para verificar o comportamento do circuito mediante excursionamento de frequência de operação e a proporção do período do *clock* com a saída vista na figura 23 e sinais tensões do *clock* e saída para as frequências marcadas na figura 23 (disposto na figura 24), e por fim, o consumo e potência dispersada presente na figura 25.

Figura 23 – Proporção entre o ciclo de *clock* e período de saída do circuito para excursionamento de frequência, marcado em 0,818GHz

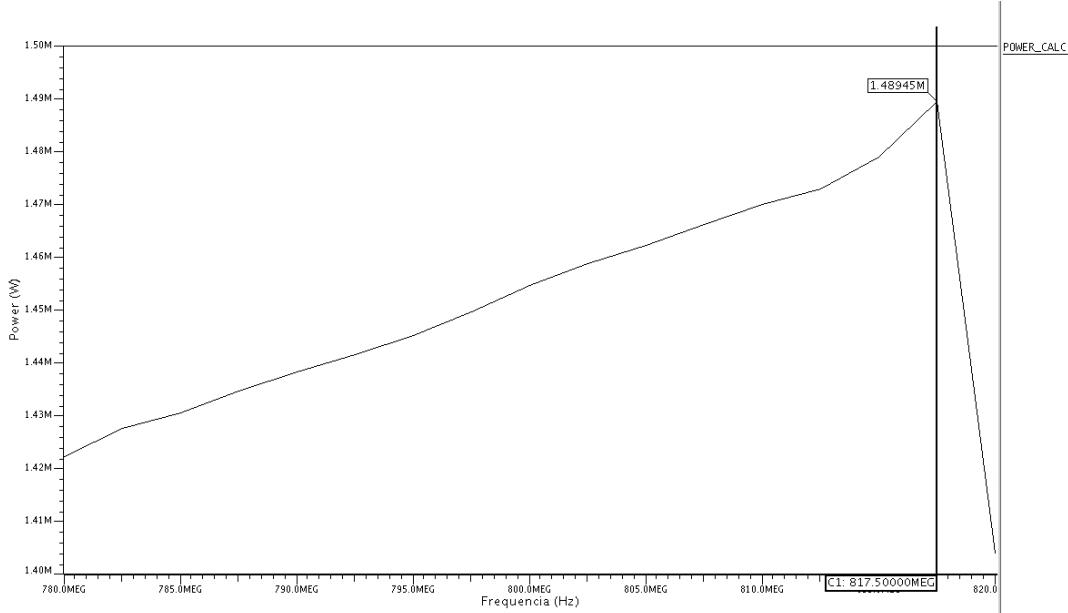


Fonte: Pelos próprios autores

Figura 24 – Sinais de tensão de saída e *clock* para frequência de 0,818GHz

Fonte: Pelos próprios autores

Figura 25 – Consumo de potência dispersada pelo divisor 4/5 para frequência de 0,818GHz



Fonte: Pelos próprios autores

Código completo da simulação:

```
.include "divisorqq.pex.netlist.pex"
.subckt DIVISORQQ N_CLOCK_X14_M0_g N_OUT_X14_M12_d N_MC_M11_g N_VSS_X14_M0_b N_VDD
mM0 N_VSS_M0_d N_6_M0_g N_8_M0_s N_VSS_X14_M0_b MODN L=3.5e-07 W=3e-06
+ AD=1.0225e-12 AS=2.69e-12 PD=5.5e-07 PS=5.05e-06 NRD=0.126866 NRS=0.126866
```

```

mM1 N_8_M1_d N_6_M1_g N_VSS_M0_d N_VSS_X14_M0_b MODN L=3.5e-07 W=3e-06
+ AD=2.19946e-12 AS=1.0225e-12 PD=1.74401e-06 PS=5.5e-07 NRD=0.126866
+ NRS=0.126866

mM2 N_3_M2_d N_2_M2_g N_8_M1_d N_VSS_X14_M0_b MODN L=3.5e-07 W=2.975e-06
+ AD=1.03175e-12 AS=2.18304e-12 PD=5.60393e-07 PS=1.73099e-06 NRD=0.12782
+ NRS=0.12782

mM3 N_8_M3_d N_2_M3_g N_3_M2_d N_VSS_X14_M0_b MODN L=3.5e-07 W=3e-06
+ AD=2.69e-12 AS=1.0395e-12 PD=5.05e-06 PS=5.64607e-07 NRD=0.126866 NRS=0.126866

mM4 N_5_M4_d N_2_M4_g N_VSS_M4_s N_VSS_X14_M0_b MODN L=3.5e-07 W=3e-06
+ AD=2.42375e-12 AS=2.93e-12 PD=1.8e-06 PS=5.05e-06 NRD=0.126866 NRS=0.126866

mM5 N_VSS_M5_d N_MC_M5_g N_5_M4_d N_VSS_X14_M0_b MODN L=3.5e-07 W=3e-06
+ AD=4.4375e-12 AS=2.42375e-12 PD=5.95e-06 PS=1.8e-06 NRD=0.126866 NRS=0.126866

mM6 N_3_M6_d N_6_M6_g N_VDD_M6_s N_VDD_X14_M13_b MODP L=3.5e-07 W=2.4e-06
+ AD=1.2e-12 AS=2.04e-12 PD=1e-06 PS=4.1e-06 NRD=0.177083 NRS=0.177083

mM7 N_VDD_M7_d N_6_M7_g N_3_M6_d N_VDD_X14_M13_b MODP L=3.5e-07 W=2.4e-06
+ AD=1.2e-12 AS=1.2e-12 PD=1e-06 PS=1e-06 NRD=0.177083 NRS=0.177083

mM8 N_3_M8_d N_2_M8_g N_VDD_M7_d N_VDD_X14_M13_b MODP L=3.5e-07 W=2.4e-06
+ AD=1.2e-12 AS=1.2e-12 PD=1e-06 PS=1e-06 NRD=0.177083 NRS=0.177083

mM9 N_VDD_M9_d N_2_M9_g N_3_M8_d N_VDD_X14_M13_b MODP L=3.5e-07 W=2.4e-06
+ AD=2.04e-12 AS=1.2e-12 PD=4.1e-06 PS=1e-06 NRD=0.177083 NRS=0.177083

mM10 11 N_2_M10_g N_VDD_M10_s N_VDD_X14_M13_b MODP L=3.5e-07 W=4.8e-06
+ AD=1.15875e-12 AS=3.685e-12 PD=4.5e-07 PS=6.15e-06 NRD=0.0825243 NRS=0.0825243

mM11 N_5_M11_d N_MC_M11_g 11 N_VDD_X14_M13_b MODP L=3.5e-07 W=4.8e-06
+ AD=3.45687e-12 AS=1.15875e-12 PD=2.025e-06 PS=4.5e-07 NRD=0.0825243
+ NRS=0.0825243

mM12 12 N_MC_M12_g N_5_M11_d N_VDD_X14_M13_b MODP L=3.5e-07 W=4.8e-06
+ AD=1.15875e-12 AS=3.45687e-12 PD=4.5e-07 PS=2.025e-06 NRD=0.0825243
+ NRS=0.0825243

mM13 N_VDD_M13_d N_2_M13_g 12 N_VDD_X14_M13_b MODP L=3.5e-07 W=4.8e-06
+ AD=3.9625e-12 AS=1.15875e-12 PD=6.15e-06 PS=4.5e-07 NRD=0.0825243 NRS=0.0825243

mX14_M0 N_VSS_X14_M0_d N_CLOCK_X14_M0_g N_X14_2_X14_M0_s N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=5e-07 AD=5.375e-13 AS=5.9e-13 PD=1.97222e-06 PS=2.7e-06 NRD=0.85
+ NRS=0.85

mX14_M1 N_X14_3_X14_M1_d N_X14_2_X14_M1_g N_VSS_X14_M0_d N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=4e-07 AD=5.7e-13 AS=4.3e-13 PD=2.8e-06 PS=1.57778e-06 NRD=1.0625
+ NRS=1.0625

mX14_M2 X14_15 N_X14_2_X14_M2_g N_VSS_X14_M2_s N_VSS_X14_M0_b MODN L=3.5e-07
+ W=1e-06 AD=2.25e-13 AS=7.45e-13 PD=4.5e-07 PS=2.7e-06 NRD=0.425 NRS=0.425

mX14_M3 N_X14_5_X14_M3_d N_3_X14_M3_g X14_15 N_VSS_X14_M0_b MODN L=3.5e-07

```

```

+ W=1e-06 AD=5e-13 AS=2.25e-13 PD=1e-06 PS=4.5e-07 NRD=0.425 NRS=0.425
mX14_M4 N_X14_6_X14_M4_d N_X14_3_X14_M4_g N_X14_5_X14_M3_d N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13 PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX14_M5 N_VSS_X14_M5_d N_X14_7_X14_M5_g N_X14_6_X14_M4_d N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5.125e-13 AS=5e-13 PD=1.025e-06 PS=1e-06 NRD=0.425
+ NRS=0.425
mX14_M6 N_X14_7_X14_M6_d N_X14_5_X14_M6_g N_VSS_X14_M5_d N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5e-13 AS=5.125e-13 PD=1e-06 PS=1.025e-06 NRD=0.425
+ NRS=0.425
mX14_M7 N_X14_X_X14_M7_d N_X14_3_X14_M7_g N_X14_7_X14_M6_d N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13 PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX14_M8 N_X14_10_X14_M8_d N_X14_2_X14_M8_g N_X14_X_X14_M7_d N_VSS_X14_M0_b
+ MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13 PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX14_M9 N_VSS_X14_M9_d N_X14_9_X14_M9_g N_X14_10_X14_M8_d N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5.875e-13 AS=5e-13 PD=1.175e-06 PS=1e-06 NRD=0.425
+ NRS=0.425
mX14_M10 N_X14_9_X14_M10_d N_X14_X_X14_M10_g N_VSS_X14_M9_d N_VSS_X14_M0_b
+ MODN L=3.5e-07 W=1e-06 AD=1.215e-12 AS=5.875e-13 PD=4.1e-06 PS=1.175e-06
+ NRD=0.425 NRS=0.425
mX14_M11 N_VSS_X14_M11_d N_X14_9_X14_M11_g N_X14_Q_X14_M11_s N_VSS_X14_M0_b
+ MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=7.45e-13 PD=1e-06 PS=2.7e-06 NRD=0.425
+ NRS=0.425
mX14_M12 N_OUT_X14_M12_d N_X14_10_X14_M12_g N_VSS_X14_M11_d N_VSS_X14_M0_b
+ MODN L=3.5e-07 W=1e-06 AD=8.5e-13 AS=5e-13 PD=2.7e-06 PS=1e-06 NRD=0.425
+ NRS=0.425
mX14_M13 N_VDD_X14_M13_d N_CLOCK_X14_M13_g N_X14_2_X14_M13_s N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1e-06 AD=1.16944e-12 AS=7.45e-13 PD=2.86111e-06 PS=2.7e-06
+ NRD=0.425 NRS=0.425
mX14_M14 N_VDD_X14_M13_d N_X14_2_X14_M14_g N_X14_3_X14_M14_s N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=8e-07 AD=9.35556e-13 AS=7.55e-13 PD=2.28889e-06 PS=3.1e-06
+ NRD=0.53125 NRS=0.53125
mX14_M15 N_X14_5_X14_M15_d N_X14_2_X14_M15_g N_X14_6_X14_M15_s N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1e-06 AD=5e-13 AS=1.355e-12 PD=1e-06 PS=4.1e-06 NRD=0.425
+ NRS=0.425
mX14_M16 X14_16 N_3_X14_M16_g N_X14_5_X14_M15_d N_VDD_X14_M13_b MODP L=3.5e-07
+ W=1.6e-06 AD=3.6e-13 AS=8e-13 PD=4.5e-07 PS=1.6e-06 NRD=0.265625 NRS=0.265625
mX14_M17 N_VDD_X14_M17_d N_X14_3_X14_M17_g X14_16 N_VDD_X14_M13_b MODP
+ L=3.5e-07 W=1.6e-06 AD=1.31625e-12 AS=3.6e-13 PD=3.3e-06 PS=4.5e-07
+ NRD=0.265625 NRS=0.265625

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mX14_M18 N_VDD_X14_M18_d N_X14_7_X14_M18_g N_X14_6_X14_M18_s N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1.6e-06 AD=9.1125e-13 AS=1.25e-12 PD=1.725e-06 PS=3.7e-06
+ NRD=0.217949 NRS=0.217949

mX14_M19 N_X14_7_X14_M19_d N_X14_5_X14_M19_g N_VDD_X14_M18_d N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1.6e-06 AD=1.25e-12 AS=9.1125e-13 PD=3.7e-06 PS=1.725e-06
+ NRD=0.217949 NRS=0.217949

mX14_M20 N_X14_X_X14_M20_d N_X14_2_X14_M20_g N_X14_7_X14_M20_s N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1e-06 AD=5e-13 AS=7.45e-13 PD=1e-06 PS=2.7e-06 NRD=0.425
+ NRS=0.425

mX14_M21 N_X14_10_X14_M21_d N_X14_3_X14_M21_g N_X14_X_X14_M20_d N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1e-06 AD=8.5e-13 AS=5e-13 PD=2.7e-06 PS=1e-06 NRD=0.425
+ NRS=0.425

mX14_M22 N_VDD_X14_M22_d N_X14_9_X14_M22_g N_X14_10_X14_M22_s N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1.6e-06 AD=9.025e-13 AS=1.455e-12 PD=1.6e-06 PS=4e-06
+ NRD=0.217949 NRS=0.217949

mX14_M23 N_X14_9_X14_M23_d N_X14_X_X14_M23_g N_VDD_X14_M22_d N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1.6e-06 AD=1.335e-12 AS=9.025e-13 PD=3.85e-06 PS=1.6e-06
+ NRD=0.217949 NRS=0.217949

mX14_M24 N_VDD_X14_M24_d N_X14_9_X14_M24_g N_X14_Q_X14_M24_s N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1.6e-06 AD=8e-13 AS=1.36e-12 PD=1e-06 PS=3.3e-06 NRD=0.265625
+ NRS=0.265625

mX14_M25 N_OUT_X14_M25_d N_X14_10_X14_M25_g N_VDD_X14_M24_d N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1.6e-06 AD=1.36e-12 AS=8e-13 PD=3.3e-06 PS=1e-06 NRD=0.265625
+ NRS=0.265625

mX15_M0 N_VSS_X15_M0_d N_CLOCK_X15_M0_g N_X15_2_X15_M0_s N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=5e-07 AD=5.375e-13 AS=5.9e-13 PD=1.97222e-06 PS=2.7e-06 NRD=0.85
+ NRS=0.85

mX15_M1 N_X15_3_X15_M1_d N_X15_2_X15_M1_g N_VSS_X15_M0_d N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=4e-07 AD=5.7e-13 AS=4.3e-13 PD=2.8e-06 PS=1.57778e-06 NRD=1.0625
+ NRS=1.0625

mX15_M2 X15_15 N_X15_2_X15_M2_g N_VSS_X15_M2_s N_VSS_X14_M0_b MODN L=3.5e-07
+ W=1e-06 AD=2.25e-13 AS=7.45e-13 PD=4.5e-07 PS=2.7e-06 NRD=0.425 NRS=0.425

mX15_M3 N_X15_5_X15_M3_d N_OUT_X15_M3_g X15_15 N_VSS_X14_M0_b MODN L=3.5e-07
+ W=1e-06 AD=5e-13 AS=2.25e-13 PD=1e-06 PS=4.5e-07 NRD=0.425 NRS=0.425

mX15_M4 N_X15_6_X15_M4_d N_X15_3_X15_M4_g N_X15_5_X15_M3_d N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13 PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425

mX15_M5 N_VSS_X15_M5_d N_X15_7_X15_M5_g N_X15_6_X15_M4_d N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5.125e-13 AS=5e-13 PD=1.025e-06 PS=1e-06 NRD=0.425
+ NRS=0.425

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mX15_M6 N_X15_7_X15_M6_d N_X15_5_X15_M6_g N_VSS_X15_M5_d N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5e-13 AS=5.125e-13 PD=1e-06 PS=1.025e-06 NRD=0.425
+ NRS=0.425

mX15_M7 N_X15_X_X15_M7_d N_X15_3_X15_M7_g N_X15_7_X15_M6_d N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13 PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425

mX15_M8 N_X15_10_X15_M8_d N_X15_2_X15_M8_g N_X15_X_X15_M7_d N_VSS_X14_M0_b
+ MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13 PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425

mX15_M9 N_VSS_X15_M9_d N_X15_9_X15_M9_g N_X15_10_X15_M8_d N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5.875e-13 AS=5e-13 PD=1.175e-06 PS=1e-06 NRD=0.425
+ NRS=0.425

mX15_M10 N_X15_9_X15_M10_d N_X15_X_X15_M10_g N_VSS_X15_M9_d N_VSS_X14_M0_b
+ MODN L=3.5e-07 W=1e-06 AD=1.215e-12 AS=5.875e-13 PD=4.1e-06 PS=1.175e-06
+ NRD=0.425 NRS=0.425

mX15_M11 N_VSS_X15_M11_d N_X15_9_X15_M11_g N_X15_Q_X15_M11_s N_VSS_X14_M0_b
+ MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=7.45e-13 PD=1e-06 PS=2.7e-06 NRD=0.425
+ NRS=0.425

mX15_M12 N_2_X15_M12_d N_X15_10_X15_M12_g N_VSS_X15_M11_d N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=8.5e-13 AS=5e-13 PD=2.7e-06 PS=1e-06 NRD=0.425 NRS=0.425

mX15_M13 N_VDD_X15_M13_d N_CLOCK_X15_M13_g N_X15_2_X15_M13_s N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1e-06 AD=1.16944e-12 AS=7.45e-13 PD=2.86111e-06 PS=2.7e-06
+ NRD=0.425 NRS=0.425

mX15_M14 N_VDD_X15_M13_d N_X15_2_X15_M14_g N_X15_3_X15_M14_s N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=8e-07 AD=9.35556e-13 AS=7.55e-13 PD=2.28889e-06 PS=3.1e-06
+ NRD=0.53125 NRS=0.53125

mX15_M15 N_X15_5_X15_M15_d N_X15_2_X15_M15_g N_X15_6_X15_M15_s N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1e-06 AD=5e-13 AS=1.355e-12 PD=1e-06 PS=4.1e-06 NRD=0.425
+ NRS=0.425

mX15_M16 X15_16 N_OUT_X15_M16_g N_X15_5_X15_M15_d N_VDD_X14_M13_b MODP
+ L=3.5e-07 W=1.6e-06 AD=3.6e-13 AS=8e-13 PD=4.5e-07 PS=1.6e-06 NRD=0.265625
+ NRS=0.265625

mX15_M17 N_VDD_X15_M17_d N_X15_3_X15_M17_g X15_16 N_VDD_X14_M13_b MODP
+ L=3.5e-07 W=1.6e-06 AD=1.31625e-12 AS=3.6e-13 PD=3.3e-06 PS=4.5e-07
+ NRD=0.265625 NRS=0.265625

mX15_M18 N_VDD_X15_M18_d N_X15_7_X15_M18_g N_X15_6_X15_M18_s N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1.6e-06 AD=9.1125e-13 AS=1.25e-12 PD=1.725e-06 PS=3.7e-06
+ NRD=0.217949 NRS=0.217949

mX15_M19 N_X15_7_X15_M19_d N_X15_5_X15_M19_g N_VDD_X15_M18_d N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1.6e-06 AD=1.25e-12 AS=9.1125e-13 PD=3.7e-06 PS=1.725e-06
+ NRD=0.217949 NRS=0.217949

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mX15_M20 N_X15_X_X15_M20_d N_X15_2_X15_M20_g N_X15_7_X15_M20_s N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1e-06 AD=5e-13 AS=7.45e-13 PD=1e-06 PS=2.7e-06 NRD=0.425
+ NRS=0.425

mX15_M21 N_X15_10_X15_M21_d N_X15_3_X15_M21_g N_X15_X_X15_M20_d N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1e-06 AD=8.5e-13 AS=5e-13 PD=2.7e-06 PS=1e-06 NRD=0.425
+ NRS=0.425

mX15_M22 N_VDD_X15_M22_d N_X15_9_X15_M22_g N_X15_10_X15_M22_s N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1.6e-06 AD=9.025e-13 AS=1.455e-12 PD=1.6e-06 PS=4e-06
+ NRD=0.217949 NRS=0.217949

mX15_M23 N_X15_9_X15_M23_d N_X15_X_X15_M23_g N_VDD_X15_M22_d N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1.6e-06 AD=1.335e-12 AS=9.025e-13 PD=3.85e-06 PS=1.6e-06
+ NRD=0.217949 NRS=0.217949

mX15_M24 N_VDD_X15_M24_d N_X15_9_X15_M24_g N_X15_Q_X15_M24_s N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1.6e-06 AD=8e-13 AS=1.36e-12 PD=1e-06 PS=3.3e-06 NRD=0.265625
+ NRS=0.265625

mX15_M25 N_2_X15_M25_d N_X15_10_X15_M25_g N_VDD_X15_M24_d N_VDD_X14_M13_b MODP
+ L=3.5e-07 W=1.6e-06 AD=1.36e-12 AS=8e-13 PD=3.3e-06 PS=1e-06 NRD=0.265625
+ NRS=0.265625

mX16_M0 N_VSS_X16_M0_d N_CLOCK_X16_M0_g N_X16_2_X16_M0_s N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=5e-07 AD=5.375e-13 AS=5.9e-13 PD=1.97222e-06 PS=2.7e-06 NRD=0.85
+ NRS=0.85

mX16_M1 N_X16_3_X16_M1_d N_X16_2_X16_M1_g N_VSS_X16_M0_d N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=4e-07 AD=5.7e-13 AS=4.3e-13 PD=2.8e-06 PS=1.57778e-06 NRD=1.0625
+ NRS=1.0625

mX16_M2 X16_15 N_X16_2_X16_M2_g N_VSS_X16_M2_s N_VSS_X14_M0_b MODN L=3.5e-07
+ W=1e-06 AD=2.25e-13 AS=7.45e-13 PD=4.5e-07 PS=2.7e-06 NRD=0.425 NRS=0.425

mX16_M3 N_X16_5_X16_M3_d N_5_X16_M3_g X16_15 N_VSS_X14_M0_b MODN L=3.5e-07
+ W=1e-06 AD=5e-13 AS=2.25e-13 PD=1e-06 PS=4.5e-07 NRD=0.425 NRS=0.425

mX16_M4 N_X16_6_X16_M4_d N_X16_3_X16_M4_g N_X16_5_X16_M3_d N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13 PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425

mX16_M5 N_VSS_X16_M5_d N_X16_7_X16_M5_g N_X16_6_X16_M4_d N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5.125e-13 AS=5e-13 PD=1.025e-06 PS=1e-06 NRD=0.425
+ NRS=0.425

mX16_M6 N_X16_7_X16_M6_d N_X16_5_X16_M6_g N_VSS_X16_M5_d N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5e-13 AS=5.125e-13 PD=1e-06 PS=1.025e-06 NRD=0.425
+ NRS=0.425

mX16_M7 N_X16_X_X16_M7_d N_X16_3_X16_M7_g N_X16_7_X16_M6_d N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13 PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425

mX16_M8 N_X16_10_X16_M8_d N_X16_2_X16_M8_g N_X16_X_X16_M7_d N_VSS_X14_M0_b

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+ MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=5e-13 PD=1e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX16_M9 N_VSS_X16_M9_d N_X16_9_X16_M9_g N_X16_10_X16_M8_d N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=5.875e-13 AS=5e-13 PD=1.175e-06 PS=1e-06 NRD=0.425
+ NRS=0.425
mX16_M10 N_X16_9_X16_M10_d N_X16_X_X16_M10_g N_VSS_X16_M9_d N_VSS_X14_M0_b
+ MODN L=3.5e-07 W=1e-06 AD=1.215e-12 AS=5.875e-13 PD=4.1e-06 PS=1.175e-06
+ NRD=0.425 NRS=0.425
mX16_M11 N_VSS_X16_M11_d N_X16_9_X16_M11_g N_X16_Q_X16_M11_s N_VSS_X14_M0_b
+ MODN L=3.5e-07 W=1e-06 AD=5e-13 AS=7.45e-13 PD=1e-06 PS=2.7e-06 NRD=0.425
+ NRS=0.425
mX16_M12 N_6_X16_M12_d N_X16_10_X16_M12_g N_VSS_X16_M11_d N_VSS_X14_M0_b MODN
+ L=3.5e-07 W=1e-06 AD=8.5e-13 AS=5e-13 PD=2.7e-06 PS=1e-06 NRD=0.425 NRS=0.425
mX16_M13 N_VDD_X16_M13_d N_CLOCK_X16_M13_g N_X16_2_X16_M13_s N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1e-06 AD=1.16944e-12 AS=7.45e-13 PD=2.86111e-06 PS=2.7e-06
+ NRD=0.425 NRS=0.425
mX16_M14 N_VDD_X16_M13_d N_X16_2_X16_M14_g N_X16_3_X16_M14_s N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=8e-07 AD=9.35556e-13 AS=7.55e-13 PD=2.28889e-06 PS=3.1e-06
+ NRD=0.53125 NRS=0.53125
mX16_M15 N_X16_5_X16_M15_d N_X16_2_X16_M15_g N_X16_6_X16_M15_s N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1e-06 AD=5e-13 AS=1.355e-12 PD=1e-06 PS=4.1e-06 NRD=0.425
+ NRS=0.425
mX16_M16 X16_16 N_5_X16_M16_g N_X16_5_X16_M15_d N_VDD_X14_M13_b MODP L=3.5e-07
+ W=1.6e-06 AD=3.6e-13 AS=8e-13 PD=4.5e-07 PS=1.6e-06 NRD=0.265625 NRS=0.265625
mX16_M17 N_VDD_X16_M17_d N_X16_3_X16_M17_g X16_16 N_VDD_X14_M13_b MODP
+ L=3.5e-07 W=1.6e-06 AD=1.31625e-12 AS=3.6e-13 PD=3.3e-06 PS=4.5e-07
+ NRD=0.265625 NRS=0.265625
mX16_M18 N_VDD_X16_M18_d N_X16_7_X16_M18_g N_X16_6_X16_M18_s N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1.6e-06 AD=9.1125e-13 AS=1.25e-12 PD=1.725e-06 PS=3.7e-06
+ NRD=0.217949 NRS=0.217949
mX16_M19 N_X16_7_X16_M19_d N_X16_5_X16_M19_g N_VDD_X16_M18_d N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1.6e-06 AD=1.25e-12 AS=9.1125e-13 PD=3.7e-06 PS=1.725e-06
+ NRD=0.217949 NRS=0.217949
mX16_M20 N_X16_X_X16_M20_d N_X16_2_X16_M20_g N_X16_7_X16_M20_s N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1e-06 AD=5e-13 AS=7.45e-13 PD=1e-06 PS=2.7e-06 NRD=0.425
+ NRS=0.425
mX16_M21 N_X16_10_X16_M21_d N_X16_3_X16_M21_g N_X16_X_X16_M20_d N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1e-06 AD=8.5e-13 AS=5e-13 PD=2.7e-06 PS=1e-06 NRD=0.425
+ NRS=0.425
mX16_M22 N_VDD_X16_M22_d N_X16_9_X16_M22_g N_X16_10_X16_M22_s N_VDD_X14_M13_b

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+ MODP L=3.5e-07 W=1.6e-06 AD=9.025e-13 AS=1.455e-12 PD=1.6e-06 PS=4e-06
+ NRD=0.217949 NRS=0.217949
mX16_M23 N_X16_9_X16_M23_d N_X16_X_X16_M23_g N_VDD_X16_M22_d N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1.6e-06 AD=1.335e-12 AS=9.025e-13 PD=3.85e-06 PS=1.6e-06
+ NRD=0.217949 NRS=0.217949
mX16_M24 N_VDD_X16_M24_d N_X16_9_X16_M24_g N_X16_Q_X16_M24_s N_VDD_X14_M13_b
+ MODP L=3.5e-07 W=1.6e-06 AD=8e-13 AS=1.36e-12 PD=1e-06 PS=3.3e-06 NRD=0.265625
+ NRS=0.265625
mX16_M25 N_6_X16_M25_d N_X16_10_X16_M25_g N_VDD_X16_M24_d N_VDD_X14_M13_b MODP
+ L=3.5e-07 W=1.6e-06 AD=1.36e-12 AS=8e-13 PD=3.3e-06 PS=1e-06 NRD=0.265625
+ NRS=0.265625
.include "divisorqq.pex.netlist.DIVISORQQ.pxi"
.ends DIVISORQQ

*** Parametros
.Param tensao=3v
.Param F=0.2G P='1/F'

*** Tensoes estabelecidas
Vdd VDD VSS DC tensao
.CONNECT VSS 0
Vclock CLOCK 0 PULSE(0 3.0 0 '0.1*P' '0.1*P' '0.49*P' P)

*** Conexao do circuito
.CONNECT MC 0
Xcir CLOCK OUT MC VSS VDD DIVISORQQ

*** Tempo de propagacao de subida e descida
.meas tran Pout trig v(OUT) val=tensao/2 rise=4 targ v(OUT) val=tensao/2 rise=5
.meas tran PClock trig v(CLOCK) val=tensao/2 rise=4 targ v(CLOCK) val=tensao/2 rise=5
.meas tran clockCir PARAM='Pout/Pclock'
*** Calculo Corrente media
.meas tran cor_avg AVG I(Vdd) FROM '5*P'
*** Calculo Corrente media
.meas tran power_calc PARAM='cor_avg*tensao'
*** Calculo Corrente media
.meas tran consum PARAM='power_calc/F'
*** Escursionando frequencia em busca da maxima
*.tran 0 '50*P' 0 '0.1*P' sweep F INCR 0.1G 0.5G 1.5G

```

```
.tran 0 '50*P' 0 '0.1*P' sweep F INCR 0.0025G 0.78G 0.82G
*****
.probe tran ALL
.include Model135_Eldo
.end
```

Questão 20: Monte uma tabela com os resultados obtidos nos exercícios 14, 16, 18 e 19. Compare e comente os resultados.

Idem ao item 11, Como solicitado apresenta-se a tabela 4 com o resultados para máxima frequência de operação.

Tabela 4 – Tabela com frequência máxima conforme extração

Tipo Extração	Frequência Máxima [GHz]
Teórico	1,056
Esquemático	1,098
R+C+CC	0,818
C+CC	0,840

Fonte: Pelos próprios autores

Com os valores de frequência máxima de operação entre as distintas formas de projetar (manipular) o circuito, verifica-se que o esquemático se aproxima do valor teórico por desprezar os componentes parasitários provenientes das propriedades físicas do projeto, e, esta relação, é verificada também entre a extração C+CC e R+C+CC, pois a segunda apresenta mais componentes parasitários que a anterior. De forma geral idem ao item 11.

Com o consumo e potência, nota-se similaridade com a relação da frequência máxima e tipos de extração distintos, devido aos mesmos motivos de complexidade da extração, logo, descrevendo estruturas parasitárias, como visto na tabela 5.

Tabela 5 – Tabela com consumo de potência conforme extração

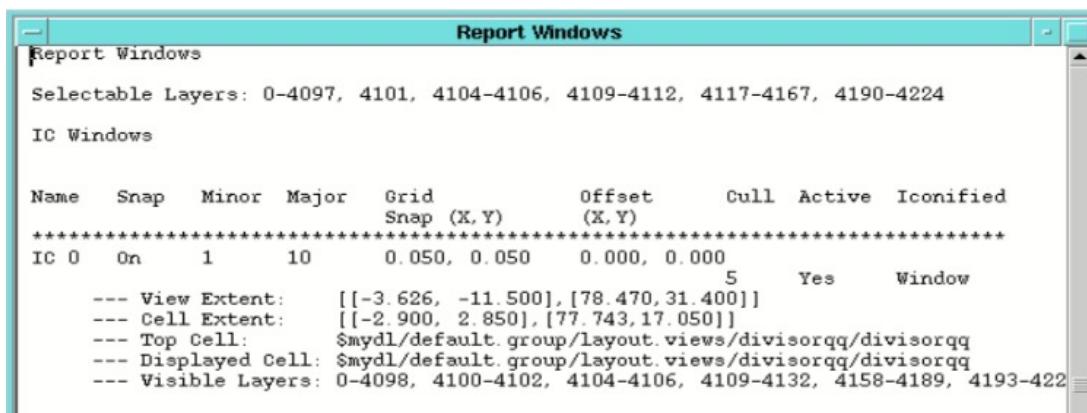
Tipo Extração	Consumo [mW/GHz]
Esquemático	1,371
R+C+CC	1,489
C+CC	1,544

Fonte: Pelos próprios autores

Questão 21: Determine a área total do circuito que desenhou.

Assim como realizado anteriormente utilizando a ferramente “Report -> Windows” temos que o circuito possui $80,643\mu m$ de largura e $14,2\mu m$ de comprimento como visto na figura 26, logo o circuito possui área de $1,15nm^2$ aproximadamente.

Figura 26 – Captura de tela Report - Windows



The screenshot shows a window titled "Report Windows" with the following content:

Name	Snap	Minor	Major	Grid Snap (X, Y)	Offset (X, Y)	Cull	Active	Iconified
IC 0	On	1	10	0.050, 0.050	0.000, 0.000	5	Yes	Window

Below the table, there are several informational lines:

- View Extent: [[-3.626, -11.500], [78.470, 31.400]]
- Cell Extent: [[-2.900, 2.850], [77.743, 17.050]]
- Top Cell: \$mydl/default.group/layout.views/divisorqq/divisorqq
- Displayed Cell: \$mydl/default.group/layout.views/divisorqq/divisorqq
- Visible Layers: 0-4098, 4100-4102, 4104-4106, 4109-4132, 4158-4189, 4193-422

Fonte: Pelos próprios autores

Referências

CORPORATION, M. G. *Mentor Graphics Corporation*. [S.l.], 2005. Disponível em: <<http://web.engr.uky.edu/~elias/tutorials/Eldo/eldo\ur.pdf>>. Acesso em: 20 Jul. 2021. Citado 3 vezes nas páginas 6, 7 e 26.