Codasip

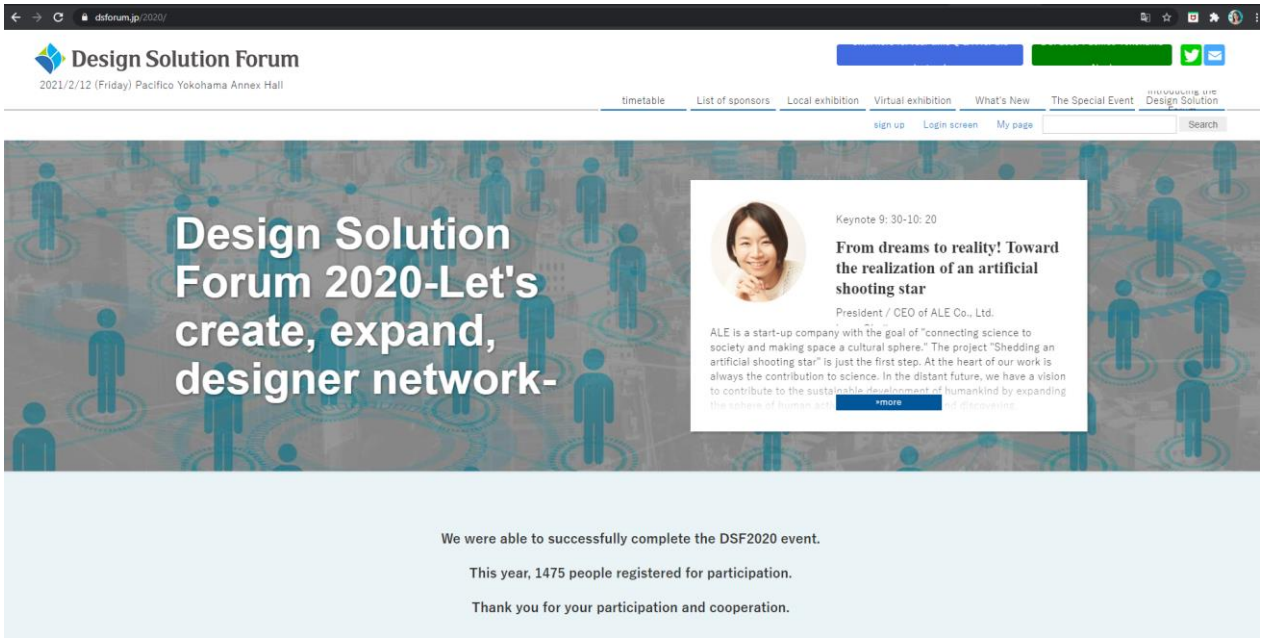
GRANT AGREEMENT # 881172
Deliverables Reporting
Work package 6 – Improve visibility across EU and Asia-Pacific
Deliverable number ref 6.8, Contribute to Design Solution Forum in Japan with a presentation in Japanese

Date: 16.02.2021
Responsible Person: Roddy Urquhart, Senior Marketing Director

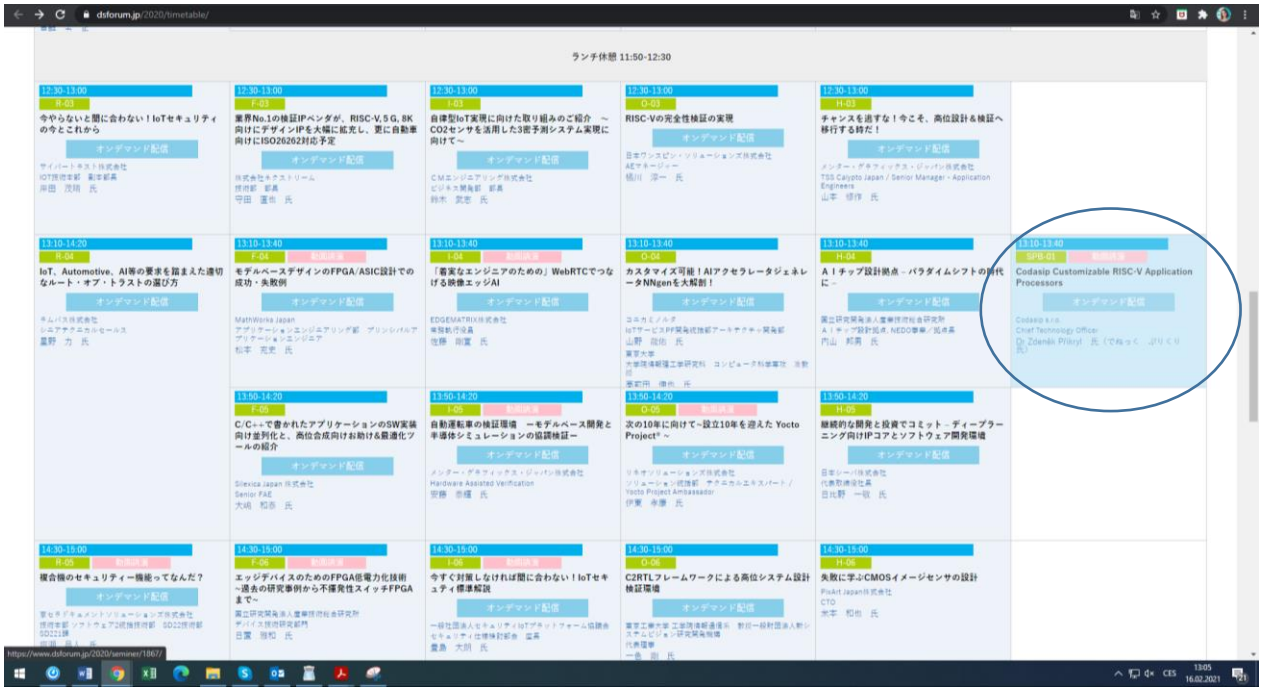
This project is co-funded by the Horizon 2020 Programme of the European Union

Design Solution Forum was finally held on 2021/02/12

On behalf of Codasip**: Zdenek Prikryl** / CTO; 2021/02/12; 13:10 JST (Japan Standard Time)



Timetable:



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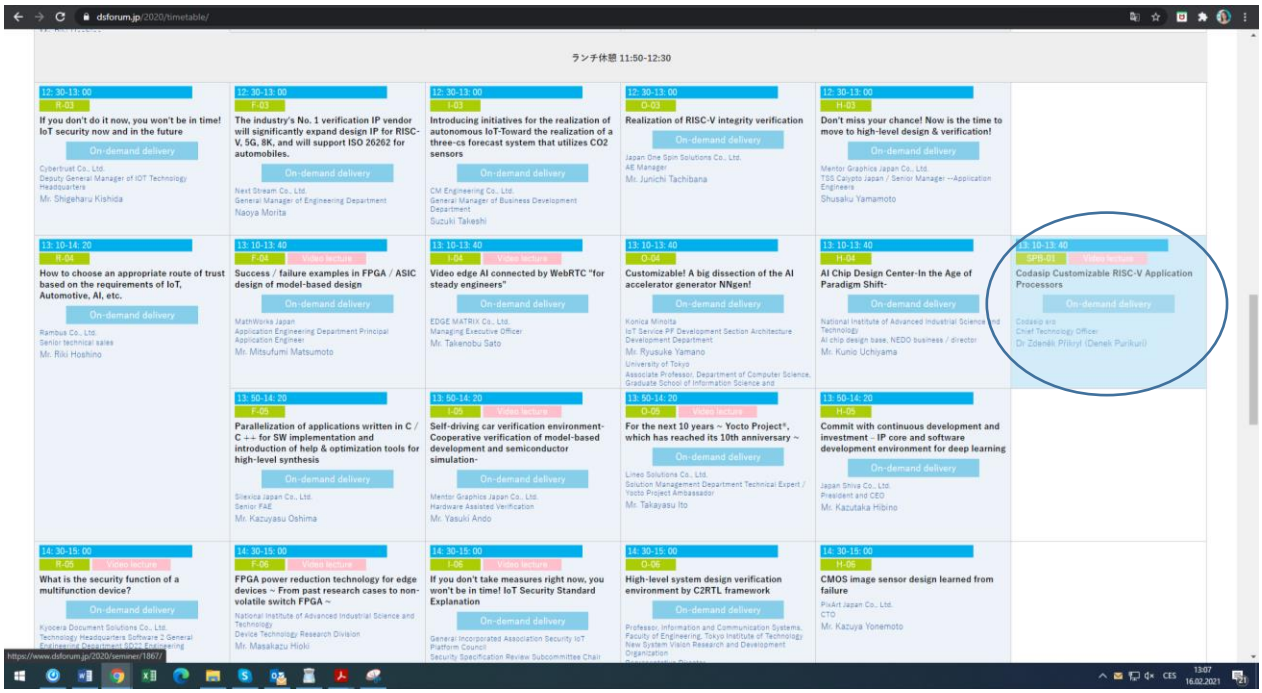

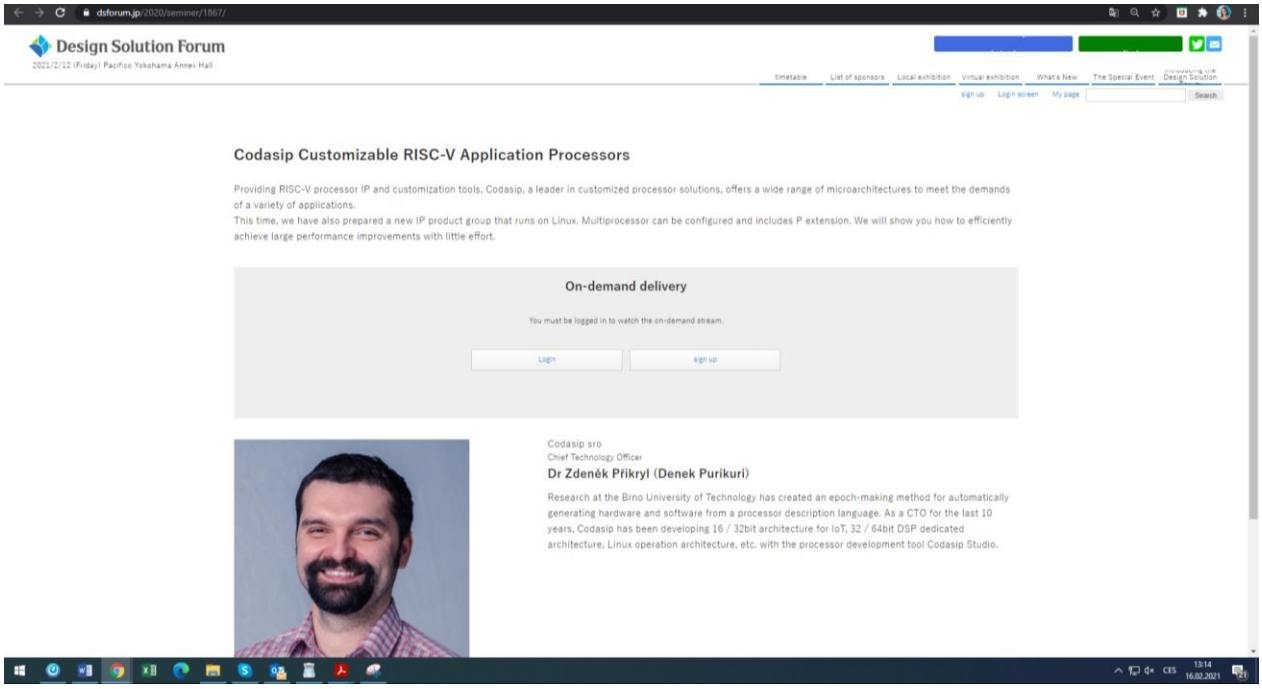

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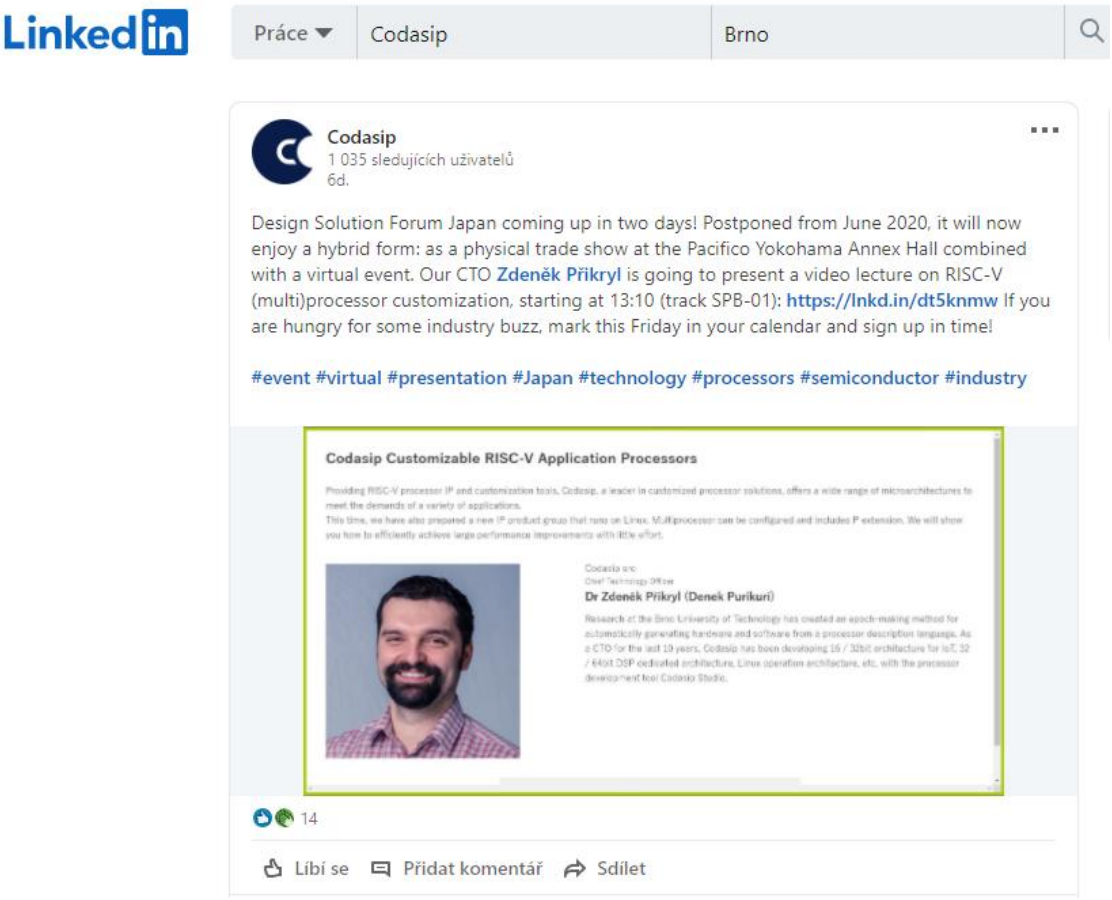

Presentation:

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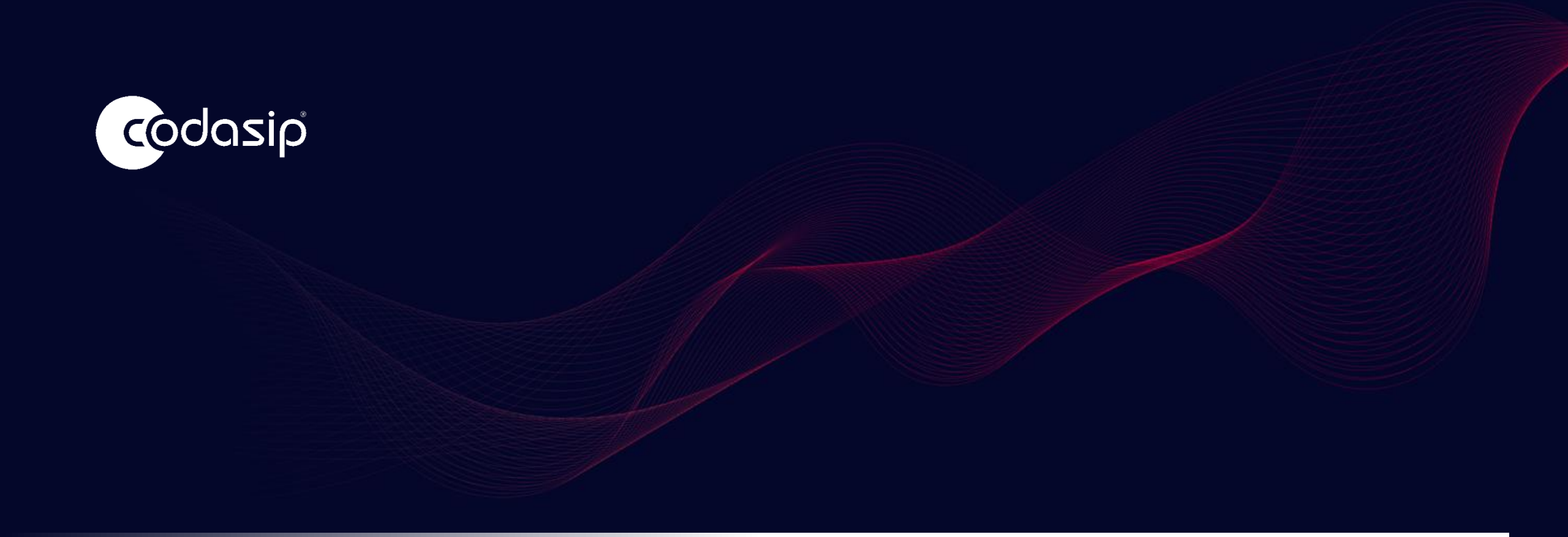

Codasip Customizable RISC-V Application Processors

Design Solution Forum 2021

February 2021

Zdenek Prikryl

Agenda

- Introduction
- Codasip RISC-V Application Processors
- P (DSP) Extension
- Multiprocessor solution
- Customization
- Conclusion

Who is Codasip?

- Leading provider of **RISC-V processor IP** and processor **design automation tools**
- Company founded in 2014 in Brno, Czech Republic
  - Based on 10 years of university research on processor design automation
  - Founding member of the RISC-V Foundation, www.riscv.org
  - Introduced world's first licensable RISC-V processor IP in November 2015
  - Active member of several RISC-V TGs and open-source projects
- Company headquarters in Germany and R&D centers located in the Czech Republic and France
  - 90+ employees
  - Veterans in CPU and cache coherency solutions
  - Technology leader in processor design automation
  - Sales offices worldwide

Codasip Solutions

codasip
RISC-V PROCESSORS

Our portfolio of RISC-V processor IP cores

- Low power embedded
- High performance embedded
- Application processors

codasip
STUDIO

Unique automation toolset for easy processor design or modification

- Make small optimizations to a proven processor IP, or
- Implement a unique processor solution using the same tools.

Codasip RISC-V Processors

	Low Power Embedded • 32bit	High Performance Embedded • 32bit or 64bit		Application • MMU • Supervisor privilege mode • Instruction + Data cache • Atomic instructions • FD instruction set		Additional Features
7 Series • 7-9 stage • IMC instruction set • 32 registers • Branch predictor				**A70X** **A70XP**	**A70X-MP** **A70XP-MP**	Instruction + Data Cache or TCM
5 Series • 5-stage • IMC instruction set • 32 registers • Branch predictor	L50 L50F	H50X H50XF	H50P H50FP H50XP H50XFP			PMP + PMA
3 Series • 3-4 stage • IMC instruction set • 32 registers	L30 L30F	H30P H30FP				SP/DP FPU
1 Series • 3-stage • EMC instruction set • 16 registers	L10					Customization Extension

Common Features

- Available immediately
- All Codasip Processors are RISC-V compliant
  - Implement RISC-V privilege specification
  - Implement RISC-V debug specification
- All Customizable
- Pre-verified, tape-out quality IP
  - Users do not need to verify IP
- Industry-standard interfaces
  - AMBA for instruction and data bus
  - JTAG (4pin/2pin) for debugging

All Codasip RISC-V Processors are **available in many configurations** allowing our customers to choose the core which fits the best their needs.

All Codasip RISC-V Processors are **customizable** allowing our customers to add key differentiation points on ISA as well as micro-architecture level.

Deliverables

Hardware Development Kit (HDK)

- RTL (Verilog/VHDL/SystemVerilog)
- Verification report
- Integration test bench
- Sample EDA scripts

Software Development Kit (SDK)

- C/C++ LLVM compiler (improved by Codasip)
- C/C++ Libraries (newlib)
- Assembler, disassembler, linker
- High-performance instruction set and cycle accurate simulators
- Debugger and profiler

+ CodeSpace (Eclipse based IDE)

Application Class RISC-V Processors

- 7 pipeline stages, *mostly* in-order architecture
- Optimized for effective compute
- SV39 MMU
- Linux capable
- Four base ISAs
  - IMAC
  - IMAC**P**
  - GC
  - GC**P**
- High performance FPU

```
OpenSBI v0.6
   ____                    _____ ____ _____
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Platform Name          : Codasip
Platform HART Features : RV64ACDFIMSU
Platform Max HARTs     : 1
Current Hart           : 0
Firmware Base          : 0x80000000
Firmware Size          : 64 KB
Runtime SBI Version    : 0.2

MIDELEG : 0x0000000000000222
MEDELEG : 0x000000000000b109

[    0.000000] OF: fdt: No chosen node found, continuing without
[    0.000000] OF: fdt: Ignoring memory range 0x80000000 - 0x80200000
[    0.000000] Linux version 5.4.36 (codasip@build) (gcc version 9.2.0 (GCC)) #1
SMP Thu Sep 17 12:08:58 CEST 2020
[    0.000000] initrd not found or empty - disabling initrd
[    0.000000] Zone ranges:
[    0.000000]   DMA32    [mem 0x0000000080200000-0x0000000081ffffff]
[    0.000000]   Normal   empty
[    0.000000] Movable zone start for each node
[    0.000000] Early memory node ranges
[    0.000000]   node   0: [mem 0x0000000080200000-0x0000000081ffffff]
[    0.000000] Initmem setup node 0 [mem 0x0000000080200000-0x0000000081ffffff]
[    0.000000] software IO TLB: Cannot allocate buffer
```
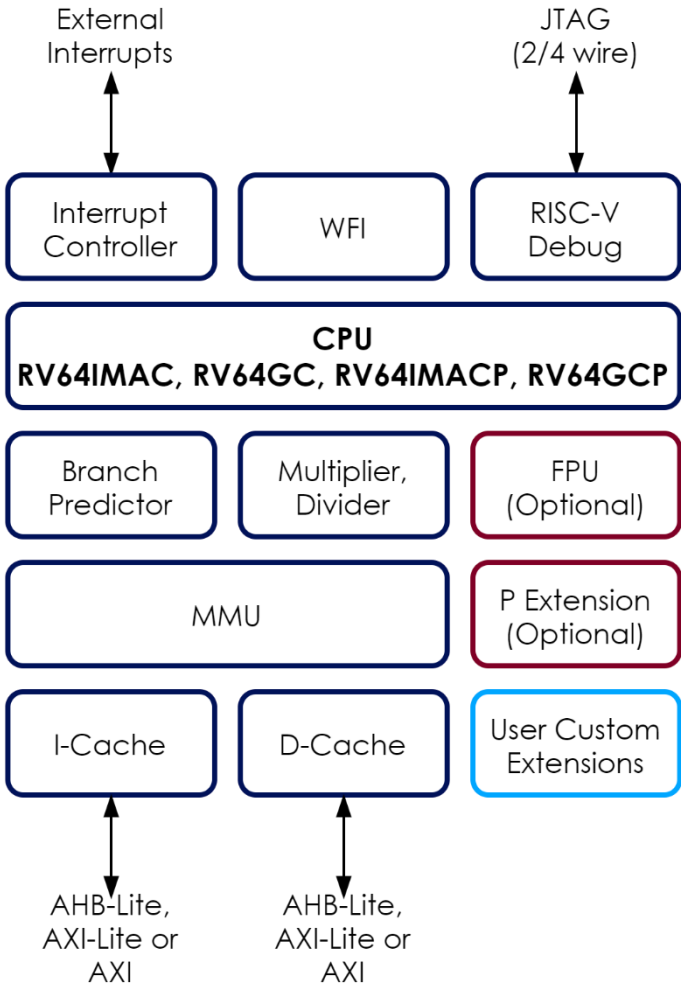
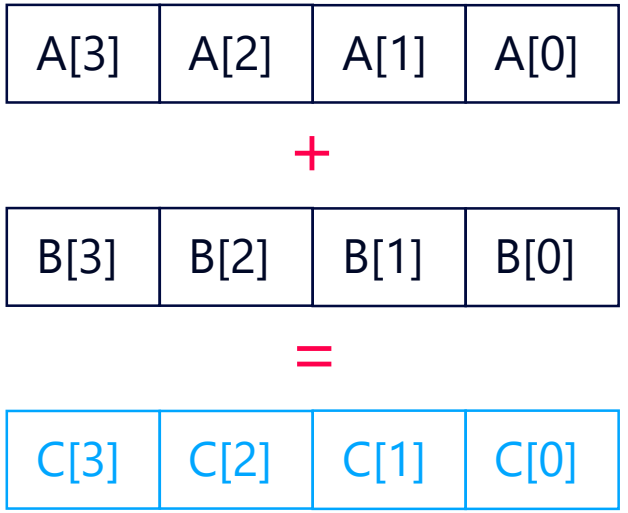

Application Class RISC-V Processors

- Highly Configurable
  - Cache
  - Branch Predictor
  - ISA
  - JTAG or cJTAG
  - Single processor or multiprocessor
- Customizable
  - ISA
  - Microarchitecture
- Virtual prototypes
  - Functional
  - Cycle-accurate



P Extension

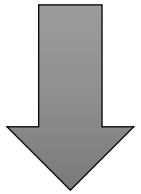
- Single instruction, multiple data operations (SIMD) are used mostly to accelerate digital signal processing (DSP). This covers domains such as:
  - Audio encoding/decoding
  - Computer vision
  - Sensor fusion
  - Compact AI/ML applications on the edge
- P extension:
  - Works on the integer register file
  - Contains approximately 331 instructions split into groups
    - Can be enabled/disabled based on the configuration
  - Enables RISC-V processors run DSP applications with higher performance and lower power consumption.



Programming model

- GCC C compiler
  - Standard intrinsic/inline assembly approach
- LLVM C compiler
  - Standard intrinsic/inline assembly approach
  - **Plus C compiler**
    - C compiler does auto-vectorization and other advanced features

```
#define SIZE 1024

void foo(char* a, const char* b)
{
    for (int ii = 0; ii < SIZE; ++ii)
        a[ii] = a[ii] + b[ii];
}
```

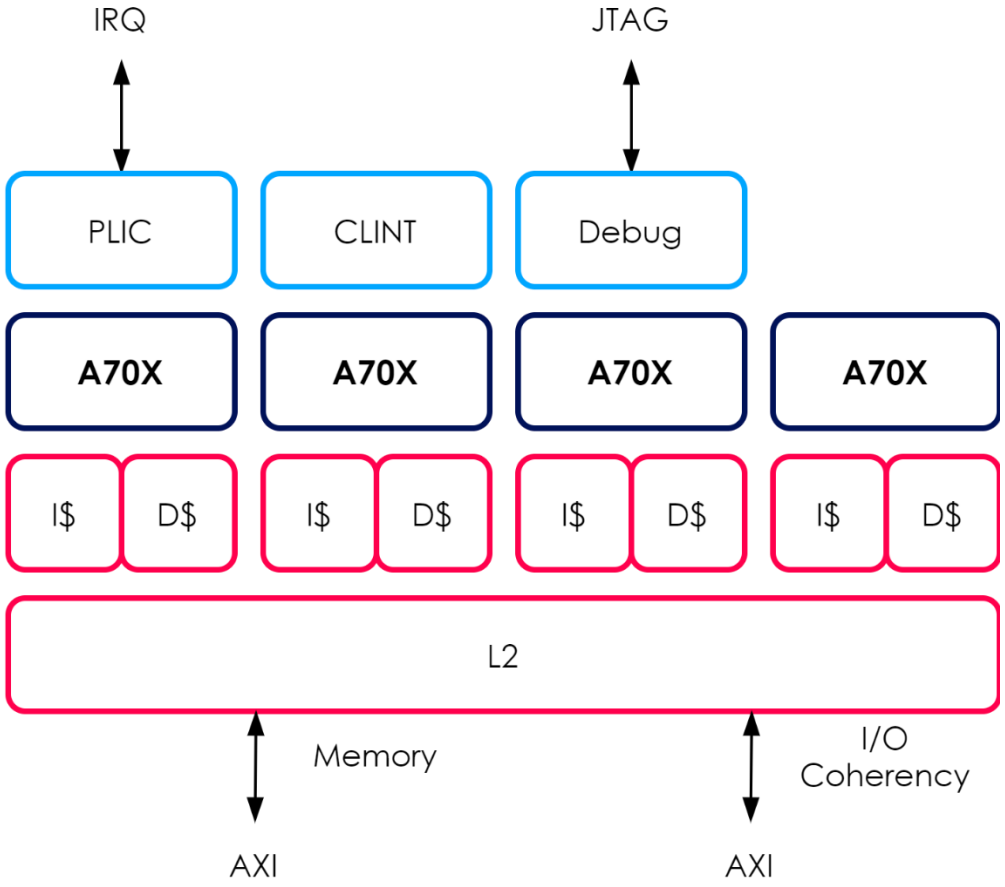


```
$foo:                                   //  @foo
    c.li x12, 0
    add x13, x0, 1024
LBB0_1:                                 //  %vector.body
                                        //  =>This Inner Loop Header: Depth=1
    add x14, x10, x12
    add x15, x11, x12
    c.lw x14, 0 ( x14 )
    lw x16, 0 ( x15 )
    c.add x12, 4
    add8 x14, x14, x16
    c.sw x14, 0 ( x15 )
    bne x12, x13, LBB0_1
LBB0_2:                                 //  %for.cond.cleanup
    c.jr ra
```

Multiprocessor Solution – Overview

- Codasip RISC-V application processors
  - Up to 4 cores
  - Coherent L1 and L2 caches scalable micro-architecture
  - AXI external interface followed by support of CHI protocol
  - I/O Coherency port
  - Optimized for efficient computing including streaming
  - Embeds data prefetchers at L1 and L2.
  - Per core and cluster power domain.

- **Verified and qualified with ideal and real-life downstream IPs.**



Multiprocessor Solution – Configuration Options

	Configuration parameters
Number of cores	1, 2, 3, 4
L1 Size	32kB, 64kB
L2 Size	128kB - 8MB (increments of power of 2)
Number of ways L1 / L2	4, 8, 16
Cache line size	32B, 64B
Error protection	L1 & L2, L2 only, Disabled
Internal resources sizing for PPA tradeoffs	Configurable (Optimized for performance or area)
Master interface	AXI4 (or CHI in Q4'21) 64b width, 128b width
I/O Coherency port	Optional

Availabilities:

- Intra-cluster coherency AXI master
  - Preview / early evaluation - Q1 2021
  - Production ready - Q2-2021
- Full system coherency CHI based
  - Production ready - Q4-2021

Not Found The Processor You Were Looking For?

RISC-V **open-source instruction set** architecture was designed for **customizations**

- Differentiate your product while keeping the ecosystem benefits
- Optimize the ISA to achieve better PPA
- Use any existing Codasip RISC-V Processor as a **baseline** for your customization
- Customize any RISC-V processor yourself using **Codasip Studio!**

Codasip Studio **automates** customization

- Design space exploration
- **Generates** SDK using custom ISA
  - Compiler, assembler & linker
  - Debugger & profiler
  - Instruction set simulator (ISS)
- Corresponding HDK is also **generated**
  - RTL
  - Testbench
  - UVM environment

codasip STUDIO

What is Codasip Studio?

A unique collection of tools for **fast & easy modification** of RISC-V processors.

All-in-one, highly automated. Introduced in 2014, **silicon-proven** by major vendors.

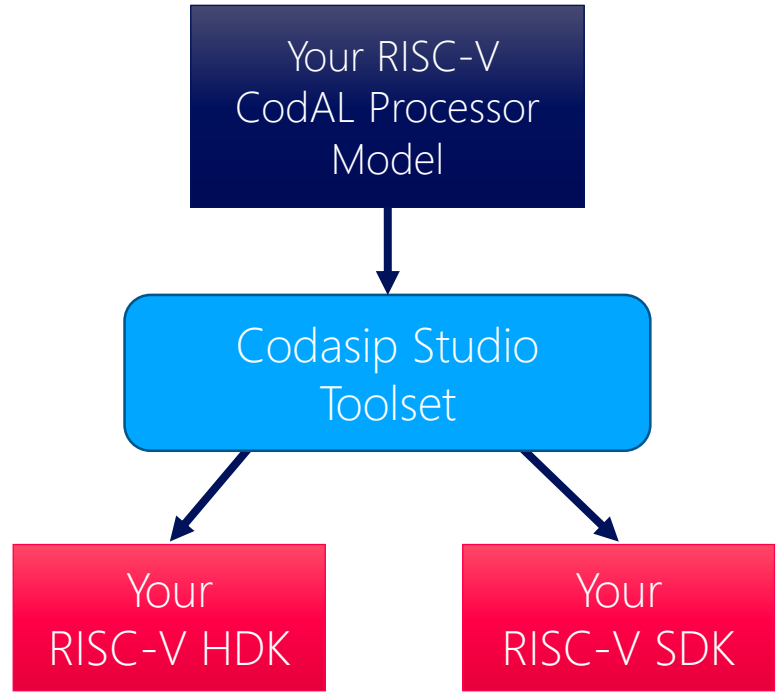
Processor described in **high-level** architecture description language

Allows customization of:

- Instruction set architecture (ISA)
- Micro-architecture

Users may choose to:

- **Modify** an existing Codasip RISC-V Processor
- **Design** new processor from scratch



CodAL™

Easy-to-understand **C-like language** that models a rich set of processor capabilities

All Codasip processors are created and verified using CodAL

Multiple microarchitectures can be implemented in a single CodAL model

CodAL models are provided to Codasip IP customers as **a starting point** for their processor optimizations and modifications

CodAL Description

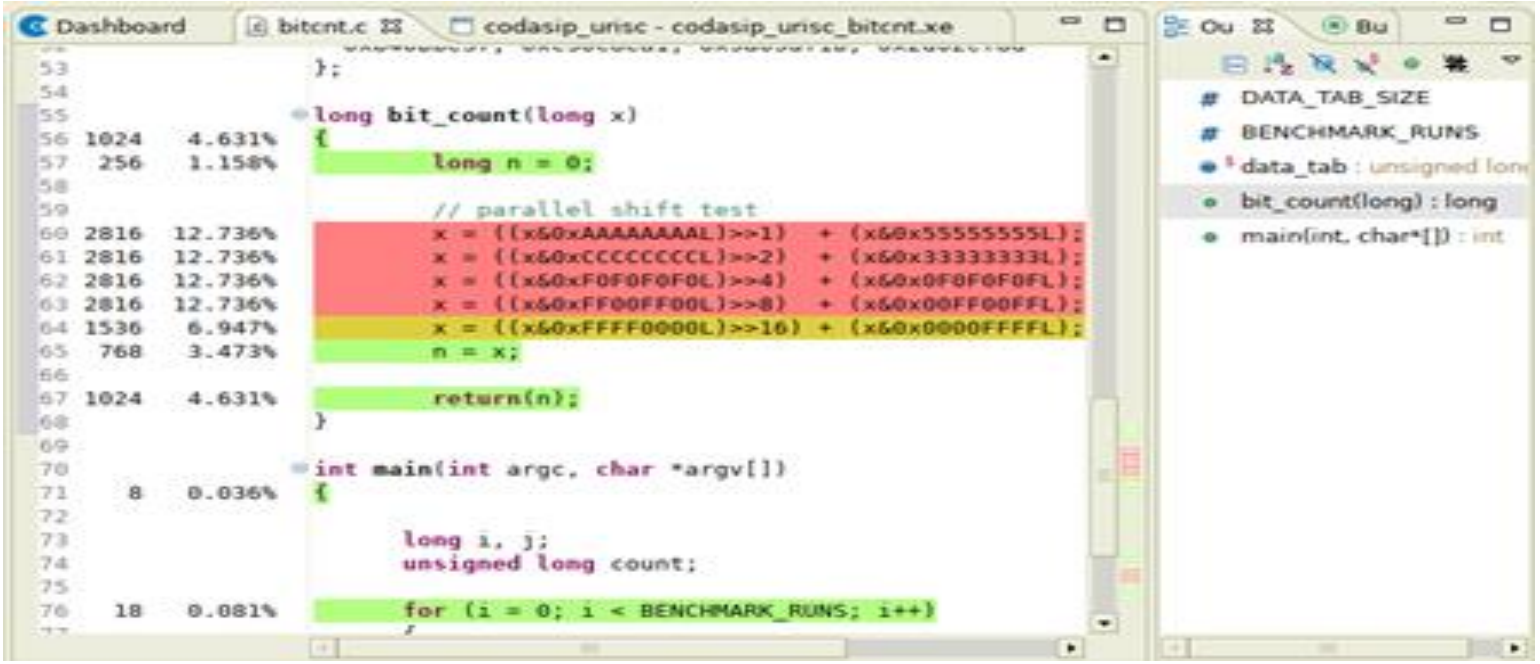

```
/*    Multiply and accumulate: semantics
                    dst += src1 * src2
*/

element i_mac {
          use reg as dst, src1, src2;
          assembly { “mac” dst “,” src1 “,” src2 };
          binary { OP_MAC:8 dst src1 src2 0:9 };
          semantics {
                    rf[dst] += rf[src1] * rf[src2];
          };
};
```

Design Space Exploration

Profiling of embedded software detects possibilities for processor optimization

ISA extensions are quickly implemented which allows **analysis** of their impact

Codasip Studio automatically generates all processor IP design kits and verifies for RISC-V compliance (you still need to verify your own resources and instructions)



Processor IP Verification

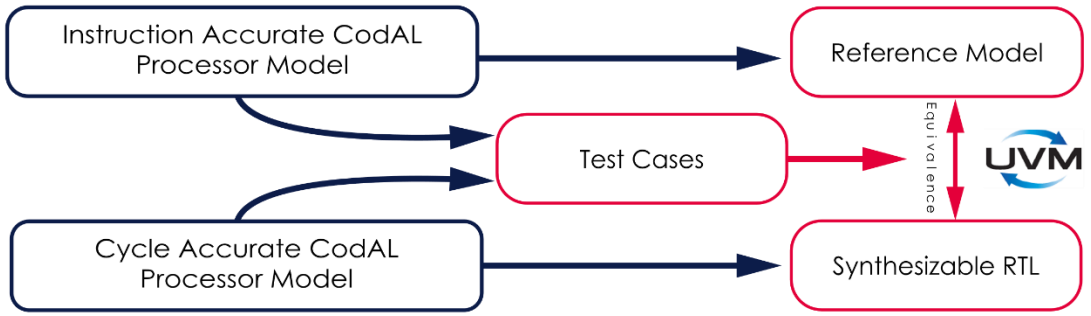
Strong methodology based on standardized approach, simulation, and static formal analysis

Consistency checker

Random assembler program generator

UVM verification environment

- Environment in SystemVerilog generated automatically by Codasip Studio
- Checks that RTL corresponds to specification



Conclusion

- Rich offering of RISC-V processors
  - Low power embedded
  - High performance embedded
  - Application
- Application RISC-V processors in the multiprocessor configuration
- Optional P Extension
- Fully verified solution
- Advanced configurability and customizability of IPs
- Based on powerful and reliable technology Codasip Studio
- Reduced time, cost, and effort
- Easy-to-integrate results

Now, it's your turn!

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