

# Codasip

GRANT AGREEMENT # 881172

Deliverables Reporting

Work package 6 – Improve visibility across EU and Asia-Pacific

Deliverable number ref 6.8, Contribute to Design Solution Forum in Japan with a presentation in Japanese

Date: 16.02.2021

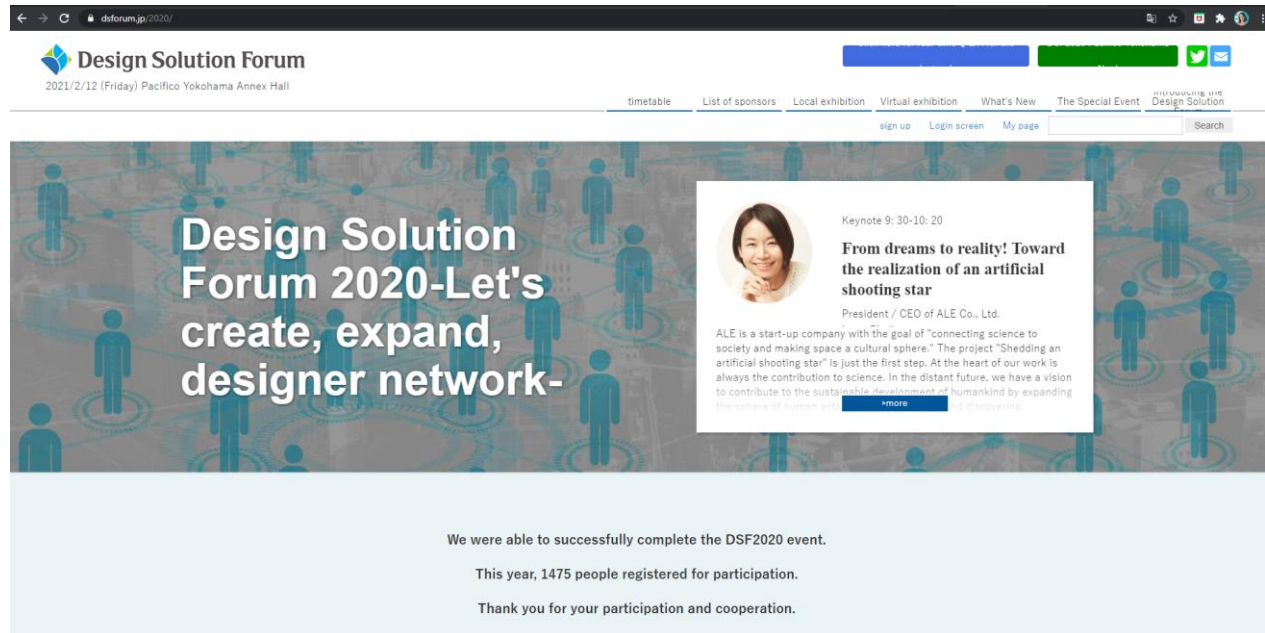
Responsible Person: Roddy Urquhart, Senior Marketing Director



This project is co-funded by the  
Horizon 2020 Programme of the  
European Union

Design Solution Forum was finally held on 2021/02/12

On behalf of Codalasip: **Zdenek Prikryl** / CTO; 2021/02/12; 13:10 JST (Japan Standard Time)



## Timetable:

ランチ休憩 11:50-12:30					
<b>12:30-13:00</b> <b>H-04</b> <b>IoTセキュリティの今とこれから</b> <b>オンデマンド配信</b> <small>サイバーセキュリティ株式会社 IoT技術本部 奥本 彰彦 岸田 茂樹 氏</small>	<b>12:30-13:00</b> <b>H-05</b> <b>業界No.1の検証IPベンダーが、RISC-V 5G 8K 向けにデザインIPを大躍進に拡大し、更に自動車向けにISO26262対応予定</b> <b>オンデマンド配信</b> <small>株式会社エヌ・エス・システム 技術本部 部長 守田 直樹 氏</small>	<b>12:30-13:00</b> <b>H-06</b> <b>自律型IoT実用に向けた取り組みのご紹介 ~ CO2センサーを活用した3要素システム実用に向けて ~</b> <b>オンデマンド配信</b> <small>CMエンジニアリング株式会社 ビジネス開発部 部長 鈴木 英志 氏</small>	<b>12:30-13:00</b> <b>H-07</b> <b>RISC-Vの完全性検証の実現</b> <b>オンデマンド配信</b> <small>日本電子システム・ソリューションズ株式会社 AEシステム部 堀川 淳一 氏</small>	<b>12:30-13:00</b> <b>H-08</b> <b>ゲートウェイを越す！今こそ、高品質設計と検証へ移行する時だ！</b> <b>オンデマンド配信</b> <small>インテリジェント・システム・ソリューションズ株式会社 TSS Cayago Japan / Senior Manager - Application Engineer 山本 修平 氏</small>	
<b>13:10-13:40</b> <b>H-09</b> <b>IoT, Automotive, AI等の要求を満たした適切なルート・オブ・トラストの選び方</b> <b>オンデマンド配信</b> <small>サムバックス株式会社 システムエンジニアリング部 廣野 力 氏</small>	<b>13:10-13:40</b> <b>H-10</b> <b>モデルベースデザインのFPGA/ASIC設計での成功・失敗例</b> <b>オンデマンド配信</b> <small>MathWorks Japan アプリケーションエンジニアリング部 プリンシパルアプリケーションエンジニア 松本 亮太 氏</small>	<b>13:10-13:40</b> <b>H-11</b> <b>「最先端エンジニアのための」WebRTCでつなげる映像エッジAI</b> <b>オンデマンド配信</b> <small>EDGE MATRIX株式会社 専務取締役 佐藤 博康 氏</small>	<b>13:10-13:40</b> <b>H-12</b> <b>カスタマイズ可能！AIアクセラレータジェネレータNgenを大躍進！</b> <b>オンデマンド配信</b> <small>ユニコム・システム・ソリューションズ株式会社 IoTサービス・ソリューション部 アーテック・開発部 山野 昭信 氏 東京大学 大学院情報理工学系研究科 コンピュータ科学専攻 准教授 斎藤 博 氏</small>	<b>13:10-13:40</b> <b>H-13</b> <b>A1チップ設計拠点 - パラダイムシフトの時代 -</b> <b>オンデマンド配信</b> <small>富士通株式会社 システム・ソリューション部 山本 昭彦 氏</small>	<b>13:10-13:40</b> <b>H-14</b> <b>Codalasip Customizable RISC-V Application Processors</b> <b>オンデマンド配信</b> <small>Codalasip s.r.o. Chief Technology Officer Dr. Zdenek Prikryl 氏 (でんぞく・ぷりくりー)</small>
<b>13:50-14:20</b> <b>H-15</b> <b>IoT, Automotive, AI等の要求を満たした適切なルート・オブ・トラストの選び方</b> <b>オンデマンド配信</b> <small>サムバックス株式会社 システムエンジニアリング部 廣野 力 氏</small>	<b>13:50-14:20</b> <b>H-16</b> <b>C/C++で書かれたアプリケーションのIoT実装向け最適化と、高品質化に向けた最適化ツールの紹介</b> <b>オンデマンド配信</b> <small>Silence Japan 株式会社 Senior FAE 大崎 和幸 氏</small>	<b>13:50-14:20</b> <b>H-17</b> <b>自動車産業の検証環境 - モデルベース開発と半導体シミュレーションの協調検証 -</b> <b>オンデマンド配信</b> <small>メソテック・システム・ソリューションズ株式会社 Hardware Assisted Verification 安藤 幸徳 氏</small>	<b>13:50-14:20</b> <b>H-18</b> <b>次の10年に向けて~設立10年を越えた Yocto Project~</b> <b>オンデマンド配信</b> <small>ヨクト・プロジェクト・ジャパン株式会社 ソリューション部部長 サブディレクター / Yocto Project Ambassador 伊賀 孝雄 氏</small>	<b>13:50-14:20</b> <b>H-19</b> <b>継続的な開発と検証でコスト・デザイン・エンジニア向けIPコアとソフトウェア開発環境</b> <b>オンデマンド配信</b> <small>日本電子システム・ソリューションズ株式会社 システム・ソリューション部 田比野 一敏 氏</small>	
<b>14:30-15:00</b> <b>H-20</b> <b>集合体のセキュリティ機能ってなんだ？</b> <b>オンデマンド配信</b> <small>富士通株式会社 システム・ソリューション部 山本 昭彦 氏</small>	<b>14:30-15:00</b> <b>H-21</b> <b>エッジデバイスのためのFPGA低電力化技術 - 過去の研究事例から不揮発性スイッチFPGAまで -</b> <b>オンデマンド配信</b> <small>富士通株式会社 システム・ソリューション部 山本 昭彦 氏</small>	<b>14:30-15:00</b> <b>H-22</b> <b>今すぐ対策しなければ間に合わない！IoTセキュリティ標準解説</b> <b>オンデマンド配信</b> <small>一般社団法人セキュリティ・IoT・ネットワークフォーラム協議会 セキュリティ・IoT標準解説部 部長 奥野 大樹 氏</small>	<b>14:30-15:00</b> <b>H-23</b> <b>C2RTLフレームワークによる高品質システム設計検証環境</b> <b>オンデマンド配信</b> <small>富士通株式会社 システム・ソリューション部 田比野 一敏 氏</small>	<b>14:30-15:00</b> <b>H-24</b> <b>失敗に学ぶCMOSイメージセンサの設計</b> <b>オンデマンド配信</b> <small>Pixart Japan 株式会社 CTO 松本 和也 氏</small>	

ランデブー 11:50-12:30

<p><b>12:30-13:00</b></p> <p><b>SP-02</b></p> <p>If you don't do it now, you won't be in time to IoT security now and in the future</p> <p>On-demand delivery</p> <p>Cybertrust Co., Ltd. Deputy General Manager of IoT Technology Headquarters Mr. Shigeharu Kishida</p>	<p><b>12:30-13:00</b></p> <p><b>SP-03</b></p> <p>The industry's No. 1 verification IP vendor will significantly expand design IP for RISC-V, 5G, 8K, and will support ISO 26262 for automobiles.</p> <p>On-demand delivery</p> <p>Next Stream Co., Ltd. General Manager of Engineering Department Naoya Morita</p>	<p><b>12:30-13:00</b></p> <p><b>SP-04</b></p> <p>Introducing initiatives for the realization of autonomous IoT-Toward the realization of a three-cs forecast system that utilizes CO2 sensors</p> <p>On-demand delivery</p> <p>CVI Engineering Co., Ltd. General Manager of Business Development Department Suzuki Takeshi</p>	<p><b>12:30-13:00</b></p> <p><b>SP-05</b></p> <p>Realization of RISC-V integrity verification</p> <p>On-demand delivery</p> <p>Japan One Spin Solutions Co., Ltd. AI Manager Mr. Junichi Tachibana</p>	<p><b>12:30-13:00</b></p> <p><b>SP-06</b></p> <p>Don't miss your chance! Now is the time to move to high-level design &amp; verification!</p> <p>On-demand delivery</p> <p>Mentor Graphics Japan Co., Ltd. TSS Calypto Japan / Senior Manager - Application Engineers Shuaku Yamamoto</p>
<p><b>13:10-14:20</b></p> <p><b>SP-07</b></p> <p>How to choose an appropriate route of trust based on the requirements of IoT, Automotive, AI, etc.</p> <p>On-demand delivery</p> <p>Rambus Co., Ltd. Senior technical sales Mr. Riki Hoshino</p>	<p><b>13:10-14:20</b></p> <p><b>SP-08</b></p> <p>Success / failure examples in FPGA / ASIC design of model-based design</p> <p>On-demand delivery</p> <p>MathWorks Japan Application Engineering Department Principal Application Engineer Mr. Mitsufumi Matsumoto</p>	<p><b>13:10-14:20</b></p> <p><b>SP-09</b></p> <p>Video edge AI connected by WebRTC "for steady engineers"</p> <p>On-demand delivery</p> <p>EDGE MATRIX Co., Ltd. Managing Executive Officer Mr. Takanobu Sato</p>	<p><b>13:10-14:20</b></p> <p><b>SP-10</b></p> <p>Customizable AI big dissection of the AI accelerator generator NNGen!</p> <p>On-demand delivery</p> <p>Konica Minolta IoT Service IP Development Section Architecture Development Department Mr. Ryusuke Yamano University of Tokyo Associate Professor, Department of Computer Science, Graduate School of Information Science and</p>	<p><b>13:10-14:20</b></p> <p><b>SP-11</b></p> <p>AI Chip Design Center-In the Age of Paradigm Shift</p> <p>On-demand delivery</p> <p>National Institute of Advanced Industrial Science and Technology AI chip design base, NEDO business / director Mr. Kunio Uchiyama</p>
<p><b>13:50-14:20</b></p> <p><b>SP-12</b></p> <p>Parallelization of applications written in C / C++ for SW implementation and introduction of help &amp; optimization tools for high-level synthesis</p> <p>On-demand delivery</p> <p>Silevis Japan Co., Ltd. Senior FAE Mr. Kazuyasu Oshima</p>	<p><b>13:50-14:20</b></p> <p><b>SP-13</b></p> <p>Self-driving car verification environment-Cooperative verification of model-based development and semiconductor simulation</p> <p>On-demand delivery</p> <p>Mentor Graphics Japan Co., Ltd. Hardware Assisted Verification Mr. Yasuaki Ando</p>	<p><b>13:50-14:20</b></p> <p><b>SP-14</b></p> <p>For the next 10 years - Yocto Project*, which has reached its 10th anniversary ~</p> <p>On-demand delivery</p> <p>Linux Solutions Co., Ltd. Solution Management Department Technical Expert / Yocto Project Ambassador Mr. Tetsuya Ito</p>	<p><b>13:50-14:20</b></p> <p><b>SP-15</b></p> <p>Commit with continuous development and investment - IP core and software development environment for deep learning</p> <p>On-demand delivery</p> <p>Japan Shiva Co., Ltd. President and CEO Mr. Kazutaka Hirobe</p>	<p><b>13:50-14:20</b></p> <p><b>SP-16</b></p> <p>Codasip Customizable RISC-V Application Processors</p> <p>On-demand delivery</p> <p>Codasip sro Chief Technology Officer Dr. Zdenek Prikryl (Denek Purikuri)</p>
<p><b>14:30-15:00</b></p> <p><b>SP-17</b></p> <p>What is the security function of a multifunction device?</p> <p>On-demand delivery</p> <p>Kyocera Document Solutions Co., Ltd. Technology Headquarters Software 2 General Technical Development Office Engineering Mr. Masakazu Hoshi</p>	<p><b>14:30-15:00</b></p> <p><b>SP-18</b></p> <p>FPGA power reduction technology for edge devices - From past research cases to non-volatile switch FPGA ~</p> <p>On-demand delivery</p> <p>National Institute of Advanced Industrial Science and Technology Device Technology, Research Division Mr. Masakazu Hoshi</p>	<p><b>14:30-15:00</b></p> <p><b>SP-19</b></p> <p>If you don't take measures right now, you won't be in time! IoT Security Standard Explanation</p> <p>On-demand delivery</p> <p>General Incorporated Association Security IoT Platform Council Security Specification Review Subcommittee Chair</p>	<p><b>14:30-15:00</b></p> <p><b>SP-20</b></p> <p>High-level system design verification environment by C2RTL framework</p> <p>On-demand delivery</p> <p>Professo, Information and Communication Systems, Faculty of Engineering, Tokyo Institute of Technology New System Vision Research and Development Organization</p>	<p><b>14:30-15:00</b></p> <p><b>SP-21</b></p> <p>CMOS image sensor design learned from failure</p> <p>On-demand delivery</p> <p>PuMi Japan Co., Ltd. CTO Mr. Kazuya Yonemoto</p>

Design Solution Forum

2021/2/12 (Friday) Pacifico Yokohama Annex Hall

timetable List of sponsors Local exhibition Virtual exhibition What's New The Special Event

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### Codasip Customizable RISC-V Application Processors


Providing RISC-V processor IP and customization tools, Codasip, a leader in customized processor solutions, offers a wide range of microarchitectures to meet the demands of a variety of applications.

This time, we have also prepared a new IP product group that runs on Linux. Multiprocessor can be configured and includes P extension. We will show you how to efficiently achieve large performance improvements with little effort.

**On-demand delivery**


You must be logged in to watch the on-demand stream.

login sign up



Codasip sro  
Chief Technology Officer  
**Dr Zdenek Prikryl (Denek Purikuri)**

Research at the Brno University of Technology has created an epoch-making method for automatically generating hardware and software from a processor description language. As a CTO for the last 10 years, Codasip has been developing 16 / 32bit architecture for IoT, 32 / 64bit DSP dedicated architecture, Linux operation architecture, etc. with the processor development tool Codasip Studio.




**Codalip**  
 1 035 sledujících uživatelů  
 6d.


Design Solution Forum Japan coming up in two days! Postponed from June 2020, it will now enjoy a hybrid form: as a physical trade show at the Pacifico Yokohama Annex Hall combined with a virtual event. Our CTO **Zdeněk Přikryl** is going to present a video lecture on RISC-V (multi)processor customization, starting at 13:10 (track SPB-01): <https://lnkd.in/dt5knmw> If you are hungry for some industry buzz, mark this Friday in your calendar and sign up in time!




#event #virtual #presentation #Japan #technology #processors #semiconductor #industry

**Codalip Customizable RISC-V Application Processors**  
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Codalip and  
 Intel Technology Office  
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 14

 Líbí se
  Přidat komentář
  Sdílet

Presentation:



# Codasip Customizable RISC-V Application Processors

*Design Solution Forum 2021*

*February 2021*

*Zdenek Prikryl*

# Agenda

- Introduction
- Codasip RISC-V Application Processors
- P (DSP) Extension
- Multiprocessor solution
- Customization
- Conclusion



# Who is Codasip?

- Leading provider of **RISC-V processor IP** and processor **design automation tools**
- Company founded in 2014 in Brno, Czech Republic
  - Based on 10 years of university research on processor design automation
  - Founding member of the RISC-V Foundation, [www.riscv.org](http://www.riscv.org)
  - Introduced world's first licensable RISC-V processor IP in November 2015
  - Active member of several RISC-V TGs and open-source projects
- Company headquarters in Germany and R&D centers located in the Czech Republic and France
  - 90+ employees
  - Veterans in CPU and cache coherency solutions
  - Technology leader in processor design automation
  - Sales offices worldwide

# Codasip Solutions

## **codasip**

### RISC-V PROCESSORS

Our portfolio of RISC-V processor IP cores

- Low power embedded
- High performance embedded
- **Application processors**

## **codasip**

### STUDIO

Unique automation toolset for easy processor design or modification

- Make small optimizations to a proven processor IP, or
- Implement a unique processor solution using the same tools.



# Codasip RISC-V Processors

	Low Power Embedded <ul style="list-style-type: none"><li>32bit</li></ul>	High Performance Embedded <ul style="list-style-type: none"><li>32bit or 64bit</li></ul>		Application <ul style="list-style-type: none"><li>MMU</li><li>Supervisor privilege mode</li><li>Instruction + Data cache</li><li>Atomic instructions</li><li>FD instruction set</li></ul>		Additional Features
7 Series <ul style="list-style-type: none"><li>7-9 stage</li><li>IMC instruction set</li><li>32 registers</li><li>Branch predictor</li></ul>				A70X A70XP	A70X-MP A70XP-MP	Instruction + Data Cache or TCM
5 Series <ul style="list-style-type: none"><li>5-stage</li><li>IMC instruction set</li><li>32 registers</li><li>Branch predictor</li></ul>	L50 L50F	H50X H50XF	H50P H50FP H50XP H50XFP			PMP + PMA
3 Series <ul style="list-style-type: none"><li>3-4 stage</li><li>IMC instruction set</li><li>32 registers</li></ul>	L30 L30F	H30P H30FP				SP/DP FPU
1 Series <ul style="list-style-type: none"><li>3-stage</li><li>EMC instruction set</li><li>16 registers</li></ul>	L10					Customization Extension

# Common Features

- Available immediately
- All Codasip Processors are RISC-V compliant
  - Implement RISC-V privilege specification
  - Implement RISC-V debug specification
- All Customizable
- Pre-verified, tape-out quality IP
  - Users do not need to verify IP
- Industry-standard interfaces
  - AMBA for instruction and data bus
  - JTAG (4pin/2pin) for debugging

All Codasip RISC-V Processors are **available in many configurations** allowing our customers to choose the core which fits the best their needs.

All Codasip RISC-V Processors are **customizable** allowing our customers to add key differentiation points on ISA as well as micro-architecture level.

# Deliverables

## Hardware Development Kit (HDK)

- RTL (Verilog/VHDL/SystemVerilog)
- Verification report
- Integration test bench
- Sample EDA scripts

## Software Development Kit (SDK)

- C/C++ LLVM compiler (improved by Codasip)
- C/C++ Libraries (newlib)
- Assembler, disassembler, linker
- High-performance instruction set and cycle accurate simulators
- Debugger and profiler

+ CodeSpace (Eclipse based IDE)



# Application Class RISC-V Processors

- 7 pipeline stages, *mostly* in-order architecture
- Optimized for effective compute
- SV39 MMU
- Linux capable
- Four base ISAs
  - IMAC
  - IMACP
  - GC
  - GCP
- High performance FPU

OpenSBI v0.6



```
Platform Name      : Codasip
Platform HART Features : RV64ACDFIMSU
Platform Max HARTs  : 1
Current Hart       : 0
Firmware Base      : 0x80000000
Firmware Size      : 64 KB
Runtime SBI Version : 0.2
```

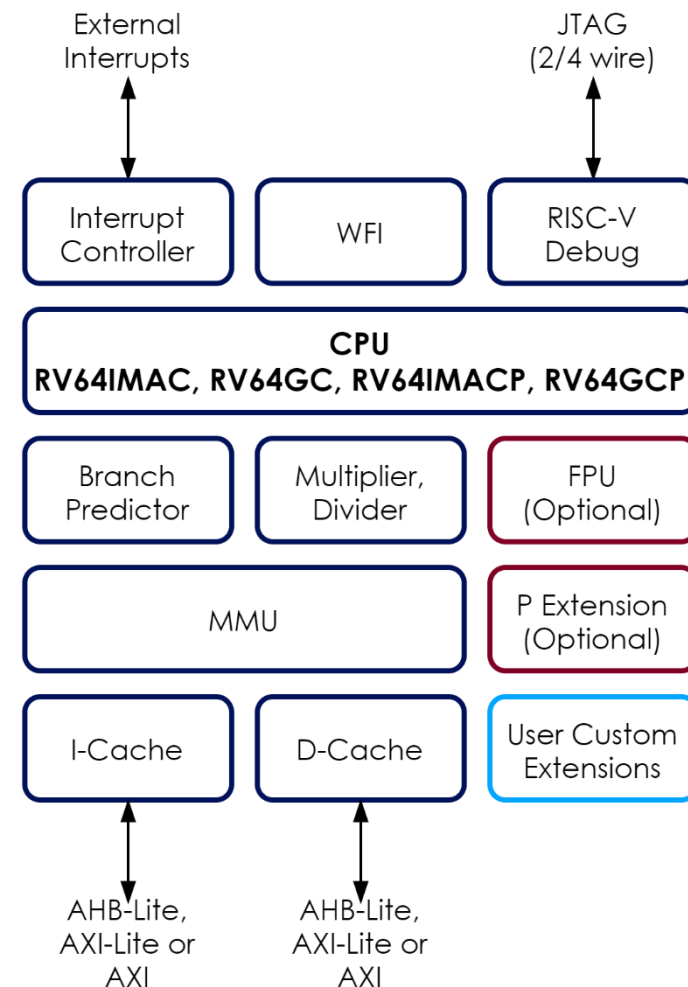
```
MIDELEG : 0x0000000000000222
```

```
MEDELEG : 0x000000000000b109
```

```
[ 0.000000] OF: fdt: No chosen node found, continuing without
[ 0.000000] OF: fdt: Ignoring memory range 0x80000000 - 0x80200000
[ 0.000000] Linux version 5.4.36 (codasip@build) (gcc version 9.2.0 (GCC)) #1
SMP Thu Sep 17 12:08:58 CEST 2020
[ 0.000000] initrd not found or empty - disabling initrd
[ 0.000000] Zone ranges:
[ 0.000000]   DMA32    [mem 0x0000000080200000-0x0000000081ffffff]
[ 0.000000]   Normal    empty
[ 0.000000] Movable zone start for each node
[ 0.000000] Early memory node ranges
[ 0.000000]   node 0: [mem 0x0000000080200000-0x0000000081ffffff]
[ 0.000000] Initmem setup node 0 [mem 0x0000000080200000-0x0000000081ffffff]
[ 0.000000] software IO TLB: Cannot allocate buffer
```

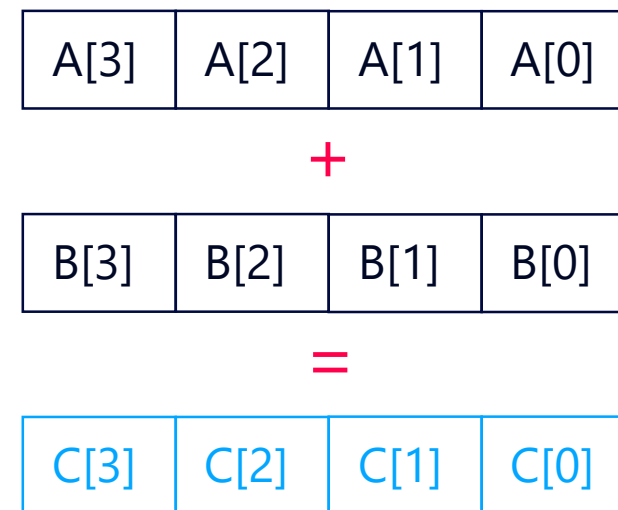
# Application Class RISC-V Processors

- Highly Configurable
  - Cache
  - Branch Predictor
  - ISA
  - JTAG or cJTAG
  - Single processor or multiprocessor
- Customizable
  - ISA
  - Microarchitecture
- Virtual prototypes
  - Functional
  - Cycle-accurate




## P Extension

- Single instruction, multiple data operations (SIMD) are used mostly to accelerate digital signal processing (DSP). This covers domains such as:
  - Audio encoding/decoding
  - Computer vision
  - Sensor fusion
  - Compact AI/ML applications on the edge
- P extension:
  - Works on the integer register file
  - Contains approximately 331 instructions split into groups
    - Can be enabled/disabled based on the configuration
  - Enables RISC-V processors run DSP applications with higher performance and lower power consumption.



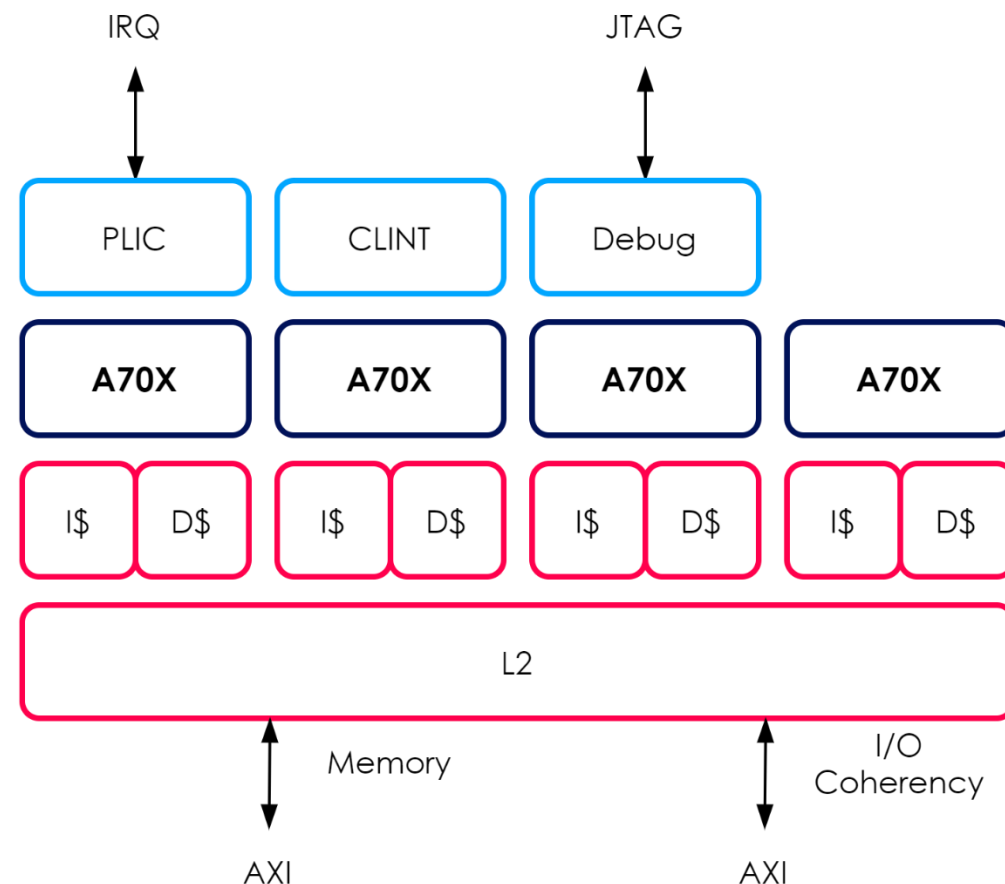
- GCC C compiler
  - Standard intrinsic/inline assembly approach
- LLVM C compiler
  - Standard intrinsic/inline assembly approach
  - **Plus C compiler**
    - C compiler does auto-vectorization and other advanced features

[illegible]



# Multiprocessor Solution – Overview

- Coda<sup>sip</sup> RISC-V application processors
  - Up to 4 cores
  - Coherent L1 and L2 caches scalable micro-architecture
  - AXI external interface followed by support of CHI protocol
  - I/O Coherency port
  - Optimized for efficient computing including streaming
  - Embeds data prefetchers at L1 and L2.
  - Per core and cluster power domain.
- **Verified and qualified with ideal and real-life downstream IPs.**



# Multiprocessor Solution – Configuration Options

	Configuration parameters
Number of cores	1, 2, 3, 4
L1 Size	32kB, 64kB
L2 Size	128kB - 8MB (increments of power of 2)
Number of ways L1 / L2	4, 8, 16
Cache line size	32B, 64B
Error protection	L1 & L2, L2 only, Disabled
Internal resources sizing for PPA tradeoffs	Configurable (Optimized for performance or area)
Master interface	AXI4 (or CHI in Q4'21) 64b width, 128b width
I/O Coherency port	Optional

## Availabilities:

- Intra-cluster coherency AXI master
  - Preview / early evaluation - Q1 2021
  - Production ready - Q2-2021
- Full system coherency CHI based
  - Production ready - Q4-2021

# Not Found The Processor You Were Looking For?

RISC-V **open-source instruction set** architecture was designed for **customizations**

- Differentiate your product while keeping the ecosystem benefits
- Optimize the ISA to achieve better PPA
- Use any existing Codasip RISC-V Processor as a **baseline** for your customization
- Customize any RISC-V processor yourself using **Codasip Studio!**

Codasip Studio **automates** customization

- Design space exploration
- **Generates** SDK using custom ISA
  - Compiler, assembler & linker
  - Debugger & profiler
  - Instruction set simulator (ISS)
- Corresponding HDK is also **generated**
  - RTL
  - Testbench
  - UVM environment

# What is Cudasip Studio?

A unique collection of tools for **fast & easy modification** of RISC-V processors.

**All-in-one**, highly automated. Introduced in 2014, **silicon-proven** by major vendors.

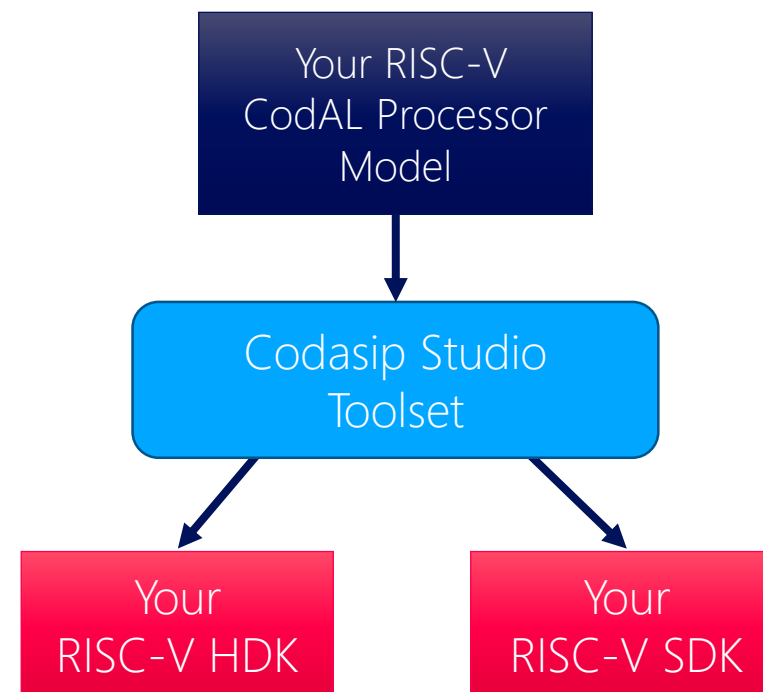
Processor described in **high-level** architecture description language

Allows customization of:

- Instruction set architecture (ISA)
- Micro-architecture

Users may choose to:

- **Modify** an existing Cudasip RISC-V Processor
- **Design** new processor from scratch



# CodAL™

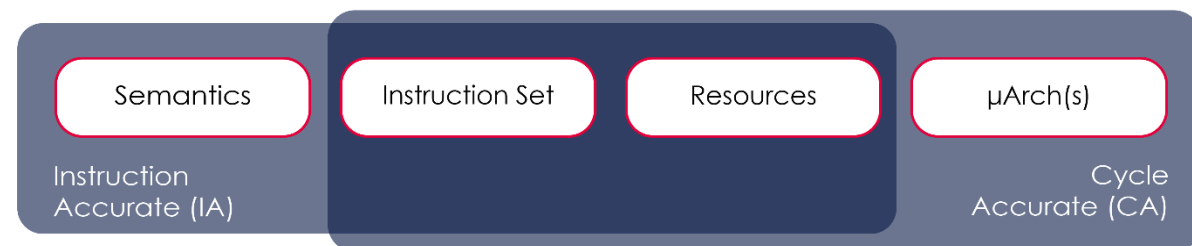
Easy-to-understand **C-like language** that models a rich set of processor capabilities

All Cudasip processors are created and verified using CodAL

**Multiple microarchitectures** can be implemented in a single CodAL model

CodAL models are provided to Cudasip IP customers as **a starting point** for their processor optimizations and modifications

## CodAL Description



```

/*      Multiply and accumulate: semantics
        dst += src1 * src2
*/

element i_mac {
    use reg as dst, src1, src2;
    assembly { "mac" dst "," src1 "," src2 };
    binary { OP_MAC:8 dst src1 src2 0:9 };
    semantics {
        rf[dst] += rf[src1] * rf[src2];
    };
};

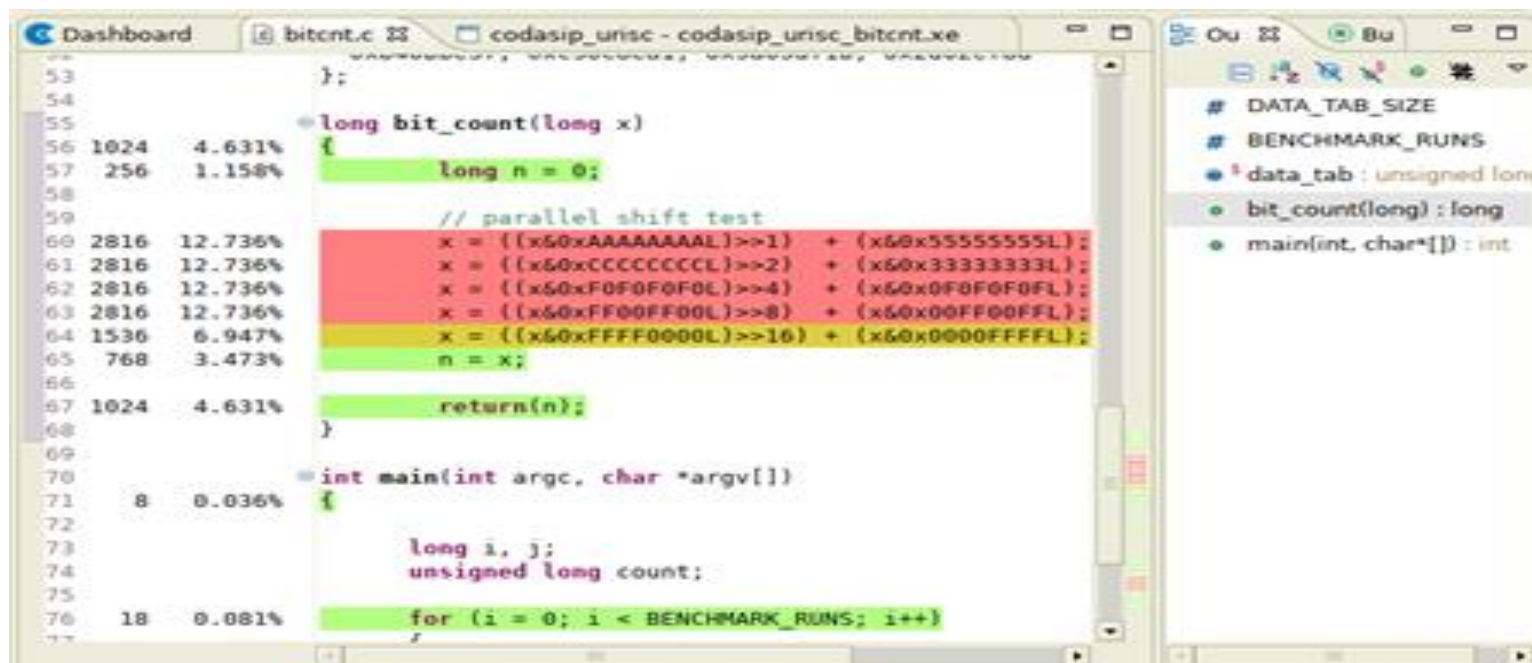
```

# Design Space Exploration

**Profiling** of embedded software detects possibilities for processor optimization

ISA extensions are quickly implemented which allows **analysis** of their impact

Cudasip Studio automatically generates all processor IP design kits and verifies for RISC-V compliance (you still need to verify your own resources and instructions)



Line	Count	Percentage	Code Snippet
53			};
54			
55			long bit_count(long x)
56	1024	4.631%	{
57	256	1.158%	long n = 0;
58			
59			// parallel shift test
60	2816	12.736%	x = ((x&0xAAAAAAAA)>>1) + (x&0x55555555L);
61	2816	12.736%	x = ((x&0xCCCCCCCC)>>2) + (x&0x33333333L);
62	2816	12.736%	x = ((x&0xF0F0F0F0L)>>4) + (x&0x0F0F0F0FL);
63	2816	12.736%	x = ((x&0xFF00FF00L)>>8) + (x&0x00FF00FFL);
64	1536	6.947%	x = ((x&0xFFFF0000L)>>16) + (x&0x0000FFFFL);
65	768	3.473%	n = x;
66			
67	1024	4.631%	return(n);
68			}
69			
70			int main(int argc, char *argv[])
71	8	0.036%	{
72			
73			long i, j;
74			unsigned long count;
75			
76	18	0.081%	for (i = 0; i < BENCHMARK_RUNS; i++)
77			{

# Processor IP Verification

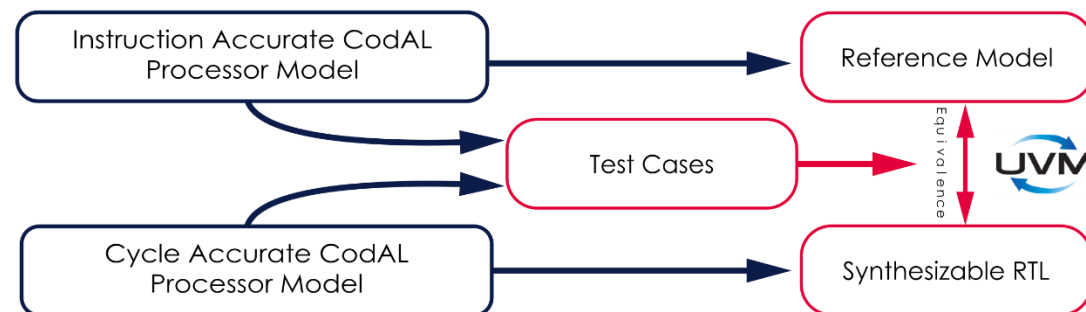
**Strong methodology** based on standardized approach, simulation, and static formal analysis

Consistency checker

Random assembler program generator

## **UVM verification environment**

- Environment in SystemVerilog generated automatically by Codasip Studio
- Checks that RTL corresponds to specification





# Conclusion

- Rich offering of RISC-V processors
  - Low power embedded
  - High performance embedded
  - Application
- Application RISC-V processors in the multiprocessor configuration
- Optional P Extension
- Fully verified solution
- Advanced configurability and customizability of IPs
- Based on powerful and reliable technology Cudasip Studio
- Reduced time, cost, and effort
- Easy-to-integrate results



Now, it's your turn!