**Tên đề tài :**

-       **Tiếng Việt: Tối ưu hóa truyền dữ liệu trong các hệ thống máy học nhúng cho các ứng dụng IoT**

-       **Tiếng Anh:****Optimization of Data Mobility in Embedded Machine Learning Systems for IoT Applications**

Mô tả đề tài:

RISC-V is an open-source hardware instruction set (ISA) architecture based on the reduced instruction set computer (RISC) architecture. Having a simple base architecture helps prevent fragmentation while also supporting customization. Many companies are taking advantage of RISC-V to create custom processors designed to handle the power and performance requirements of newer workloads for (artificial intelligence) AI, (machine learning) ML, (Internet of Things) IoT, and (virtual reality) VR/(augmented reality) AR applications.

In this project, the optimization of data mobility between CPU, ML engine, and memory is studied to improve the performance of the whole embedded systems for IoT applications.

Nhiệm vụ (yêu cầu về nội dung và số liệu ban đầu):

·       Study RISC-V architecture.

[RISC processors](https://en.wikipedia.org/wiki/Reduced_instruction_set_computer) - short for Reduced Instruction Set Computer

·       Study about ML related works on EdgeAI and RISC-V.

·       Study solutions to improve the data mobility between CPU, ML engine, and memory.

·       Implement ML core with the optimization of data mobility on RISC-V edge devices..

·       Experiment with several datasets for IoT applications

Tài liệu tham khảo: <https://riscv.org/> and other documents provided by the supervisors