1. Define the following terms using 1-3 sentences or a formula.
    a. Moore's Law

Moore's law says that the number of transistors that can be packed into a given unit of space (chip) would double every two years.

    b. Stored program computer

In a stored program computer, programs or instructions are represented in a manner suitable for electronically storing in memory alongside the data. The computer gets its instructions by reading them from memory, and a program can be set or modified by setting the values of a portion of memory.

    c. Amdahl's law

A program with parallel processing , a relatively few instruction s that have to be performed in sequence will have a limiting factor on program speedup such that adding more processor s may not make the program run faster.

    d. Instruction Set Architecture (ISA)

ISA, or simply architecture: the abstract interface between hardware and the lowest level of software that encompasses all the information necessary to write a machine language program, including instructions, registers, memory access, IO,

    e. Computer architecture

In computer engineering, **computer architecture** is a set of rules and methods that describe the functionality, organization, and implementation of computer systems

2. Write the range using 8 bits for:
    a. Unsigned integers 0 - ((2^8) -1) 0-255
    b. Signed integers (2^7) – ((2^7)-1) -128-127

Unsigned 0 - 2^n -1 n = given bits
Signed -(2^n-1) - ((2^n-1)-1)

3. Describe the steps that transform a program written in a high-level language such as C into a representation that is directly executed by a computer processor.

The use of **compiler** to reads the high-level source code and translates it into a program in **assembly** language. The use of **assembler** to transforms the **program** in assembly language into a **program** in machine language as it is the language that computer understands can work with. The compiler translates code written in a **high** level language to a lower level language, object/machine code by creating an **executable program** that converts from a high level language into machine language or simply do it directly without a **middleman**.

4. [Given the following 64-bit number, what is the most significant bit's value?
1000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000

2^64-1 if unsigned

5. Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.
    a. Which processor has the highest performance expressed in instructions per second?
    P1 = 3/1.5 = 2 * 10^9 instructions per second
    P2 = 2.5 / 1.0 = 2.5 * 10^ 9 instructions per second
    P3 = 4 / 2.2 = 1.82 * 10^9 instructions per second
    P2 is best.

    b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.
    Cycles:
    P1: 3GHz * 10 = 3 * 10^10 cycles

P2: 2.5GHz * 10 = 2.5 * 10^10 cycles
P3: 4GHz * 10 = 4 * 10^10 cycles
Num of instructions:
P1: 3GHz * 10 / 1.5 = 2 * 10^10 instructions
P2: 2.5GHz * 10 / 1.0 = 2.5 * 10^10 instructions
P3: 4GHz * 10 / 2.2 = 1.82 * 10^10 instructions

c. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

Execution time = (Num of instructions * CPI) / (Clock rate)
So if we want to reduce the execution time by 30%, and CPI increases by 20%, we have:
Execution time * 0.7 = (Num of instructions * CPI * 1.2) / (New Clock rate)
New Clock rate = Clock rate * 1.2 / 0.7 = 1.71 * Clock rate
New Clock rate for each processor:
P1: 3GHz * 1.71 = 5.13 GHz
P2: 2.5GHz * 1.71 = 4.27 GHz
P3: 4GHz * 1.71 = 6.84 GHz

6. True or False: Sign and magnitude representation and two's complement representation are used about equally in modern computers.

   False, largely two's complement is in all computers for signed computers.

7. What is the decimal value of this 64-bit two's complement number?

$$11111111\ 11111111\ 11111111\ 11111111\ 11111111\ 11111111\ 11111111\ 11111100_{\text{two}}$$

two's complement to decimal → flip all bits 1→0 and 0→1, add 1.
decimal to two's complement → flip all bits 1→0 and 0→1, add 1.
Answer is -4

8. What is 8-bit Two's complement representation for following numbers?
   i. -3_{10}
   ii. -9_{10}

3 = 00000011
flip
11111100
add 1
11111101
-3 in decimal
9 = 00001001
flip
11110110
add 1
11110111
-9 in Decimal

9. Convert the following binary into base 10
   a. 1110.1011 → 14.6875
   b. 11001111.0111 → 207.4375

10. What is the decimal value of the following 16-bit Twos complement number:
    a. 1111 1111 1111 1000

Flip
0000 0000 0000 0111
Add 1
0000 0000 0000 1000
-8 in decimal

    b. 1000 0000 0000 1111

Flip
0111 1111 1111 0000
Add
0111 1111 1111 0001
-32783 in decimal

11. Convert the following binary into hexadecimal (no calculator allowed for this problem)
    a. 1111 0010
       F2
    b. 1111 0011
       F3

Hexa	0	1	2	3	4	5	6	7
Binary	0000	0001	0010	0011	0100	0101	0110	0111

Hexa	8	9	A	B	C	D	E	F
Binary	1000	1001	1010	1011	1100	1101	1110	1111

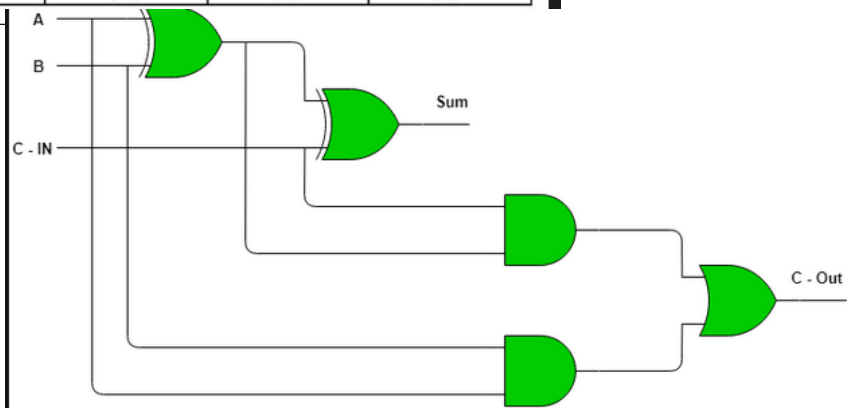
12. Write the logical left shift and arithmetic right shift by one bit for the following:
    a. 1000 1111
       Logical Left Shift 0001 1110
       Arithmetic Right Shift 1100 0111
    b. 1111 0001
       Logical Left Shift 1110 0010
       Arithmetic Right Shift 1111 1000
13. Write the truth table and draw the digital circuit using logic gates for the 1-bit full adder

Inputs			Outputs	
A	B	C – IN	Sum	C - Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$S = A.B.cin + A.\bar{B}.\overline{cin} + \bar{A}.B.\overline{cin} + \bar{A}.\bar{B}\,cin$

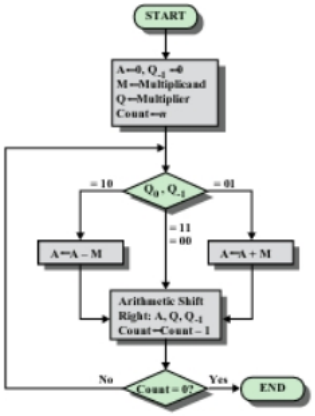
And Or

$C_{out} = A.B + A.cin + B.cin$



14. Compute using booths algorithm 8x-6(use 5 bits to represent the numbers). Please show all the steps

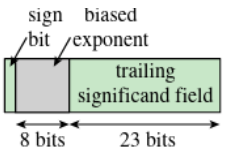
- Bits of the multiplier are scanned one at a a time (the current bit Q_0)
- As bit is examined the bit to the right is considered also (the previous bit Q_{-1})
- Then:
  - 00: Middle of a string of 0s, so no arithmetic operation.
  - 01: End of a string of 1s, so add the multiplicand to the left half of the product (A).
  - 10: Beginning of a string of 1s, so subtract the multiplicand from the left half of the product (A).
  - 11: Middle of a string of 1s, so no arithmetic operation.
- Then shift A, Q, bit Q_{-1} right one bit using an arithmetic right shift
- In an **arithmetic shift, the msb remains unchanged**



A	Q	Q_{-1}	M	Log
0000	1010	0	1000	Populate Data
0000	0101	0	1000	Shift
1000	0101	0	1000	A = A - M
1100	0010	1	1000	Shift
0100	0010	1	1000	A = A + M
0010	0001	0	1000	Shift
1010	0001	0	1000	A = A - M
1101	0000	1	1000	Shift

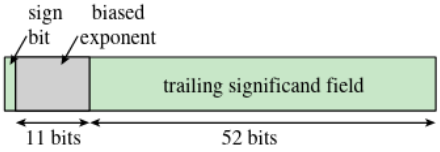
15. Compute using booths algorithm 3x-3(use 4 bits to represent the numbers). Please show all the steps

A	Q	Q_{-1}	M	Log
000	101	0	011	Populate Data
101	101	0	011	A = A - M
110	110	1	011	Shift
001	110	1	011	A = A + M
000	111	0	011	Shift
101	111	0	011	A = A - M
110	111	1	011	Shift



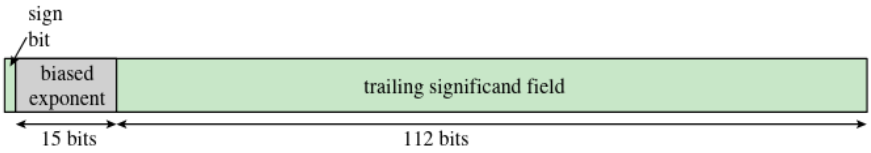
Single-precision

(a) binary32 format



double-precision

(b) binary64 format



extended-precision

(c) binary128 format

Sign bit: Exponent signficand
0 = + decimal value – 127 = exponent iimplied 1.0000
1 = -

16. Write the normalized form for the following
    a. 10000.111

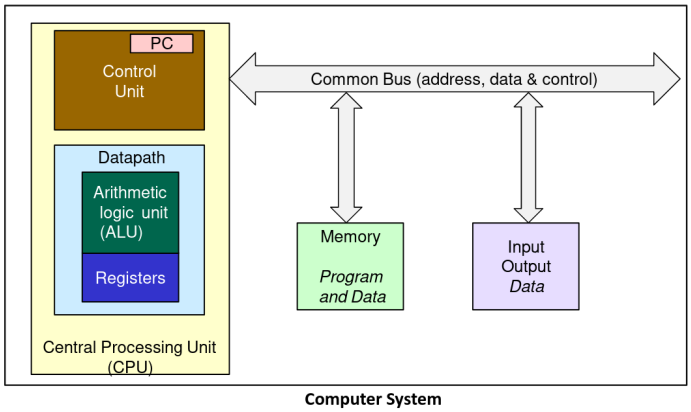
       1.0000111 * 2^4

    b. 0.0000 1010 1111

       1.0101111 * 2^-5

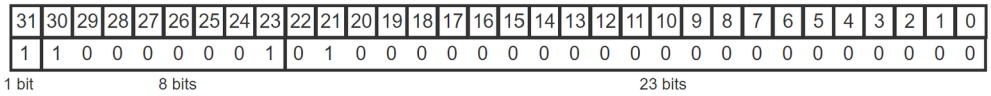
17. Let AAAA0000 be a floating-point number in IEEE 32-bit floating expressed in hexadecimal. What is the decimal value of the number?
    -1.3281250 * 10^-42

18. Show the IEEE 754 binary representation of the number -0.75_{10} in 32-bit format.
    .75 * 2 = 1.5 → 1
    .5 * 2 = 1 → 1
    .11 → 1.1 * 2^-1
    E = 126 = 01111111
    M = 1
    1 01111110 10000000000000000000000
    sign exponent mantissa



Computer System

19. What decimal number is represented by the following 32 bit IEEE format?



exponent = 129
exponent = 129 – 127 = 2

number will be negative due to sign bit.
Mantissa = .25

-1.25 *2^2
-1.25 * 4 = -5

Examples:
Clock time. If clock frequency is 900MHz, calculate the cycle time (1 point).
Cycle time = 1/f = 1/900 MHz = 1.11 GHz

Clock Speed. A program runs in 15 seconds on Computer A, which has a clock frequency of 600 MHz. We are trying to help a computer designer build a new machine B, that will run this program in 6 seconds. One thing the designer can do is increase the clock frequency which will affect the CPU design causing machine B to require 1.5 times as many clock cycles as machine A for the same program. What clock rate should we tell the computer designer to target?
Given information:
Computer A: 15 sec and frequency = 600 MHz
Computer B: 6 sec and frequency =Y
If computer A takes X cycles, the computer B will take 1.5X cycles.
Program A runs for 15 sec= X/600 MHz ---------1)
Program B runs for 6 = 1.5X/Y ----------2)
Dividing 1) by 2)
15/6= X/600 MHz /1.5X/Y
15/6 = Y/900 MHz
13500/6=Y
Y = 2250 MHz or2.25 GHz