

Four-Stage Audio Amplifier

Under the Course: Electronics Workshop 2

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Abstract—The objective of this project is to design and implement a Four-stage audio amplifier as part of the Electronics Workshop 2 course. The aim is to analyze the amplification process through multiple stages, optimize signal quality, and ensure efficient power handling. This study focuses on understanding the working principles of different amplifier stages, their frequency response, and their role in audio signal processing. The project also emphasizes practical circuit implementation, measurement, and characterization of key performance parameters such as gain, distortion, and efficiency.

I. INTRODUCTION

Audio amplifiers are essential in signal processing, enhancing weak audio signals to drive output devices such as speakers and headphones. This project focuses on designing and implementing a **Four-stage audio amplifier** to study its performance across multiple amplification stages. The amplifier is designed using *LTSpice simulations* and is later tested through *hardware implementation* to validate its efficiency, gain, and frequency response.

Each stage of the amplifier serves a specific function:

- 1) **Preamplifier Stage** – Amplifies low-level signals from an audio source while minimizing noise.
- 2) **Gain Stage** – Further increases signal amplitude while maintaining linearity and minimizing distortion.
- 3) **Filter Stage** – Removes unwanted frequency components and optimizes signal clarity.
- 4) **Power Amplifier Stage** – Provides high power output suitable for driving loudspeakers.
- **Final Circuit Implementation** – Integrates all stages and evaluates real-world performance.

The project involves comprehensive analysis through LTSpice simulations, practical hardware implementation, and performance evaluation. Key parameters such as **gain, distortion, power efficiency, and signal clarity** are measured to optimize the circuit. Additionally, challenges faced during the design and implementation process are documented to ensure a thorough understanding of amplifier performance in real-world scenarios.

II. AIM

The aim of the project is to build an audio amplifier with the following specifications:

- 1) **Supply Voltage:** 0 to 5 V
- 2) **Input small signal voltage:** 10–40 mV peak-to-peak
- 3) **Gain:** $G_1 \times G_2 \geq 500$ (Preamplifier and Gain stage)
- 4) **Frequency:** Audible Range (20 Hz to 20 kHz)
- 5) **Power:** ≥ 1.5 W
- 6) **Filter:** should not attenuate the input signal
- 7) **Power Amplifier:** should not provide voltage gain
- 8) **Load:** 10Ω

III. PRE-AMP

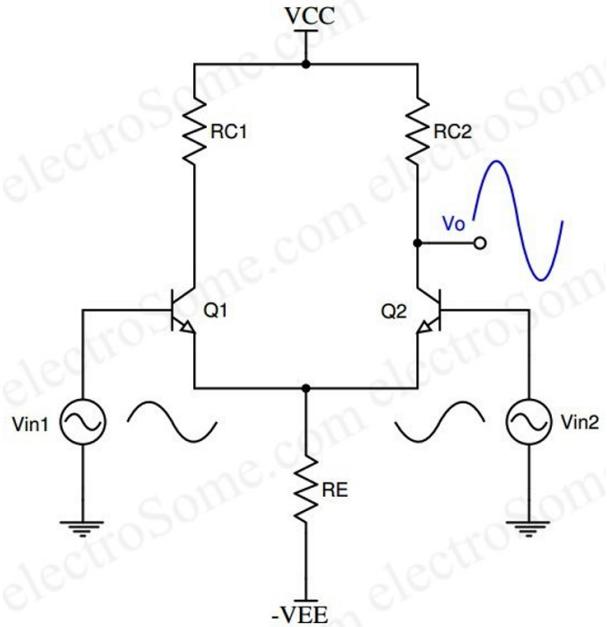


Fig. 1. Pre-Amplifier

A. Pre-Amplifier Stage

- The pre-amp stage is required for initial amplification.
- Ideally, the input resistance should not be low as this will cause the amplifier to draw high current, which the microphone cannot supply, leading to ineffective operation of the amplifier.

- For this reason, the common-emitter differential amplifier can be used as it has a high input and output impedance, with good noise performance.
- If the noise performance of a pre-amp is bad, the already weak signal ($10mV - 40mV$) could be completely overpowered by noise.
- In summation, the pre-amp's main purpose is to provide initial amplification to the signal to send it to the gain stage, while also preventing noise from entering the system.

B. Operation of the Differential Amplifier

- For proper operation, the two NPN BJTs must be in active mode (i.e., Base-Emitter junction in forward bias, Base-Collector junction in reverse bias).
- The input can be applied to either transistor's base with the choice of either grounding the other transistor's base or applying an equal and opposite input to the other transistor's base (effectively twice amplification).
- In this case, a resistor (R_e) is used instead of an independent current source and $I_{e1} + I_{e2}$ is the current that flows through it.

C. Small Signal Analysis

- The bias current values were obtained by the above method, and these were used in the small signal analysis of the circuit.
- To find input resistance, the output must be grounded and a test voltage should be given at the output. The ratio of the input voltage to input current (test) is the input resistance.
- To find output resistance, the differential inputs are grounded and a test voltage is to be given at the output.

D. Common Mode Rejection Ratio (CMRR)

- The CMRR is calculated by supplying a common mode signal to the differential amplifier and measuring common mode gain (A_c) and by supplying another differential mode signal to the differential amplifier and measuring the differential gain (A_d).

Then, the CMRR is found using:

$$CMRR = 20 \log \left(\frac{A_d}{A_c} \right)$$

E. Derivations

$$V_{CC} - I_C R_C = V_C$$

$$5 - I_C (9000) = V_C$$

$$V_{BE} = V_B - V_E = -V_E$$

$$V_E - I_E R_E = V_{EE}$$

$$V_{EE} - I_E R_E = -V_{BE}$$

$$I_C = \frac{\beta}{\beta + 1} I_E$$

Substituting values, we'd get:

$$I_C \approx 0.1mA$$

$$gain = g_m R_C = \frac{I_C R_C}{V_T}$$

- Substituting, we'll get theoretical gain as **72.48**.

F. LTSpice Simulation

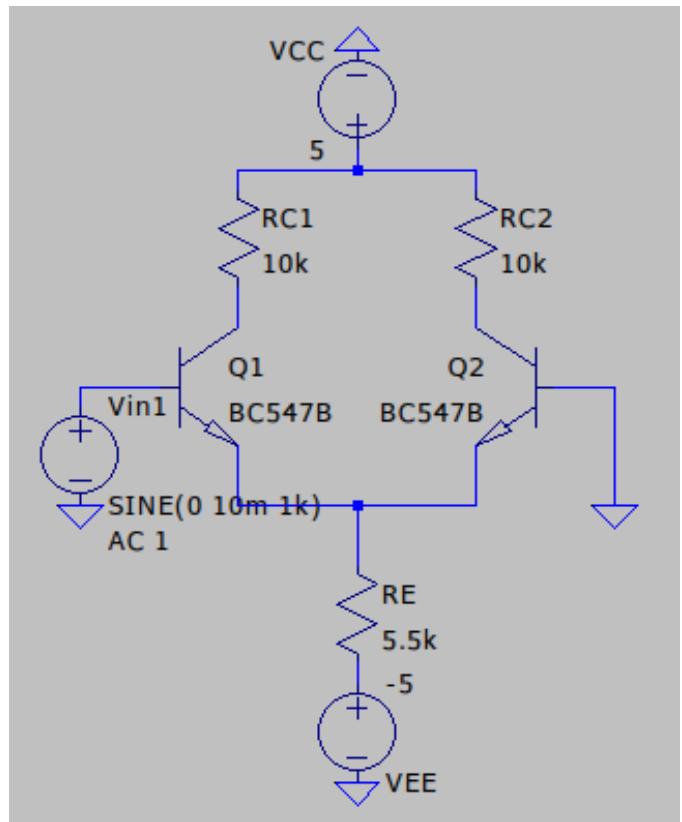


Fig. 2. LTSpice Schematic of the Pre-Amplifier



Fig. 3. LTSpice Output of the Pre-Amplifier

- The gain observed from the schematic was 29.3.

G. Hardware

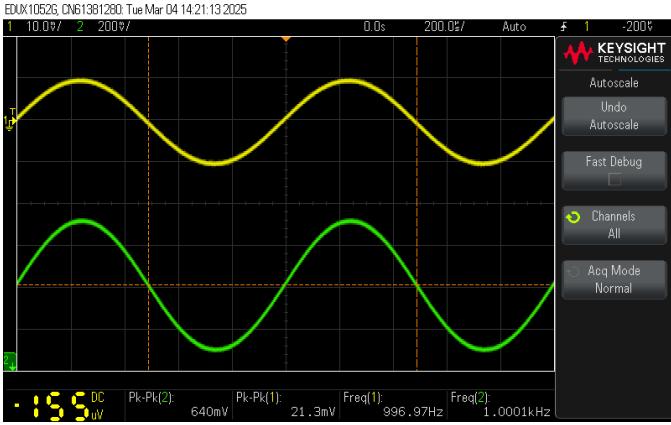


Fig. 4. Oscilloscope Output of the Pre-Amplifier

- The gain observed through hardware implementation came out to be 30.42.

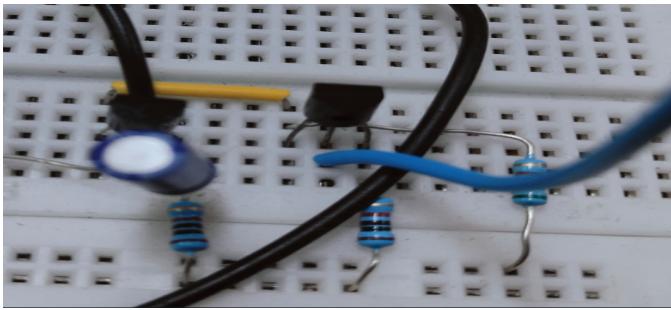


Fig. 5. Hardware Implementation of the Pre-Amplifier

IV. GAIN STAGE

- For this stage, we used a BJT based CE amplifier as it has low input impedance and high output impedance.

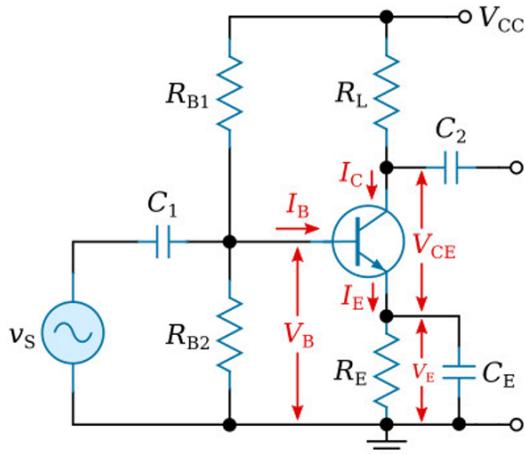


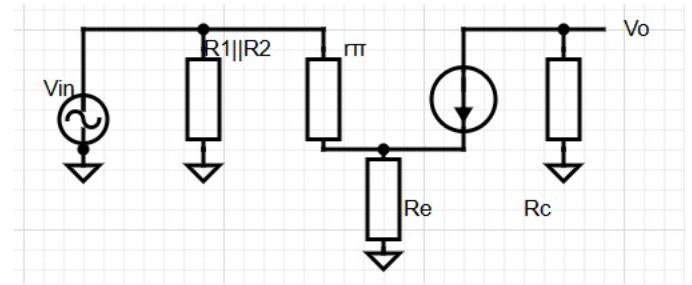
Fig. 6. Gain Stage

A. Capacitors and Biasing Components

- The input capacitor C_1 serves to block the DC components of the input signal V_s and contributes a pole to the system.
- In this case, the frequency lies between 20Hz and 20kHz , so C_1 needs to be set such that it allows everything below 20kHz to pass.
- Additionally, if C_1 is too small, the low-frequency components of the input will be lost, and it will allow more current to pass, causing a larger I_B , which will decrease the current gain.
- C_E serves to block DC current flowing to ground.
- C_2 provides the second pole to the system and provides AC coupling to the filtering stage.
- R_{B1} and R_{B2} are bias resistors, which form a voltage divider with respect to V_{CC} . This is used to bias the transistor (Base-emitter junction in forward bias and Base-Collector junction in negative bias).

B. Derivation of Circuit Components

- Plotting I_C in LTSpice, we got $I_C = 0.527\text{mA}$.



- Using small signal analysis, deriving gain for the CE amplifier:

$$\begin{aligned}
 v_o &= -g_m v_{be} R_C \\
 \frac{v_{be}}{r_\pi} - \frac{v_i - v_{be}}{R_E} + g_m v_{be} &= 0 \\
 \frac{v_i}{R_E} &= v_{be}(r_\pi^{-1} + R_E^{-1} + g_m) \\
 \frac{v_o}{v_i} &= \frac{-g_m v_{be} R_C}{v_{be} R_E (r_\pi^{-1} + R_E^{-1} + g_m)} \\
 \frac{v_o}{v_i} &= -\frac{g_m R_C}{R_E} (r_\pi^{-1} + R_E^{-1} + g_m)^{-1} \\
 &= 0.268 \left(\frac{1}{13.2 \times 10^3} + \frac{527 \times 10^{-6}}{26 \times 10^{-3}} + \frac{527 \times 10^{-6}}{0.026 \times 250} \right)^{-1} \\
 \therefore \text{gain} &= 13.21
 \end{aligned}$$

- So, we're getting a theoretical gain of 13.21.
- Note that, we've taken $\beta = 250$ using the datasheet for the transistor model.

C. LTSpice simulation

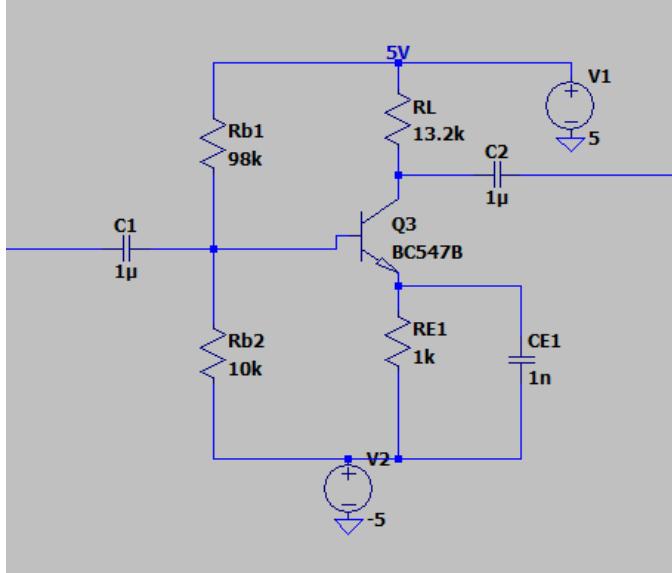


Fig. 7. LTSpice Schematic of the Gain Stage



Fig. 8. LTSpice Output of the Gain Stage

- The gain observed from the schematic was 13.62.
- This matches closely with the theoretical gain as calculated previously.

D. Hardware

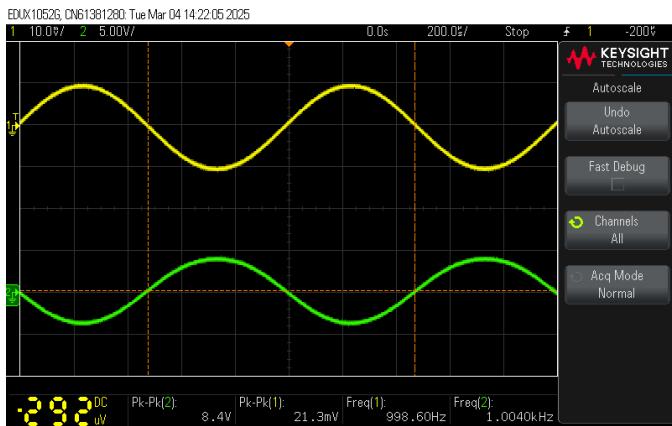


Fig. 9. Oscilloscope Output of the Gain Stage

- The gain is observed to be 13.81 with an output peak-to-peak of 8.4V, indicating an amplification of 420.

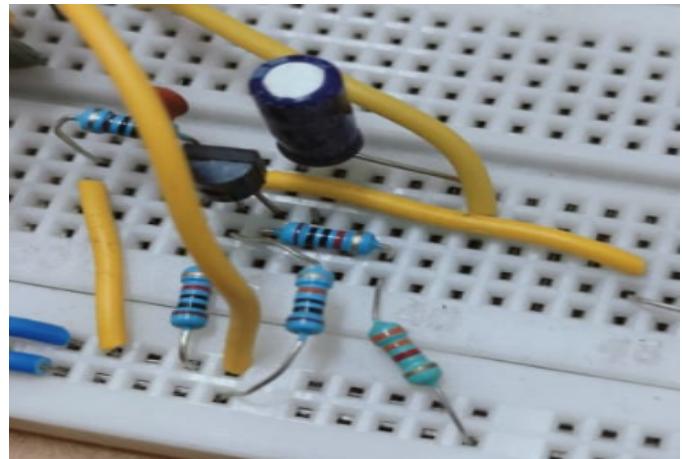


Fig. 10. Hardware Implementation of the Gain Stage

V. FILTER STAGE

A. Basics

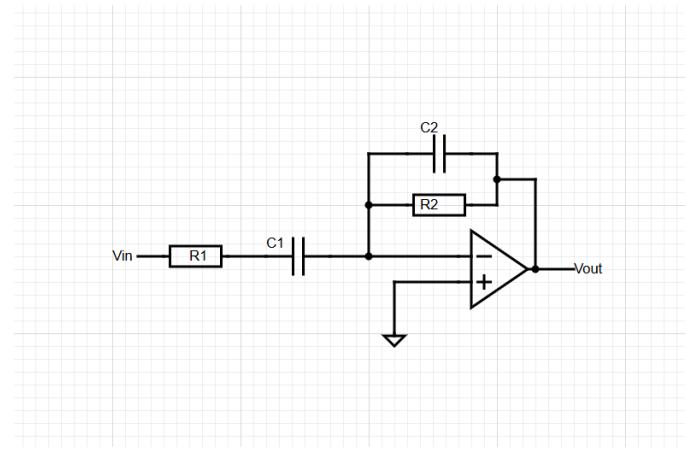


Fig. 11. Circuit Diagram

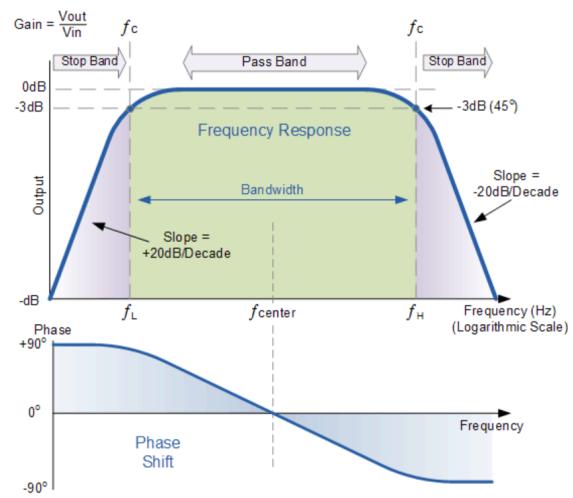


Fig. 12. Frequency Response of Active Bandpass Filter

B. Derivations

- The transfer function of the active bandpass filter is given by:

$$\frac{V_o}{V_{in}} = \frac{sC_1R_2}{(1 + sC_1R_1)(1 + sC_2R_2)} \quad (1)$$

where:

- R_1, R_2 are resistances
- C_1, C_2 are capacitances
- $s = j\omega$ is the complex frequency variable

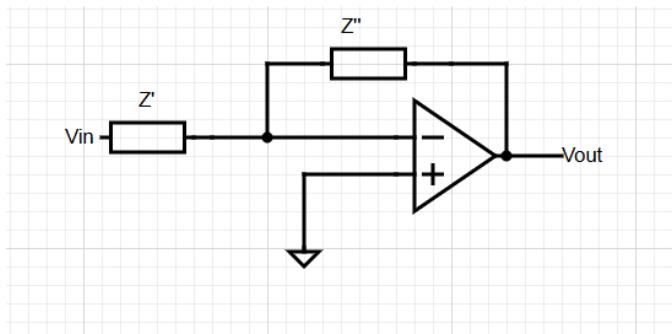


Fig. 13. Circuit Diagram with Impedances

C. Poles and Cutoff Frequencies

- The poles are given by:

$$\omega_{p1} = \frac{1}{R_1 C_1}, \quad \omega_{p2} = \frac{1}{R_2 C_2} \quad (2)$$

- These correspond to the lower and upper cutoff frequencies as below:

$$f_{c1} = \frac{1}{2\pi R_1 C_1}, \quad f_{c2} = \frac{1}{2\pi R_2 C_2} \quad (3)$$

- For a broadband band-pass filter with a frequency range of 20 Hz to 20 kHz, we impose:

$$f_{c1} = 20 \text{ Hz}, \quad f_{c2} = 20 \text{ kHz} \quad (4)$$

1) Gain Calculations:

- The gain of the circuit is given by:

$$\text{Gain} = \frac{V_{out}}{V_{in}} = \frac{Z''}{Z'} \quad (5)$$

- Here,

$$Z' = R_1 + \frac{1}{sC_1}, \quad Z'' = \frac{1}{\left(\frac{1}{R_2} + sC_2\right)} \quad (6)$$

$$\therefore \frac{V_{out}}{V_{in}} = -\frac{Z''}{Z'} \quad (7)$$

- For a unity gain filter, we set:

$$A_v = \frac{R_2}{R_1} = 1 \Rightarrow R_2 = R_1 \quad (8)$$

D. Design Considerations

- For proper filtering conditions:

$$R_1 \gg \frac{1}{C_1}, \quad \frac{1}{C_2} \gg R_2 \quad (9)$$

- This simplifies to

$$R_1 + \frac{1}{sC_1} \approx R_1, \quad R_2 \parallel \frac{1}{sC_2} \approx R_2 \quad (10)$$

Here, we choose $R_1 = R_2 = 800\text{k}\Omega$. Using Equation (3), we find $C_1 = 12\text{nF}$ and $C_2 = 12\text{pF}$.

Thus, the circuit satisfies the bandpass filtering condition with specified gain and frequency response.

E. LTSpice Simulation

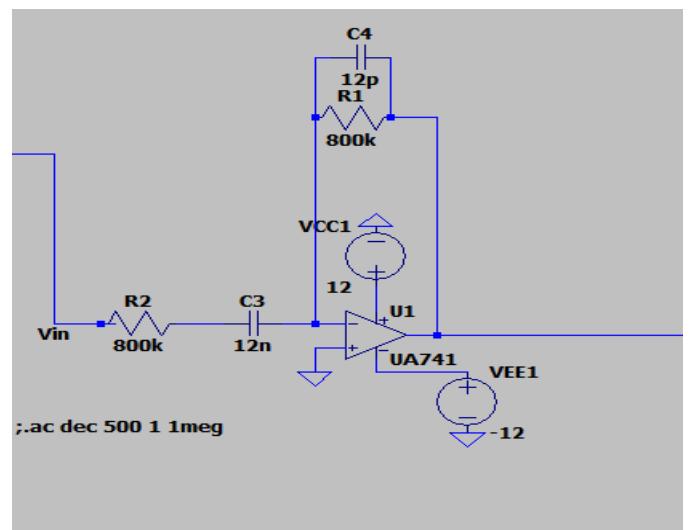


Fig. 14. LTSpice Schematic of the Filter

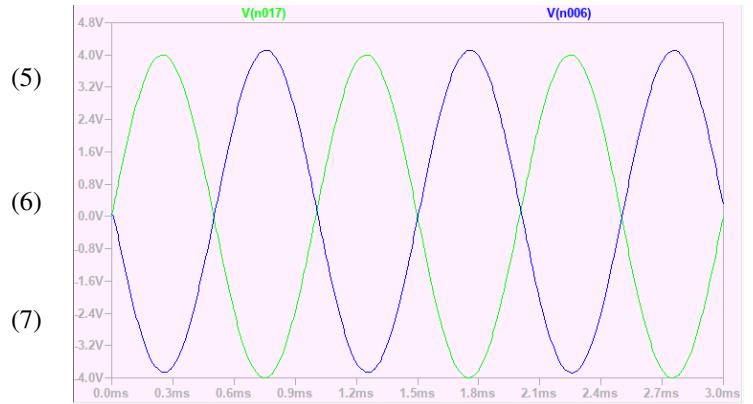


Fig. 15. LTSpice Output of the Filter

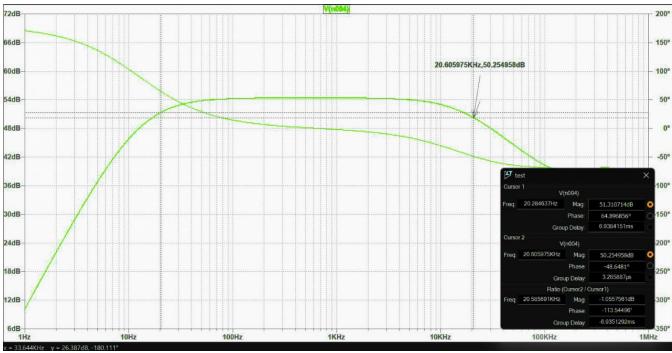


Fig. 16. LTSpice AC Analysis of the Filter

It allows frequencies in the range 20-20KHz to pass through.

F. Hardware



Fig. 17. Oscilloscope Output of the Filter

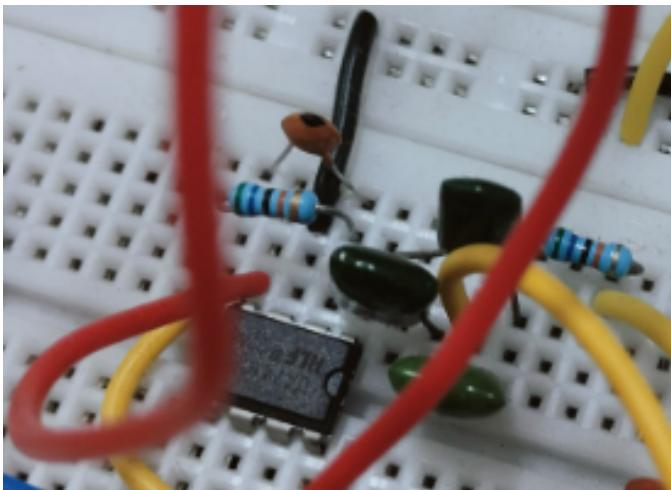


Fig. 18. Hardware Implementation of the Filter

VI. POWER AMPLIFIER

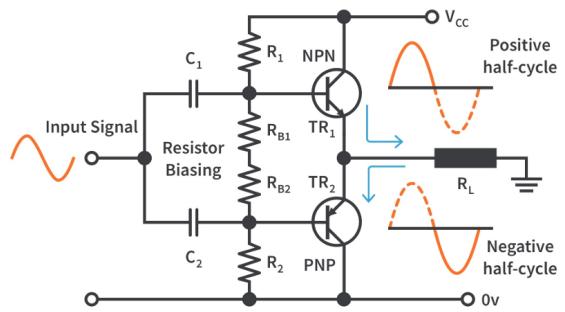


Fig. 19. AB Amplifier

A. Transistor Biasing and Components Function

- The function of R_1 , R_{B1} , R_{B2} , and R_2 is to bias the bases of the transistors to put them in the appropriate regions of operation in the positive and negative cycles of the input.
- For the NPN transistor to conduct, the Base-Emitter junction must be in forward bias and the Base-Collector junction must be in reverse bias.
- The opposite is true for PNP transistors.
- For this, we used two diodes with the ideal bias voltages of 0.7V in series in order to assure that the above operating conditions for the transistors are satisfied throughout the working of the circuit.
- R_1 and R_2 must be equal, and the separation of R_{B1} and R_{B2} has been done to show symmetry in the configuration.
- Note that, instead of R_{B1} and R_{B2} , we've used 1N4148 diodes for biasing.
- C_1 and C_2 are used to minimize the base current for both transistors, which will increase the current gain, further increasing the power gain.
- Additionally, no gain was desired, which was achieved by setting the bias resistances aptly.

B. Advantages of Class-AB Amplifiers over Class-A and Class-B Amplifiers

- Higher Efficiency:** Class AB amplifiers are more efficient than Class A amplifiers because they reduce the power dissipation by allowing both transistors to conduct for slightly less than half the input cycle.
- Reduced Crossover Distortion:** Unlike Class B amplifiers, which suffer from crossover distortion due to the non-conduction region between the two transistors, Class AB amplifiers eliminate this issue by maintaining a small bias current to keep both transistors slightly conducting at all times.
- Balanced Performance:** Class AB amplifiers provide a trade-off between the low distortion of Class A and the high efficiency of Class B, making them suitable for audio applications.

applications where both quality and power efficiency are important.

- **Better Thermal Stability:** The biasing in Class AB reduces the excessive heat dissipation problems found in Class A amplifiers, improving thermal efficiency and stability.
- **Improved Linearity:** Class AB amplifiers offer better linearity compared to Class B, ensuring higher fidelity in signal amplification.

C. LTSpice Simulation

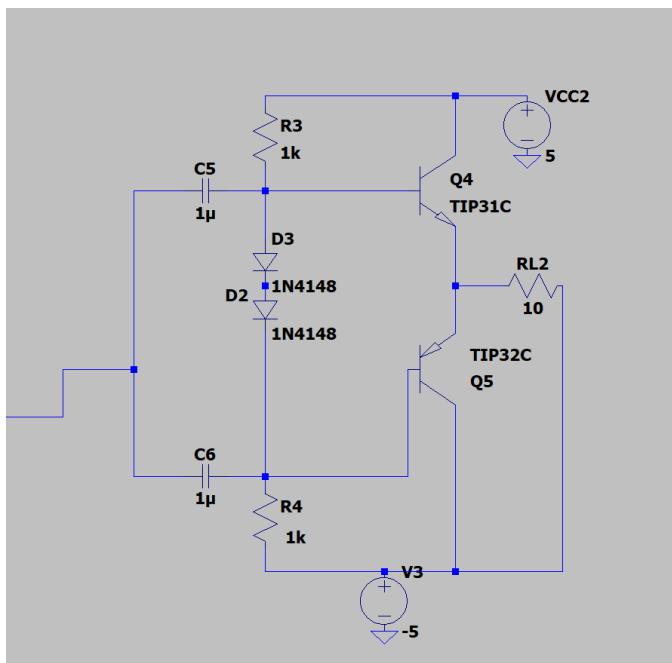


Fig. 20. LTSpice Schematic of the Power Amplifier



Fig. 21. LTSpice Output of the Power Amplifier

The voltage gain observed was 1, confirming unity gain functioning of the power amplifier.

D. Hardware

Issues faced: During the simulation of the power amplifier, several challenges were encountered:

1) Biasing Issues:

- Incorrect selection of biasing resistors led to **transistor saturation or cutoff**, preventing proper operation.
- Adjustments were made to ensure the **transistors operate in the active region***, improving signal fidelity.

2) Thermal Runaway Concerns:

- High power dissipation in transistors caused **thermal runaway**, which could lead to failure.
- **Thermal stability techniques** such as **negative feedback and heat sinks** were explored to mitigate this issue.

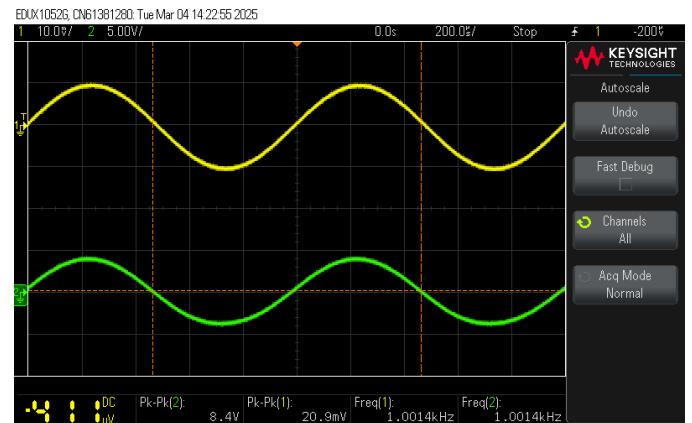


Fig. 22. Oscilloscope Output of the Power Amplifier

The output is 8.4V i.e the voltage gain is 1 as desired and the current is increased.

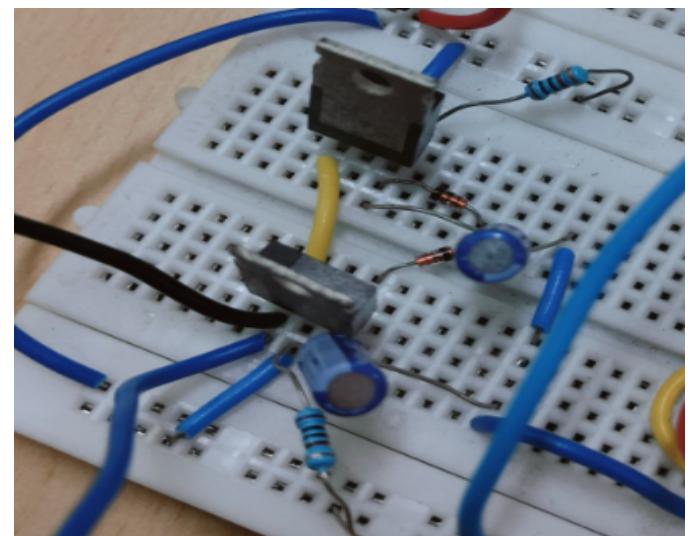


Fig. 23. Hardware Implementation of the Power Amplifier

VII. FINAL CIRCUIT

A. LTSpice Simulation

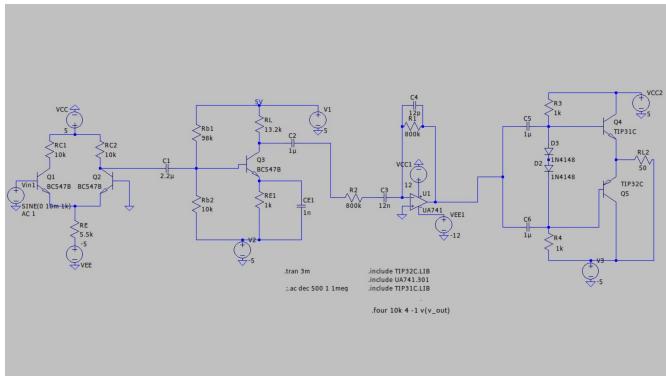


Fig. 24. LTSpice Schematic of the Complete Circuit

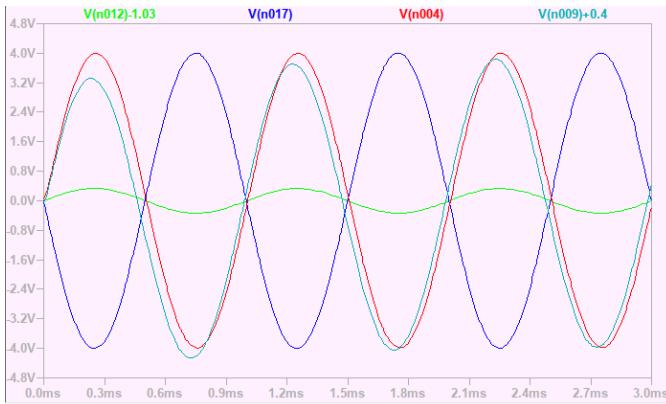


Fig. 25. LTSpice Output of the Complete Circuit

B. Hardware

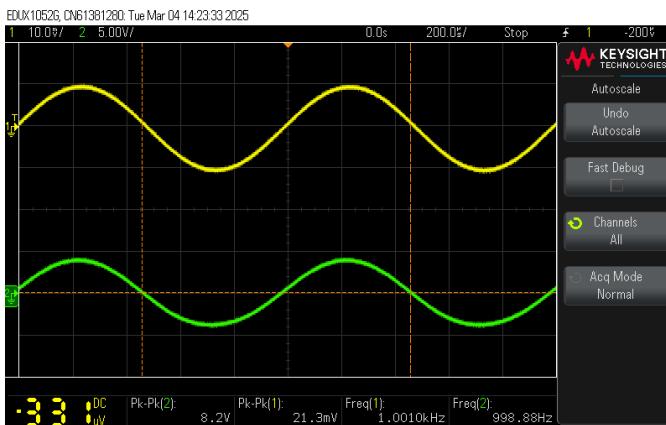


Fig. 26. Final Oscilloscope Transient Output



Fig. 27. Oscilloscope Frequency Response Analysis- Lower Limit

- The voltage gain is seen to be 1. It allows signals in the frequency range 121.2Hz-31.62kHz to pass through.



Fig. 28. Oscilloscope Frequency Response Analysis- Upper Limit

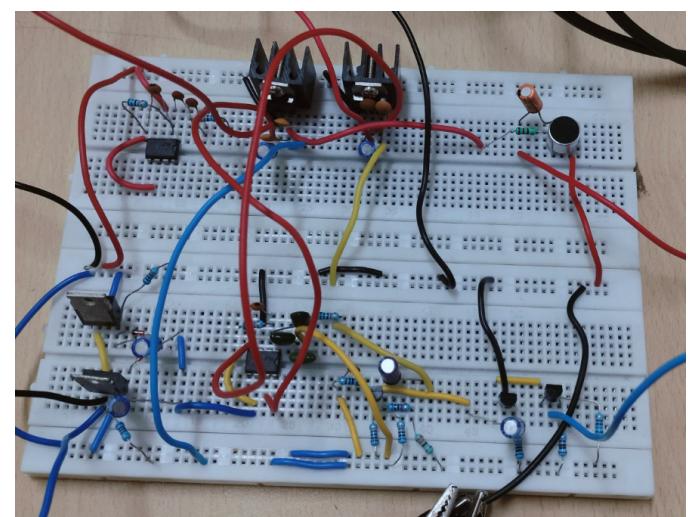


Fig. 29. Hardware Implementation of the Audio Amplifier

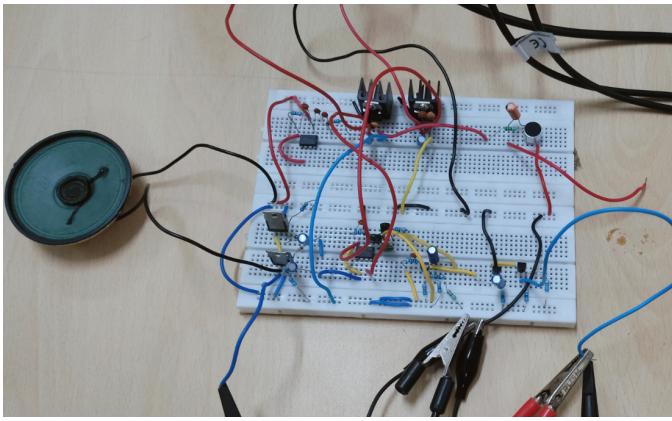


Fig. 30. Hardware Implementation of the Audio Amplifier with Speaker

C. Other Subcircuits Used

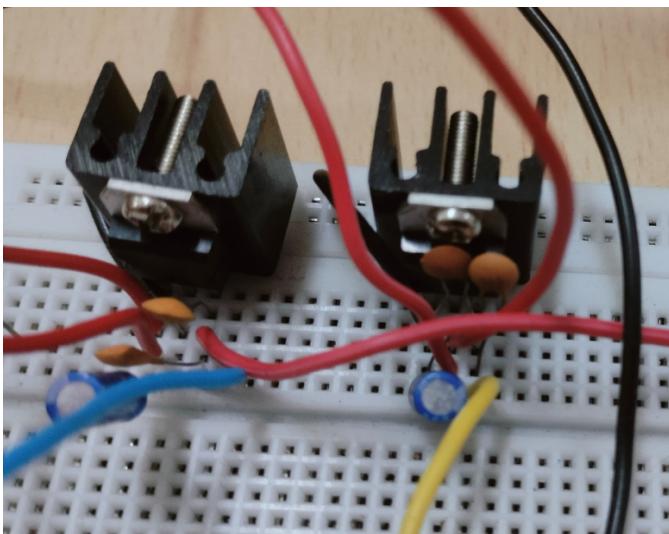


Fig. 31. Hardware Implementation of the Voltage Divider

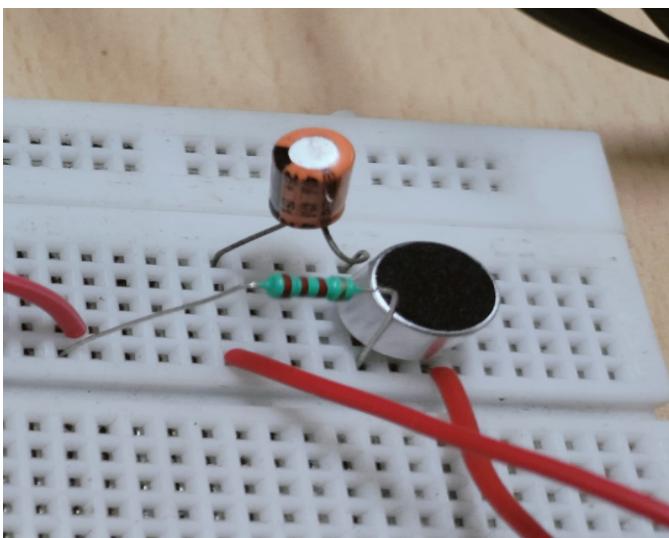


Fig. 32. Hardware Implementation of the Microphone Circuit

D. Videos Showcasing the Working of the Audio Amplifier

- Audio Amplifier Frequency Response Analysis
- Audio Amplifier Demonstration with a Song

VIII. OTHER CALCULATIONS

A. Total Harmonic Distortion (THD)

Distortion Analysis is done to figure out the amount of unwanted harmonic content in the frequency content of a signal. It can further elaborate on the behaviour of the circuit at different frequencies.

- The main formula used was -

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_{n_RMS}^2}}{V_{f_RMS}} \quad (11)$$

where:

- THD is the total harmonic distortion present in the signal.
- V_{n_RMS} is the RMS voltage of the n^{th} harmonic.
- V_{f_RMS} is the RMS voltage of the fundamental frequency.
- The voltages can be found using the FFT of a sine signal in the *wavegen*, which can be plugged into the formula accordingly.
- Here's our THD Analysis:

```

SPICE Error Log: C:\Users\Ritama\Downloads\ckt\ckt\test.log
Circuit: * C:\Users\Ritama\Downloads\ckt\ckt\test.asc
WARNING: Node N015 is floating.

Direct Newton iteration for .op point succeeded.
N-Period=all
Fourier components of V(v_out)
DC component:-1.67502

Harmonic    Frequency    Fourier    Normalized    Phase    Normalized
Number      [Hz]        Component   Component [degree]  Phase [deg]
1          1.000e+04    3.309e+00    1.000e+00    -28.48°    0.00°
2          2.000e+04    7.473e-02    2.258e-02    -126.15°   -97.67°
3          3.000e+04    2.612e-02    7.894e-03    -31.70°    -3.22°
4          4.000e+04    1.466e-02    4.431e-03    42.65°    71.12°
Total Harmonic Distortion: 2.433083%(4.069856%)

Date: Thu Mar 20 23:27:24 2025
Total elapsed time: 0.174 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 5259
traniter = 5246
tranpoints = 2010
accept = 1568
rejected = 442
matrix size = 70
fillins = 55

```

- We ended up getting a theoretical Total Harmonic Distortion of 2.43%, which is acceptable for audio amplifiers as some distortion is expected.
- THD could have been improved by minimizing the circuit interference and by adding filters to shut down higher unwanted harmonic currents in the system.

B. Slew Rate

Slew Rate is defined as the maximum rate of change of output voltage per unit time. It is an important parameter in amplifiers and other electronic circuits, particularly in high-frequency applications.

$$S.R. = \max \left(\frac{dV_{\text{out}}}{dt} \right)$$

- An ideal amplifier should have an infinitely high slew rate so that it can faithfully reproduce even high-frequency signals without distortion. However, practical circuits have limitations due to capacitances and current-driving capabilities, which restrict the maximum achievable slew rate. If the slew rate is not high enough, the circuit may fail to track rapid changes in the input signal, resulting in distortion.
- The slew rate can be increased by:
 - Raising the maximum operating voltage.
 - Reducing the capacitive impedances in the circuit.
 - Optimizing the biasing and compensation techniques in amplifiers.
- For a sinusoidal signal, the slew rate can be approximated as:

$$S = 2\pi f_m V_m$$

where:

- S is the slew rate,
- f_m is the maximum frequency of the signal,
- V_m is the peak voltage amplitude.
- If $V_m = 15mV$ and f varies based on input audio, the slew rate will depend on the input frequency.

IX. PROBLEMS FACED

- 1) In the gain stage, we had to carefully adjust the load resistor (R_L) to ensure the circuit operated within the $\pm 5V$ supply voltage constraint. Improper values led to clipping, as the transistor was leaving the biasing zones.
- 2) While designing the bandpass filter, we observed that the theoretical cutoff frequencies did not exactly align with the hardware tolerances. To ensure the full 20Hz–20kHz audio range passed without attenuation, we slightly increased the upper cutoff frequency.
- 3) After assembling the power amplifier, we noticed that the TIP31C and TIP32C transistors overheated much sooner than expected. The excessive heat buildup made us frequently switch off the power supply. To deal with this, we used heat sinks to improve thermal dissipation.
- 4) While testing the speaker, we were required to use a small microphone for verification. However, we encountered multiple faulty microphones, which introduced inconsistencies in our testing and delayed progress. Despite these challenges, we managed to source a reliable mic and complete the circuit on time.

X. ACKNOWLEDGEMENTS

We would like to express our sincere gratitude to:

- **Professor Spandan Roy** for his valuable guidance and insightful feedback throughout the project.
- **Professor Arti Yardi** for her support and expertise in circuit design and analysis.
- **Professor K Madhava Krishna** for his mentorship and encouragement in tackling technical challenges.
- The **Teaching Assistants** for their continuous assistance in troubleshooting and refining the implementation.

XI. REFERENCES

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- Neso Academy – Introduction to Amplifiers (YouTube Video): https://www.youtube.com/watch?v=Qwd-5H24tRo&ab_channel=NesoAcademy
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