

# Harikrishnan R

rharikrishnan95@gmail.com | +91 7774054512 | me@illustris.tech

## EDUCATION

### BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI, GOA CAMPUS

B.E. (HONS.) ELECTRONICS & ELECTRICAL ENGINEERING  
Grad. Aug 2018 | Goa, India  
CGPA: 6.59

### KENDRIYA VIDYALAYA, PATTOM

CBSE | 12TH GRADE  
Grad. May 2013 | Trivandrum, India  
Percentage : 89%

## LINKS

[github.com/illustris](https://github.com/illustris)  
[linkedin.com/in/illustris](https://www.linkedin.com/in/illustris)

## COURSEWORK

### COMPLETED

Mobile Telecom Networks • Analog Electronics • Power Electronics • Power Systems • Microprocessor and Interfacing • Computer Architecture • Cryptography • Digital Design • Control Systems • Data Communication Networks • Microelectronics • Computer Programming • Analog and Digital VLSI Design • Communication Systems • Realtime Systems • Digital Signal Processing • Software dev for portable devices

## ACHIEVEMENTS

International finalist, SpaceX Hyperloop Pod Competition '17 • 168th rank, Google CTF '16 • 98th rank, TrendMicro CTF '16 • 57th rank, Sunshine CTF '16

## SKILLS

### PROGRAMMING

C • C++ • Python • PHP • HTML • LISP • Shell Scripting • Haskell • Redstone • Assembly(x86,MIPS,ARM,RISCV) • Go

### SECURITY

Reverse Engineering • Data Forensics • Network Forensics • Web Exploits • Cryptography • Penetration Testing • Dynamic Analysis • Intrusion Detection

## EXPERIENCE

### MEDIA.NET | DEVOPS ENGINEER

July 2018 - present | DirectiPlex, Mumbai, India

- Manage large Hadoop, Druid, Kafka and Elastic Stack clusters
- Design and deploy large scale monitoring, logging and alerting systems
- Identify issues and scopes for optimization in the infrastructure

### RECONFIGURABLE INTELLIGENT SYSTEMS ENGINEERING LAB | THESIS

Jan 2018 - June 2018 | IIT Madras, India

- Designed a secure processor and compiler toolchain that protects against memory corruption and buffer overflow exploits

### RECONFIGURABLE INTELLIGENT SYSTEMS ENGINEERING LAB | RESEARCH INTERN

Dec 2016 - Jan 2017 | IIT Madras, India

- Learned Bluespec HDL and worked on 32 bit 3 stage RISC-V processor designs
- Ported FreeRTOS RISC-V ISA version 1.9.1

## PROJECTS

### TRUSTED EXECUTION ENVIRONMENT BASED DYNAMIC ANALYSIS ON ARM | GSoC 2018

June 2018 - August 2018

Developed TEE-Monitor, a stealthy dynamic analysis tool for ARM that can observe and analyze the execution of malware on ARM devices

### MULTI-LEVEL MIXED CRITICALITY REALTIME SCHEDULING | DESIGN PROJECT

August 2016 - Present | Goa, India

Worked with Dr. Biju K Raveendran to design and implement multilevel mixed criticality scheduling algorithms in Real Time Operating Systems

### HYPERLOOP INDIA | ELECTRONIC SYSTEMS LEAD

May 2016 - Sep 2017 | Goa, India

Led the team working on the electronics and control systems of the Hyperloop pod for the SpaceX Hyperloop Design Competition. One among 24 teams to build and test a hyperloop pod at the SpaceX test track

## POSITIONS OF RESPONSIBILITY

### HYPERLOOP INDIA | ENGINEERING LEAD

Sep 2017 - Feb 2018 | Goa, India

Supervising all electronics, control systems and software work for the Indian team participating in the SpaceX Hyperloop pod competition scheduled for 2018

### BITSKRIEG | CLUB FOUNDER AND COORDINATOR | BITS PILANI, GOA

January 2016 - April 2017 | Goa, India

Founded the cyber security and pentesting club BITSkrieg. Participated in over 30 CTF competitions in 2016 and ranked within the global top 100 in 8 of them

## INTERESTS

Capture The Flag cybersecurity competitions • Disassembling, reverse engineering and modding PC games • Setting up and maintaining a self-hosted data centre at home running on a virtualization cluster