Lab session #10

December 5, 2024

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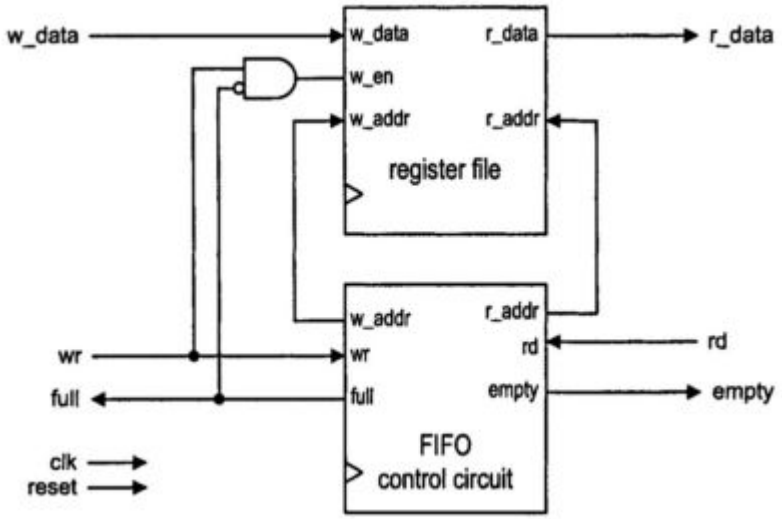
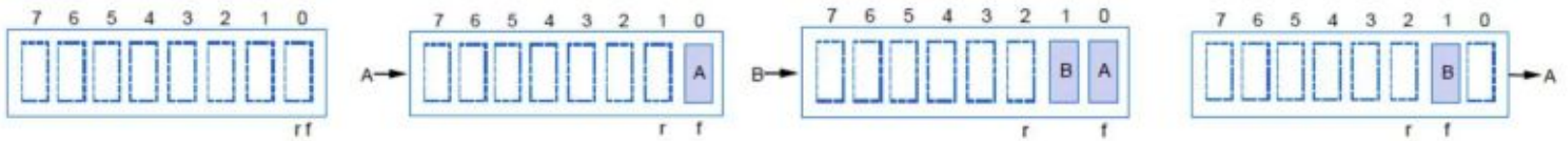
FIFO

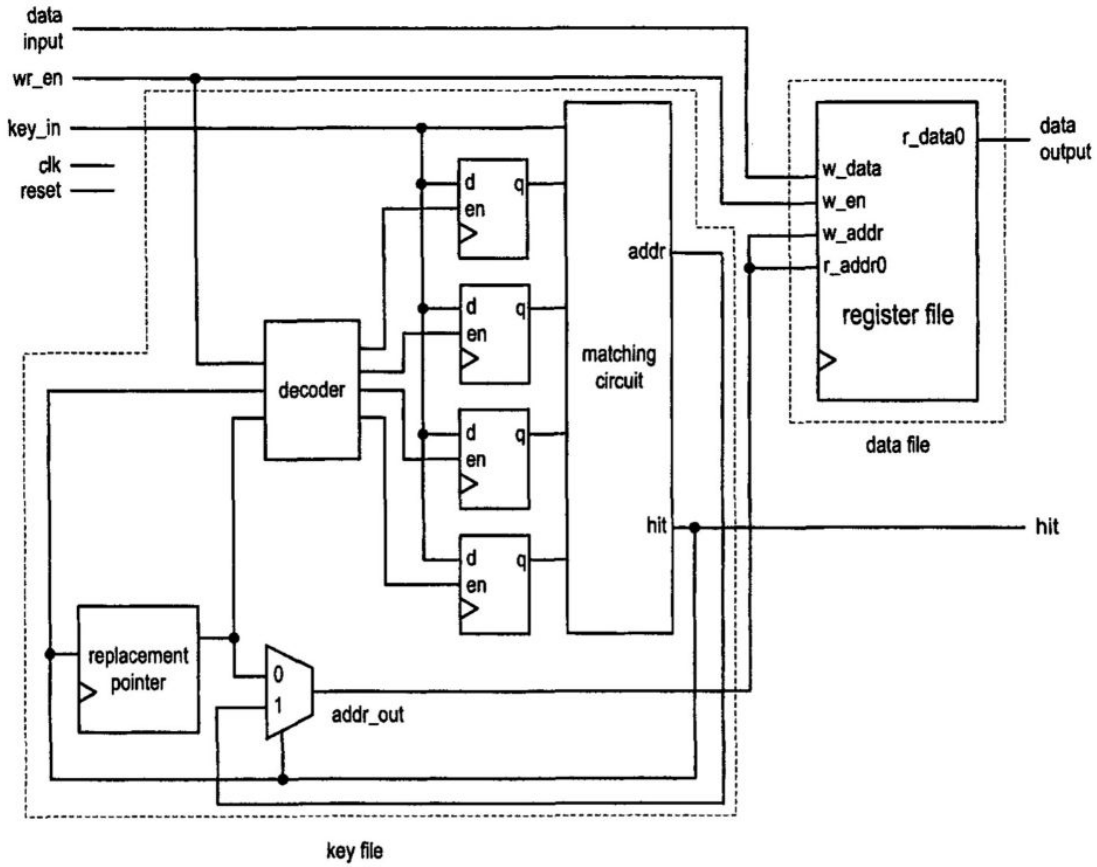


- Design a First-In-First-Out (FIFO) memory resorting to behavioral description of the datapath and the controller and a FSM-D approach.
  - Total of 2^M (M=3) N-bit words (N=16)
  - Implement the FIFO as a 2^MxN register file
- Input signals *wr* and *rd* are used to signal the beginning of a enqueuing or dequeuing operation, respectively.
- Output signals *full* and *empty* must be used to signal the two specific cases

- Design a testbench to validate your design on relevant cases



Content-Addressable Memory



- Design a Content-Addressable memory using FSMD approach as described in the lab guideline:
  - 4 words 16-bit wide
  - supports for read and write operations
  - Only one match is allowed
- Read: a signal *match* is asserted if the *key_in* has a match inside the memory. The generated *addr* is used to access the register file containing the data which is given at the output with the assertion of the *hit* signal.
- Write with match: Similar to the read operation, but the *addr* is used to write inside the register file and replace the old data.
- Write without match: the new *key* is written inside the register pointed by *rep_ptr*, same for the *data*. *rep_ptr* is updated

- Design a testbench to validate your design on relevant cases