Lab session #06

November 7, 2024

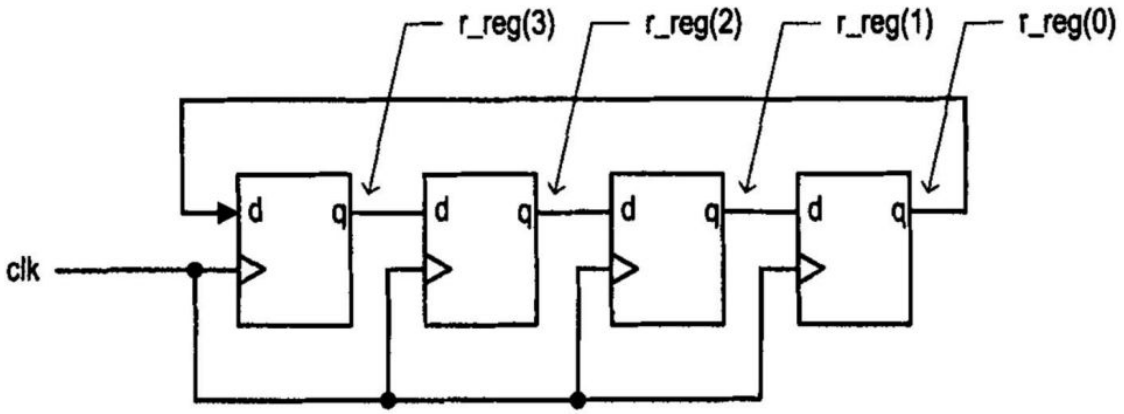
Michelangelo Barocci, michelangelo.barocci@polito.it

Politecnico di Torino,

PhD Student @ EDA Group - DAUIN

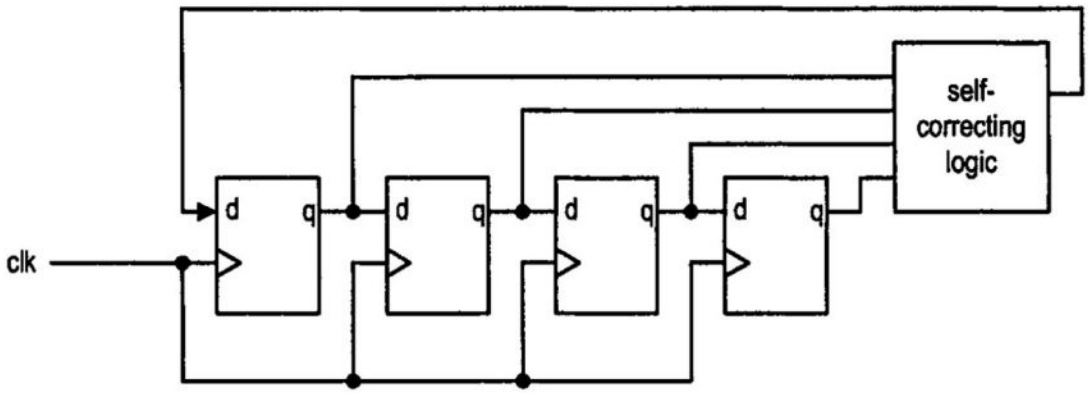
Dpt. of Computer and Control engineering (DAUIN)

N-bit Ring Counter



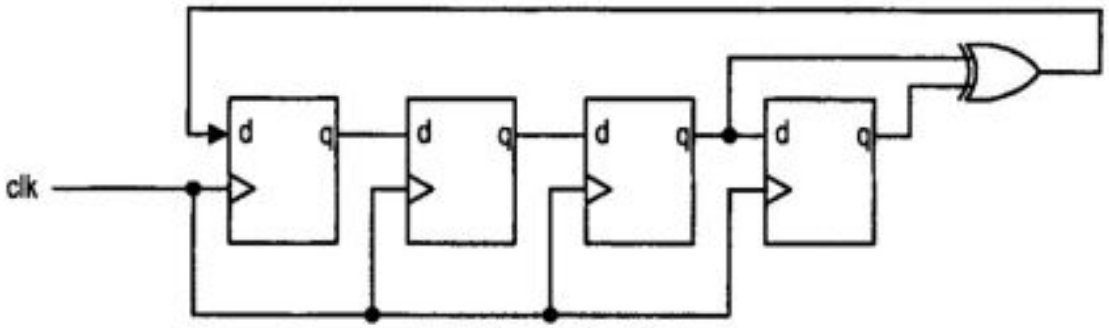
- Design a N-bit counter with such characteristics:
  - one-hot encoding of its outputs, hence N possible states
  - Circulates repeatedly between such states
  - resets synchronously
  - can be enabled or disabled externally
- Design the architecture such that it implements a N-bit (=4 in this case) shift register that auto-feeds its output reg[4] at its input (MSB)
- Write a testbench to test the architecture in a way that it starts from one of the possible N values and continuously cycles between the states

N-bit self-correcting Ring Counter



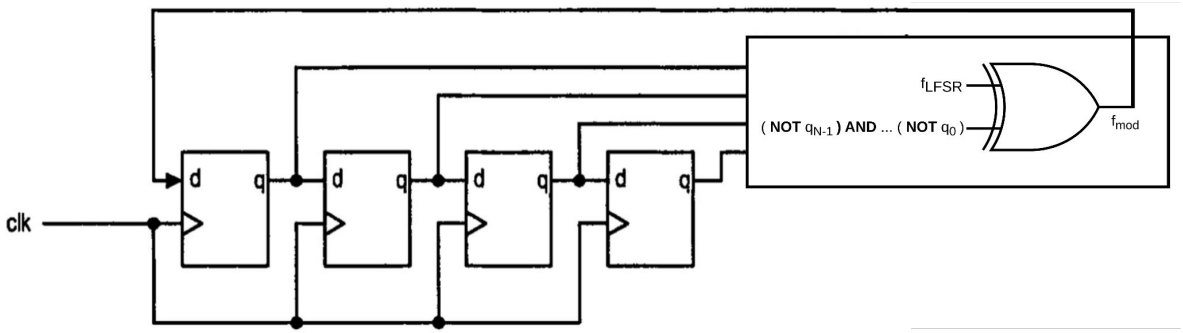
- Modify the architecture of the previous exercise by implementing the feature of "cleaning" the current state to make it compliant with the wanted N states. The algorithm shall perform a logical right shift on the input until all bits are '0' except one '1'.
- Write a testbench to test the architecture by using suitable and relevant input vectors

8-bit LFSR



- Design a N-bit Linear Feedback Shift Register by modifying the previous designs. A LFSR is a circuit that is capable of cycling between all 2^N states (minus the "all 0" state) in a pseudo-random (actually the succession is deterministic) way.
- Implement the LFSR by using XOR gates at the right positions. (N=8)
- Write a testbench to test the architecture in a way that it starts from a value given by a signal *seed* and cycles through the states.

8-bit de Brujin counter



- Modify the LFSR and transform it into a de Brujin counter by adding the necessary logic to have also the "all 0" state.
- Write a testbench to test the architecture in a way that it starts from a value given by a signal *seed* and cycles through the states.