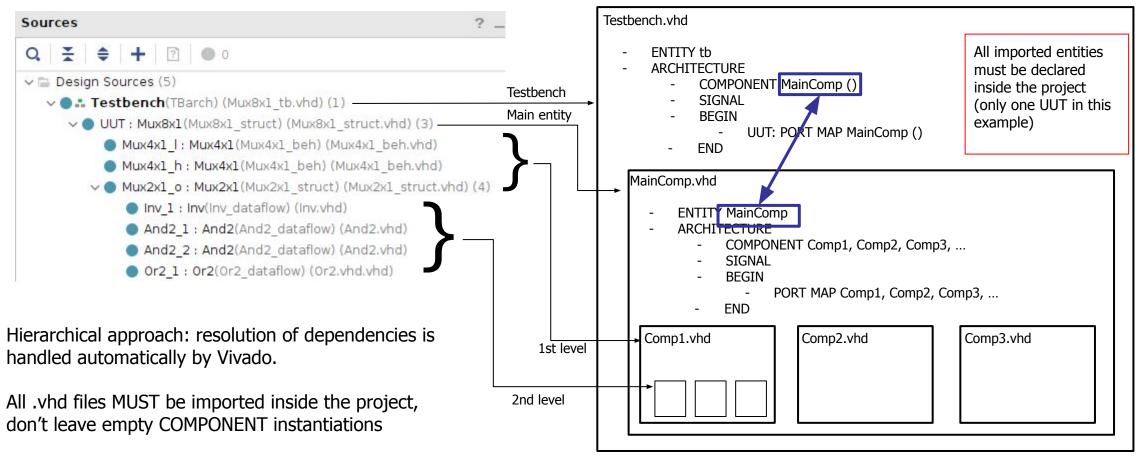


Michelangelo Barocci, michelangelo.barocci@polito.it PhD Student @ EDA Group - DAUIN Politecnico di Torino

### Before we start

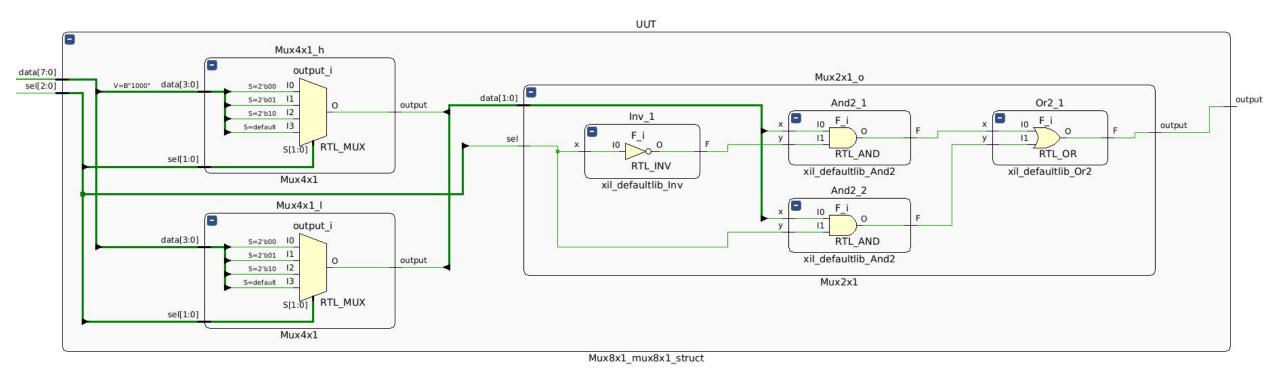
Vivado project structure:



A.Y.: 2024/2025 SSDS - Lab#02 October 4, 2024

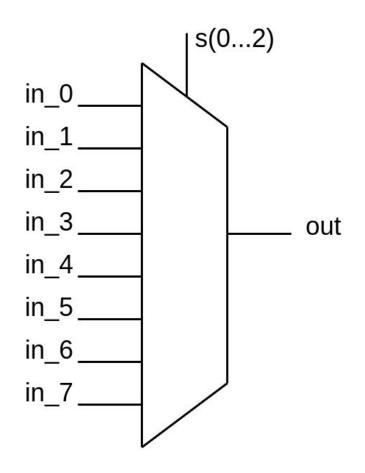
# Before we start

### Vivado RTL structure:



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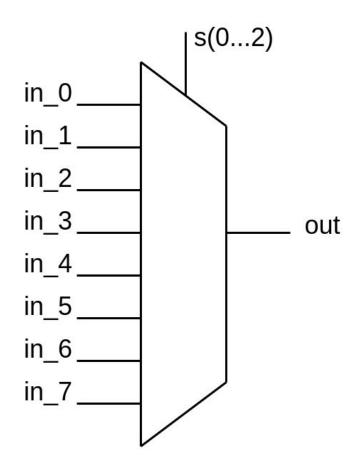
### 8to1 Multiplexer



- ☐ Describe a 8to1 MUX using 5 different styles:
  - □ DATAFLOW with WHEN ELSE statements
  - □ DATAFLOW with WITH SELECT WHEN statement
  - BEHAVIORAL with IF THEN ELSIF statements
  - BEHAVIORAL with CASE WHEN statement
  - □ STRUCTURAL with a hierarchical approach (2x 4to1 BEHAVIORAL MUX and 1 2to1 STRUCTURAL MUX
- Develop an appropriate testbench to perform the simulation and verify if the design is correct
- You should use a CONFIGURATION statement to enable switching between configurations



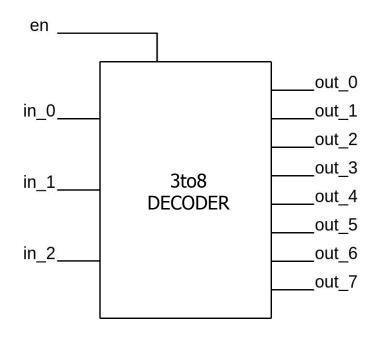
### 8to1 Multiplexer



### 8to1 MUX truth table:

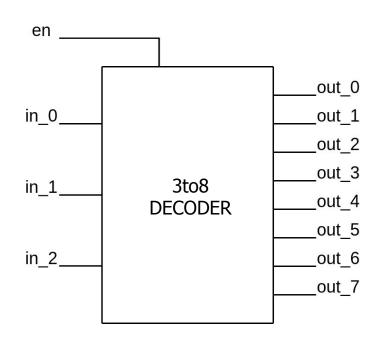
s0	s1	s2	out
0	0	0	in_0
0	0	1	in_1
0	1	0	in_2
0	1	1	in_3
1	0	0	in_4
1	0	1	in_5
1	1	0	in_6
1	1	1	in_7

### 3to8 Decoder



- ☐ Describe a 3to8 DECODER using 4 different styles:
  - □ DATAFLOW with WHEN ELSE statements
  - □ DATAFLOW with WITH SELECT WHEN statement
  - □ BEHAVIORAL with IF THEN ELSIF statements
  - ☐ BEHAVIORAL with CASE WHEN statement
- Develop an appropriate testbench to perform the simulation and verify if the design is correct

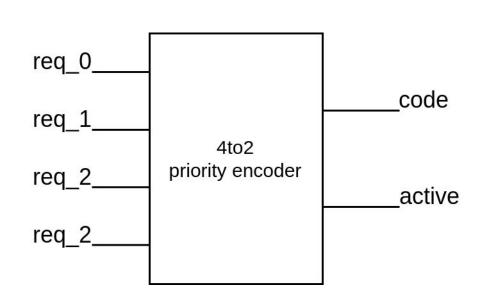
### 3to8 Decoder



in_0	in_1	in_2	en	out_0	out_1	out_2	out_3	out_4	out_5	out_6	out_7
0	0	0	1	1	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	1	0	0
1	1	0	1	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1
-	-	-	0	0	0	0	0	0	0	0	0

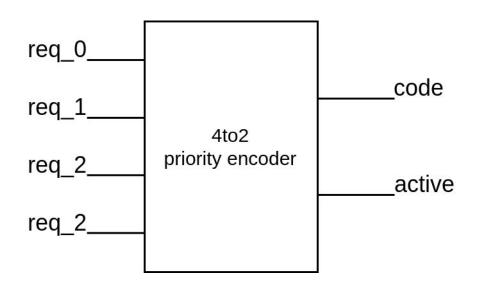
A.Y.: 2024/2025 SSDS - Lab#02 October 4, 2024

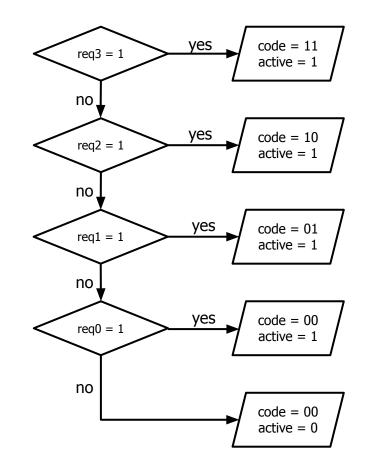
### 4to2 Priority Encoder



- Describe a 4to2 PRIORITY ENCODER using 4 different styles:
  - □ DATAFLOW with WHEN ELSE statements
  - □ DATAFLOW with WITH SELECT WHEN statement
  - BEHAVIORAL with IF THEN ELSIF statements
  - BEHAVIORAL with CASE WHEN statement
- Develop an appropriate testbench to perform the simulation and verify if the design is correct

### 4to2 Priority Encoder





## Synthesis

Lastly, run synthesis on your designed multiplexer, decoder and priority encoder.

- Understand the differences between the different description styles of the same circuit, do the reported results change?
- Are you able to estimate a maximum working frequency? How?