Lab session #11

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Michelangelo Barocci, michelangelo.barocci@polito.it

Politecnico di Torino,

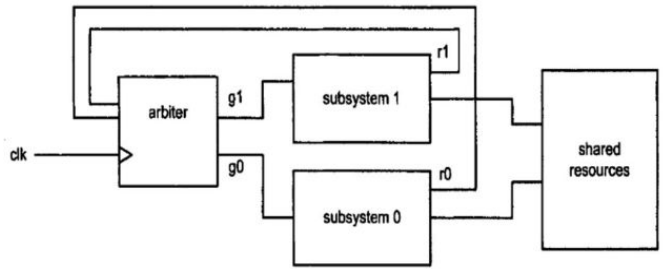
PhD Student @ EDA Group - DAUIN

Dpt. of Computer and Control engineering (DAUIN)

2-request arbiter (Verilog)

Throwback to Lab 7:

FSM-based 2-request arbiter



- Design a Moore FSM-based arbiter circuit that handles multiple access requests (two in this case) towards a common shared resource (e.g. a memory).
- The arbiter makes sure that the access to the resource happens in the correct way, following a precise decision. When only one subsystem tries to access, the arbiter grants that request, while if multiple requests are issued it decides the correct order.
- Implement the arbiter such that the order of resource accesses is established following two guidelines:
  - Fixed priority to a given subsystem;
  - Last subsystem that accessed the resource has least priority.
- Write a testbench to test the architecture in relevant cases.

Design the same 2-request arbiter circuit as described in Lab #07 with these modifications:

- Use Verilog description language
- For simultaneous accesses, resort to strategy #1, i.e. give priority to one specific subsystem
- Describe the Moore FSM in two ways:
  - With one *always* block
  - With two *always* blocks

Write a suitable testbench to test the circuit on relevant cases