Altay Ýlker Yiðitel cs224 04 22203024

module topoftop(input clk, reset, output memwrite, output [6:0] seg, output dp, output [3:0] an , output [14:0]pc); logic [31:0] writedata; logic [31:0]dataadr; logic[31:0] readdata; logic [31:0]instr; logic [16:0]pcrest;

top topmod(clk, reset,writedata, dataadr,readdata,memwrite,instr,{pcrest,pc}); pulse_controller pulse(clk,switch,reset,clk_pulse); display_controller display(clk,dataadr[7:4],dataadr[3:0],writedata[7:4],writedata[3:0],seg,dp,an);

endmodule

module topoftop(input clk, reset, output memwrite, output [6:0] seg, output dp, output [3:0] an , output [14:0]pc); logic [31:0] writedata; logic [31:0]dataadr; logic[31:0] readdata; logic [31:0]instr; logic [16:0]pcrest;

top topmod(clk, reset,writedata, dataadr,readdata,memwrite,instr,{pcrest,pc}); pulse_controller pulse(clk,switch,reset,clk_pulse); display_controller display(clk,dataadr[7:4],dataadr[3:0],writedata[7:4],writedata[3:0],seg,dp,an);

endmodule

module top_tb;

logic clk; logic reset; logic[31:0] dataadr; logic[31:0] writedata; logic[31:0] readdata; logic memwrite; logic [31:0]instr; logic [31:0]pc;

topoftop mymips(.clk(clk), .reset(reset), .memwrite(memwrite), .instr(instr), .pc(pc));

always begin #10 clk = ~clk; end

initial begin

clk = 0; reset = 1; #1; reset = 0; end

endmodule