**Abstract**

Hardware emulator is a machine that can accept specific software modeling language called RTL (which describes logical circuits, which in turn becomes CPU), and emulate the described design in hardware. Benefits of using this type of emulation versus existing software existing tools are in up to 100X speed benefits. Despite the big performance benefit its big cost that is ranged from 0.5 to 1 million dollars make forces to manage the resource as optimal as possible.

A model for emulator allocation was derived with aligned with one of chip manufacturer customer requirements, where the emphasis is on completing as much tasks as possible in their given due date. Our problem type is a multiprocessor job scheduling problem where each job can use more than one machine at a time.

This problem is NP-Complete as shown in [Ref1]. We prove a lower bound based on Moore and Hodgson [Ref2] algorithm that minimizes the total tardiness for a single machine. Special case where all jobs have identical size and identical process time is solved in polynomial time based on [Ref3]. Additionally we provide a compare between three different formulations, two relational formulations and one time based formulation and show their behavior in different environment parameters.