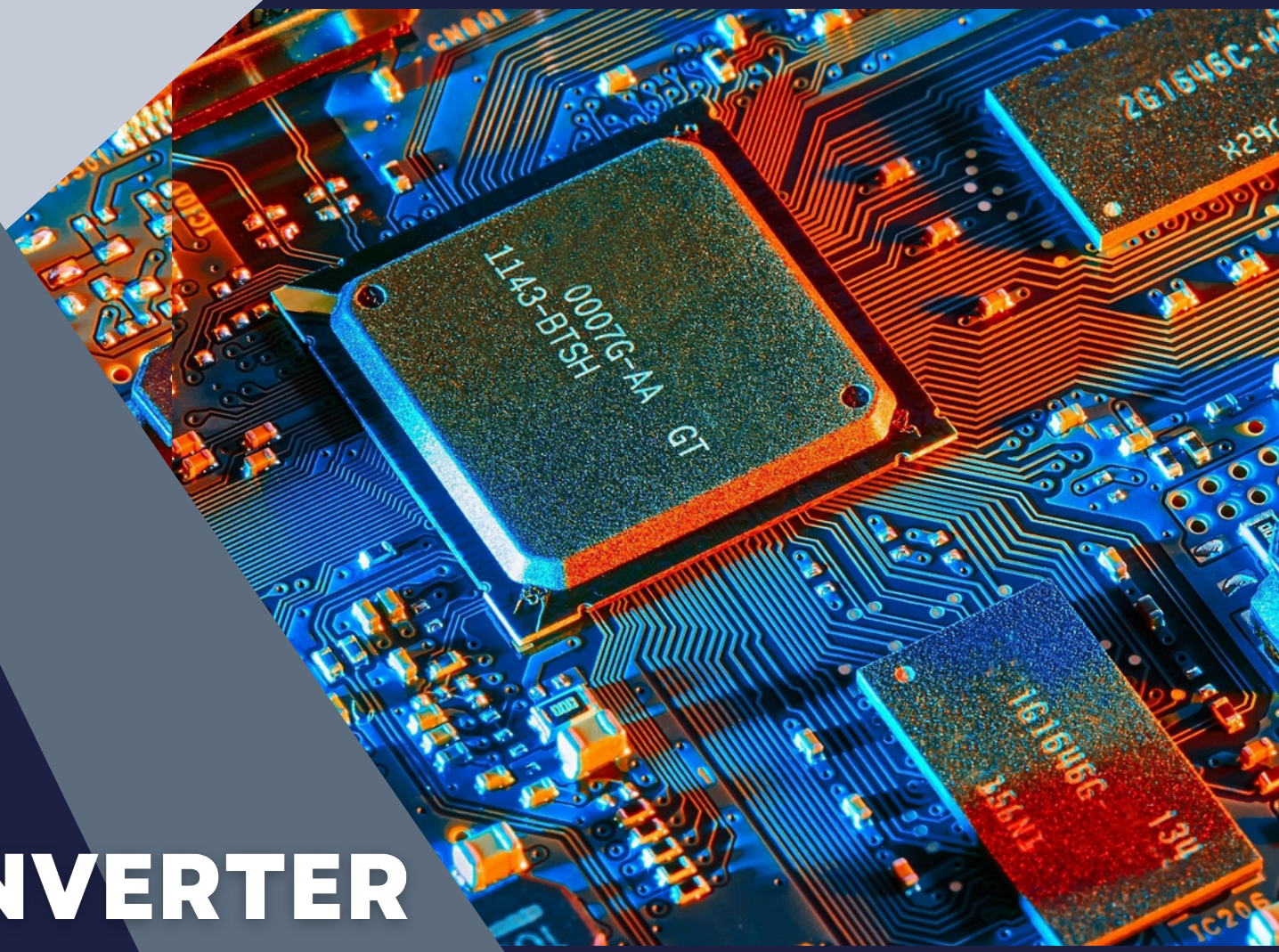
INTEGRATED CIRCUITS
ELECTRONICS



INVERTER CHAIN BUFFER

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Literature Review and Design of Inverter Chain Buffer

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***Abstract*—In this paper, we investigate the design and optimization of inverter chain buffers for high-speed applications, specifically targeting the driving of large capacitive loads at gigahertz frequencies. A comprehensive literature review is conducted, focusing on the application, design methodologies, and critical parameters of inverter chain buffers. The study also explores the biasing of two-stage operational amplifiers using current sources. These buffers, comprising cascaded inverters, serve to strengthen and amplify digital signals for driving capacitive loads and increasing fanout. It explores various applications of inverter chain buffers, including driving large loads, signal restoration, delay generation, and clock distribution. Key design parameters such as the number of inverters, sizing, tapering, fanout, propagation delay, and power consumption, are discussed. The advantages of using inverter chain buffers, such as enhanced drive strength and signal integrity improvement, are examined alongside their disadvantages and limitations, including increased area and power consumption. Different configurations, like tapered buffers and clock buffers are also covered. The report concludes by highlighting the importance of careful design and optimization of inverter chain buffers for modern digital integrated circuits.It also contains the trade-offs between buffer stage count, power consumption, and signal integrity in high-speed capacitive load driving scenarios.**

Keywords— buffer, digital integrated circuit, inverter chain, two-stage operational amplifier, large capacitive load, propagation delay, limitations, parameters, optimization, trade-offs, fanout, applications.

I. INTRODUCTION

An inverter chain buffer is a fundamental component in digital logic circuits, typically comprising two or more inverters connected in series [1]. While a single inverter performs a logical NOT operation, an even number of inverters connected sequentially results in a non-inverting buffer, where the output logic level mirrors the input. The primary function of such a configuration extends beyond simply passing the signal; it serves to strengthen and amplify digital signals, thereby enhancing their ability to drive substantial capacitive loads or a large number of subsequent logic gates, a concept known as fanout. This amplification is crucial for maintaining signal integrity and ensuring reliable signal transmission throughout complex digital systems.

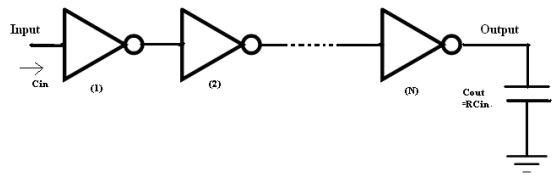

Fig.1 Inverter chain with load capacitance

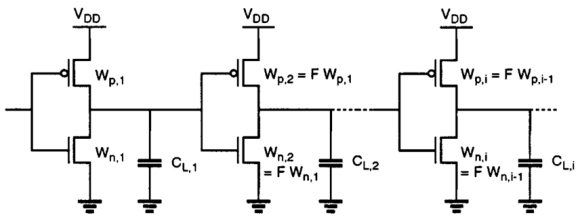

Fig.2 CMOS inverter chain with sizing factors

II. DESIGN PARAMETERS

The implementation of an effective inverter chain buffer requires careful consideration of several key design parameters [2]. This is a fundamental choice

that directly impacts the overall functionality and performance. An even number of inverters is typically used for buffering purposes, where the output logic level needs to be the same as the input. An odd number of inverters would result in a logical inversion. The total delay introduced by the chain is approximately proportional to the number of stages. For minimizing delay when driving a large load, the optimal number of stages is often related to the total fanout, with more stages being beneficial for very large fanouts.

A. Width-to-length ratio

Inverter sizing and tapering are critical techniques for optimizing the delay of an inverter chain buffer, especially when driving a significant capacitive load. Transistor sizing involves adjusting the width-to-length ratio of the PMOS and NMOS transistors within each inverter. Increasing the width generally increases the drive strength (current capability) of the transistor, allowing it to charge and discharge capacitances faster, thus reducing delay. However, larger transistors also have larger input capacitances, which can increase the delay of the preceding stage. Tapering is a strategy where the size of each subsequent inverter in the chain is increased by a certain factor relative to the previous stage. This gradual increase in size allows each stage to efficiently drive the increasing load capacitance of the next stage, leading to a minimization of the overall propagation delay through the chain. The optimal tapering factor, often denoted by 'f' (fanout), is typically found to be around the mathematical constant 'e' (approximately 2.718) for an ideal case, but in practice, values between 3 and 4 are commonly used, a rule of thumb known as the "Fanout of 4" rule.

Table K.1 Typical Values of CMOS Device Parameters

	0.8 µm		0.5 µm		0.25 µm		0.18 µm		0.13 µm		65 nm	
Parameter	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
L_{ef} (nm)	15	15	9	9	6	6	4	4	2.7	2.7	1.4	1.4
C_{ox} (fF/µm^2)	2.3	2.3	3.8	3.8	5.8	5.8	8.6	8.6	12.8	12.8	25	25
μ (cm^2/V·s)	550	250	500	180	460	160	450	100	400	100	216	40
μC_{ox} (µA/V^2)	127	58	190	68	267	93	387	86	511	128	540	100
V_{t0} (V)	0.7	–0.7	0.7	–0.8	0.5	–0.6	0.5	–0.5	0.4	–0.4	0.35	–0.35
V_{DD} (V)	5	5	3.3	3.3	2.5	2.5	1.8	1.8	1.3	1.3	1.0	1.0
$\lvert V_A' \rvert$ (V/µm)	25	20	20	10	5	6	5	6	5	6	3	3
C_{ov} (fF/µm)	0.2	0.2	0.4	0.4	0.3	0.3	0.37	0.33	0.36	0.33	0.33	0.31

Fig.3 Table of CMOS device parameters

B. Fanout

Fanout, defined as the ratio of the output capacitance of a gate to its input capacitance, is a crucial parameter in inverter chain design [3]. It quantifies the load that a buffer is driving with its input capacitance. Maintaining a uniform fanout across all stages is essential to minimize the total propagation delay through a cascaded buffer chain. A high fanout on a particular stage can significantly increase its delay, while a very low fanout might lead to an unnecessarily large number of stages, also increasing the total delay. The fanout per stage in an optimally designed N-stage inverter chain driving a load capacitance C_L from an initial input capacitance Cin is given by

$$f = \left(\frac{C_L}{C_{in}}\right)^{1/N} \qquad (1)$$

C. Propagation Delay

The propagation delay of each inverter in the chain, typically characterized by the low-to-high propagation delay (tp_{LH}) and the high-to-low propagation delay (tp_{HL}), and the overall delay of the chain are critical timing characteristics that must be carefully considered [4]. These delays dictate the speed at which the circuit can operate and must be accounted for in the timing analysis of the digital system to prevent timing violations such as setup and hold time failures. Simulation tools are often used to estimate these delays accurately based on the specific technology and design parameters.

$$t_p = \frac{t_{pLH} + t_{pHL}}{2} \qquad (2)$$

D. Power Consumption

Power consumption is another important consideration in the design of inverter chain buffers. Increasing the size of the inverters and the number of stages generally leads to higher dynamic power consumption. Dynamic power is primarily due to the charging and discharging of capacitances during switching. Larger inverters have larger gate capacitances, and more stages mean more switching events for each signal transition, both contributing to increased power dissipation. Therefore, there is often

a trade-off between performance (delay) and power consumption in the design process.

Finally, the performance of inverter chain buffers, like all semiconductor circuits, can be significantly affected by process, voltage, and temperature (PVT) variations. Manufacturing variations can lead to differences in transistor characteristics compared to their nominal values. The supply voltage and operating temperature can also fluctuate. These variations can impact the delay, drive strength, and power consumption of the inverters in the chain. Robust designs must take these variations into account to ensure proper operation across all expected conditions. This often involves simulating the circuit under different PVT corners (worst-case scenarios for delay and power).

III. TECHNOLOGY AND PARAMETERS SELECTION

A. Technology Node Selection

The 65nm CMOS technology is selected for this design due to its high switching speed, low power dissipation, and widespread availability in academic research and industry benchmarks. Compared to older nodes such as 180nm or 130nm, 65nm offers improved density and performance, making it ideal for GHz-range applications.

B. Design Specifications

1. Supply Voltage (VDD): 1.8V
2. Load Capacitance (CL): 1.5 pF
3. Frequency: 1 GHz (T = 1 ns)
4. Max Rise/Fall Time: 10% of T (100 ps)
5. Source Resistance (Rs): 50 Ω with 5% rise/fall time of T (50 ps)

C. CALCULATIONS AND DESIGN PROCEDURE

(i) Input Capacitance

For input capacitance we have,

$$C_{in} = C_{ox}\, x\, (W_n . L_n + W_p . L_p)\ x\, C_{ov\,(total)} \qquad (3)$$

By calculations, we get input capacitance as $0.15fF$.

(ii) Number of Stages (N)

By using the classic buffer sizing principle from *eq.1,*

$$f = \left(\frac{C_L}{C_{in}}\right)^{1/N} \quad ,$$

Substituting *fan-out as* $f = e\ (optimal\ value)$

$$N = \frac{ln(C_L/C_{in})}{ln(e)}$$

$$N = \frac{ln(1.5pF/1.5fF)}{ln(e)}$$

$$N \approx 6\ (number\ of\ stages)$$

(iii) Fanout

Using the number of stages, we now calculate the exact value of fanout from *eq.1*,

$$f = \left(\frac{Cl}{Cin}\right)^{1/N}$$

$$f = \left(\frac{1.5\ x\ 10^{-12}}{1.5x10^{-15}}\right)^{1/6}$$

$$f = 3.16$$

D. Inverter Sizing

The minimum width chosen for the base stage is 140 nm for NMOS whereas the width of PMOS is twice that of NMOS i.e 280 nm, which increases at each stage by a fanout factor of 3.16.

Table.1
No of stages for the inverter chain buffer

No of Stage	*NMOS W (nm)*	*PMOS W(nm)*
1	140	280
2	442.4	884.8
3	1397.98	2795.968
4	4417.629	8835.2588
5	13959.709	27919.41
6	44112.6805	88225.361

IV. SIMULATION AND TRANSIENT ANALYSIS

For simulation setup, following values are considered,

Models: Standard 65nm MOSFET models included.

Supply: VDD = 1.8V DC

Input: 1GHz pulse with 5% rise/fall time (50ps)

Load: Capacitor CL = 1.5 pF

Transient Analysis: Time step ≤ 1ps, stop time = 2ns

Measurements: tPLH, tPHL, average power using waveform calculator

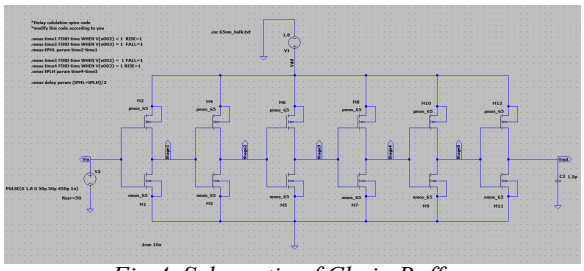

Fig 4. Schematic of Chain Buffer

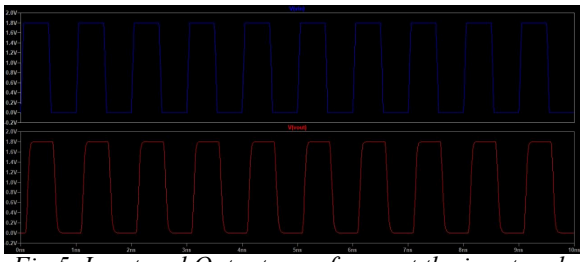

Fig 5. Input and Output waveforms at the input and output nodes respectively

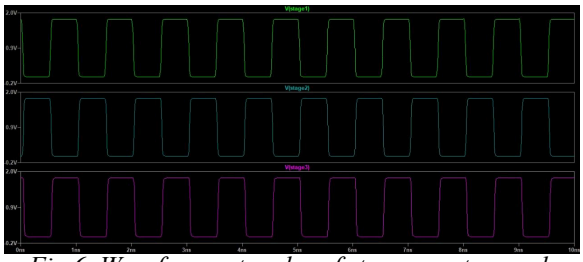

Fig 6. Waveforms at nodes of stage one, two and three

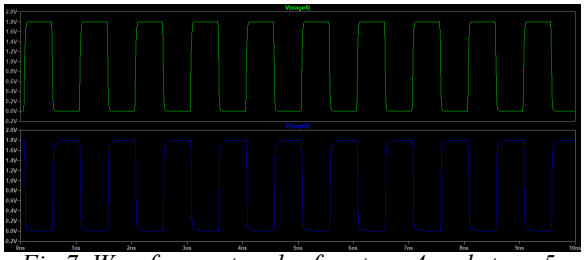

Fig 7. Waveforms at nodes for stage 4 and stage 5

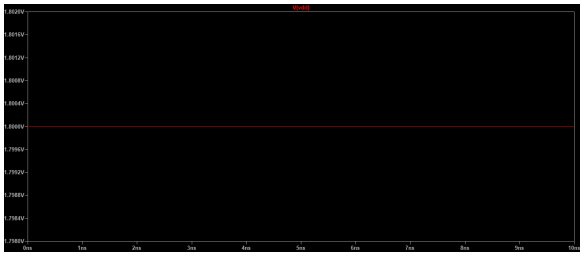

Fig 8. DC input at top node (VDD)

V. SIMULATION RESULTS

Following are the fall and rise times calculated from the graph as well as verified using the .t (Spice Directive) method.

1. $t_{pHL} = 7.794\ ps$ (fall time)

2. $t_{pLH} = 15.305\ ps$ (rise time)

3. $T = 11.55\ ps$ (propagation delay)

Power consumption is also found to be

$P_{dyn} = 296.226\ uW$

Table.2
Power consumption at each stage of the buffer

No of Stage	*Power Consumption (uW)*
1	0.27
2	2.36
3	2.85
4	23.9
5	28.6
6	237.5

VI. TRADEOFF ANALYSIS

The number of stages in a tapered buffer directly affects both delay and power consumption:

(i) Lower Number of Stages: Increases the size of each stage to meet load requirements, causing higher per-stage capacitance, increased individual delay, and higher instantaneous power consumption.

(ii) Higher Number of Stages: Reduces the required per-stage size by distributing the load capacitance over more stages, lowering delay per stage. However, the cumulative dynamic and static power increases due to additional stages contributing to overall consumption.

VII. LAYOUT DESIGN

The layout was designed using Microwind [5], an integrated CAD tool specifically developed for CMOS layout design, simulation, and verification. This tool is particularly suitable for educational and research applications because it offers an intuitive visual environment for designing and testing CMOS circuits. The layout was implemented for a CMOS inverter chain using 65 nm technology, configured with a supply voltage of 0.5V. The Microwind environment enables real-time Design Rule Check (DRC) verification, ensuring that the layout meets fabrication constraints.

A notable feature applied in this layout is the folding technique, widely used in VLSI design to optimize the layout of large MOSFETs. Folding involves splitting a wide transistor into several narrower fingers connected in parallel. In this design, both the NMOS and PMOS transistors were folded into multiple fingers to achieve several benefits. Folding reduces gate resistance and diffusion capacitance, enhances current matching, and improves thermal distribution across the layout. This technique is especially important for handling large transistor widths, where using a single wide device can lead to routing congestion, uneven heat dissipation, and increased parasitic effects. By applying folding, the layout achieves better performance, balancing area optimization, parasitic control, and current handling capability. This was successfully implemented using 65nm technology.

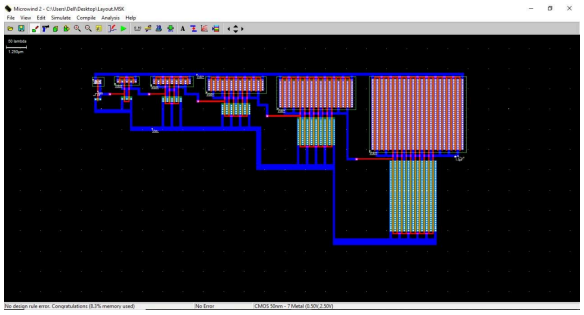

Fig 9. Microwind Layout of Inverter Chain Buffer

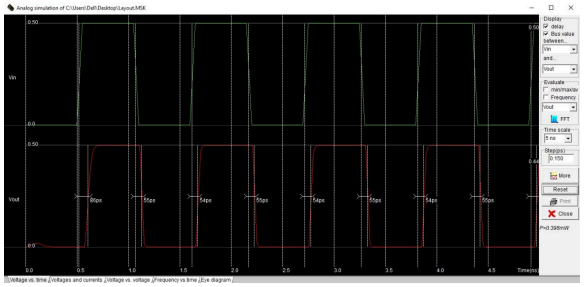

Fig 10. Analog Simulation of the Buffer in Microwind

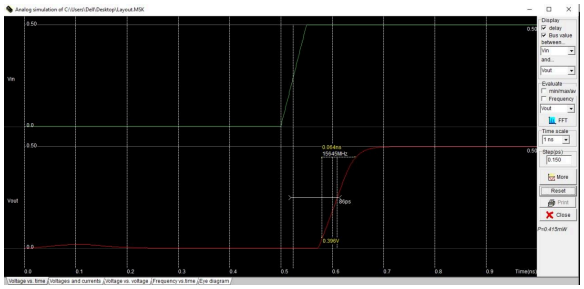

Fig 11. Rise time of the buffer in Microwind Layout

Table 3. Folding width of each NMOS and PMOS

Stages	*NMOS (µm)*	*PMOS (µm)*
1	*0.14*	*0.28*
2	*0.221*	*0.221*
3	*0.349*	*0.349*
4	*0.736*	*0.736*
5	*1.744*	*1.744*
6	*4.411*	*4.411*

VIII. APPLICATIONS

Inverter chain buffers find widespread use in various aspects of digital integrated circuit design due to their ability to enhance signal characteristics and provide essential functionalities [6]. One of their most critical applications is in driving large capacitive loads and increasing fanout. In complex digital systems, a single logic gate often needs to drive the inputs of numerous other gates or long interconnects, both of which present significant capacitive loads. If the driving gate has insufficient current capability, the signal transitions at the driven nodes will be slow, and the signal levels might not reach the required voltage thresholds, leading to incorrect operation. An inverter chain buffer, with its increased drive strength, can effectively charge and discharge these large capacitances, ensuring fast and reliable signal transitions. This is particularly important for signals that need to be distributed across a large number of nodes, such as clock signals or control signals in memory arrays.

Inverter chain buffers also play a vital role in signal restoration and waveform shaping. As digital signals propagate through circuits, they can become degraded due to factors like resistive losses, capacitive loading, and noise. This degradation can manifest as slow rise and fall times, rounded edges, and voltage levels that deviate from the ideal high and low values. An inverter chain buffer, especially one with multiple stages, can effectively regenerate these degraded signals. The sharp switching characteristics of each inverter in the chain help to produce clean, fast transitions at the output, restoring the signal to its intended form. The noise margin of CMOS inverters, which represents the range of input voltage around the ideal logic levels that will still be correctly interpreted, contributes to this signal restoration capability.

Another significant application of inverter chain buffers is in **i**ntroducing controlled delay. In synchronous digital circuits, precise timing is crucial for correct operation. Sometimes, it is necessary to introduce a specific amount of delay in a signal path for synchronization purposes or to meet timing constraints. An inverter chain, with its inherent propagation delay through each stage, can serve as a simple and effective delay element. The total delay introduced by the chain is approximately the sum of the delays of the individual inverters. For small delay requirements, a buffer consisting of two cascaded inverters is often sufficient.

Inverter chain buffers are extensively used in clock distribution networks [7]. The clock signal is the heartbeat of a synchronous digital system, and it needs to be distributed to all sequential elements (like flip-flops) across the entire chip with minimal skew (the difference in arrival times at different destinations) and a well-defined insertion delay (the delay from the clock source to the clocked elements). Clock buffers, often implemented using carefully designed inverter chains, are inserted along the clock paths to balance these delays and provide the necessary drive strength for the high fanout of the clock network. These clock buffers often have specific design properties, such as equal rise and fall times, to maintain the duty cycle of the clock signal and minimize duty cycle distortion.

Furthermore, reducing rise and fall times is another key application of inverter chain buffers, particularly in the form of tapered inverter chains [8]. When driving a large capacitive load, a single large inverter might seem like a solution to provide high drive strength. However, this large inverter would also present a large input capacitance to the preceding stage, potentially slowing it down. A tapered inverter chain, where the size (and thus drive strength) of each subsequent inverter is gradually increased, offers a more efficient way to drive large loads with faster transition times. This is because each stage is optimally sized to drive the next stage, minimizing the overall delay through the chain.

Beyond these major applications, inverter chain buffers find use in other scenarios, such as generating reset signals, synchronizing inverted clock inputs, and debouncing switches. In essence, any situation requiring signal strengthening, controlled delay, or waveform shaping in a digital circuit can potentially benefit from the use of an inverter chain buffer.

IX. LIMITATIONS AND VARIATIONS

Inverter chain buffers also have certain limitations that designers need to be aware of [9]. One notable drawback is the increased area and power

consumption associated with using multiple inverters. Each inverter in the chain occupies a certain amount of silicon area on the integrated circuit. As the number of stages in the chain increases, so does the total area consumed. Additionally, each switching event in an inverter dissipates dynamic power. Therefore, a longer inverter chain or one with larger transistors will generally consume more power compared to a single buffer or a shorter chain. This trade-off between performance (drive strength, delay) and resource utilization (area, power) is a common consideration in digital design.

Another potential limitation is the risk of timing violations if not designed carefully. While inverter chains can be used to introduce controlled delay, an improperly designed chain, with an incorrect number of stages or inappropriate sizing, can lead to excessive delay or mismatches in timing between different signal paths. This can result in functional errors in the digital circuit, such as setup or hold time violations in sequential elements. Therefore, accurate timing analysis and careful design optimization are crucial when using inverter chain buffers.

While individual CMOS inverters have good noise margins, sensitivity to noise can become a concern in very long inverter chains, although this is generally manageable with proper design practices and within specified operating conditions. Each stage in the chain can potentially introduce or amplify noise to some extent. While the noise margin of each gate helps to filter out small noise perturbations, in extreme cases, accumulated noise over a long chain might impact the signal integrity.

Finally, at ultra-high operating frequencies, conventional CMOS inverters and, thus, inverter chain buffers can face certain limitations. Factors such as the lower mobility of holes in PMOS transistors compared to electrons in NMOS transistors can affect the switching speed. Additionally, at very high frequencies, effects like parasitic capacitances, inductances, and transmission line behavior of interconnects become more pronounced, potentially limiting the performance of inverter chains. For extremely high-speed applications, alternative buffer architectures might be considered.

While inverter chains are primarily digital components, they can sometimes be employed or adapted for specific analog signal conditioning scenarios. For example, the sharp switching threshold of a CMOS inverter can be used for crude level detection or signal shaping in certain non-critical analog applications. However, for precise linear amplification or more complex analog signal processing, dedicated analog buffer circuits are typically preferred over inverter chains.

X. CONCLUSION AND RECOMMENDATIONS

The effective design and application of inverter chain buffers require careful consideration of several factors. Designers should pay close attention to the load capacitance they need to drive and optimize the number of stages and the sizing of the inverters within the chain to achieve the desired performance in terms of delay and drive strength [10]. For applications involving clock signals, ensuring balanced rise and fall times is crucial to prevent duty cycle distortion.. Throughout the design process, it is essential to consider the impact of process, voltage, and temperature variations on the buffer's performance and to utilize simulation tools to verify its behavior under various operating conditions.

For future advancements, research continues to focus on optimizing inverter chain buffers for low-power and high-speed applications, especially in the context of increasingly scaled semiconductor technologies. Techniques for minimizing delay and power consumption while maintaining signal integrity and robustness against variability remain key areas of investigation. As digital circuits become more complex and operate at higher frequencies, the role of carefully designed and optimized inverter chain buffers will continue to be of paramount importance in ensuring the functionality and performance of integrated systems.

This 6-stage tapered buffer using 65nm CMOS technology effectively meets the specified load-driving and timing requirements at 1GHz while maintaining acceptable power consumption. The tradeoff study confirms that six stages provide an optimal balance, minimizing delay without excessive power penalties.

XII. REFERENCES

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4-Week Sprint Plan: Inverter Chain Buffer Project

Project Duration: 21 March 2025 - 17 April 2025

Sprint	Dates	Objectives	Deliverables	Team Members
Week 1	21 Mar - 26 Mar	Literature survey, choose technology node (<1µm), gather IEEE citations, and define design goals.	Survey document, selected tech node, list of citations, problem definition.	Hadeel Faheem (Literature Survey)
Week 2	27 Mar - 02 Apr	Design inverter chain buffer (logical effort, stage sizing), start LTSpice schematic and model integration.	Initial schematic, inverter sizing calculations, model libraries setup.	Fatima Imran (LTSpice Design and Simulation)
Week 3	03 Apr - 09 Apr	Complete LTSpice simulations (transient, power analysis), measure rise/fall times and delays at all nodes.	Simulation screenshots, waveform plots, power-delay analysis.	Fatima Imran (LTSpice Simulation, Analysis)
Week 4	10 Apr - 16 Apr	Start layout design in Microwind. Finalize report: insert schematic, waveforms, analysis, apply project management summary, and review.	Full report with all sections, appendices, and sprint summaries.	Aiman Sabir (Project Management, Report Presentation), Abdullah Wasi (Microwind)

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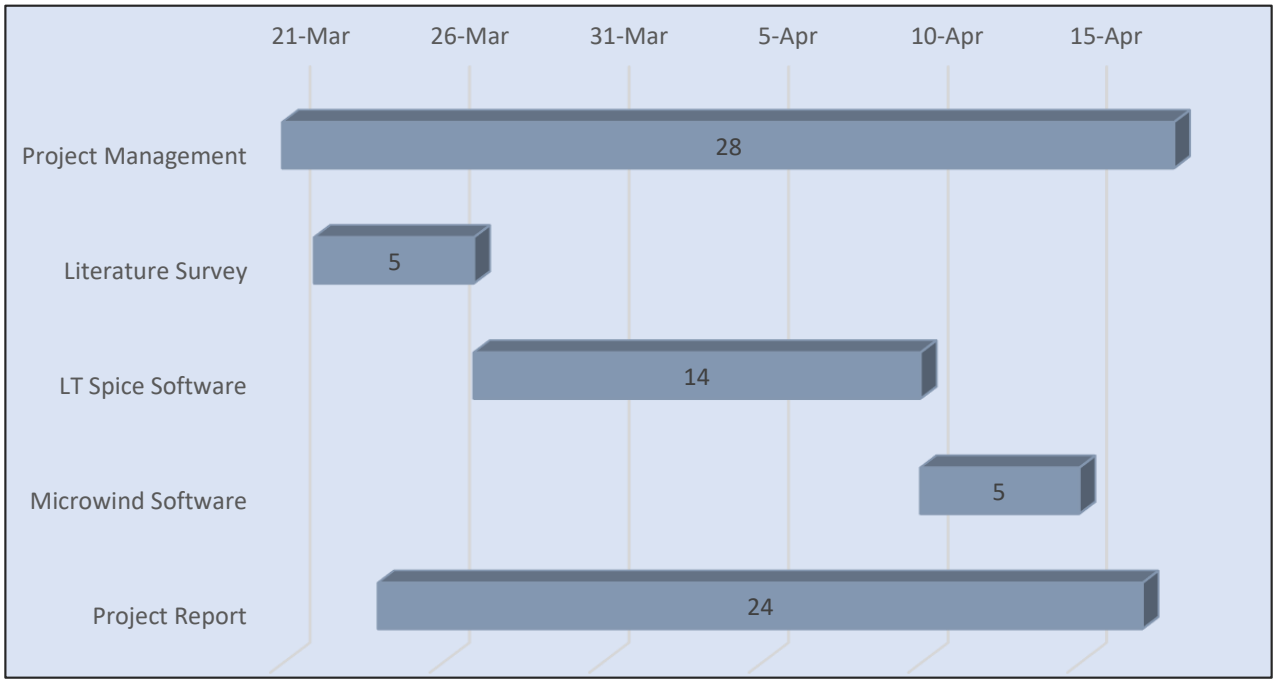
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