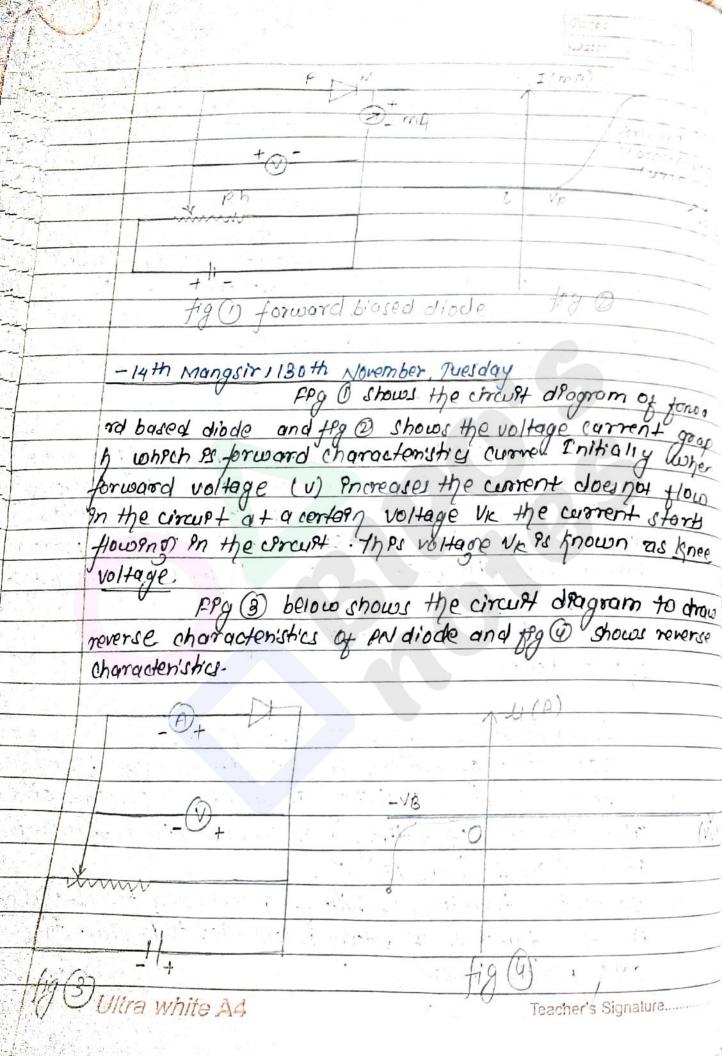
In this case, the radioactive Date: 4. In this case, the stable nucleus es almeady unstable nucleus turnes proto unstable and finally turns into stable nucleus. Semiconductor Service. [tolerance es high] P-N function (or sem ?- conductor dode) Eg :- Germinium Seme conductor having half pentavalent dropping and half trivalent dopping pe known as P-N junction. The region where the two doped region meet Ps called p-Njunchion at the Enstant of junction formation free lelection on N-spore drypt towards p-spore depletion region and near the junction they combine and there fare some region near the function gets deflected from holes and freeelectrons these region is called deflection region. Potential
difference developed across deflection region is colled potential
barnier denoted by VB. It value is 0.3 ev for (SP) diode and 0.7 volt for (ge) Node. Frg (2) shows the corcupt symbol of P-N diode Characteristics curve for P-NdPode.

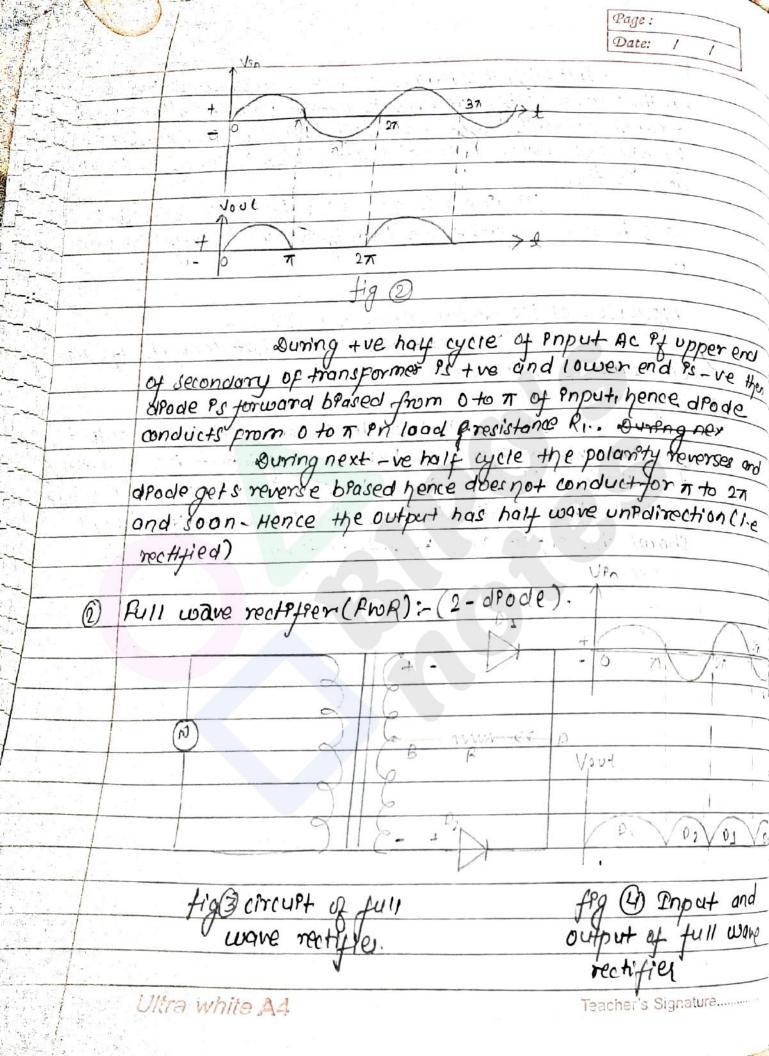
Connection of battery in a circupt is colled blasend. 4) It positive terminal of battery is connected to p-side and neg brive terminal of battery y 95 connected to N-side then 97 95 called forward brasing. If pastitue terminal of battery as connected to N-side and regative terminal of battery is connected to P-side then it is colled negative blassnop Ultra white A4 Teacher's Signature.....



Control of the sea Internity up a consider important to design our into believe to - or the resource as large reaches to making such a - ve the access by very high owners proved the variety of several boards (Aut also que en claure in sont ou minutes pour on the comes because of gots fined I domage of due to many high come De Is brown as rectifier. Holf wave rectifier when I PN drode is connected to the output of a transformer then only half wave of mont ac is mittigen and the circuit is known as half wave margar. Fig @ toto w shows the circuit diagram of half wave routifier fig(5) Shows the enpert and surpert bottoger TIA DEFRONT OF KIND

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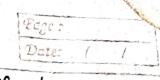


fig (3) shows full wave rectifier using I connected two drode p, and p, and from shows the input and output sign als of full wave rectifier.

And the tre half cycle of Priput Ac. Let the appearance of the and lower end is negative. Then also be (DI) will be forward brosed and will conduct through load resistance along AB. while (B) to be

In neversed brased does not conduct. For, the next-ve half cycle the polarity reverses, De gets forward brased and conduct through load resistance (R.) along AB while diade De being

reversed brased does not conduct from A to 27 and . so on.
Thus, the output has full wave rectified
[1-e unid rectional

Full wave bridge recit recitifier

Yout 1

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fig @ Input and output of full was

D(-> AC: W Page: AC-7 OC = rechification In full wave rectifier. 4 diodes & 1, D2, D3, A

nnected to the secondary of transformer along with
pristance R Pn the form of a bridge as shown in figuresistance. During the holf cycle of input AC of upper end of along the holf cycle of input AC of upper end of and lower and is a rether address of the analysis of the an Now, Pn the next -ve half cycle of Pnput Ac larsty reverses making Ds, Bu forward brosed and D, 1B, erse brased. So. D.3, Du conduct a through RL along An d Di, 22 docanot conduct. thus output as unidirection (1 e mortifier) Teacher's Signature.... Ultra white A4

2 → 0 ml

Pago → 0 f l

Date: / /

Logic gates:
The electronic circuit that gives the output corresponding to different input is called loope gates. It can ave one or more inputs but only one output

OR gate:
OR gate:
OR gate hos two or more Populs but only one

Output. The output Ps hPgh (+) when one or more inputs

are hPgh. #9 (1) below shows the 100 PC symbol of twols

Propute OR gate and toble (1) shows Hs truth table.

-H •	+	9=4+6 - Op+pu	
В			
10	fig-O	3	
(8)	lock diagram of	OR gode) 5	
Table: -	· /		
	Inputs A B	Outputs.	
	0 0	0	
	0 1	1	
	1 0	1	
	1 1.	1.	-2211 1-2
it, for the late	Mr. State of Mr	The Control	
	come out his time		

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			Page: OR Date: /
* 101			
1 K-1	AND gate:-	2 -1 -0 10 16	21/2-11/2
	And gate	PS a logic gate the	L PS high only when all
•	anputs but only one	output. The output	F PS might when all
4	Inputs are high.	1 10 and 2 may (1 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2	
	Fig () Show	us the block dragne	on of two mout AND gave
	and Table I shows A	s thru truth topic	Two
		g a class to the second	
1 1 1	A		11 0 10
	e factorial design and sold	NWO)	J=A·B
	page date and		Oupul
	B inputs		
		fig=1(Block	diagram of AND gare
			1 1 1 1 1 1
	Pable 1; Pruth Table	! OF AND gate:-	
	Table 1) fram		
-	annull		
	2nputs	Outputs	
-	AB	0017	
	0 0		7:3:00
	0 0	0	
	0 1	0	
	1 0	Q	
	1 1	1	
10	INT OUR !-		
1	107 9462	2 10:01: 0:10	which has one input an inverted input.
-	NOT gare 9	s a logic gare	which has one input un
0	nly one output. The	output of the i	inverted input.
	V	i i	,
1	_		1
1	A	outrut	
	Imput	4 = A	
	fig O	Block diogram	of No-gate.
	Ultra white A4		Teacher's Signature
Sign of			

2 3		
		Fage:
		Date: / /
Table 2: Truth +	able of NOT	gate:-
Enput A Output y	1=A	

NAND GATE :gate. It may have two or more Inputs but only one output gate. It may have go any when all inputs one high w. s. - The output is low only when all inputs one high w. .

If (3) Shows the block diagram of two inputs NAND CHATE and table (3) shows its truth table.

BURA OUTPUT B Input fig-3 (Block dragrom of NAND Table 3: Truth table of NAND GATE. Inputs Output B A 0 0 1 0 1 1 0

NOT

Y = A.B

NOP GATE: - OR gate followed by NOT grass or called NOR gate . It may have two more enputs but only one Output

Tig (4) Shows block diagram of two inputs NOR gate
Ultra white A4 table (4) Shows At thruth table signature.

