

DA-IICT

CT215 LAB5

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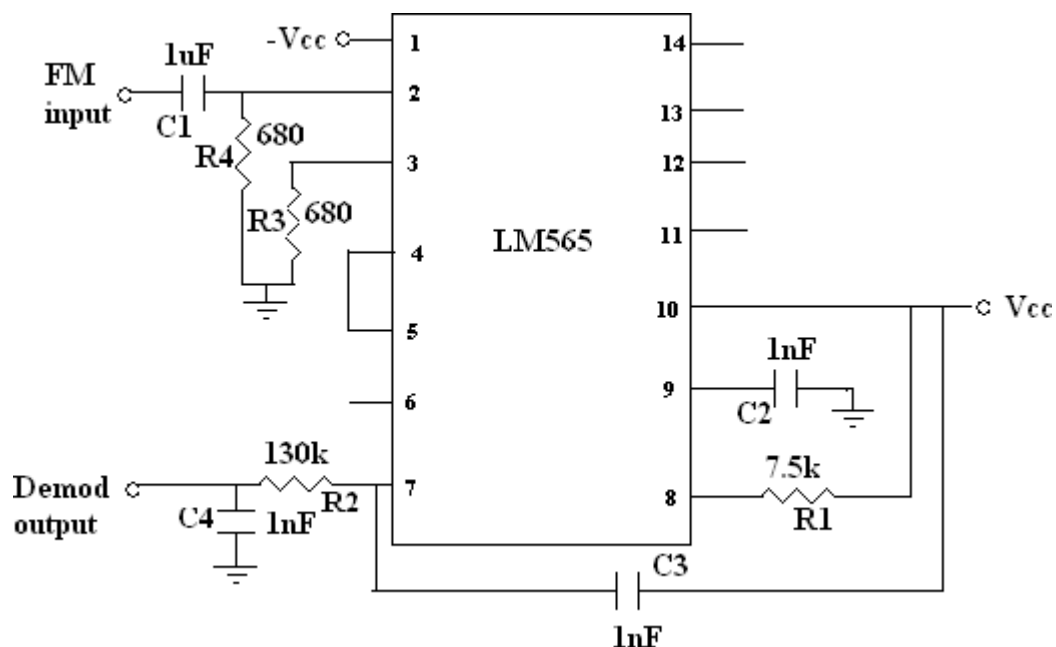
Date: 8th March 2021

Aim: To perform FM demodulation using Phase Locked Loop (PLL).

Apparatus:

- Function Generator
- DSO
- IC LM565
- Power supply
- Resistors
- Capacitors

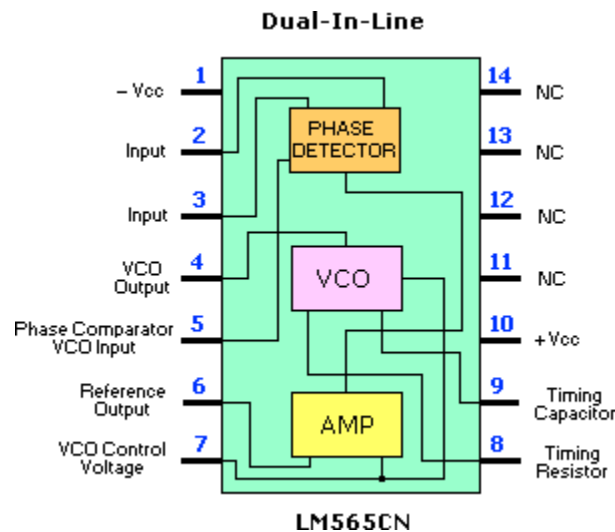
Circuit Diagram:



Procedure:

- 1) Connect the FM demodulator circuit as shown above.
- 2) Take FM input from function generator. You need to share this signal with neighboring group using T. Keep carrier frequency $F_c = 35$ KHz and amplitude $A_c = 5$ Vpp and message signal frequency $F_m = 1$ KHz and amplitude $A_m = 4$ Vpp.
- 3) Observe the demodulated output across $C4$, and measure the frequency of demodulated output and compare with message signal.
- 4) Draw waveforms of message signal, FM signal and demodulated signal.
- 5) Vary modulating signal frequency and observe the output.

Components of Phase Locked Loop (PLL):

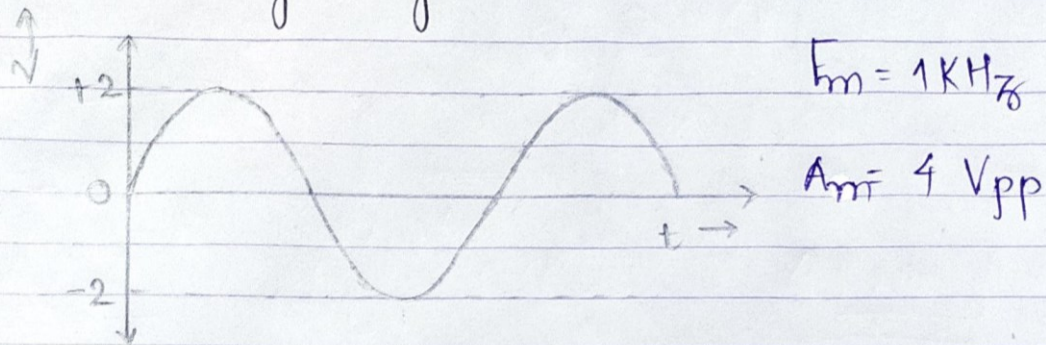


Explanation:

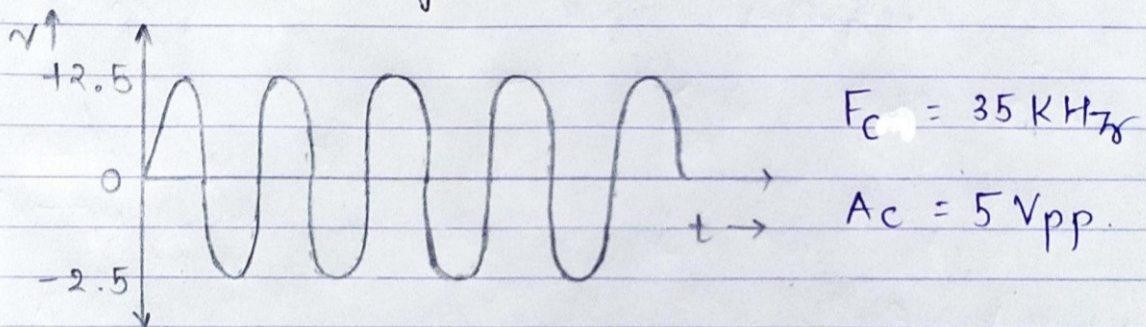
- The input FM signal and the output of the VCO is applied to the phase detector circuit.
- The output of the phase detector is filtered using a low pass filter, the amplifier and then used for controlling the VCO.
- When there is no carrier modulation and the input FM signal is in the center of the pass band (i.e., carrier wave only) the VCO's tune line voltage will be at the center position.
- When deviation in carrier frequency occurs (that means modulation occurs) the VCO frequency follows the input signal in order to keep the loop in lock. As a result, the tune line voltage to the VCO varies and this variation is proportional to the modulation done to the FM carrier wave. This voltage variation is filtered and amplified in order to get the demodulated signal.
- So, here PLL circuit makes sure that input and VCO output frequency will be equal in phase and here loop is in **"locked"**. And if there is phase difference then between two signals loop is **"unlocked"**. So PLL circuit synchronizes VCO output signal with the input signal and reduce any error in phase that may occur.
- This synchronization is significant as the amplitude of message is reflected in the frequency of input signal (modulated signal), which is a part of phase of modulated signal. The frequency range the PLL is able to lock - in when starting from an unlocked loop is called **"Capture range"**. And the frequency range the PLL is able to follow the input frequency variations once loop is locked is called **"Lock range"**.

Waveform Plots:

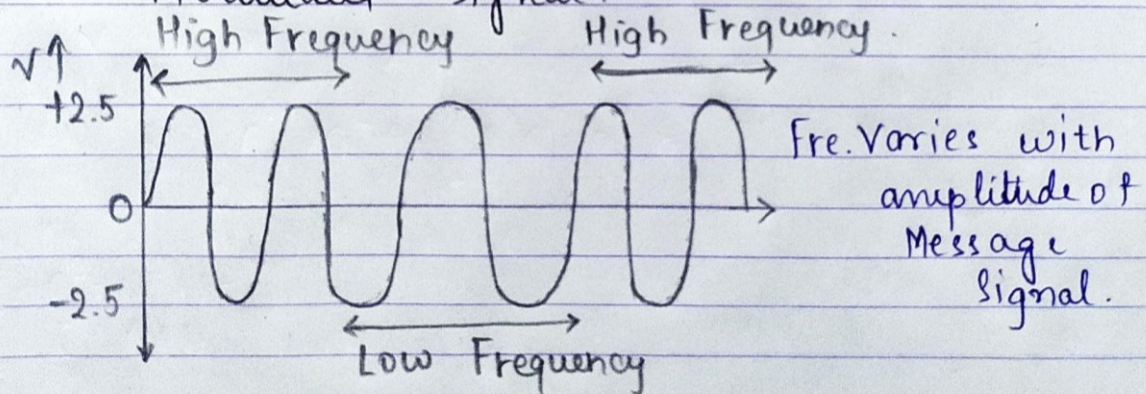
→ Message Signal:-



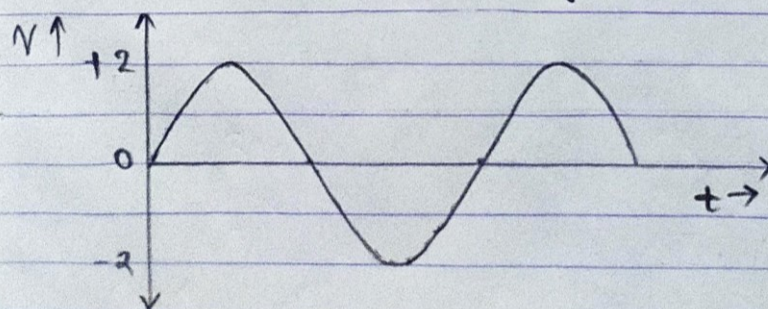
→ Carrier signal:-



→ Modulated signal:-



→ Demodulated signal:-



Conclusion:

- The Phase - Locked loop will be locked whenever the input frequency enters in the capture range and then for the entire lock range it remains locked.
- On answering the effect of varying Modulating signal frequency on the demodulated output is as follows: Varying F_m and keeping the frequency deviation constant will affect the bandwidth of the spectrum very slightly. Hence, known as the constant bandwidth system.
- We are simply collecting the error values given by the phase detector.