Dhirubhai Ambani Institute of Information and Communication Technology

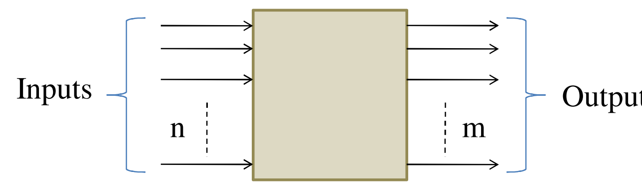
EL114

Digital Logic Design

Dr. Yash Agrawal
Assistant Professor,
DA-IICT, Gandhinagar

Introduction

Combinational logic Circuit



Multiplexer (MUX)

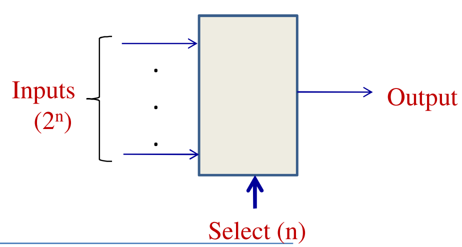
Multiplexer:

Many inputs to One output.

The inputs are selected based on the select line(s).

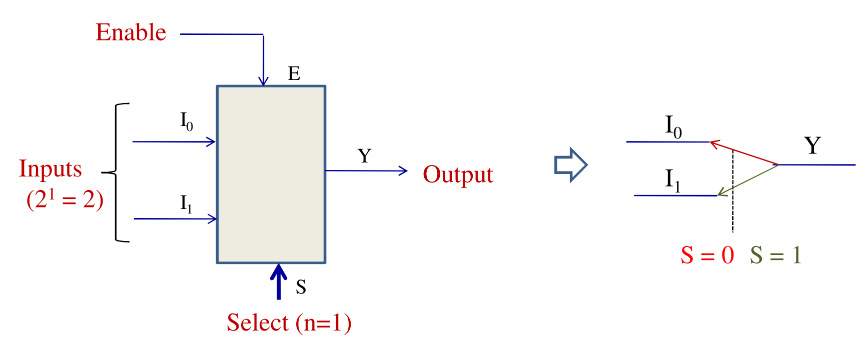
The inputs are in the form of 2^n, where n is the select line.

Used in many switching applications, implementing logic.



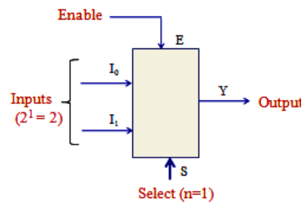
Multiplexer Example

2:1 Multiplexer:



Multiplexer Example

2:1 Multiplexer:



Number of Inputs = 4 (E, S, I_1, I_0)

⇩

Number of Input Combinations = $2^4 = 16$

Please Note: Enable is optional. And Many MUX may not have Enable input.

First Step:
Truth Table Formation

Determined number of inputs to be 4

Determined number of outputs to be 1

Inputs of 2:1 MUX | Output of MUX

E	S	I_1	I_0	Y
0	0	0	0	z
0	0	0	1	z
0	0	1	0	z
0	0	1	1	z
0	1	0	0	z
0	1	0	1	z
0	1	1	0	z
0	1	1	1	z
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

2:1 Multiplexer

Second Step:
Determining Boolean Expression
(For this K-map can be used)

K-map and Boolean Expression determination for Y

ES \ I_1I_0	00	01	11	10
00	m0	m1	m3	m2
01	m4	m5	m7	m6
11	m12	m13	1 m15	1 m14
10	m8	1 m9	1 m11	m10

Y= $ES'I_0 + ESI_1$

Inputs of 2:1 MUX | Output of MUX

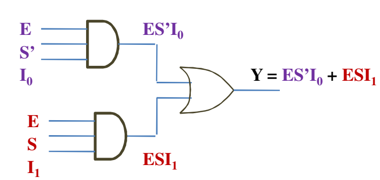
E	S	I_1	I_0	Y
0	0	0	0	z
0	0	0	1	z
0	0	1	0	z
0	0	1	1	z
0	1	0	0	z
0	1	0	1	z
0	1	1	0	z
0	1	1	1	z
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

2:1 Multiplexer

Third Step:
Realization of Boolean Expression by Logic Gates

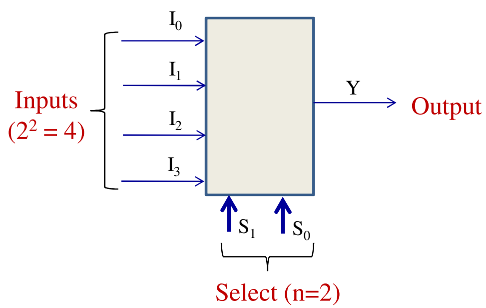
$Y = ES'I_0 + ESI_1$

⇩



Multiplexer Example

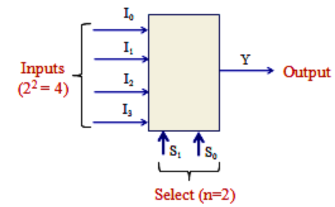
4:1 Multiplexer:



Please Note: Here Enable is not shown. However, in practical ICs Enable input shall be present.

Multiplexer Example

4:1 Multiplexer:



Number of Inputs = 6 (S_1, S_0, I_3, I_2, I_1, I_0)

Number of Input Combinations = $2^6 = 64$

4:1 Multiplexer

First Step:
Truth Table Formation

Number of Input Combinations = $2^6 = 64$

Its huge to tabulate, hence can be concisely given as

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

4:1 Multiplexer

Second Step:
Determining Boolean Expression

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

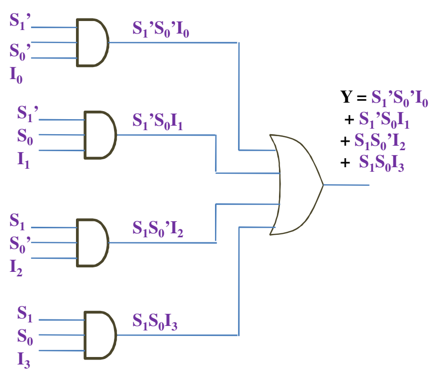
$$Y = S_1'S_0'I_0 + S_1'S_0I_1 + S_1S_0'I_2 + S_1S_0I_3$$

4:1 Multiplexer

Third Step:
Realization of Boolean Expression by Logic Gates

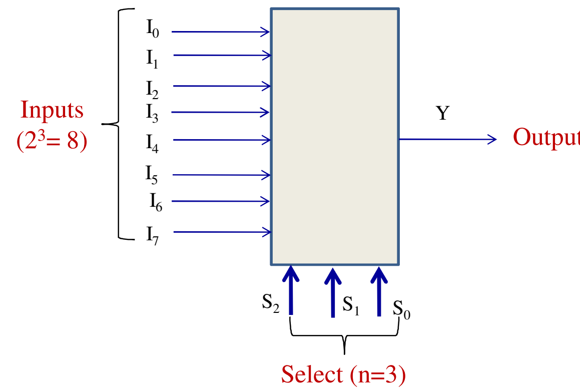
$$Y = S_1'S_0'I_0 + S_1'S_0I_1 + S_1S_0'I_2 + S_1S_0I_3$$

⇨



Multiplexer Example

8:1 Multiplexer:



8:1 Multiplexer

First Step:
Truth Table Formation

S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

8:1 Multiplexer

Second Step:
Determining Boolean Expression

S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

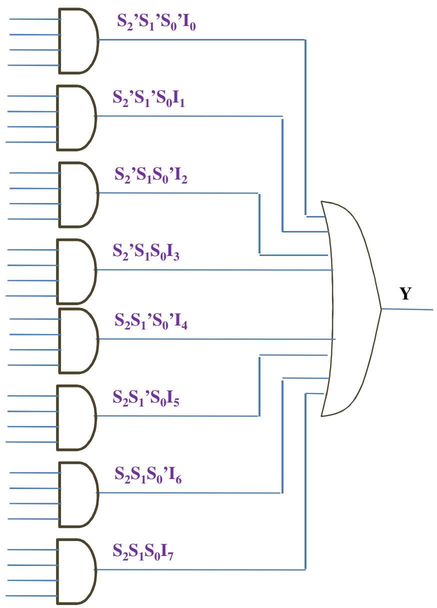
⇨

$$Y = S_2'S_1'S_0'I_0 + S_2'S_1'S_0I_1 + S_2'S_1S_0'I_2 + S_2'S_1S_0I_3 + S_2S_1'S_0'I_4 + S_2S_1'S_0I_5 + S_2S_1S_0'I_6 + S_2S_1S_0I_7 +$$

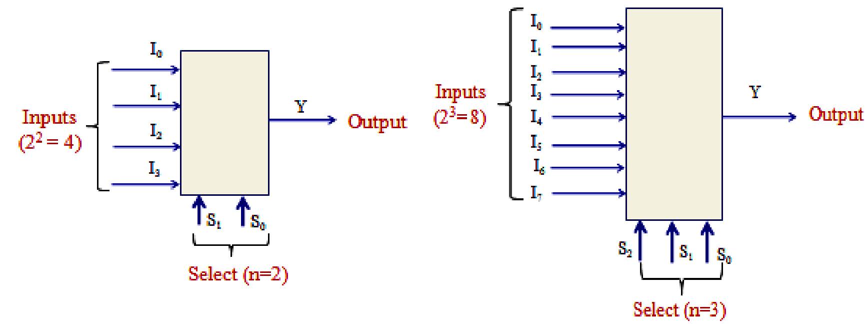
Third Step:
Realization of Boolean Expression by Logic Gates

$$
\begin{aligned}
Y = {} & S_2'S_1'S_0'I_0\ + \\
& S_2'S_1'S_0I_1\ + \\
& S_2'S_1S_0'I_2\ + \\
& S_2'S_1S_0I_3\ + \\
& S_2S_1'S_0'I_4\ + \\
& S_2S_1'S_0I_5\ + \\
& S_2S_1S_0'I_6\ + \\
& S_2S_1S_0I_7\ +
\end{aligned}
$$

⇨



Implement 8:1 Multiplexer using 4:1 Multiplexer



4:1 MUX
4 Inputs
2 Select lines
1 Output

8:1 MUX
8 Inputs
3 Select lines
1 Output

Implement 8:1 Multiplexer using 4:1 Multiplexer

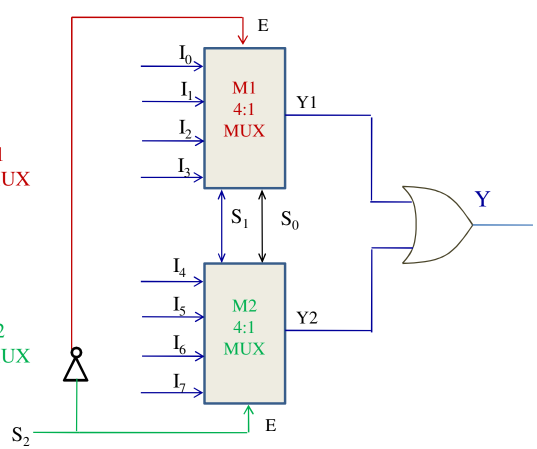
To implementing 8:1 MUX using 4:1 MUX, Enable signal can be utilized

E

S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

M1
4:1 MUX

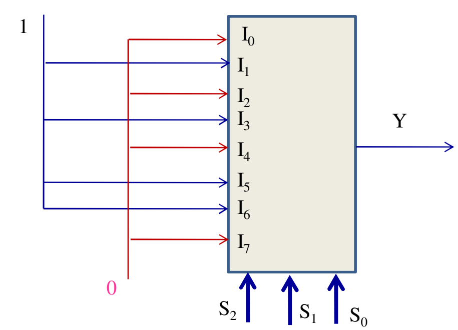
M2
4:1 MUX



Numerical

1. Implement the following Boolean Function using 8:1 MUX.

   $f(A, B, C) = \Sigma m(1, 3, 5, 6)$



Numerical

2. Implement the following Boolean Function using 4:1 MUX (without using any Enable signal).

$f(A, B, C) = \Sigma m(1, 3, 5, 6)$

First Step:
Truth Table Formation

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Numerical

2. Implement the following Boolean Function using 4:1 MUX (without using any Enable signal).

$f(A, B, C) = \Sigma m(1, 3, 5, 6)$

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Second Step:
Implementation Table Formation

A \ BC	I_0	I_1	I_2	I_3
0	0	1	2	3
1	4	5	6	7
	0	1	A	A'

Rules:
Scan Each column
1. If No Circle – Place '0'
2. If All Circles – Place '1'
3. If Single Circle – Place corresponding A/A'

Please Note: Implementation table is different from K-Map.

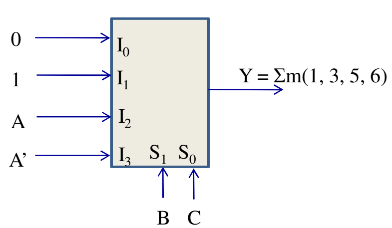
Numerical

2. Implement the following Boolean Function using 4:1 MUX (without using any Enable signal).

$f(A, B, C) = \Sigma m(1, 3, 5, 6)$

Third Step:
Realize the circuit

A \ BC	I_0	I_1	I_2	I_3
0	0	1	2	3
1	4	5	6	7
	0	1	A	A'



Assignment-3

1. Implement the following Boolean Function using 8:1 MUX (without using any Enable signal).

$f(P, Q, R, S) = \Sigma m(0, 1, 3, 4, 8, 9, 15)$