Dhirubhai Ambani Institute of Information and Communication Technology

EL114

Digital Logic Design

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Level of Abstraction

High Level Language Program (E.g. C)

```
temp = v[k];
V[k] = v[k+1];
V[k+1] = temp;
```

Compiler

Assembly Language Program (E.g. MIPS)

```
lw  $t0, 0 ($2)
lw  $t1, 4 ($2)
sw  $t1, 0 ($2)
sw  $t0, 4 ($2)
```

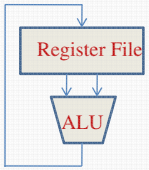
Assembler

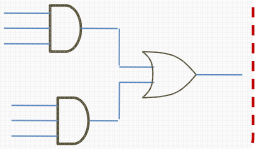
Machine Language Program (MIPS)

```
0000 1001 1100 0110 1010 1111 0101 1000
1010 1111 0101 1000 0000 1001 1100 0110
1100 0110 1010 1111 0101 1000 0000 1001
0101 1000 0000 1001 1100 0110 1010 1111
```

Machine Interpretation

Hardware Architecture Description (Block Diagram)





Machine Interpretation

Logic Circuit Description (Gate and Circuit Diagram)

Introduction

What is
Combinational
&
Sequential
Concept…?

Logical Interpretation

Combinational vs. Sequential

1. Concept of Execution

Logical Interpretation

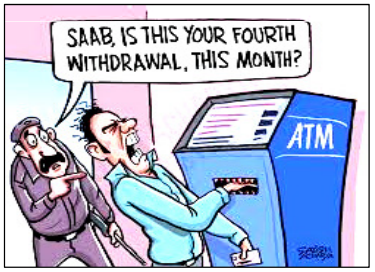
Combinational vs. Sequential

2. Concept of Memory

Logical Interpretation

Combinational vs. Sequential

3. Concept of Input(s) Present/Requirement

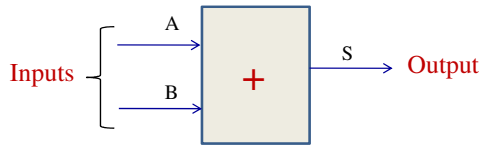


Practical Inference

Combinational vs. Sequential

1. Implement

$S = A + B$



Practical Inference

Combinational vs. Sequential

2. Implement

$S = S + (A + B)_i$

where i is integer and varying with time.

$S = 0$ at starting of time i.e. at $i = 0$

⇩

$S = 0$

for $(i = 1, i < t, i = i+1)$

$S_i = S_{i-1} + (A + B)_i$

Combinational vs. Sequential

2. Implement

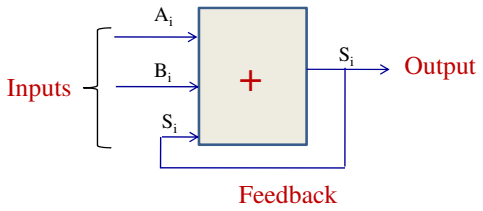
$S = 0$
for $(i = 1, i < t, i = i+1)$
$S_i = S_{i-1} + (A + B)_i$

Can You realize it using combinational logic…?

Combinational vs. Sequential

2. Implement using Sequential Logic

$S = 0$
for $(i = 1, i < t, i = i+1)$
$S_i = S_{i-1} + (A + B)_i$

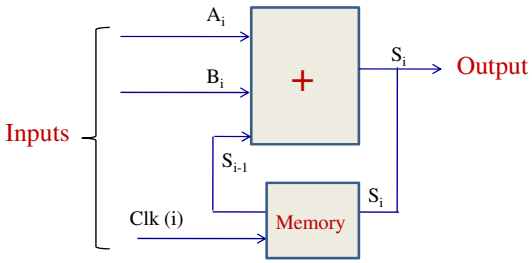


Does this work

Combinational vs. Sequential

2. Implement using Sequential Logic

$S = 0$
for $(i = 1, i < t, i = i+1)$
$S_i = S_{i-1} + (A + B)_i$



Now validate the discussed points for sequential logic as in 'Logical Interpretation'.

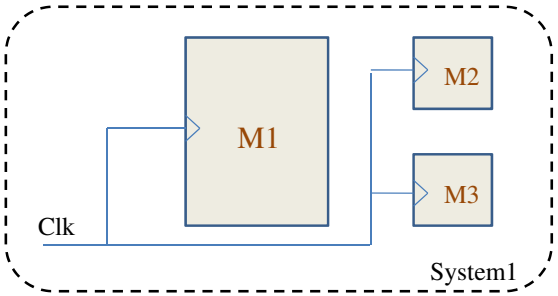
- ✓ Concept of Execution
- ✓ Concept of Memory
- ✓ Concept of Input(s) Present/Requirement

- Memory Requirement
- Clock/Enable Requirement
- Inputs
- Speed
- Design Complexity

Synchronous Systems

All operations are controlled by one central common clock signal.

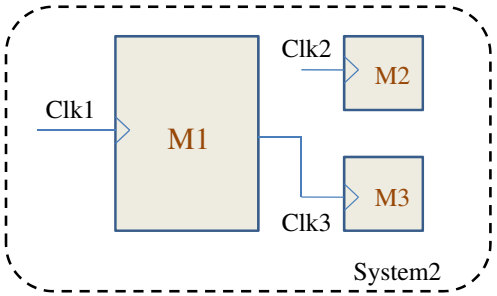
The clock signal is used to determine/control the exact time at which any output can change its state



Asynchronous Systems

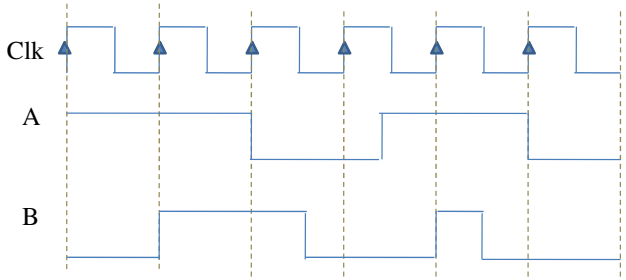
Different modules are triggered by different clock/controlling signals.

In Asynchronous systems, the output of the logic circuit can change its state at any time, as soon as any input changes its state.

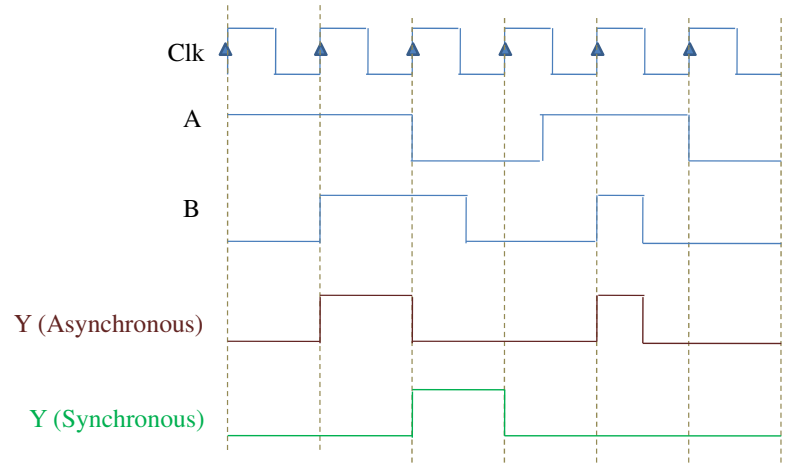


Numerical

1. Determine the output of 2-input single-bit AND gate for the given set of inputs for the following cases
   (i) If the system is designed as Asynchronous.
   (ii) If the system is designed as Synchronous.



Numerical



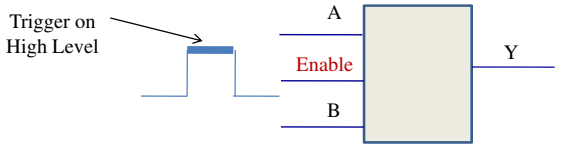
Control Signals

- Sequential circuits are dependent on the control trigger signals that are provided at its input.
- Depending on type of control signal, the output of the sequential circuit changes.
- There are four major control Trigger signals as

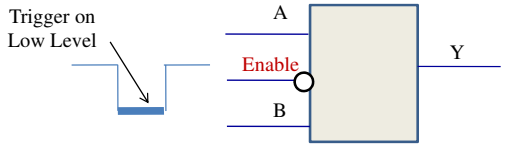
1. High Level Triggering
2. Low Level Triggering
3. Positive Edge Triggering
4. Negative Edge Triggering

Control Signals

1. High Level Triggering

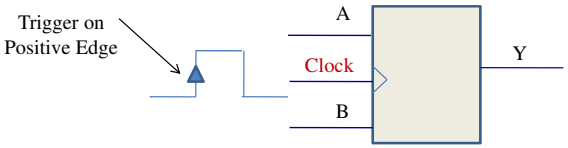


2. Low Level Triggering

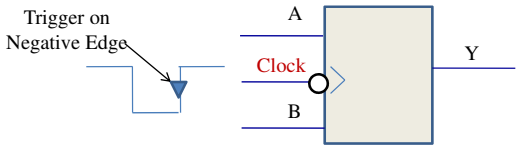


Control Signals

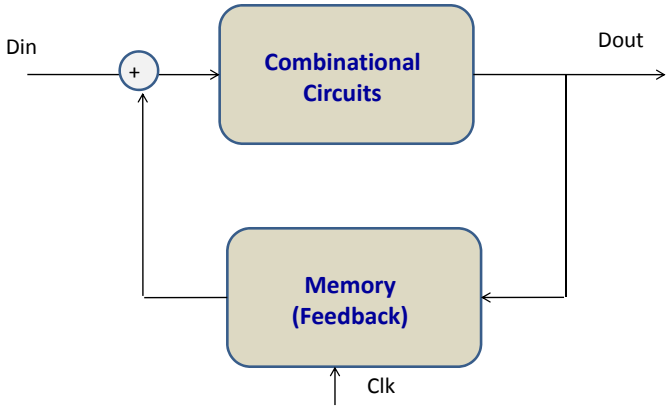
3. Positive Edge Triggering



4. Negative Edge Triggering



Sequential Circuit



Basic Building Blocks of Sequential Circuits

Types of latches and Flip-flops

- S-R
- D
- J-K
- T

Inter-conversion between different flip-flops

Sequential Circuits

- Register
- Counter

Sequential Circuits

Numericals

on

Sequential Circuits