

Dhirubhai Ambani Institute of Information and Communication Technology

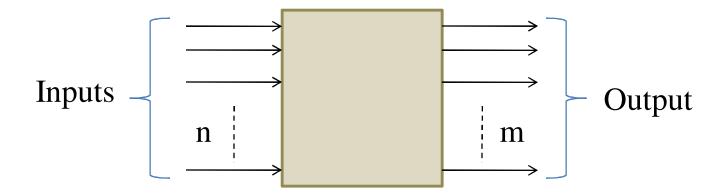
EL114

Digital Logic Design

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Introduction

Combinational logic Circuit



Combinational Circuits

Combinational Circuit Realization for

- Given Statement and Requirement
- Given Truth Table

Given Boolean Expression, Minterms/Maxterms

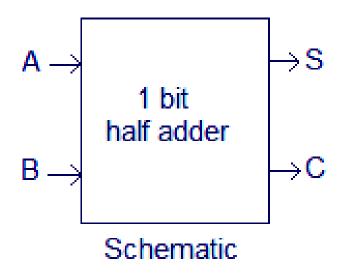
Combinational Circuits

Combinational Circuit Realization for

Various Code-converters

- Various Half Adders/Full Adders
- Various Half Subtarctors/Full Subtractors

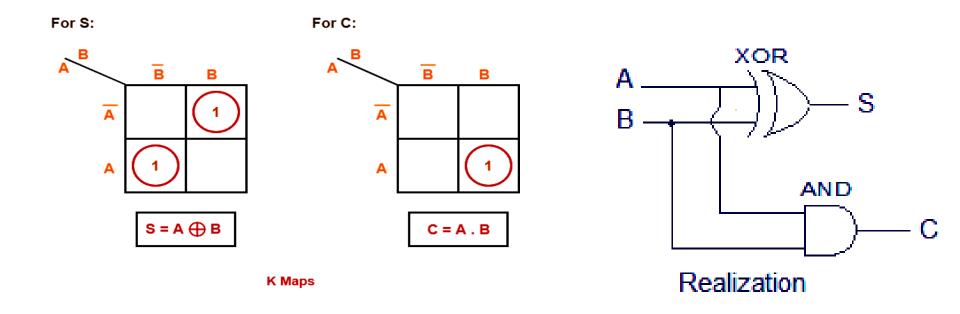
Half Adder and Full Adder



Inputs		Outputs		
Α	В	S	U	
0	0	0	0	
1	0	1	0	
0	1	1	0	
1	1	0	1	

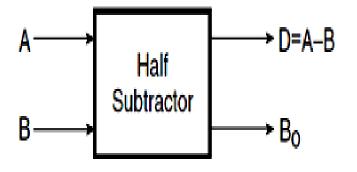
Truth table

Half Adder and Full Adder



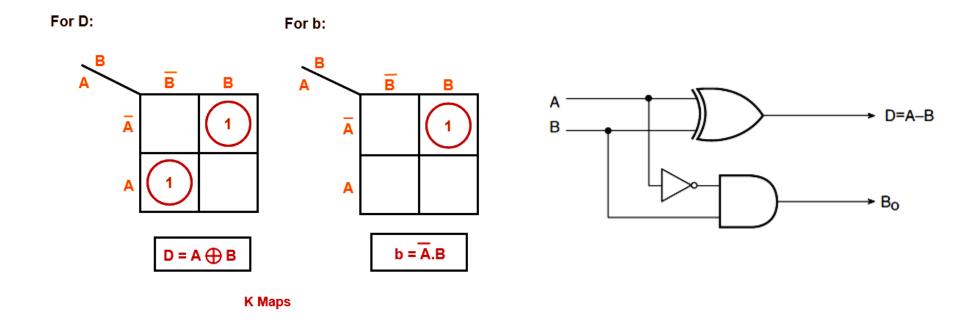
Assignment: Try to realize Full Adder using logic Gates

Half and Full Subtratcor



Α	В	D	Bo
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Half and Full Subtratcor



Assignment: Try to realize Full Subtractor using logic Gates

Combinational Circuits

Combinational Circuit design using various Integrated Circuits (ICs)/ Digital Blocks

- Multiplexer
- Demultiplexer
- Encoder

Decoder

Multiplexer (MUX)

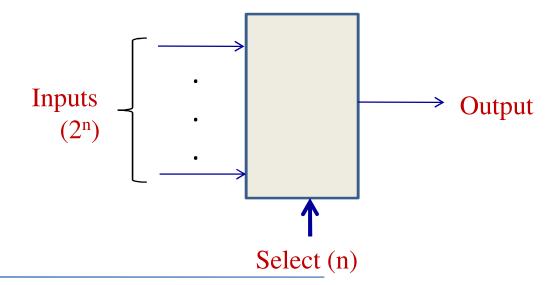
Multiplexer:

Many inputs to One output.

The inputs are selected based on the select line(s).

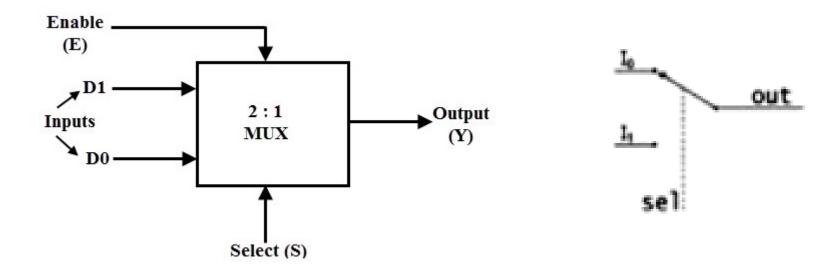
The inputs are in the form of 2ⁿ, where n is the select line.

Used in many switching applications.



Multiplexer Example

2:1 Multiplexer:



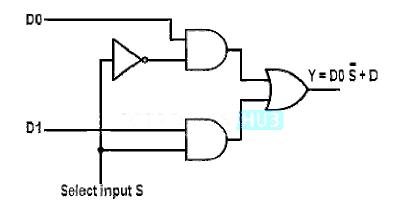
Multiplexer Example

2:1 Multiplexer:

$$\mathbf{Y} = \mathbf{D}_0 \, \mathbf{\bar{S}} + \mathbf{D}_1 \, \mathbf{S}$$

Enable(E)		
Inputs D0	2:1 MUX	Output (Y)
	Select (S)	

Select	Inputs		Output
0	0	0	0
0	0	1	1
1	1	0	1
1	1	1	1



Assignment: Try to realize 4:1 multiplexer, 8:1 multiplexer

Demultiplexer (DeMUX)

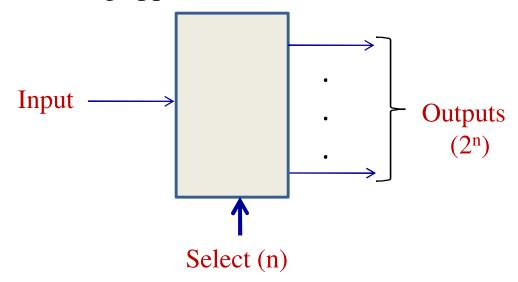
Demultiplexer:

One input to Many outputs.

The Output line is selected based on the select line(s).

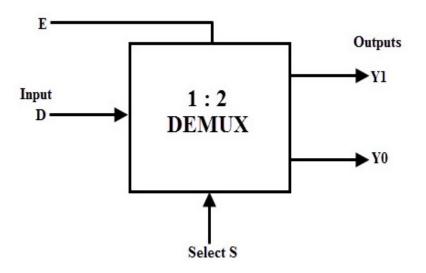
The outputs are in the form of 2ⁿ, where n is the select line.

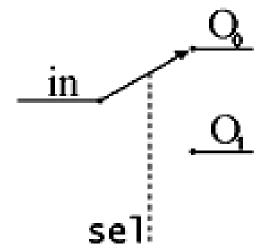
Used in many switching applications.



Demultiplexer Example

1:2 Demultiplexer:

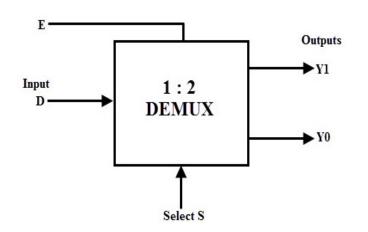


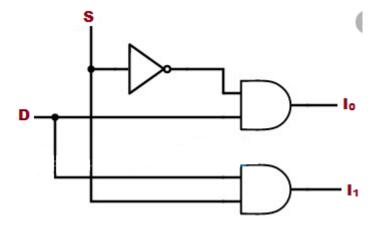


Demultiplexer Example

1:2 Demultiplexer:

Select	Input	Out	puts
S	D	Υ ₁	Y ₀
0	0	0	0
0	1	0	1
1	0	0	0
1	1	1	0





Assignment: Try to realize 1:4 demultiplexer, 1:8 demultiplexer

Encoder

Encoder:

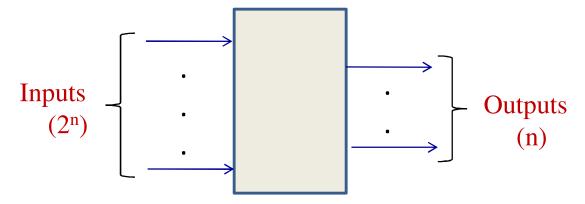
2ⁿ inputs to n outputs.

The Outputs are defined based on the active input line.

Usually only one input is active at a time or otherwise priority line is added to resolve ambiguity.

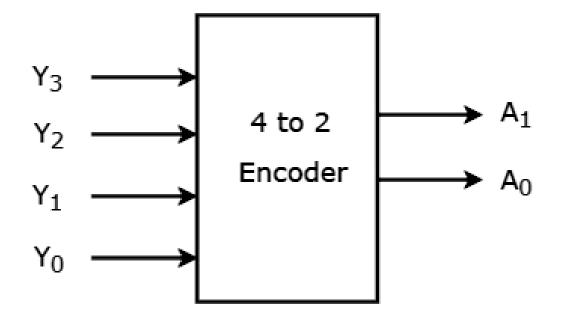
It possesses No select line.

Used in many code converters, modulators, controller designs, etc.



Encoder Example

4:2 Encoder:

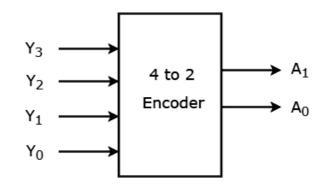


Encoder Example

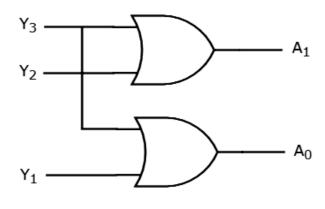
4:2 Encoder:

$$A_1 = Y_3 + Y_2$$

$$A_0 = Y_3 + Y_1$$



Inputs				Outputs		
Y ₃	Y ₂	Y ₁	Υ ₀	A ₁	A ₀	
0	0	0	1	0	0	
0	0	1	0	0	1	
0	1	0	0	1	0	
1	0	0	0	1	1	



Assignment: Try to realize 8:3 Encoder, 8:3 Priority Encoder

Decoder

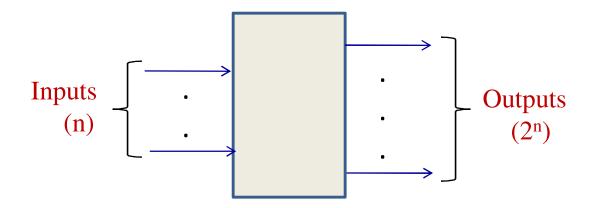
Decoder:

n inputs to 2ⁿ outputs.

Based on inputs, one of the active line goes to logic high (becomes active).

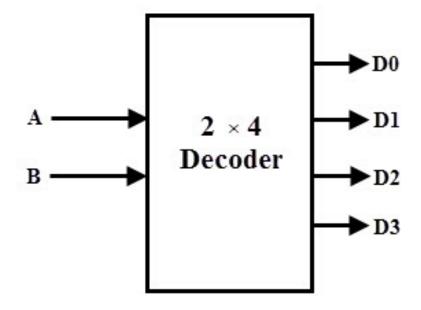
It possesses No select line.

Used in many code converters, demodulators, controller designs, etc.



Decoder Example

2:4 Decoder:



Decoder Example

2:4 Decoder:

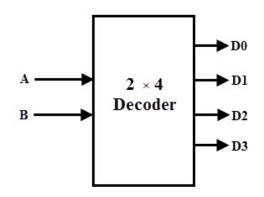
Truth Table

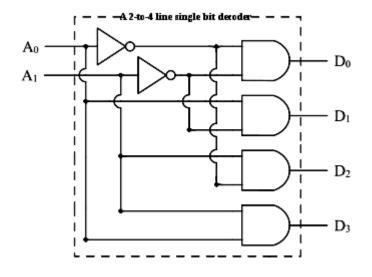
A_1	A_0	\mathbf{D}_3	D_2	\mathbf{D}_1	\mathbf{D}_0
0	Ō	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Minterm Equations

$$\begin{aligned} D_0 &= \overline{A}_1 \cdot \overline{A}_0 \\ D_1 &= \overline{A}_1 \cdot A_0 \\ D_2 &= A_1 \cdot \overline{A}_0 \\ D_3 &= A_1 \cdot A_0 \end{aligned}$$

Assignment: Try to realize 3:8 Decoder





Combinational Circuits

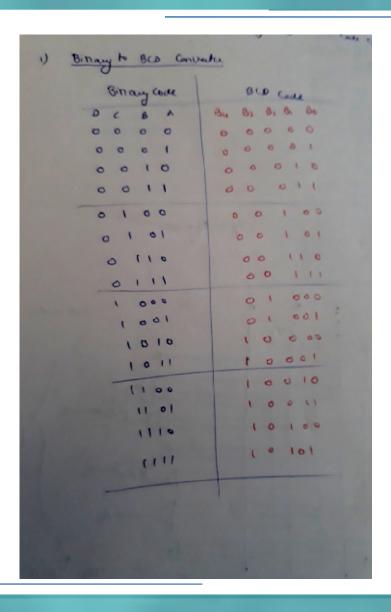
Numericals and Combination Circuit Realization

using

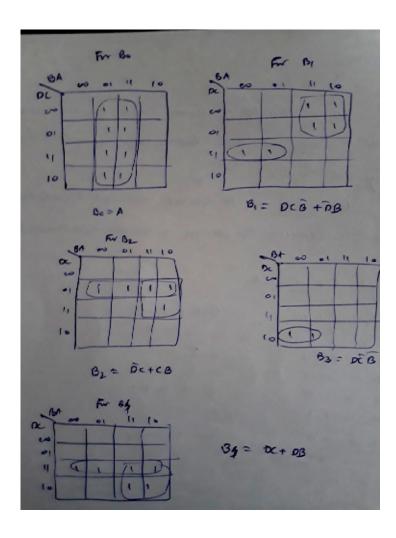
Multiplexers, Demultiplexers,

Encoders and Decoders

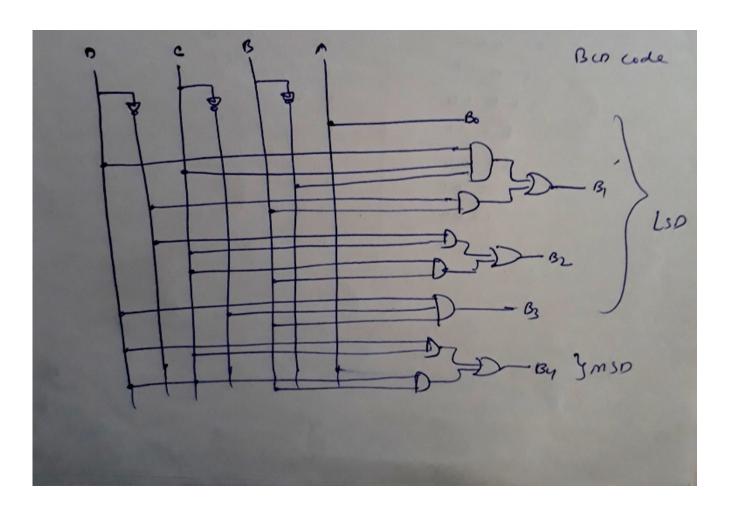
Code Converter Example



Code Converter Example



Code Converter Example



Assignment: Practice more numericals from text books.