Dhirubhai Ambani Institute of Information and Communication Technology

EL114

Digital Logic Design

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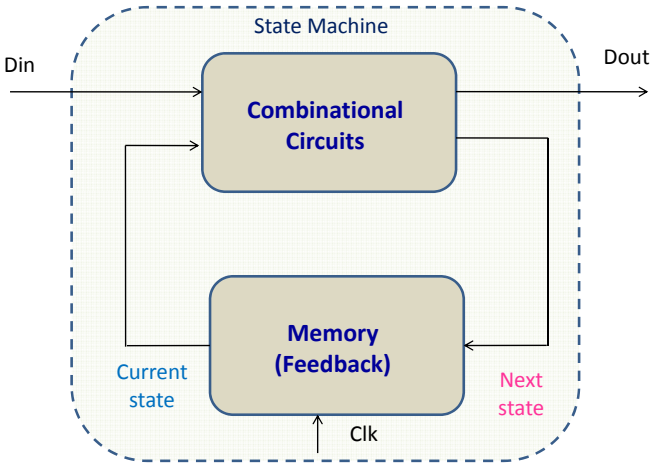
Introduction

Sequential Circuit



Applications of Flip-flop

- Memory design and data storage
- Logic control devices
- Shift registers
- Frequency division
- Counters

Introduction

Counters

What is Counter…?

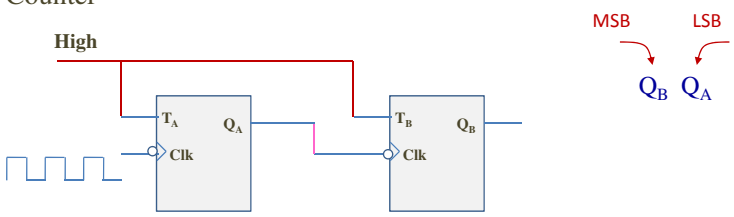
Types of Counters

- Asynchronous (Ripple)
- Synchronous

- Also called Ripple Counter/Serial Counter.
- Clock to all modules/flip-flops doesn't change at same time.
- The invalid states are by-passed by providing a suitable feedback.
- In ripple counter, in general terms, LSB is the Q output of FF to which external clock is applied.

2-bit Asynchronous (Ripple) Counter

Up-Counter



Count Value: 0 to $(2^N - 1)$

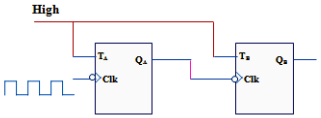
where N is the number of flip-flops

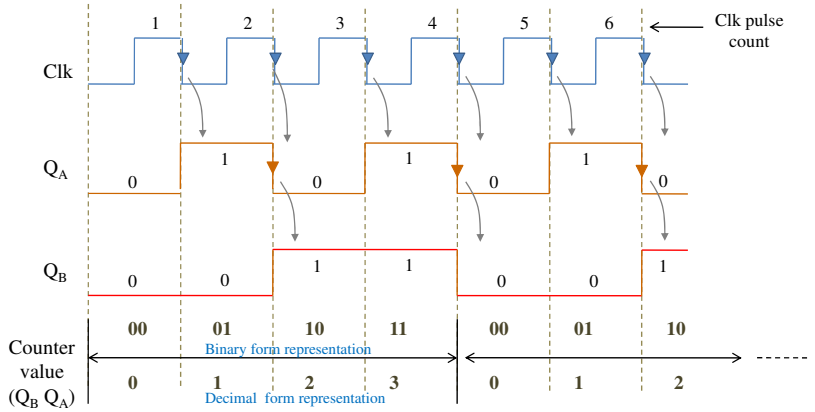
Number of States (n) = 2^N

Mod n counter

Asynchronous Counter

2-bit Asynchronous (Ripple) Up-Counter

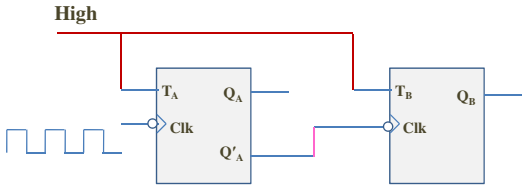




Asynchronous Counter

2-bit Asynchronous (Ripple) Counter

Down-Counter (Design 1)



Count Value: $(2^N - 1)$ to 0

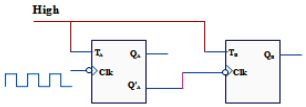
where N is the number of flip-flops

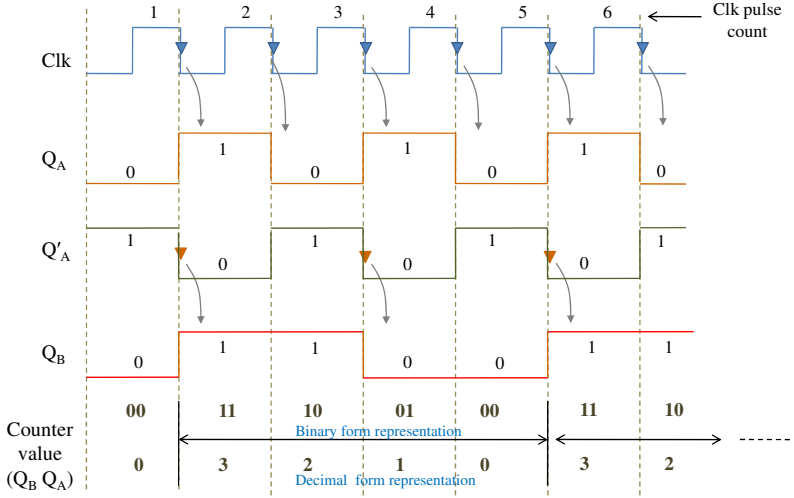
Number of States (n) = 2^N

Mod n counter

Asynchronous Counter

2-bit Asynchronous (Ripple) Down-Counter

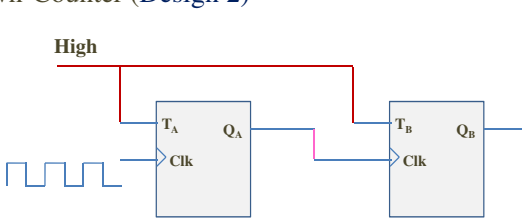




Asynchronous Counter

2-bit Asynchronous (Ripple) Counter

Down-Counter (Design 2)



Count Value: $(2^N - 1)$ to 0

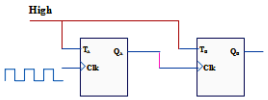
where N is the number of flip-flops

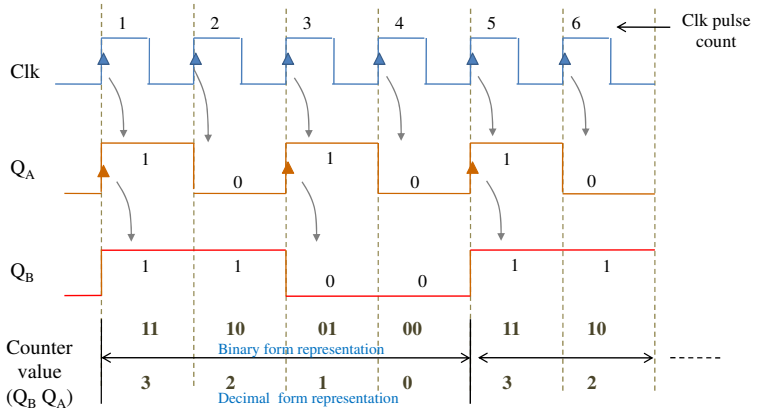
Number of States (n) = 2^N

Mod n counter

Asynchronous Counter

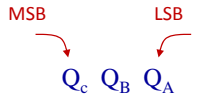
2-bit Asynchronous (Ripple) Down-Counter

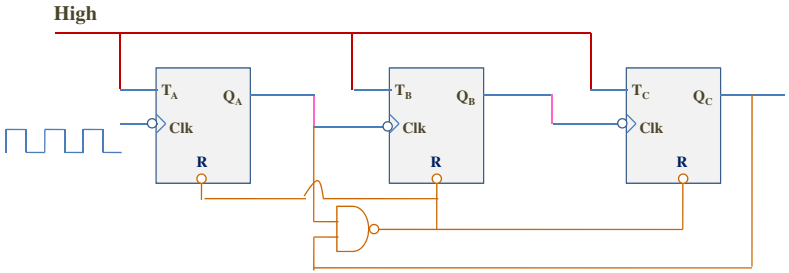




Numerical

3-bit Asynchronous Counter



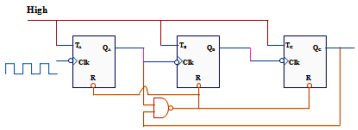


Determine Count Sequence

Determine Mod counter number

Numerical

3-bit Asynchronous Counter



Clk count number	Q_C	Q_B	Q_A
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
	1	0	1

Count Sequence: 000, 001, 010, 011, 100

Determine Mod counter number: 5 (Mod 5 Counter)

Asynchronous Counters

Design Parameters

Output frequency = (Clock frequency)/ Mod number

Total delay = (Number of flip-flops) x (Delay of each flip-flop)

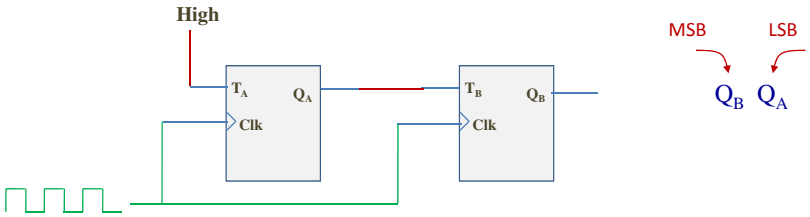
Maximum frequency = 1/ Total delay

Synchronous Counter

- Also sometimes referred to as Parallel Counter.
- Simultaneously clock given to all modules.
- The invalid states are taken as don't care condition.
- It attributes higher speed than Asynchronous counter.

Synchronous Counter

2-bit Synchronous Counter



Count Value: 0 to $(2^N - 1)$

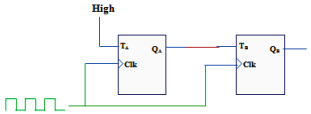
where N is the number of flip-flops

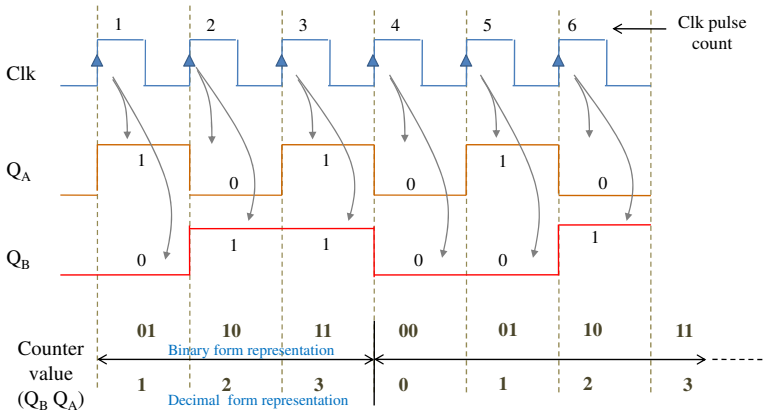
Number of States (n) = 2^N

Mod n counter

Synchronous Counter

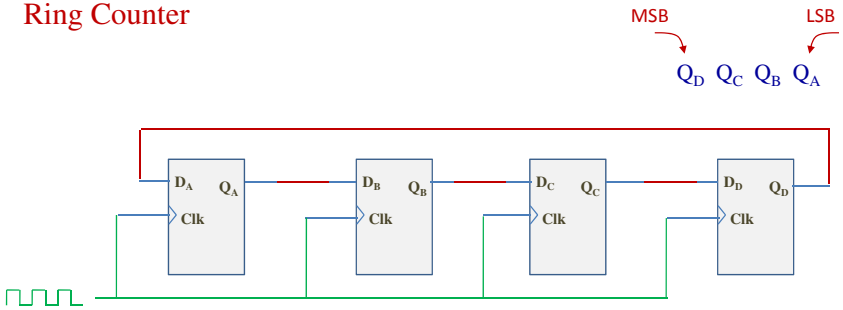
2-bit Synchronous Counter





Synchronous Counter

Ring Counter

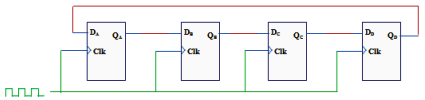


Maximum Mod number = N

where N is the number of flip-flops

Ring Counter

Initially input to the flip-flop is given asynchronously using preset/reset or from external supply.



Clk count number	Q_D	Q_B	Q_C	Q_A
1	0	0	0	1
2	0	0	1	0
3	0	1	0	0
4	1	0	0	0

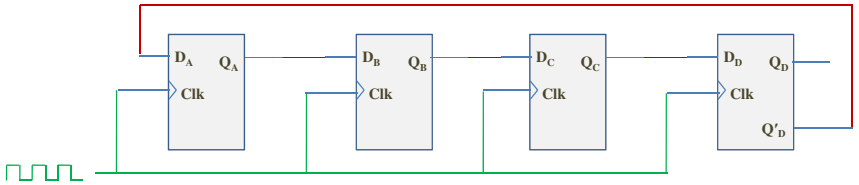
Count Sequence: 0001, 0010, 0100, 1000

Determine Mod counter number: 4 (Mod 4 Counter)

Johnson Counter or Twisted Ring Counter

MSB LSB

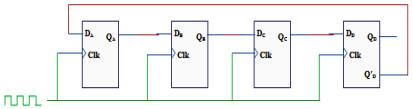
Q_D Q_C Q_B Q_A



Maximum Mod number = 2N

where N is the number of flip-flops

Johnson Counter



Clk count number	Q_D	Q_B	Q_C	Q_A
1	0	0	0	0
2	0	0	0	1
3	0	0	1	1
4	0	1	1	1
5	1	1	1	1
6	1	1	1	0
7	1	1	0	0
8	1	0	0	0

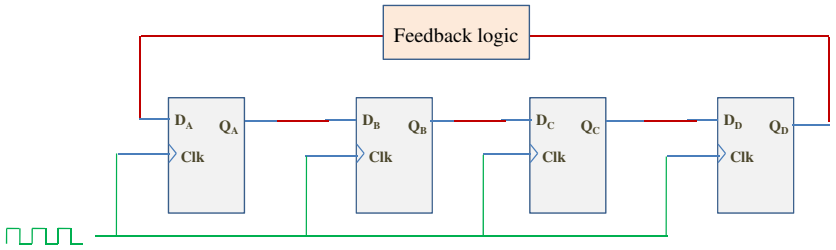
Count Sequence: 0000, 0001, 0011, 0111, 1111, 1110, 1100, 1000

Determine Mod counter number: 8 (Mod 8 Counter)

Pseudo-Random Binary Sequence (PRBS) Generator or Linear Feedback Shift Key

MSB LSB

Q_D Q_C Q_B Q_A



Maximum Mod number = $2^N - 1$

where N is the number of flip-flops

Assignment-9

1. Implement 4-bit Asynchronous Up-Counter.

2. Implement 4-bit Synchronous Down-Counter.