Dhirubhai Ambani Institute of Information and Communication Technology

EL114

Digital Logic Design

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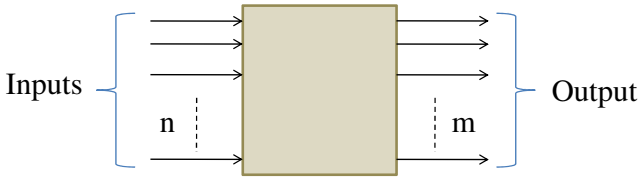
Introduction

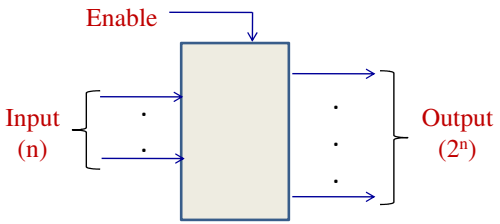
Combinational logic Circuit



Decoder

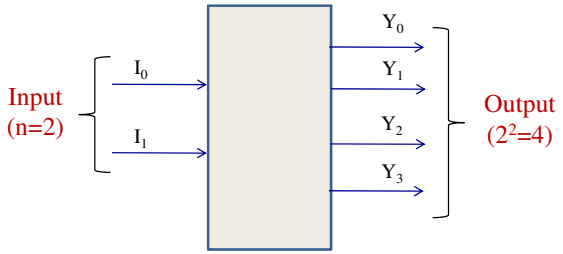
Decoder:

- 'n' inputs to '2^n' outputs.
- It has no select lines.
- Used in many applications such as memory system, code conversion, implementation of function.



Decoder Example

2:4 Decoder:



2:4 Decoder

First Step:
Truth Table Formation

Input of Decoder Output of Decoder

I_1	I_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	**1**
0	1	0	0	**1**	0
1	0	0	**1**	0	0
1	1	**1**	0	0	0

2:4 Decoder

Second Step:
Determining Boolean Expression

Input of Decoder Output of Decoder

I_1	I_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	(1)
0	1	0	0	(1)	0
1	0	0	(1)	0	0
1	1	(1)	0	0	0

$Y_0 = I_1' \cdot I_0'$

$Y_1 = I_1' \cdot I_0$

$Y_2 = I_1 \cdot I_0'$

$Y_3 = I_1 \cdot I_0$

2:4 Decoder

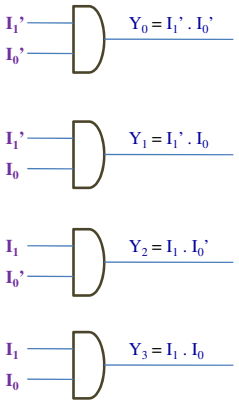
Third Step:
Realization of Boolean Expression by Logic Gates

$Y_0 = I_1' \cdot I_0'$

$Y_1 = I_1' \cdot I_0$

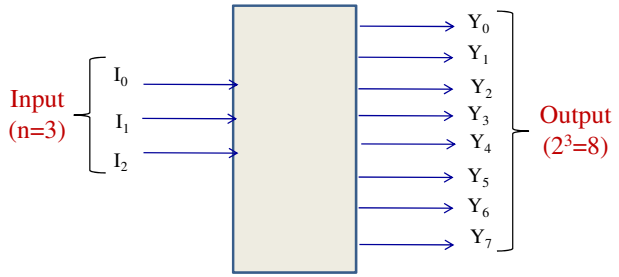
$Y_2 = I_1 \cdot I_0'$

$Y_3 = I_1 \cdot I_0$



Decoder Example

3:8 Decoder:



3:8 Decoder

First Step:
Truth Table Formation

Input of Decoder			Output of Decoder							
I_2	I_1	I_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	0	**1**
0	0	1	0	0	0	0	0	0	**1**	0
0	1	0	0	0	0	0	0	**1**	0	0
0	1	1	0	0	0	0	**1**	0	0	0
1	0	0	0	0	0	**1**	0	0	0	0
1	0	1	0	0	**1**	0	0	0	0	0
1	1	0	0	**1**	0	0	0	0	0	0
1	1	1	**1**	0	0	0	0	0	0	0

3:8 Decoder

Second Step:
Determining Boolean Expression

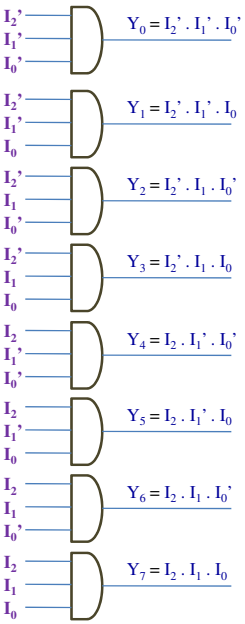
Input of Decoder			Output of Decoder							
I_2	I_1	I_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	0	(1)
0	0	1	0	0	0	0	0	0	(1)	0
0	1	0	0	0	0	0	0	(1)	0	0
0	1	1	0	0	0	0	(1)	0	0	0
1	0	0	0	0	0	(1)	0	0	0	0
1	0	1	0	0	(1)	0	0	0	0	0
1	1	0	0	(1)	0	0	0	0	0	0
1	1	1	(1)	0	0	0	0	0	0	0

$Y_0 = I_2' \cdot I_1' \cdot I_0'$
$Y_1 = I_2' \cdot I_1' \cdot I_0$
$Y_2 = I_2' \cdot I_1 \cdot I_0'$
$Y_3 = I_2' \cdot I_1 \cdot I_0$
$Y_4 = I_2 \cdot I_1' \cdot I_0'$
$Y_5 = I_2 \cdot I_1' \cdot I_0$
$Y_6 = I_2 \cdot I_1 \cdot I_0'$
$Y_7 = I_2 \cdot I_1 \cdot I_0$

3:8 Decoder

Third Step:
Realization of Boolean Expression by Logic Gates

$Y_0 = I_2' \cdot I_1' \cdot I_0'$
$Y_1 = I_2' \cdot I_1' \cdot I_0$
$Y_2 = I_2' \cdot I_1 \cdot I_0'$
$Y_3 = I_2' \cdot I_1 \cdot I_0$
$Y_4 = I_2 \cdot I_1' \cdot I_0'$
$Y_5 = I_2 \cdot I_1' \cdot I_0$
$Y_6 = I_2 \cdot I_1 \cdot I_0'$
$Y_7 = I_2 \cdot I_1 \cdot I_0$



Numerical

1. Implement the following Boolean function using
   (i) A Demultiplexer and external gates
   (ii) A Decoder and external gates.

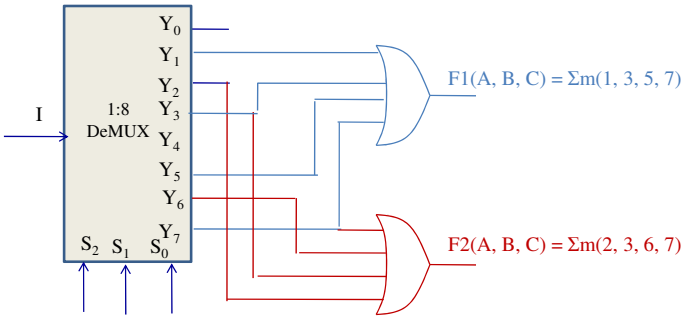
   F1(A, B, C) = Σm(1, 3, 5, 7)
   F2(A, B, C) = Σm(2, 3, 6, 7)

Numerical

1. Implement the following Boolean function using
   (i) A Demultiplexer and external gates
   (ii) A Decoder and external gates.

   F1(A, B, C) = Σm(1, 3, 5, 7)
   F2(A, B, C) = Σm(2, 3, 6, 7)

(i) Implementation using a Demultiplexer and external gates

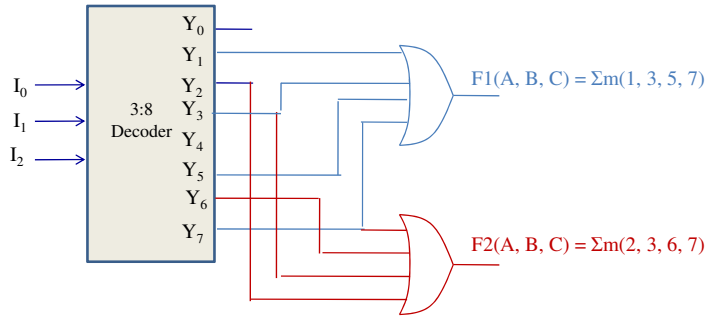


Numerical

1. Implement the following Boolean function using
   (i) A Demultiplexer and external gates
   (ii) A Decoder and external gates.

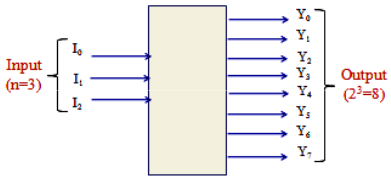
   F1(A, B, C) = Σm(1, 3, 5, 7)
   F2(A, B, C) = Σm(2, 3, 6, 7)

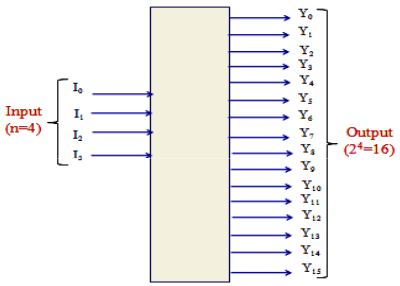
(ii) Implementation using a Decoder and external gates



Numerical

1. Implement 4:16 Decoder using two 3:8 Decoders.



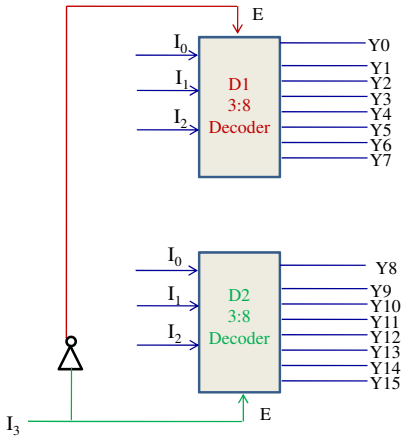


3:8 Decoder
3 Inputs
8 Outputs

4:16 Decoder
4 Inputs
16 Output

Implement 4:16 Decoder using 3:8 Decoder

To implementing 4:16 Decoder using 3:8 Decoder, Enable signal can be utilized



Assignment-6

1. Implement Full Adder using a suitable Decoder.

2. Implement 5:32 Decoder using 2:4 Decoder(s) and one 1:8 Demultiplexer.
   (More than one 2:4 decoders can be used)