Dhirubhai Ambani Institute of Information and Communication Technology

EL114

Digital Logic Design

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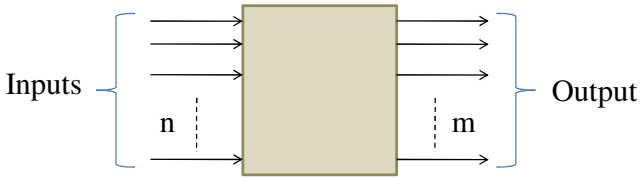
Introduction

Combinational logic Circuit



Demultiplexer (DeMUX)

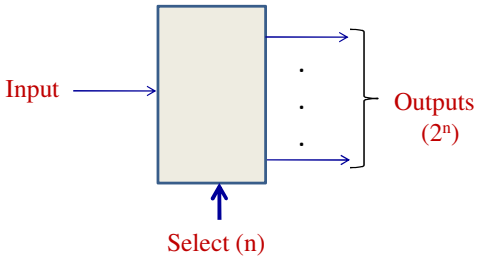
Demultiplexer:

One input to Many outputs.

The Output line is selected based on the select line(s).

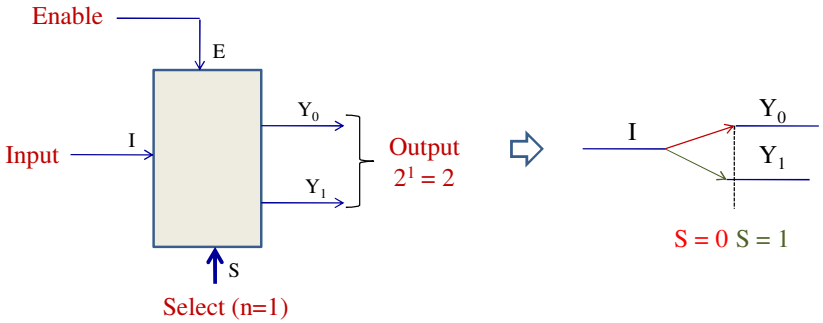
The outputs are in the form of 2^n, where n is the select line.

Used in many switching applications.



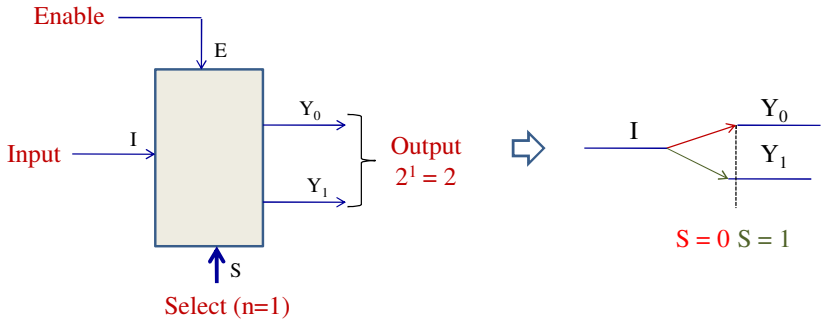
Demultiplexer Example

1:2 Demultiplexer:



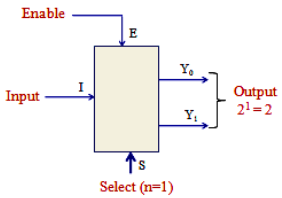
Demultiplexer Example

1:2 Demultiplexer:



Demultiplexer Example

1:2 Demultiplexer:



Number of Inputs = 3 (E, S, I,)

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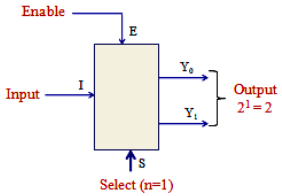
Number of Input Combinations = $2^3 = 8$

Please Note: Enable is optional. And Many DeMUX may not have Enable input.

First Step:
Truth Table Formation

Determined number of inputs to be 3

Determined number of outputs to be 2



Inputs of 1:2 DeMUX Output of DeMUX

E	S	I	Y_1	Y_0
0	0	0	z/0	z/0
0	0	1	z/0	z/0
0	1	0	z/0	z/0
0	1	1	z/0	z/0
1	0	0	0	0
1	0	1	0	1
1	1	0	0	0
1	1	1	1	0

⇨

E	S	output
0	0	z/0
0	1	z/0
1	0	Y_0
1	1	Y_1

1:2 Demultiplexer

Second Step:
Determining Boolean Expression
(For this K-map can be used)

K-map and Boolean Expression determination for Y_0

E \ SI	00	01	11	10
0	m0	m1	m3	m2
1	m4	1 m5	m7	m6

E	S	I	Y_1	Y_0
0	0	0	z/0	z/0
0	0	1	z/0	z/0
0	1	0	z/0	z/0
0	1	1	z/0	z/0
1	0	0	0	0
1	0	1	0	1
1	1	0	0	0
1	1	1	1	0

$Y_0 = ES'I$

1:2 Demultiplexer

Second Step:
Determining Boolean Expression
(For this K-map can be used)

E	S	I	Y_1	Y_0
0	0	0	z/0	z/0
0	0	1	z/0	z/0
0	1	0	z/0	z/0
0	1	1	z/0	z/0
1	0	0	0	0
1	0	1	0	1
1	1	0	0	0
1	1	1	1	0

K-map and Boolean Expression determination for Y_1

E \ SI	00	01	11	10
0	m0	m1	m3	m2
1	m4	m5	1 m7	m6

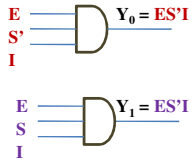
$Y_1 = ESI$

1:2 Demultiplexer

Third Step:
Realization of Boolean Expression by Logic Gates

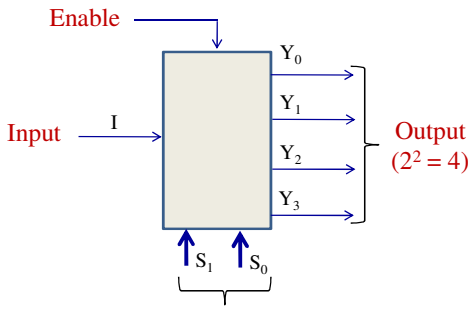
$Y_0 = ES'I$

$Y_1 = ESI$



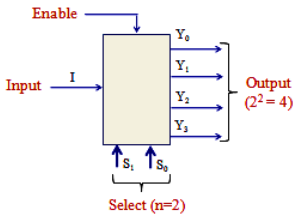
Demultiplexer Example

1:4 Demultiplexer:



Demultiplexer Example

1:4 Demultiplexer:



Number of Inputs = 4 (E, S_1, S_0, I)

Number of Input Combinations = $2^4 = 16$

Input of 1:4 DeMUX Output of DeMUX

First Step:
Truth Table Formation

Determined number of inputs to be 4

Determined number of outputs to be 4

E	S_1	S_0	I	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	1
1	0	1	0	0	0	0	0
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	1	0	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	0

E	S_1	S_0	output
0	x	x	0
1	0	0	Y_0
1	0	1	Y_1
1	1	0	Y_2
1	1	1	Y_3

1:4 Demultiplexer

Second Step:
Determining Boolean Expression

E	S_1	S_0	output
0	x	x	0
1	0	0	Y_0
1	0	1	Y_1
1	1	0	Y_2
1	1	1	Y_3

$Y_0 = ES_1'S_0'I$

$Y_1 = ES_1'S_0I$

$Y_2 = ES_1S_0'I$

$Y_3 = ES_1S_0I$

1:4 Demultiplexer

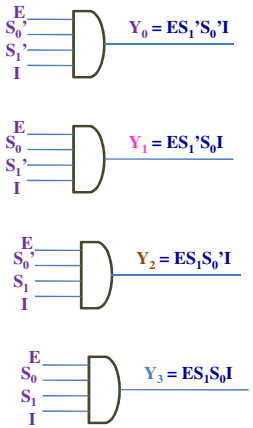
Third Step:
Realization of Boolean Expression by Logic Gates

$Y_0 = ES_1'S_0'I$

$Y_1 = ES_1'S_0I$

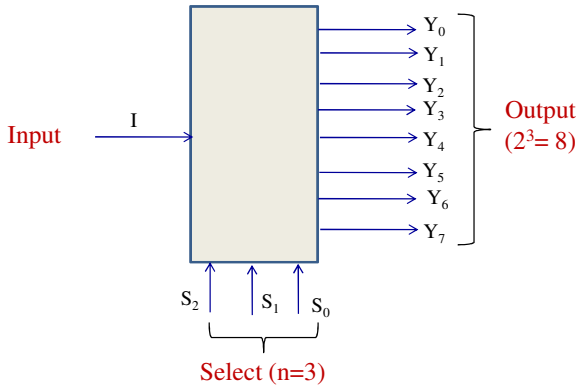
$Y_2 = ES_1S_0'I$

$Y_3 = ES_1S_0I$



Demultiplexer Example

1:8 Demultiplexer:



1:8 Demultiplexer

First Step:
Truth Table Formation

S_2	S_1	S_0	Output
0	0	0	Y_0
0	0	1	Y_1
0	1	0	Y_2
0	1	1	Y_3
1	0	0	Y_4
1	0	1	Y_5
1	1	0	Y_6
1	1	1	Y_7

1:8 Demultiplexer

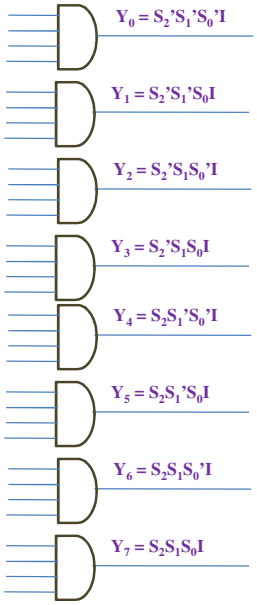
Second Step:
Determining Boolean Expression

S_2	S_1	S_0	Output
0	0	0	Y_0
0	0	1	Y_1
0	1	0	Y_2
0	1	1	Y_3
1	0	0	Y_4
1	0	1	Y_5
1	1	0	Y_6
1	1	1	Y_7

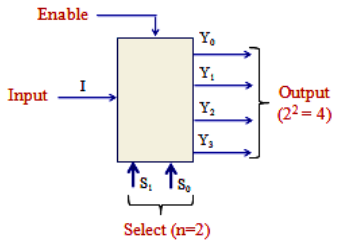
$$Y_0 = S_2'S_1'S_0'I$$
$$Y_1 = S_2'S_1'S_0I$$
$$Y_2 = S_2'S_1S_0'I$$
$$Y_3 = S_2'S_1S_0I$$
$$Y_4 = S_2S_1'S_0'I$$
$$Y_5 = S_2S_1'S_0I$$
$$Y_6 = S_2S_1S_0'I$$
$$Y_7 = S_2S_1S_0I$$

Third Step:
Realization of Boolean Expression by Logic Gates

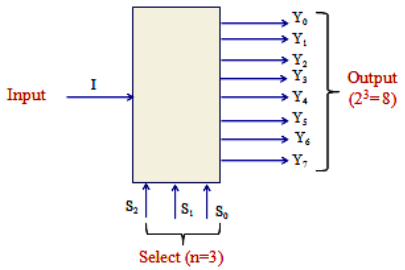
$$Y_0 = S_2'S_1'S_0'I$$
$$Y_1 = S_2'S_1'S_0I$$
$$Y_2 = S_2'S_1S_0'I$$
$$Y_3 = S_2'S_1S_0I$$
$$Y_4 = S_2S_1'S_0'I$$
$$Y_5 = S_2S_1'S_0I$$
$$Y_6 = S_2S_1S_0'I$$
$$Y_7 = S_2S_1S_0I$$



Implement 1:8 Demultiplexer using 1:4 Demultiplexer



1:4 DeMUX
1 Input
2 Select lines
4 Output



1:8 DeMUX
1Input
3 Select lines
8 Output

Implement 1:8 Demultiplexer using 1:4 Demultiplexer

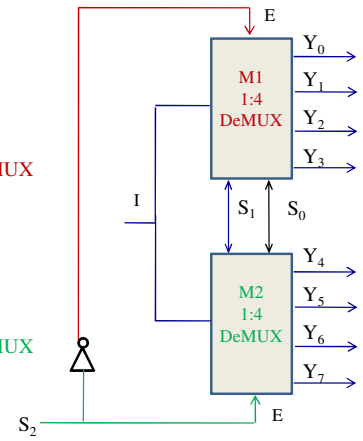
To implementing 1:8 DeMUX using 1:4 DeMUX, Enable signal can be utilized

E

S_2	S_1	S_0	Output
0	0	0	Y_0
0	0	1	Y_1
0	1	0	Y_2
0	1	1	Y_3
1	0	0	Y_4
1	0	1	Y_5
1	1	0	Y_6
1	1	1	Y_7

M1
1:4 DeMUX

M2
1:4 DeMUX



Numerical

1. Implement Full Subtractor using Demultiplexer.

First Step:
Truth Table Formation

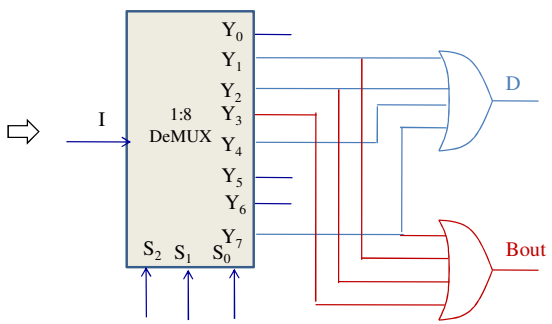
A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Numerical

1. Implement Full Subtractor using Demultiplexer.

Second Step:
Realization using DeMUX

A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



Assignment-4

1. Implement the following Boolean Function using 1:8 DeMUX (without using any Enable signal).

   $f(P, Q, R, S) = \Sigma m(0, 1, 3, 4, 8, 9, 15)$