Answers to Lab2 questions
The XOR gate has been implemented as a combination of OR, NAND and AND gates since the logic equation can be written as :
A xor B = (A or B) and (A nand B)

This can be shown visually shown as follows:

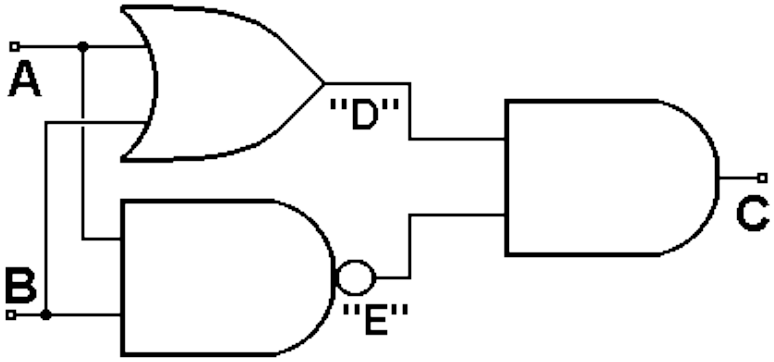

Figure 1: XOR gate.

Different Training data has been used to train the respective gates.
Question 1:
The minimum number of gates required is 3.
They should be connected as follows.

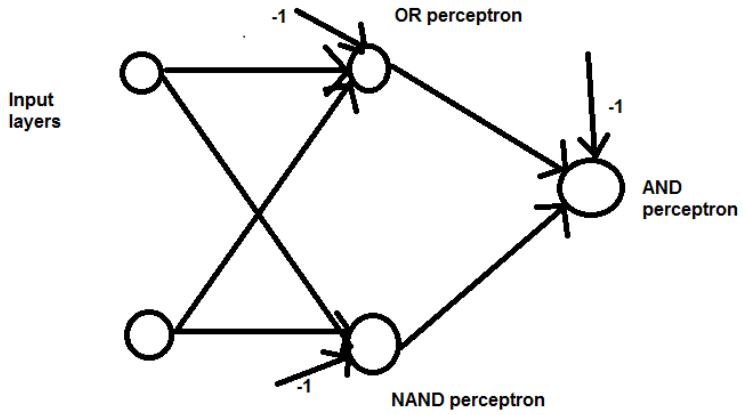

Figure 2: sXOR gate with perceptron

Question 2

The minimum number of training examples needed was 12, 4 for each gate(NAND, AND and OR).
I used more training examples in order for the perceptron to tolerate fuzzy logic.