CURTIS ELECTROMUSIC SPECIALTIES

# CEM 3310

## Voltage Controlled Envelope Generator

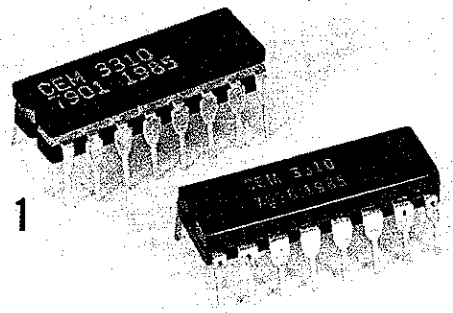
The CEM3310 is a self-contained, precision ADSR type of envelope generator intended for electronic music and other sound generation applications. Attack, decay and release times are exponentially voltage controllable over a wide range, and the sustain level is linearly voltage controllable from 0 to 100% of the peak voltage. A unique design approach allows for a 10,000 times improvement in control voltage rejection over conventional designs. In addition, much care has been given to the accuracy, repeatability and tracking of the parameters from unit to unit without external trimming. The times are to a first order determined only by the external resistor and capacitor and constant of physics, KT/q. Wide tolerance monolithic resistors are not used to set up the time constants or the control scale. Finally, all four control inputs are isolated from the rest of the circuitry so that the control pins of tracking units may be simply tied together. Although a low voltage process has been used to lower the cost and lower the leakage currents, an internal 6.5 volt Zener diode allows the chip to be powered by ± 15 volts supplies, as well as +15, -5 volt supplies.

* **Zero to -5V Varies the Times from 2mS to 20S**

** **Zero to +5V Varies the Sustain Level from 0 to 100%**

### Features

- Low Cost
- Third Generation Design
- Large Time Control Range: 50,000 min
- Full ADSR Response
- True RC Envelope Shape
- Exceptionally Low Control Voltage Feedthrough: 90μV max
- Accurate Exponential Time Control Scales
- Isolated Control Inputs
- Good Repeatability and Tracking Between Units Without External Trim
- Independent Gate and Trigger
- ± 15 Volt Supplies

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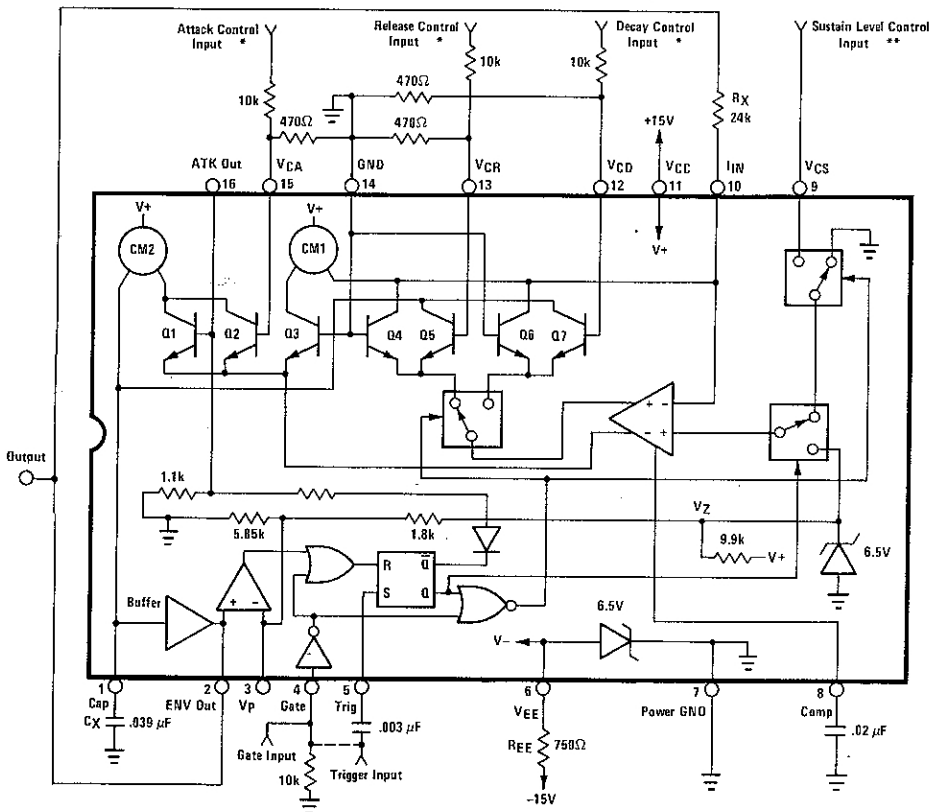
## Circuit Block and Connection Diagram



# CEM 3310

## Electrical Characteristics

| $V_{CC}$ = +15.0V $V_{EE}$ = −5.0 to −15.0V $R_X$ = 24K $T_A$ = 25°C | | | | |
|---|---|---|---|---|
| | MIN | TYP | MAX | Units |
| Time Control Range | 50,000:1 | 250,000:1 | — | |
| Attack Asymtote Voltage ($V_Z$) | 6.1 | 6.5 | 6.9 | V |
| Attack Peak Voltage ($V_p$) | 4.7 | 5.0 | 5.3 | V |
| Attack Peak to Asymptote Tracking | — | 1.5 | 4 | % |
| Control Scale Sensitivity | 58.5 | 60 | 61.5 | mV/Decade |
| Temperature Coefficient of Control Scale | +3,000 | +3,300 | +3,600 | ppm |
| ATK, DCY, RLS Scale Tracking | −300 | 0 | +300 | μV/Decade |
| Exponential Full Scale Control Accuracy[1] | | | | |
| 50nA < $I_O$ < 50 μA | — | 0.3 | 1.5 | % |
| 2nA < $I_O$ < 200 μA | — | 2 | 10 | % |
| Attack C.V. Feedthrough[2] | — | 6 | 90 | μV |
| Decay C.V. Feedthrough[2] | | NONE | | |
| Release C.V. Feedthrough[2] | | NONE | | |
| Sustain Final Voltage Error ($V_O$-$V_{CS}$) | −3 | +10 | +23 | mV |
| Release Final Voltage Error ($V_O$) | −3 | +10 | +23 | mV |
| RC Curve Asymptote Error[3] | | | | |
| $V_{CA,D,R}$ = 0 | — | −6 | −60 | μV |
| $V_{CA,D,R}$ = −240mV | — | −125 | −1250 | mV |
| Input Current ($I_{IN}$) to Output Current ($I_O$) Ratio, $V_{CA,D,R}$ = 0.5[5] | | | | |
| Charge Current (ATK) | .75 | 1 | 1.3 | |
| Discharge Current (DCY, RLS) | .83 | 1 | 1.2 | |
| Buffer Input Current ($I_{B2}$) | — | 0.5 | 5 | nA |
| Op Amp Input Current ($I_{B1}$) | 150 | 400 | 800 | nA |
| Gate Threshold | 2.0 | 2.3 | 2.6 | V |
| Gate Input Current | 5 | 25 | 100 | μA |
| Trigger Pulse Required to Trigger Envelope | +1.1 | +1.3 | +1.5 | V |
| Trigger Input Impedance | 2.4 | 3 | 4 | KΩ |
| Time Control Input Current | 0.5 | — | 2500 | nA |
| Sustain Control Input Current | 150 | 400 | 800 | nA |
| Attack Output Signal | −.4 | −.8 | −1.2 | V |
| Output Current Sink Capability | 420 | 560 | 700 | μA |
| Buffer Output Impedance | 100 | 200 | 350 | Ω |
| Positive Supply Voltage Range | +12.5 | — | +18 | V |
| Negative Supply Voltage Range[4] | −4.5 | — | −18 | V |
| Supply Current | 5.6 | 7.5 | 9.4 | mA |

**Note 1:** Scale factor determined at mid-range. Spec represents total deviation from ideal at range extremities.

**Note 2:** Output is at either sustain final voltage or release final voltage. $V_{CA,D,R}$ varies 0 to −240mV.

**Note 3:** Spec represents the difference between the actual final voltages (attack asymptote voltage, sustain final voltage, and release final voltage in the case of attack, decay, and release respectively) and the apparent voltage to which the output seems to be approaching asymptotically.

**Note 4:** Current limiting resistor required when $V_{EE}$ > −6.0 volts.

**Note 5:** Spec also represents time constant variation between units for $V_{CA,D,R}$ = 0.

## Application Hints

### Supply

Since the device can withstand no more than 24 volts between its supply pins, an internal 6.5 volt ± 10% zener diode has been provided to allow the chip to run off virtually any negative supply voltage. If the negative supply is between −4.5 and −6.0 volts, it may be connected directly to the negative supply pin (pin 6). For voltages greater than −7.5 volts, a series current limiting resistor must be added between pin 6 and the supply. Its value is calculated as follows:

$$R_{EE} = (V_{EE} - 7.2)/.010.$$

The circuit was designed for a positive supply of +15 volts. Voltages other than +15 volts will cause the peak threshold voltage to be either at a minimum of .33$V_{CC}$ or at a maximum of 5.5 volts.

### Gate and Trigger Inputs

The gate input is referenced to ground and therefore will accept any ground referenced TTL or CMOS logic level up to +18 volts. If the gate pin is left floating, it will be interpreted as a high level. The trigger input is referenced to the $V_{EE}$ pin (pin 6) and therefore, a ground referenced trigger pulse should be capacitively coupled to the trigger input pin (pin 5).

### Input Control Voltages

As the scale sensitivity on the three time control inputs is 60mV/decade, attenuation of the incoming control voltages will in most cases be required. Four decades of control requires only a 240mV voltage excursion. The more negative the voltages the longer the times. For best scale accuracy at the shortest times, the impedance at the time control pins should be kept low. At the shortest times (corresponding to 200 μA of peak

current), every 100Ω will cause a 1% increase in control scale error. As the times are increased, this error will decrease in direct proportion.

The voltage applied to the sustain level control input will directly determine the sustain voltage of the output envelope (minus the sustain final voltage error). Voltages greater than the threshold voltage will cause the envelope to ramp up to this higher voltage when the peak threshold is reached. The rate at which this occurs will be equal to the fastest attack rate.

Since all four control inputs are connected only to the bases of NPN transistors, the control input pins of tracking units may be simply tied together. Therefore, in the case of the time control inputs, only one attenuator network is required to control the same parameter in a multiple chip system.

### Selection of $R_X$ and $C_X$

As is shown in the envelope equations, the RC time constant of the attack, decay and release curves is given by $R_XC_X$ times the exponential multiplier, $\exp(-V_C/V_T)$. Practical circuit limitations determine $R_X$ and the multiplier, from which $C_X$ can then be calculated. The peak capacitor charging and discharging currents is given by $(V_Z/R_X)\exp(V_{CA}/V_T)$, $(V_{CS}/R_X)\exp(V_{CD}/V_T)$, and $(V_P/R_X)\exp(V_{CR}/V_T)$ for the attack, decay, and release phases respectively. For the best scale accuracy and tracking at the shortest times, these currents should be kept less than 100 μA, and in all cases they should not be allowed to exceed 300 μA. This sets the minimum value for $R_X$ at 24K. Larger values of $R_X$ will allow positive time control voltages to be used. However, as can also be seen from the envelope equations, the sustain/final voltage error, the asymptote error, and the control voltage feedthrough are all affected by $R_X$. A practical maximum of 240K is recommended for $R_X$ when the internal buffer is used and 1M if an external FET buffer is used.

### Trimming the Envelope Times

The RC time constants of the output envelope will typically track to within ± 15% from unit to unit, even at the longest time settings. If better tracking is required, the best method for trimming the time constants is to simply adjust $R_X$ with a trimming potentiometer.

### Output Drive Capability

The buffer output can sink at least 400 μA and can source up to 10mA, but with considerable degradation in performance. An output load no less than 20K to ground is recommended.

The buffer has a somewhat high output impedance. As a result of this, small steps (50mV) appear in the output waveform at the phase transitions, due to the sudden change in drive the output must provide to $R_X$. The largest step is at the beginning of the envelope and is given by $(R_O/R_X)V_Z$. It may be decreased by increasing $R_X$, lowering $R_O$, or using an external buffer with a low output impedance. $R_O$ may be lowered by adding a resistor from the output pin to $V_{EE}$. However, every 1mA of current drawn from the output pin may increase the buffer input current as much as 5–6 nA with consequent degradation in performance.

## Absolute Maximum Ratings

| | |
|---|---|
| Voltage Between $V_{CC}$ and $V_{EE}$ Pins | 24V |
| Voltage Between $V_{CC}$ and Ground Pins | +18V |
| Voltage Between $V_{EE}$ and Ground Pins | −6.0V |
| Current Into $V_{EE}$ Pin | ±50mA |
| Voltage Between Control and Ground Pins | ±6.0V |
| Voltage to Gate and Trigger Input Pins | $V_{EE}$ to $V_{CC}$ |
| Storage Temperature Range | −55°C to +150°C |
| Operating Temperature Range | −25°C to +75°C |

## Envelope Equations

**Attack Curve**

$$V_{OA} = V_Z\,(1-\exp(-\frac{t}{R_XC_X}\,e^{V_{CA}/V_T}))$$

**Decay Curve**

$$V_{OD}=(V_P-V_{CS})\exp(-\frac{t}{R_XC_X}\,e^{V_{CD}/V_T})+V_{CS}$$

**Release Curve**

$$V_{OR} = V_{CS}\exp(-\frac{t}{R_XC_X}\,e^{V_{CR}/V_T})$$

**Sustain/Release Final Voltage Error**

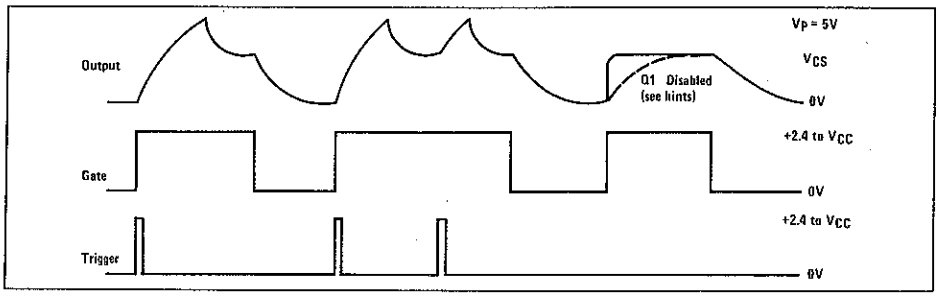
$$\epsilon_F = V_{OS} + I_{B1}R_X - I_{B2}R_X/1+e^{V_{CA}/V_T}$$

**Attack/Decay/Release Asymptote Error**

$$\epsilon_A = V_{OS} + I_{B1}R_X - I_{B2}R_X\,e^{-V_{CA,D,R}/V_T}$$

$V_{CA}$ = Attack Control Voltage
$V_{CD}$ = Decay Control Voltage
$V_{CR}$ = Release Control Voltage
$V_{CS}$ = Sustain Control Voltage
$V_{OS}$ = Op Amp Offset
$I_{B1}$ = Op Amp Input Current
$I_{B2}$ = Buffer Input Current
$V_Z$ = Attack Asymptote Voltage
$V_P$ = Envelope Peak Voltage
$V_T$ = kT/q

# Input and Output Waveforms



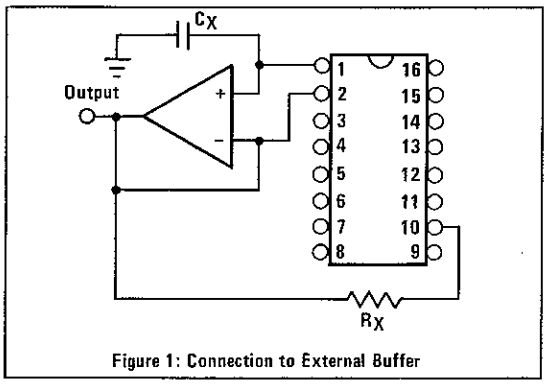




Figure 1: Connection to External Buffer

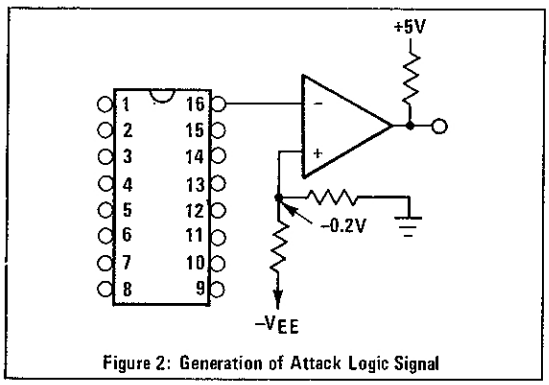



Figure 2: Generation of Attack Logic Signal

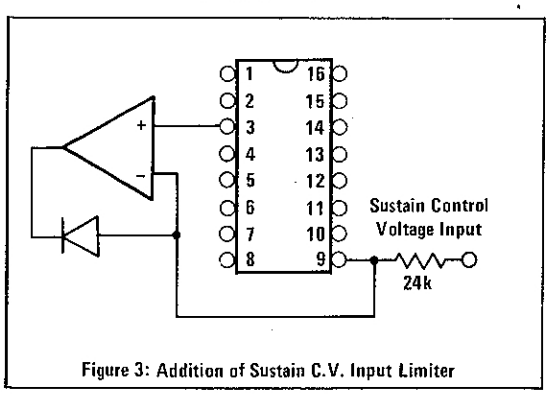



Figure 3: Addition of Sustain C.V. Input Limiter

## Use of External Buffer

For various reasons, it may be desired to use an external buffer. One possible benefit might be a lower input bias current ($I_{B2}$), with consequent improvement in the associated errors. The external buffer should be connected as shown in Figure 1. For proper operation, the buffer used should be capable of sourcing at least 700 $\mu$A and should have a positive current flowing into the input pin, such as that resulting from NPN or P channel JFET inputs.

## Disabling the Control Voltage Rejection Circuit

The purpose of Q1 (see block diagram) is to greatly reduce the control voltage feedthrough. During the attack phase, the base of Q1 is brought negative effectively disabling it and allowing Q2 to control the charging current. During the decay and release phases, however, the base of Q1 is at ground, causing negative voltage excursions on the base of Q2 to vary the charging current only a maximum of 2:1 (as opposed to the normal 10,000:1 or greater). Under normal triggering conditions (applying a trigger and a gate), this has no consequence, except to reduce the attack control voltage feedthrough to a negligible amount. However, if only a gate is applied with no trigger, the output will ramp up to the sustain level, approaching it asymptotically with a RC time constant of $R_XC_X(\exp(V_{CA}/V_T) + 1)$ (i.e. a rapid attack with only a 2:1 control range). To provide the normal full range of attack control under this mode of operation, Q1 should be disabled by connecting a resistor from pin 16 to $V_{EE}$ to generate at least –500mV at the base of Q2. This resistance may be calculated as follows:

$$R = 1100(2V_{EE}-1)$$

The result will be 5,000 times or more sustain and release final voltage shift with the attack control voltage. If external circuitry is added to apply the –500 mV only when the gate is high, then only the sustain final voltage will exhibit significant shift.

## Use of the Attack and Threshold Voltage Output Pins

The attack output pin (pin 16) and the peak threshold voltage pin (pin 3) have been provided to allow additional flexibility. Since pin 16 outputs a –.4 to –1.2 volts only during the attack phase, it may be used to provide a logic signal which indicates the attack phase (see figure 2). This signal may be ANDed with the gate to provide a logic signal indicating the decay phase. As was mentioned above, a sustain control voltage greater than the threshold voltage will result in a "jump" to the sustain level. By using the threshold voltage pin as shown in figure 3, the sustain voltage can be prevented from rising above the envelope peak, thus eliminating this undesirable effect. (This effect can also be eliminated by disabling the control voltage rejection circuit as described above).

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