LS1012A RDB

REV - D

All information is subject to change without notice.
No warranty, expressed or applied, is made as to the accuracy of the information contained herein. This schematic is provided for reference purposes only. Contact your NXP representative to obtain the latest information on this product.

Rev	Date	Changes
X1	10/09/2015	First Release
X2	18/09/2015	Implemented internal review comments
X3	19/11/2015	Implemented changes required for Layout.
A	23/11/2015	A85 Release. Implemented Power_OK changes.
AX1	28/12/2015	A70 Release: Architecture changes for UART & JTAG MUX.
AX2	15/1/2016	A70 Release: UART transceiver and bringup erratas.
B	28/1/2016	A85 Release.
BX1	28/4/2016	Implemented bringup errata. Refre Errata for more details.
C	03/05/2016	A85 Release.
CX1	03/06/2016	Added on board oscillator(25MHz) with Clock buffer to provide reference clock for LS1012 SOC and SGMII PHY. Errata in power mux 3.3V.
D	26/10/2016	A085 release.

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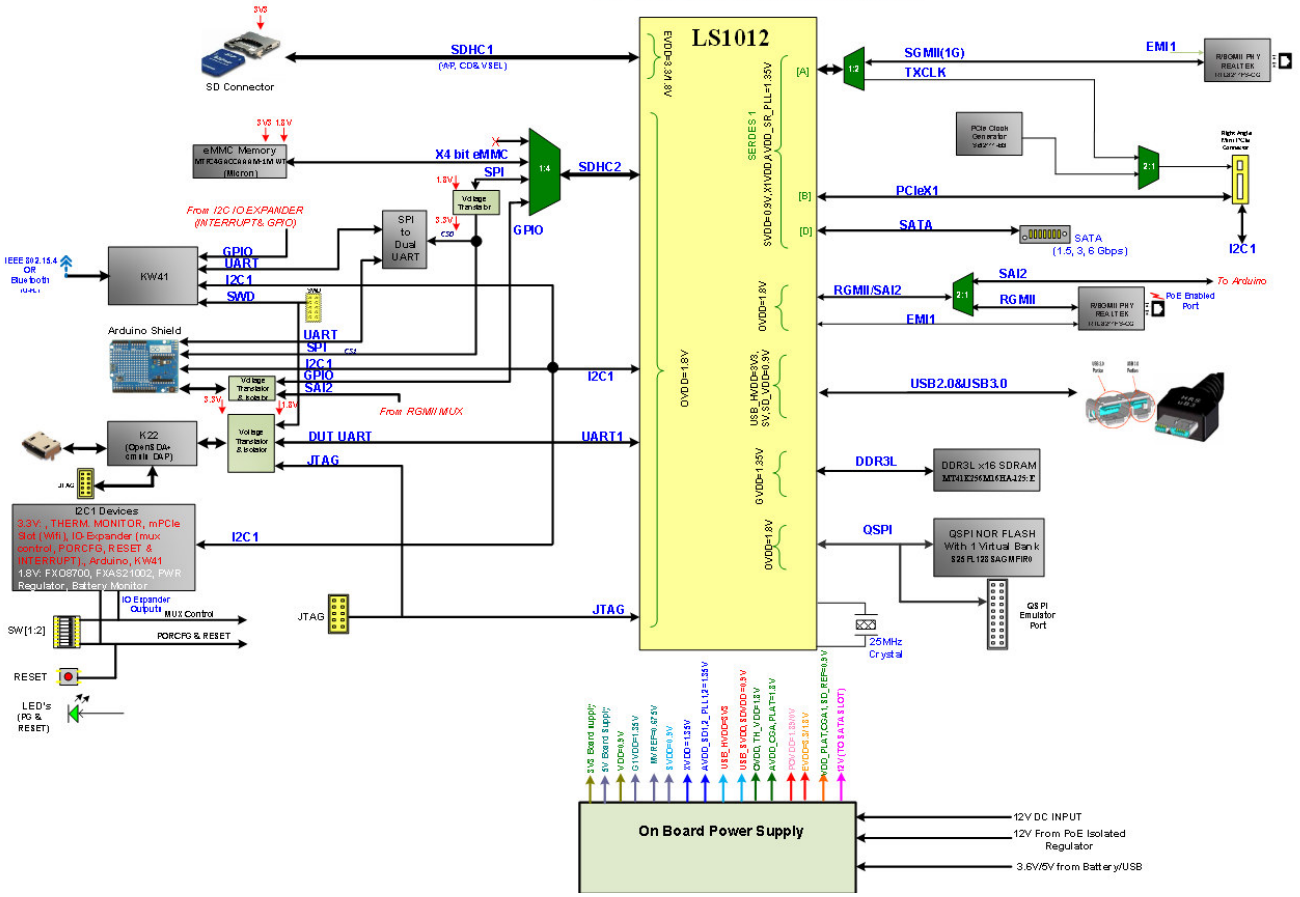
LS1012RDB Block Diagram



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PCB STACKUP

NOTE:
Stackup with low loss material TU-872LK is shown below but any stackup which meets impedance requirements can be used.

1.Materials: TU-872LK
2.trace/space (min): 3/3 mils **finish copper (Max): 1.1mils**
3.HDI design:(yes or no): no

Propose PCB Stack Up					Impedance									
Layer	Type	Thickness (mil)			Single end	Ω	+/- %	REF	Theory value	Differential	Ω	+/- %	REF	Theory value
Top side solder mask			0.70	mils										
L1	TOP	copper+plating	1.10	mils	w: 6.5 mils	50	10	2	47.96	W: 6/6/6 mils W: 5/8/5 mils	90 100	10 10	2 2	87.72 99.36
		dielectric layer	3.50	mils										
L2		copper	1.30	mils										
		dielectric layer	6.10	mils										
L3		copper	0.70	mils	w: 6.5 mils	50	10	2 5	48.52	W: 5/8/5 mils	100	10	2 5	98.39
		dielectric layer	37.00	mils										
L4		copper	0.70	mils	w: 6.5 mils	50	10	2 5	48.52	W: 5/8/5 mils	100	10	2 5	98.39
		dielectric layer	6.10	mils										
L5		copper	1.30	mils										
		dielectric layer	3.50	mils										
L6	Bottom	copper+plating	1.10	mils	w: 6.5 mils	50	10	2	47.96	W: 6/6/6 mils W: 5/8/5 mils	90 100	10 10	2 2	87.72 99.36
Top side solder mask			0.70	mils										
TOTAL			63.80	mils										
			1.62	mm										

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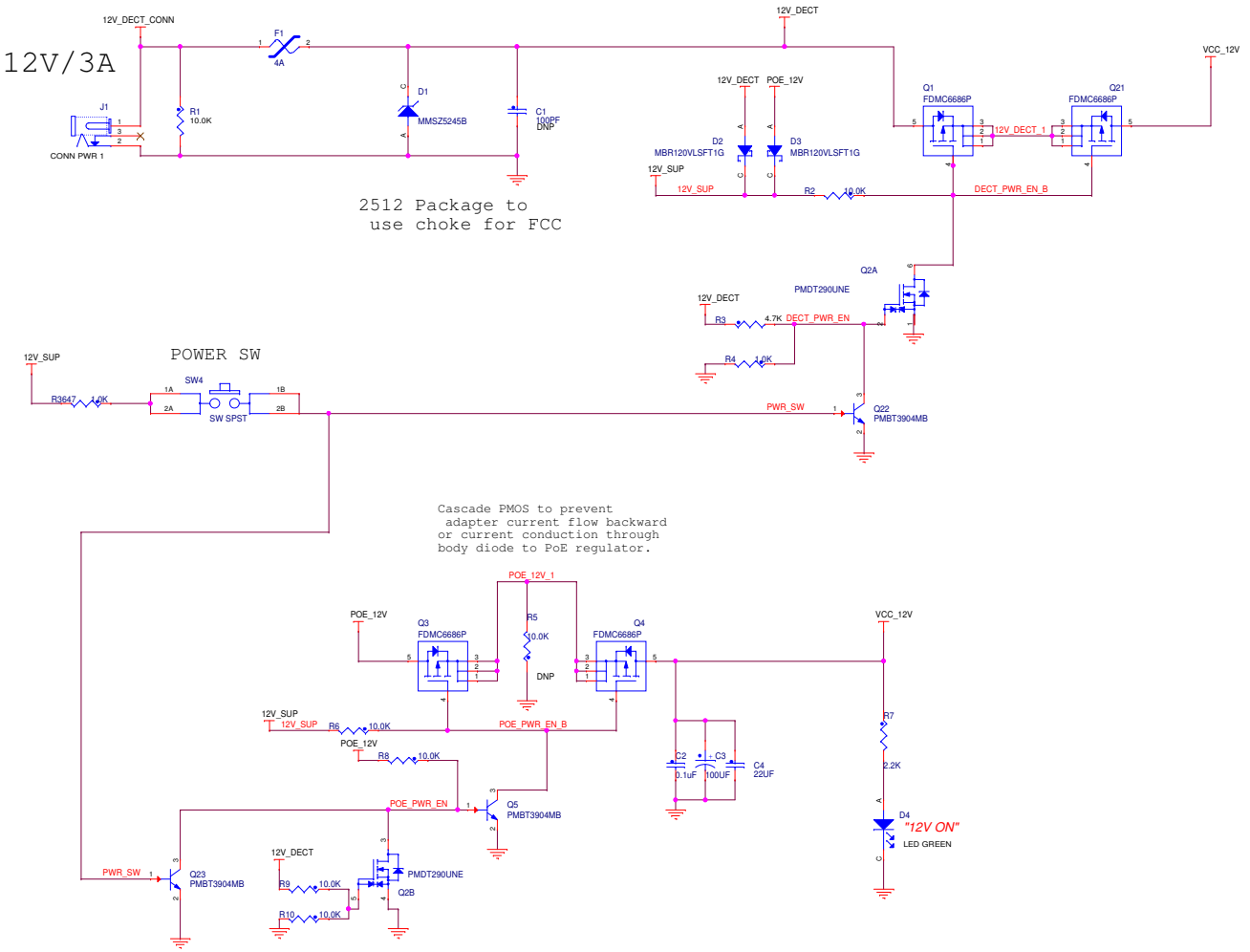
POWER ENTRY AND MULTIPLEXING



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Page Title: **004_POWER ENTRY_12V**

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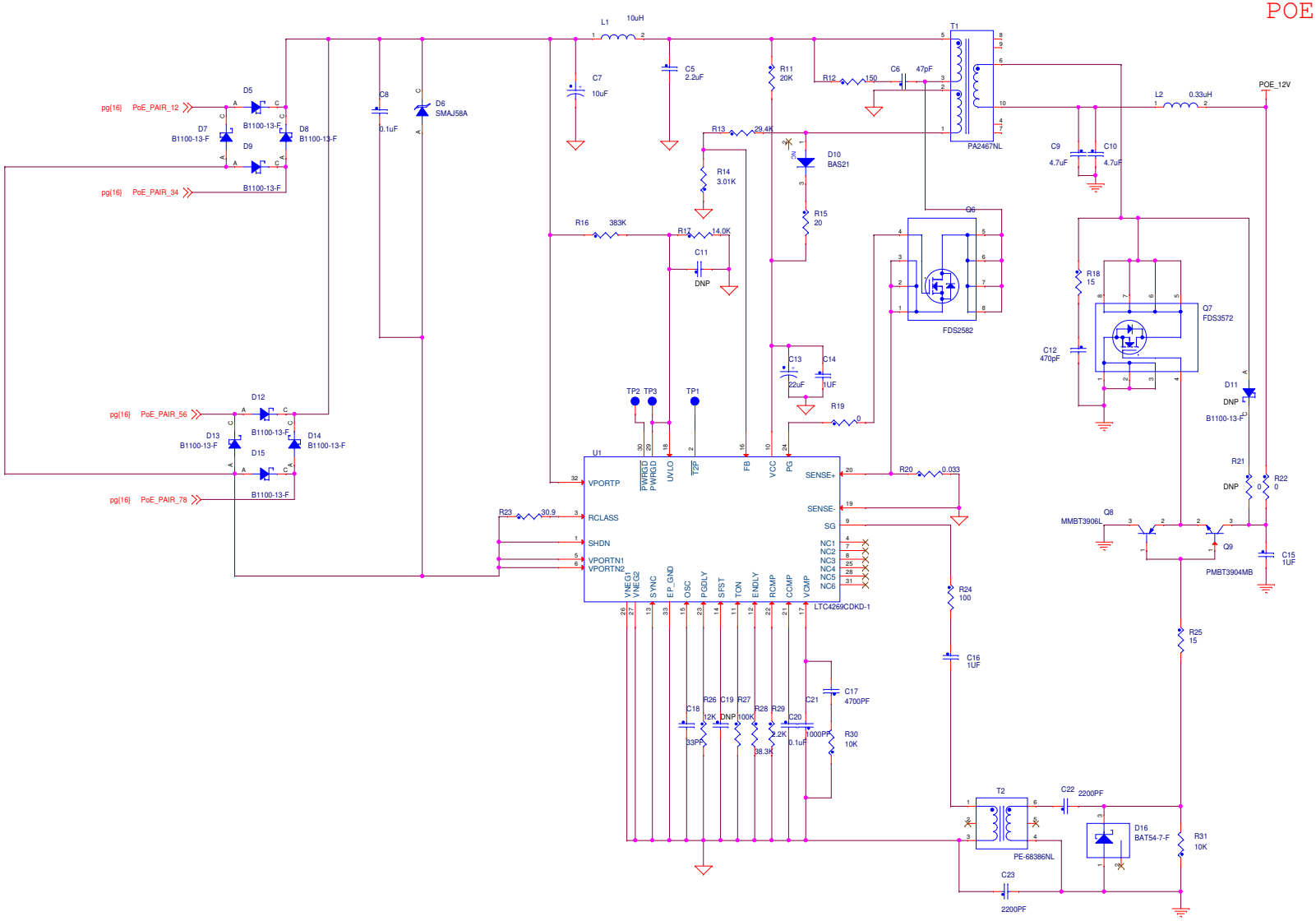

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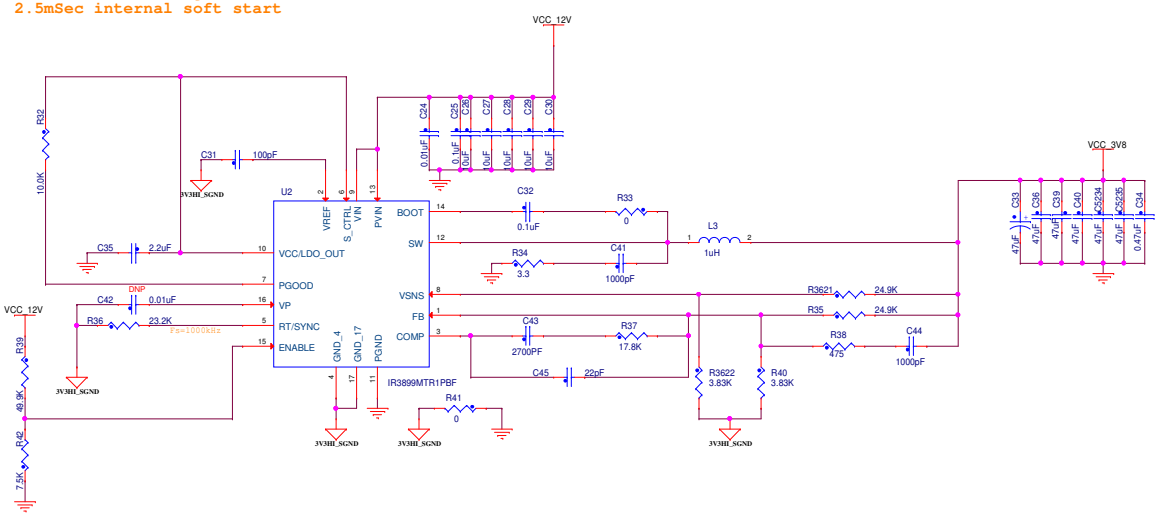
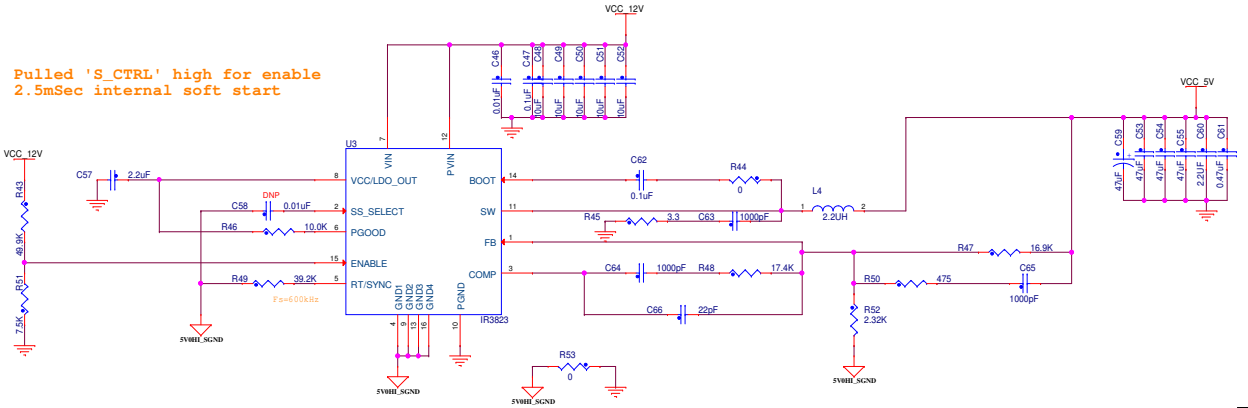
POWER 3.8V @ 9A

Pulled 'S_CTRL' high for enable
2.5mSec internal soft start



POWER 5V @ 3A

Pulled 'S_CTRL' high for enable
2.5mSec internal soft start



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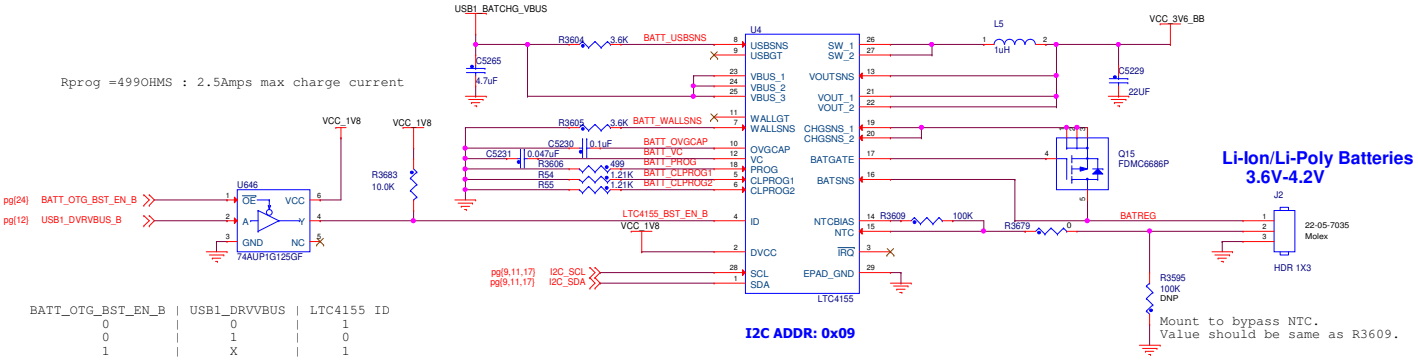
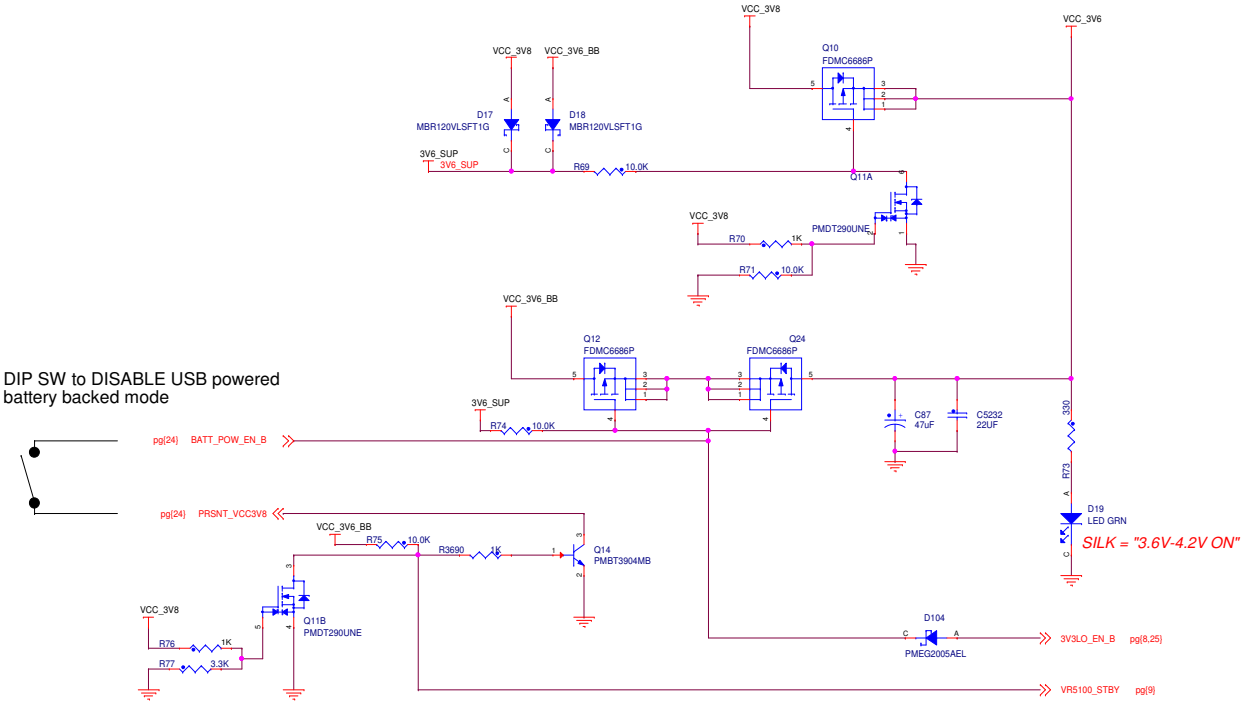
Li-ion Battery Charger & Power Manager



BATT_OTG_BST_EN_B	USB1_DRVVBUS	LTC4155 ID
0	0	1
0	1	0
1	X	1

3.6V PFET MUX (External/PoE & USB/Battery)



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Page Title:	007_PWR_BATT CHARGER & PWR MUX		
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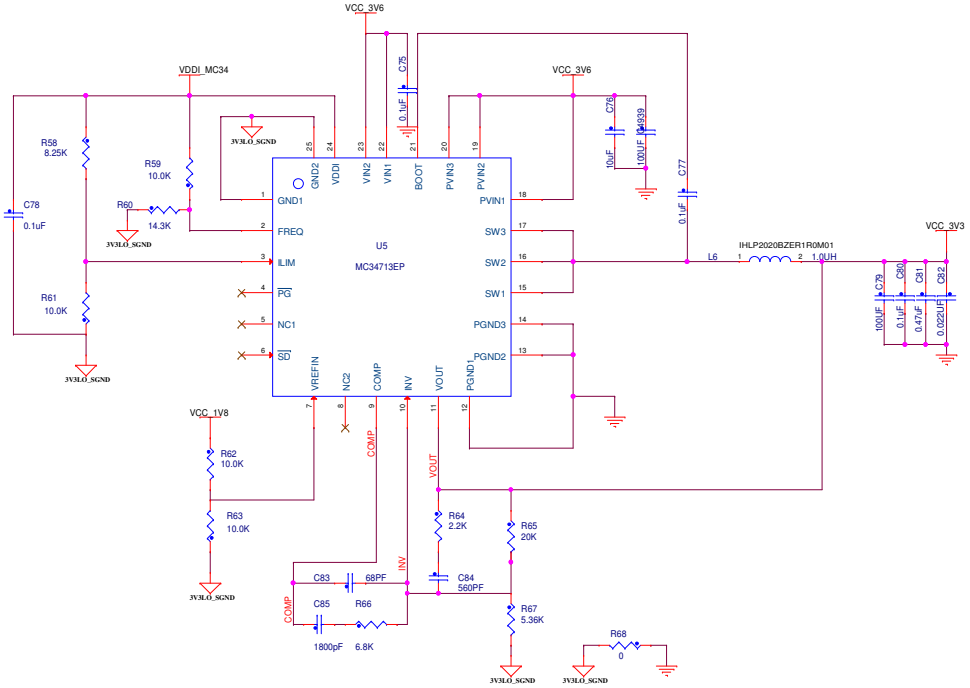
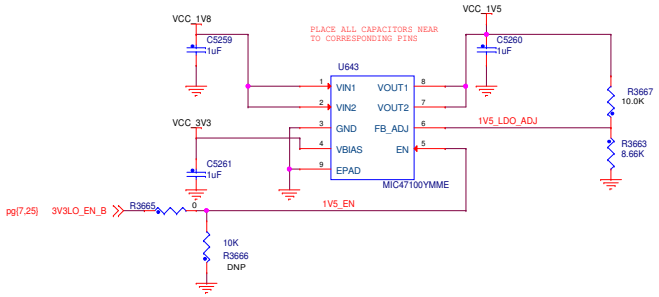
POWER 3.3V



Mini PEX (1.5V)



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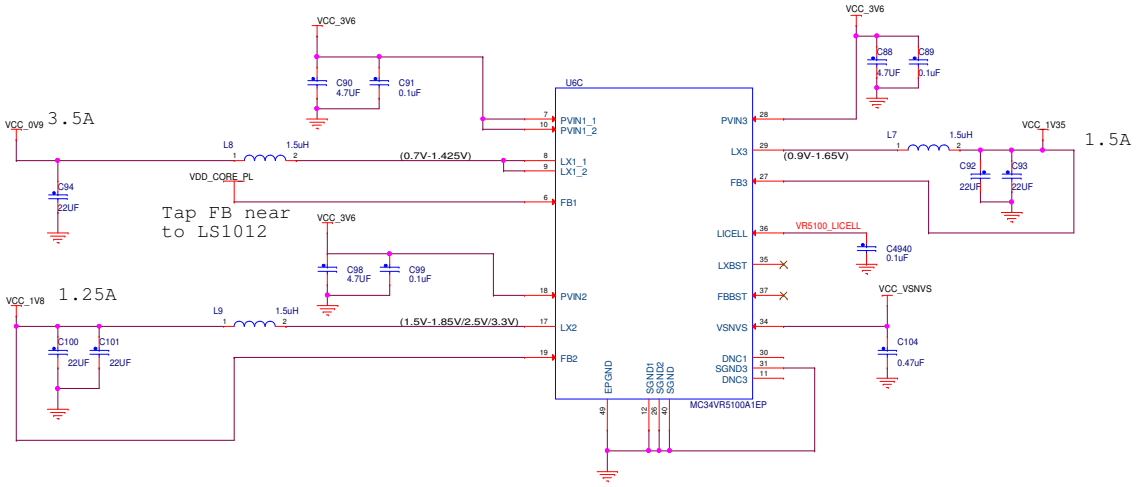
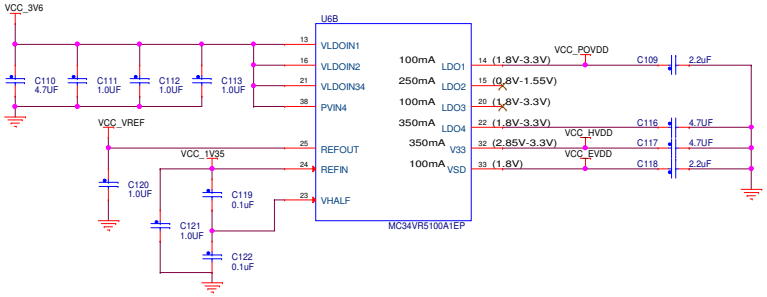
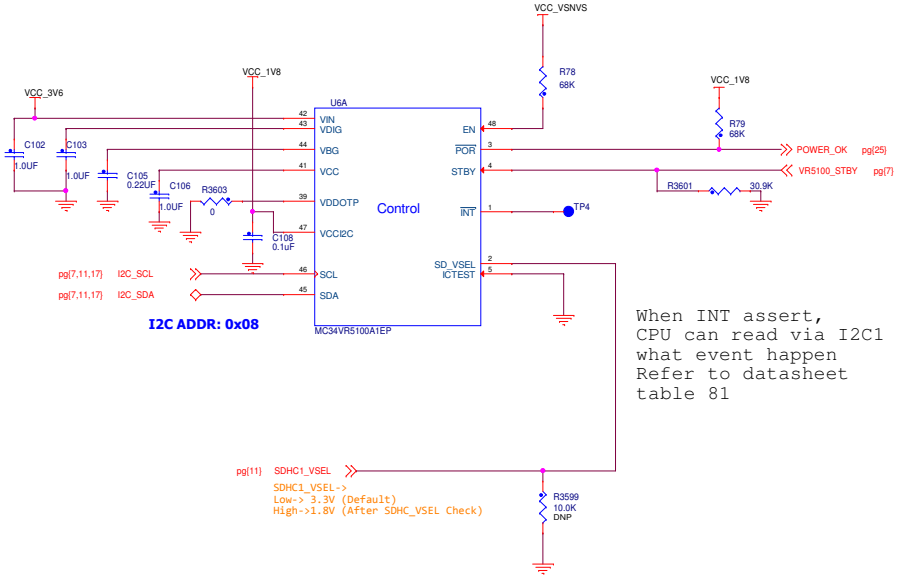
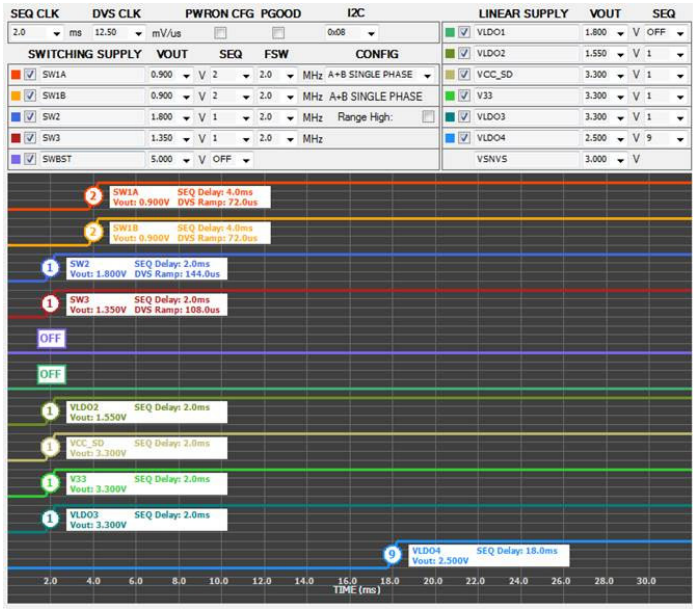
VR5100







When INT assert,
CPU can read via I2C1
what event happen
Refer to datasheet
table 81



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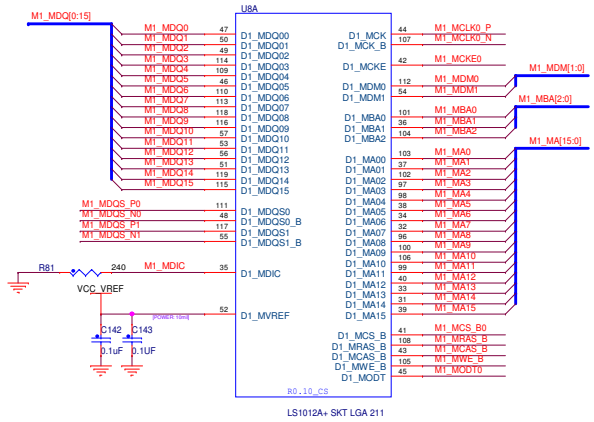
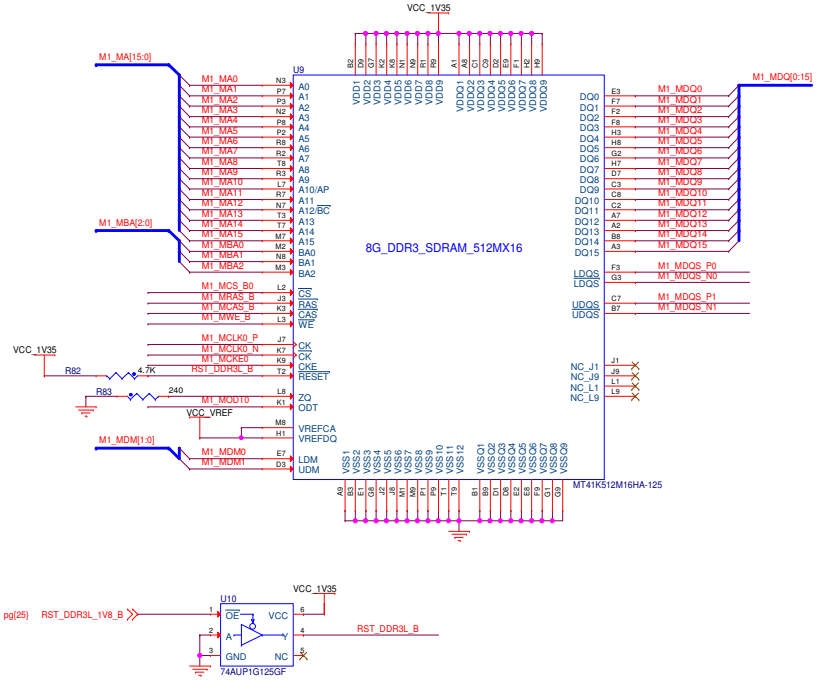
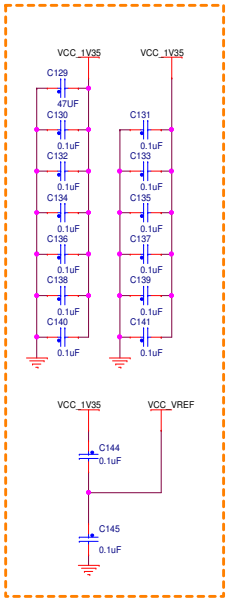
LS1012 DDR3L CONTROLLER BLOCK







Decoupling for DDR3L memory.

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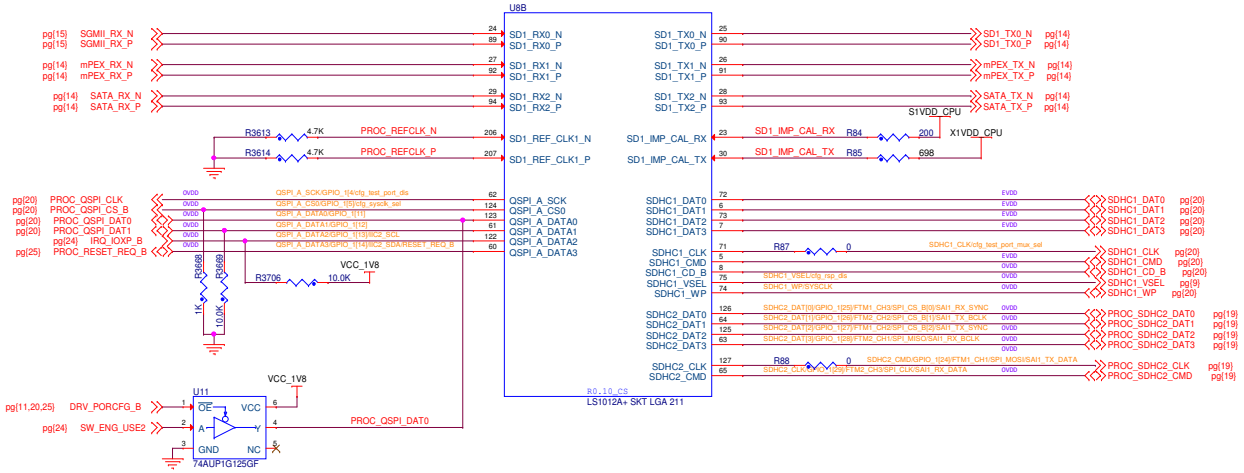
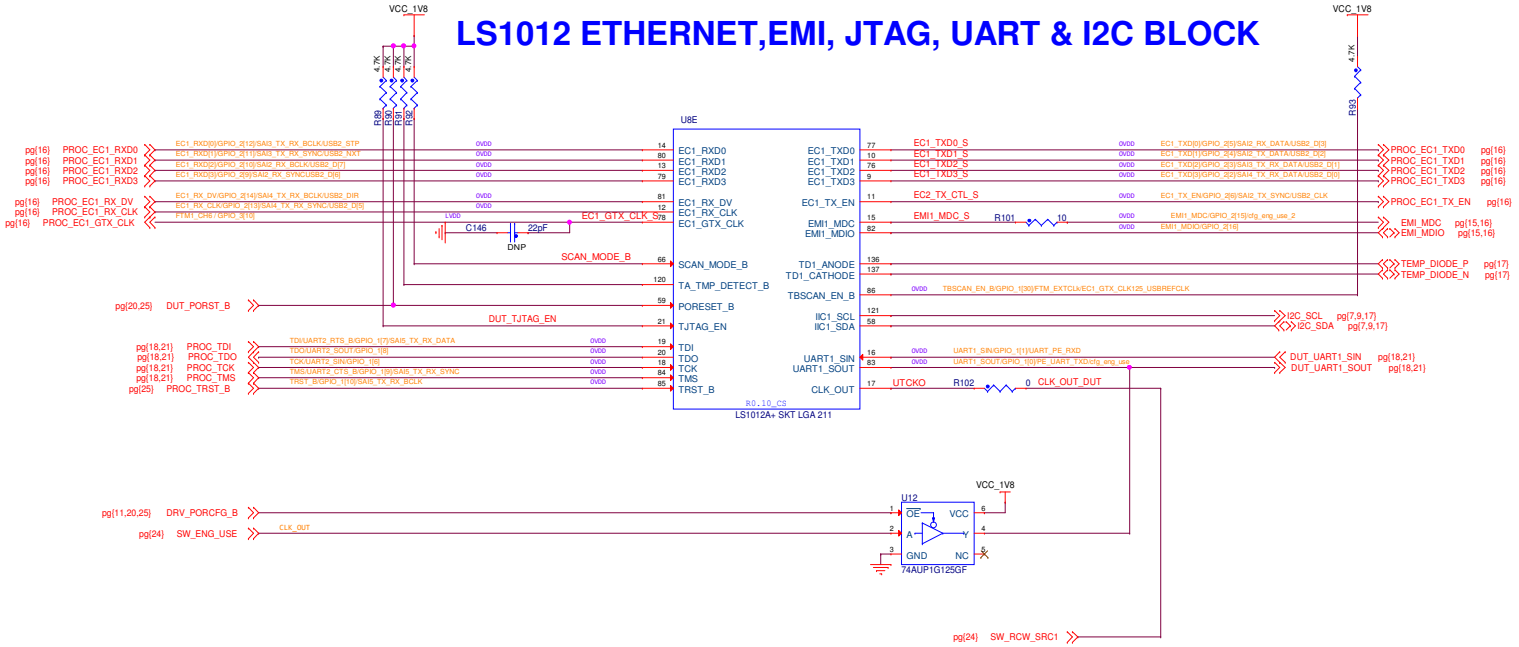
LS1012 SERDES BLOCK



LS1012 ETHERNET,EMI, JTAG, UART & I2C BLOCK



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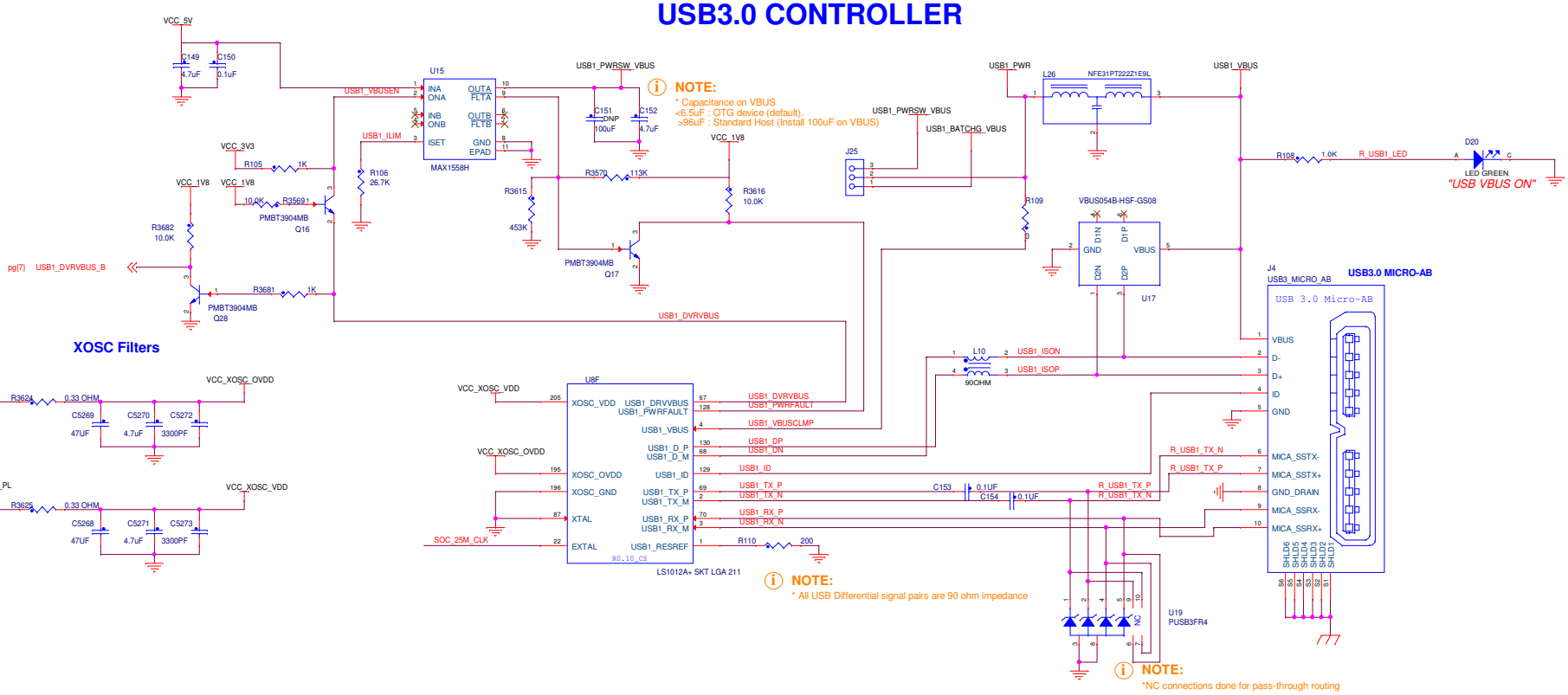
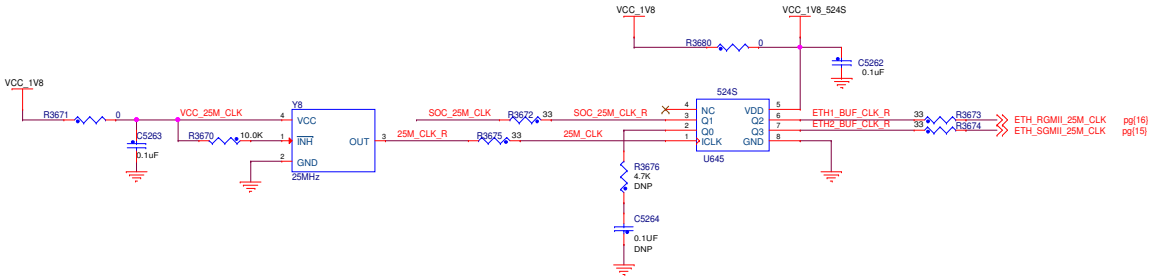
USB3.0 CONTROLLER



CLOCK



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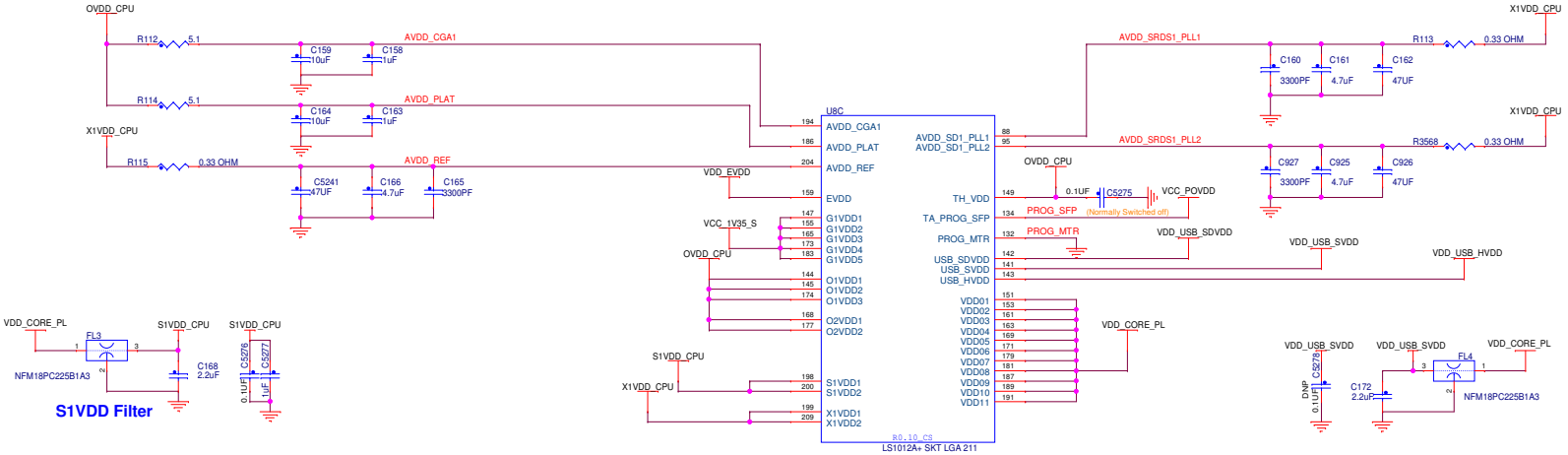
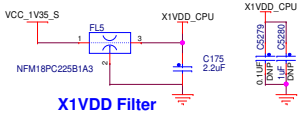
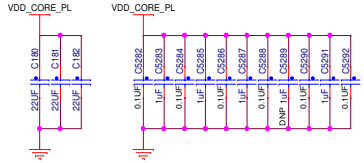
LS1012 POWER BLOCK

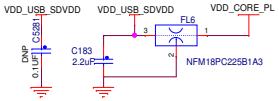


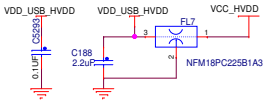
S1VDD Filter



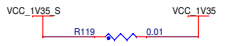
X1VDD Filter

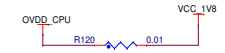


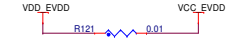


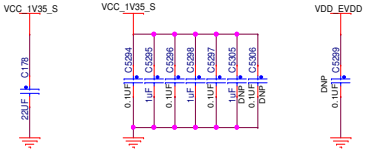


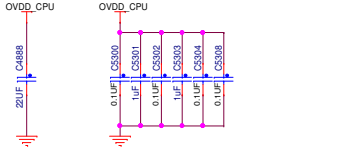
Shunt Resistors for Current Measurement

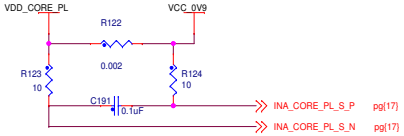


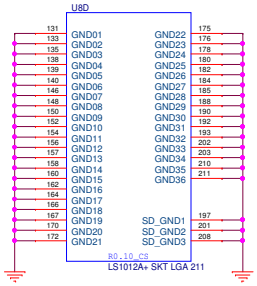












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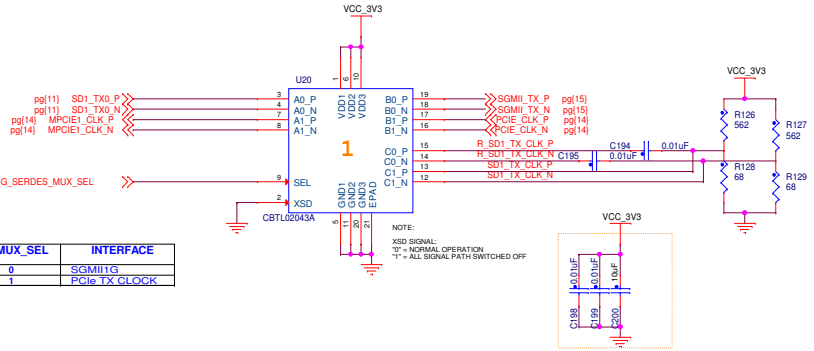
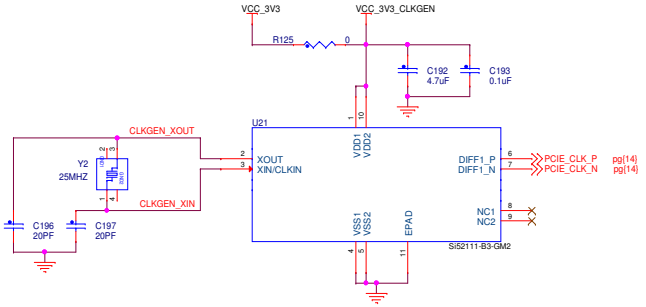
SERDES MUXES

SERDES LANEA MUX



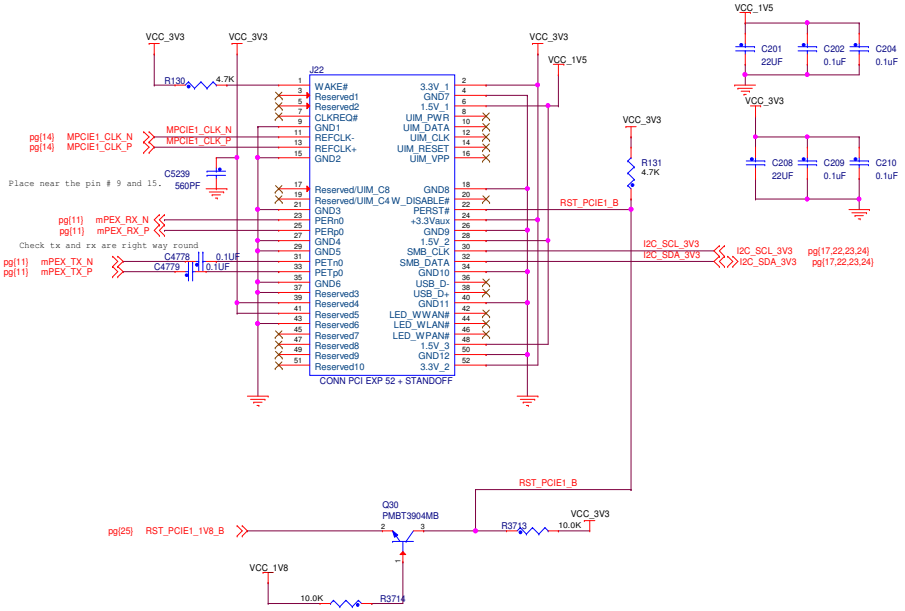
CFG_SERDES_MUX_SEL	INTERFACE
0	SGMII1G
1	PCIe TX CLOCK

PCIE HCSL CLOCK GENERATOR

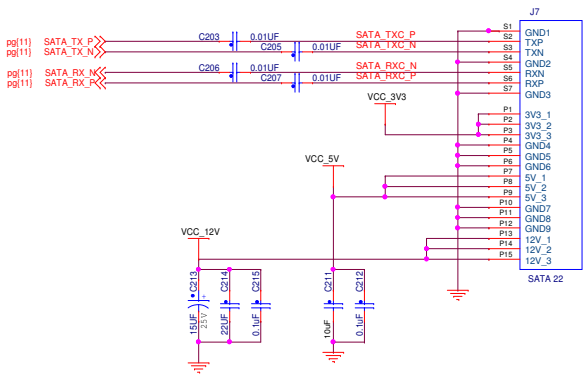


Half mini-PCIex1

MINI PCI EXPRESS1



SATA3.0 INTERFACE



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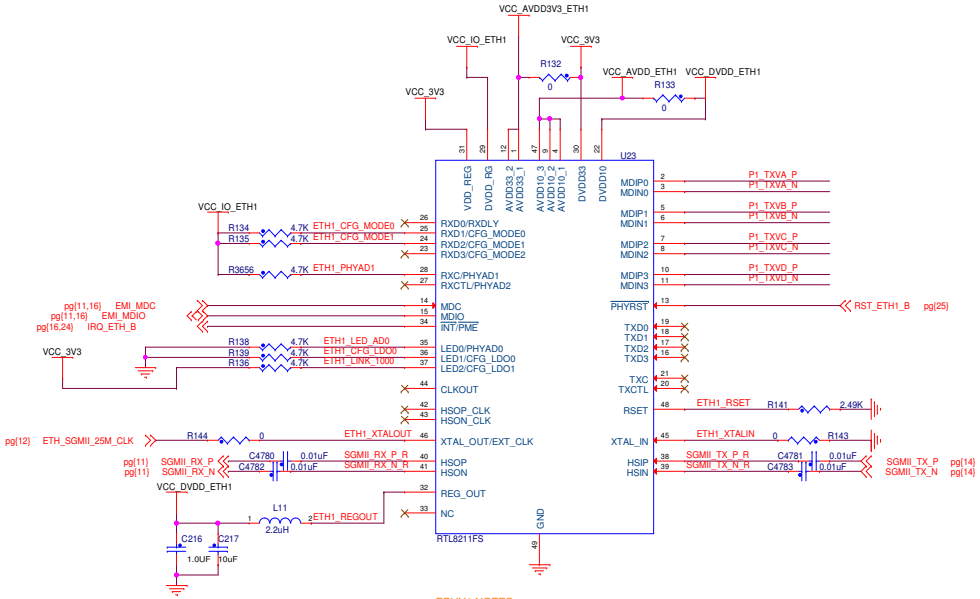
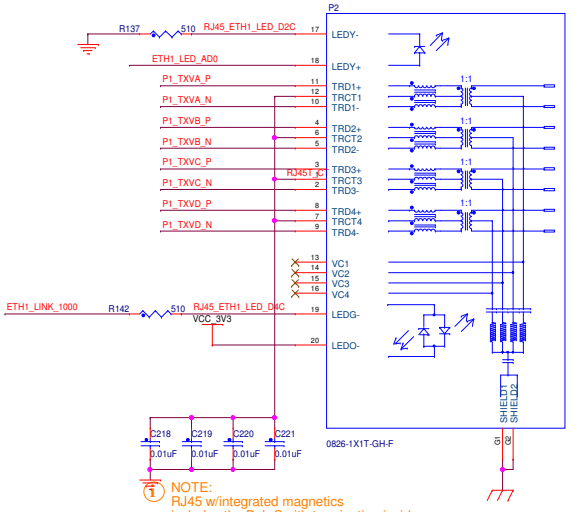
ETHERNET SGMII PHY INTERFACE



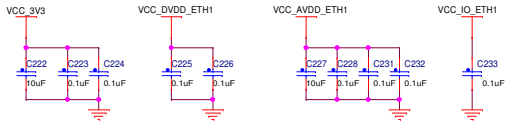
EPHY1 NOTES:

1) HARDWARE BOOTSTRAP SETTINGS:
->PHY_AD[2:0] = 010: PHY Addr = 0b00010
->CFG_MODE[2:0]=011: SGMII <=> UTP
->CFG_LDO[1:0] = 01 : RGMII IO LDO voltage selection (1.8V)
->RXDLY = X: RGMII RXC clock skew = 2.0ns

ETHERNET PORT CONNECTORS



NOTE:
RJ45 w/integrated magnetics
includes the Bob Smith termination inside.



ICAP Classification:	CP: X	IUO:	PUBI:
Drawing Title: LS1012ARDB			
Page Title: 015_SGMII PHY			
Size C	Document Number SCH-28872 PDF: SPF-28872		Rev D
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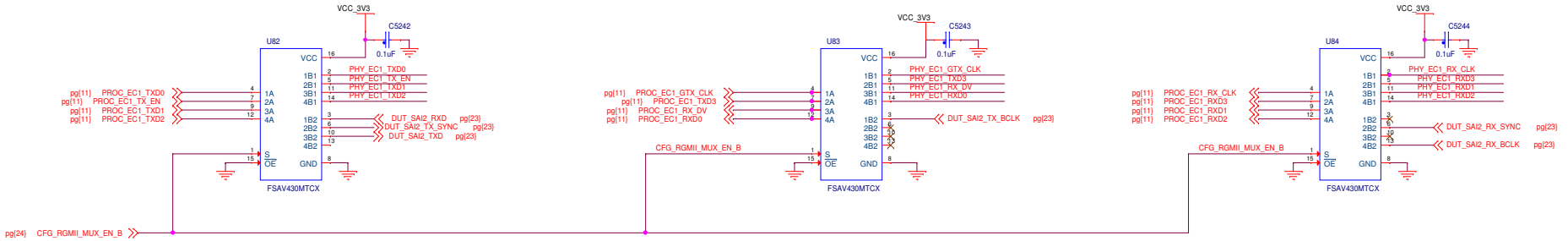
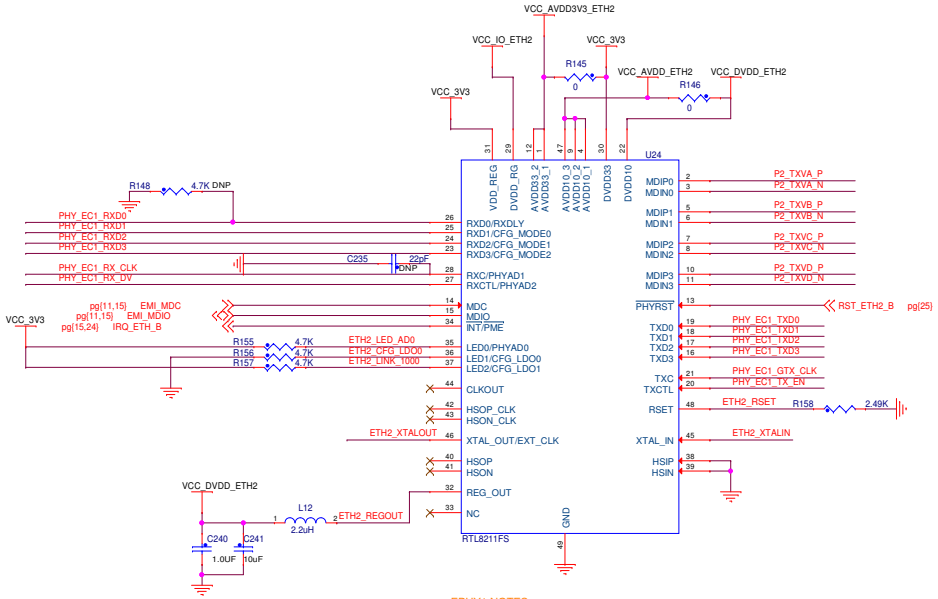
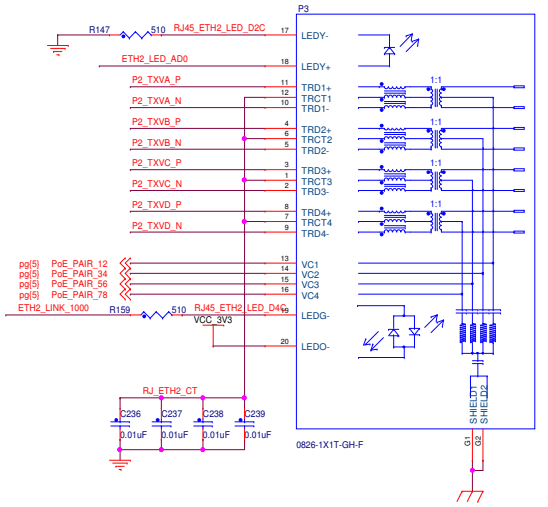
ETHERNET RGMII PHY INTERFACE





ETHERNET PORT CONNECTORS

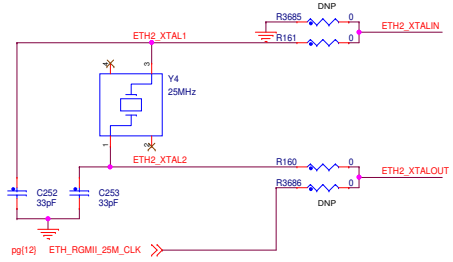


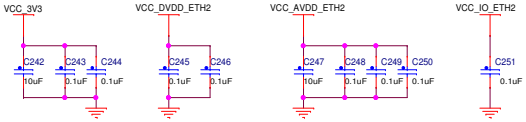
EPHY1 NOTES:

1) HARDWARE BOOTSTRAP SETTINGS:
->PHY_AD[2:0] = 001: PHY Addr = 0b00001
->CFG_MODE[2:0]=000: RGMII <=> UTP
->CFG_LDO[1:0] = 01 : RGMII IO LDO voltage selection (1.8V)
->RXDLY = X: RGMII RXC clock skew = 2.0ns

NOTE:
RJ45 w/integrated magnetics
includes the Bob Smith termination inside.

PHY CLOCK





ICAP Classification:	CP: X	IUO:	PUBI:
Drawing Title: LS1012ARDB			
Page Title: 016_RGMII&SAI: MUX & PHY(PoE)			
Size C	Document Number SCH-28872 PDF: SPF-28872		Rev D
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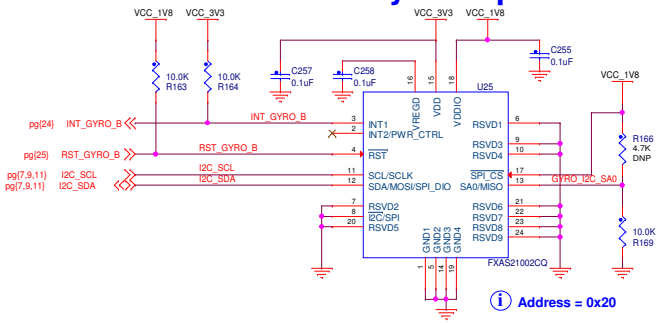
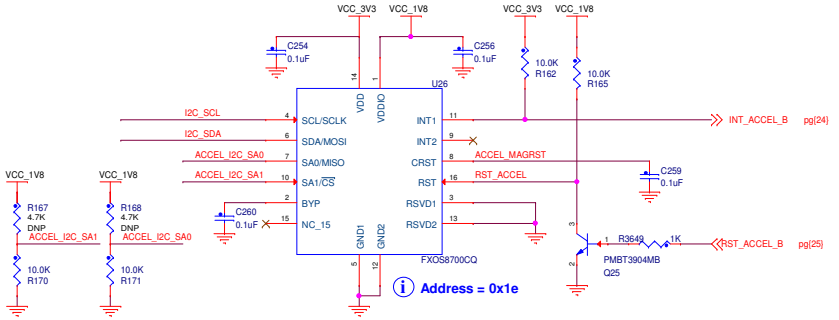
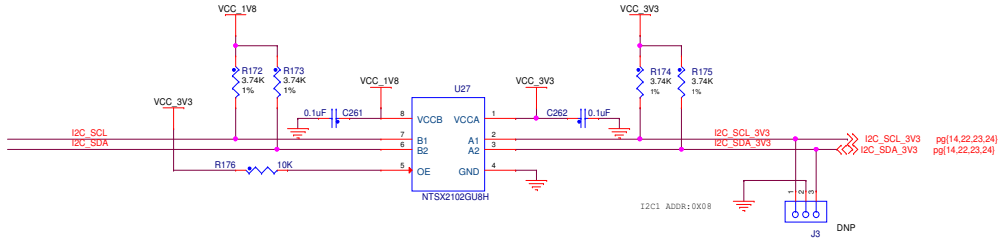
Gyroscope



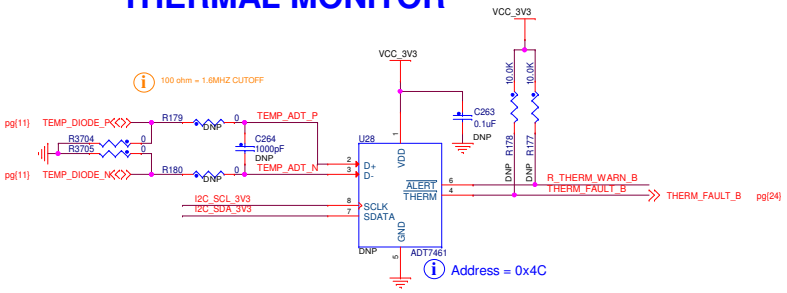
Accelerometer



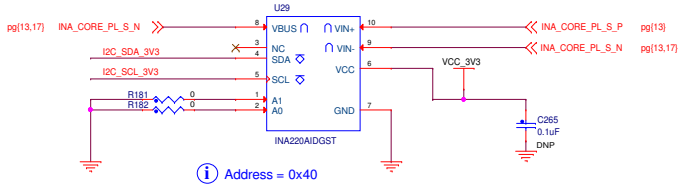
I2C 1.8V <=> 3.3V



THERMAL MONITOR



CURRENT & POWER MONITOR



ICAP Classification:	CP: X	IUO:	PUBI:
Drawing Title: LS1012ARDB			
Page Title: 017_I2C INTERFACE			
Size C	Document Number SCH-28872 PDF: SPF-28872		Rev D
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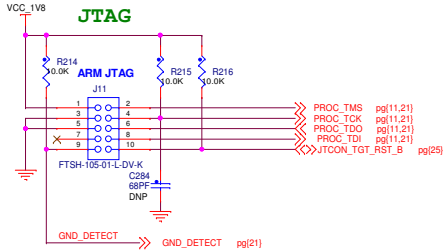
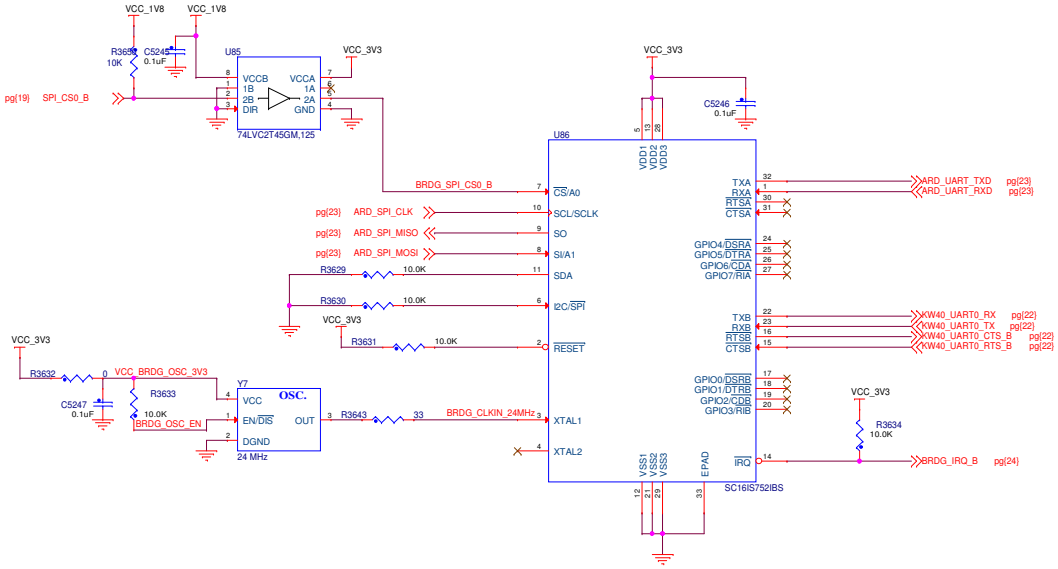
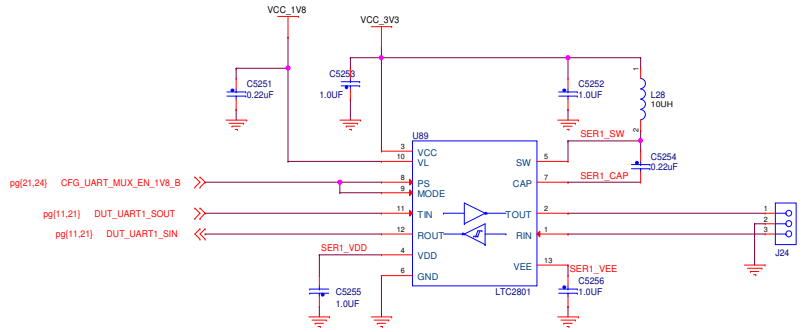
ARM JTAG CONNECTION



SPI TO DUAL-UART BRIDGE



UART TRANSCEIVER



ICAP Classification: CP: X IUO: PUBI:		
Drawing Title: LS1012ARDB		
Page Title: 018_SDHC1_MUX,JTAG & UART		
Size C	Document Number SCH-28872 PDF: SPF-28872	Rev D
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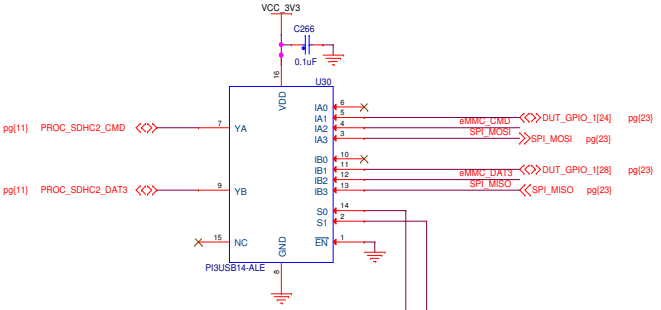
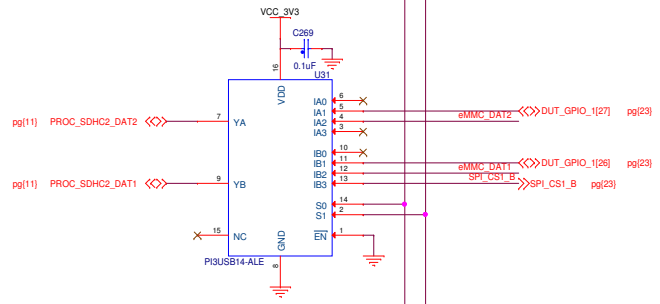
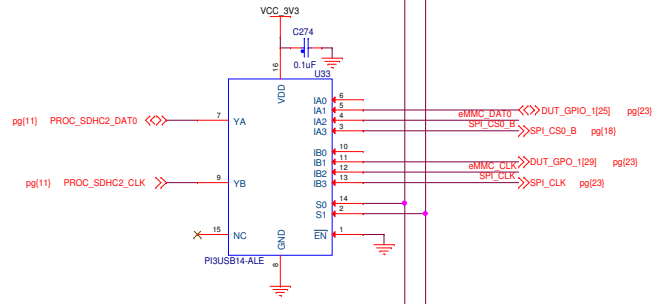
SDHC2 MUX

CFG_MUX_SDHC2_S[1:0]	INTERFACE
00	X
01	GPIO (To Arduino)
10	eMMC Memory
11	SPI



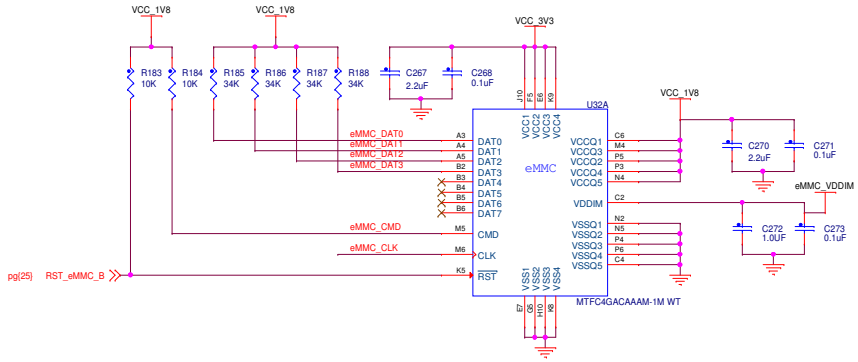


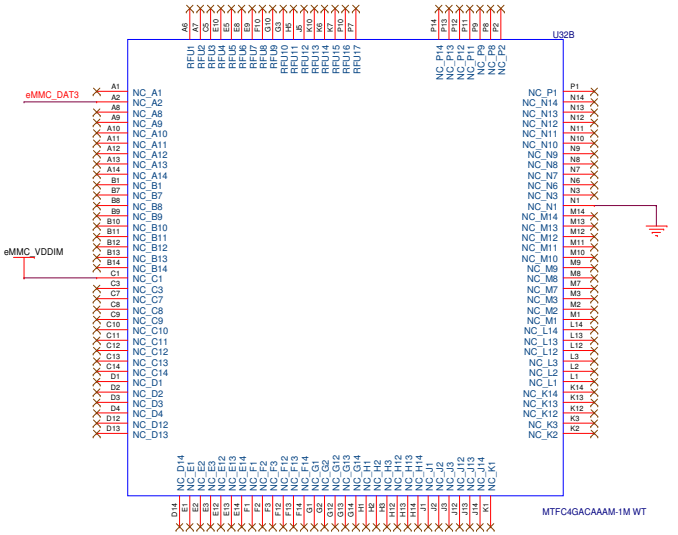


pg[24] CFG_MUX_SDHC2_S0

pg[24] CFG_MUX_SDHC2_S1

eMMC on SDHC2





ICAP Classification: CP: X IUO: PUBI:

Drawing Title: LS1012ARDB

Page Title: 019_SHDC2: eMMC MEM & SD WiFi

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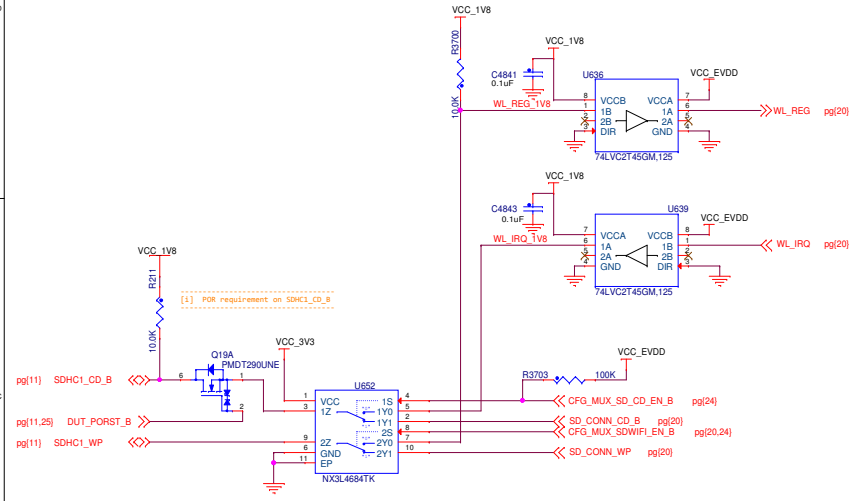
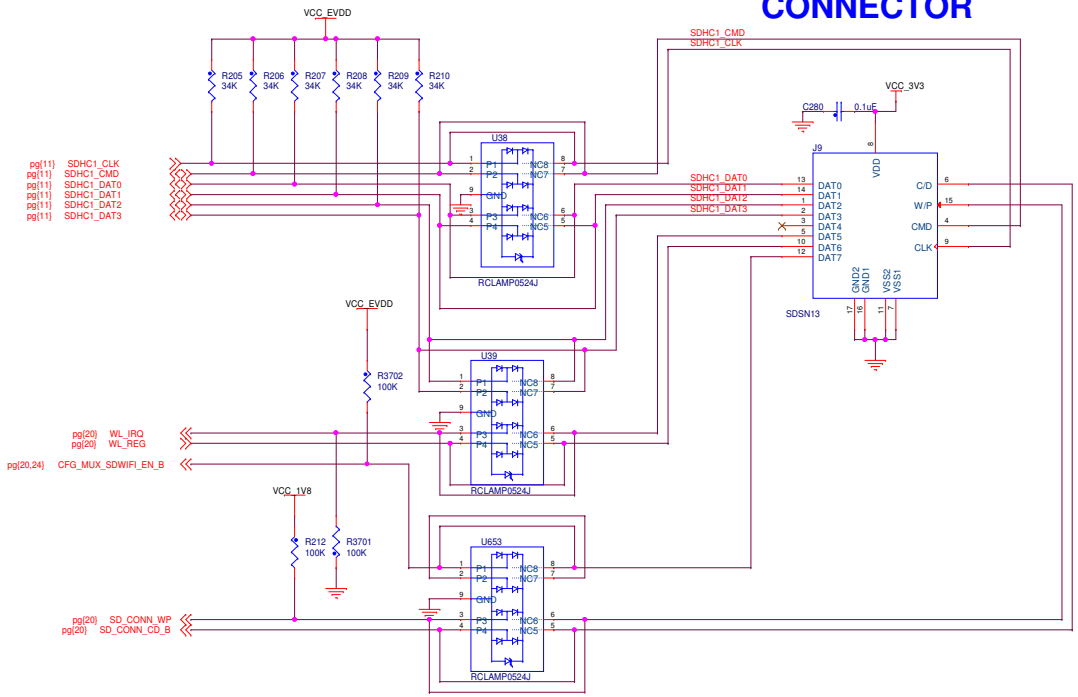
SDHC1

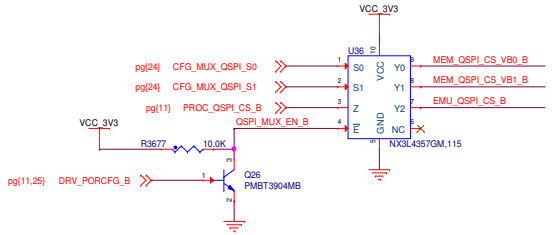
CD & WP MUX



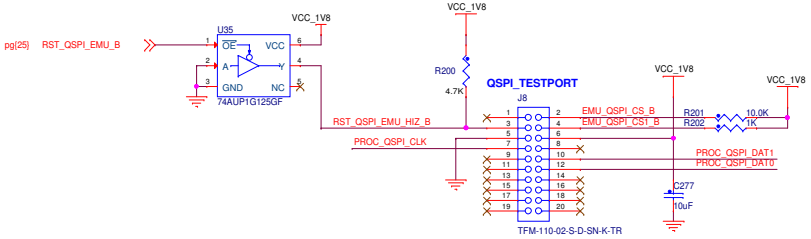
CONNECTOR



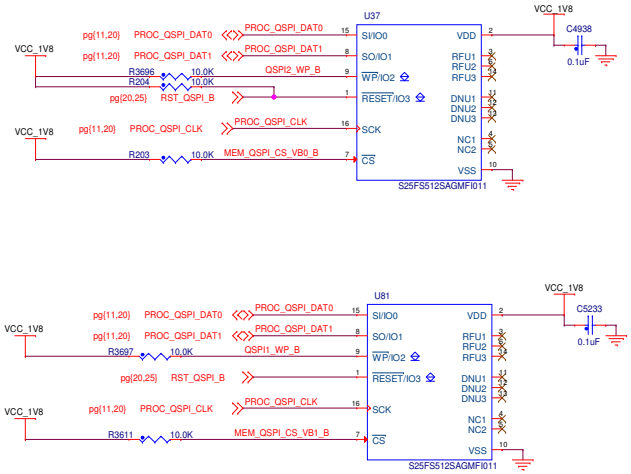
QSPI MUX



QSPI EMULATOR



QSPI FLASH (512MBIT)



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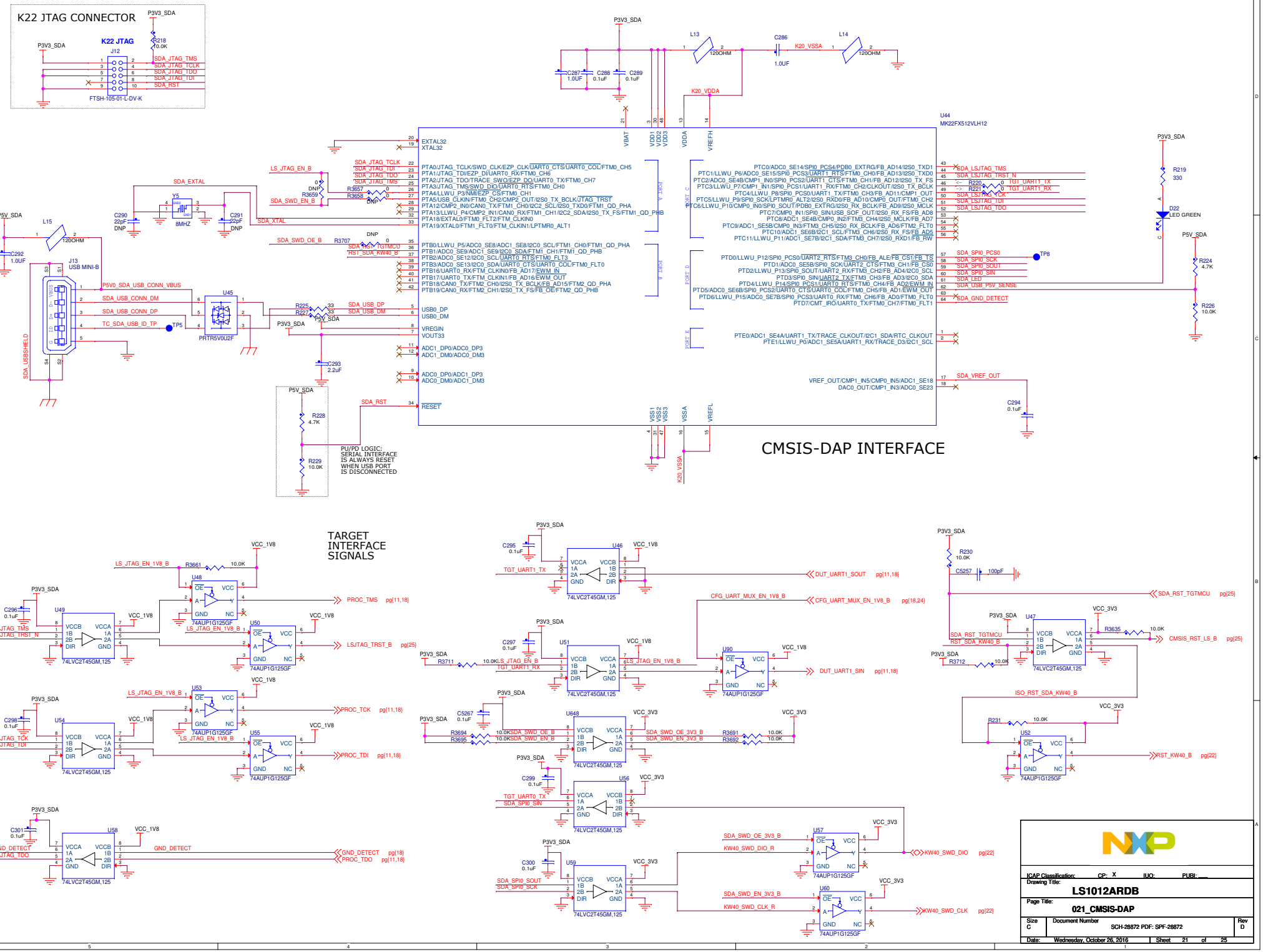
Drawing Title:	LS1012ARDB		
Page Title:	020_QSPI Device & SD Connector		
Size: C	Document Number: SCH-28872 PDF: SPF-28872		Rev: D
Date: Wednesday, October 26, 2016		Sheet 20 of 25	


K22 JTAG CONNECTOR
K22 JTAG
J12
FTSH-105-01-L-DV-K
CMSIS-DAP INTERFACE
TARGET INTERFACE SIGNALS
PU/PD LOGIC: SERIAL INTERFACE IS ALWAYS RESET WHEN USB PORT IS DISCONNECTED
MK22FX512VLH12
U44
8MHZ
PRTR5V0U2F
74LVC2T45GM,125
74AUP1G125GF
LED GREEN
USB MINI-B
LS1012ARDB
021_CMSIS-DAP
SCH-28872 PDF: SPF-28872
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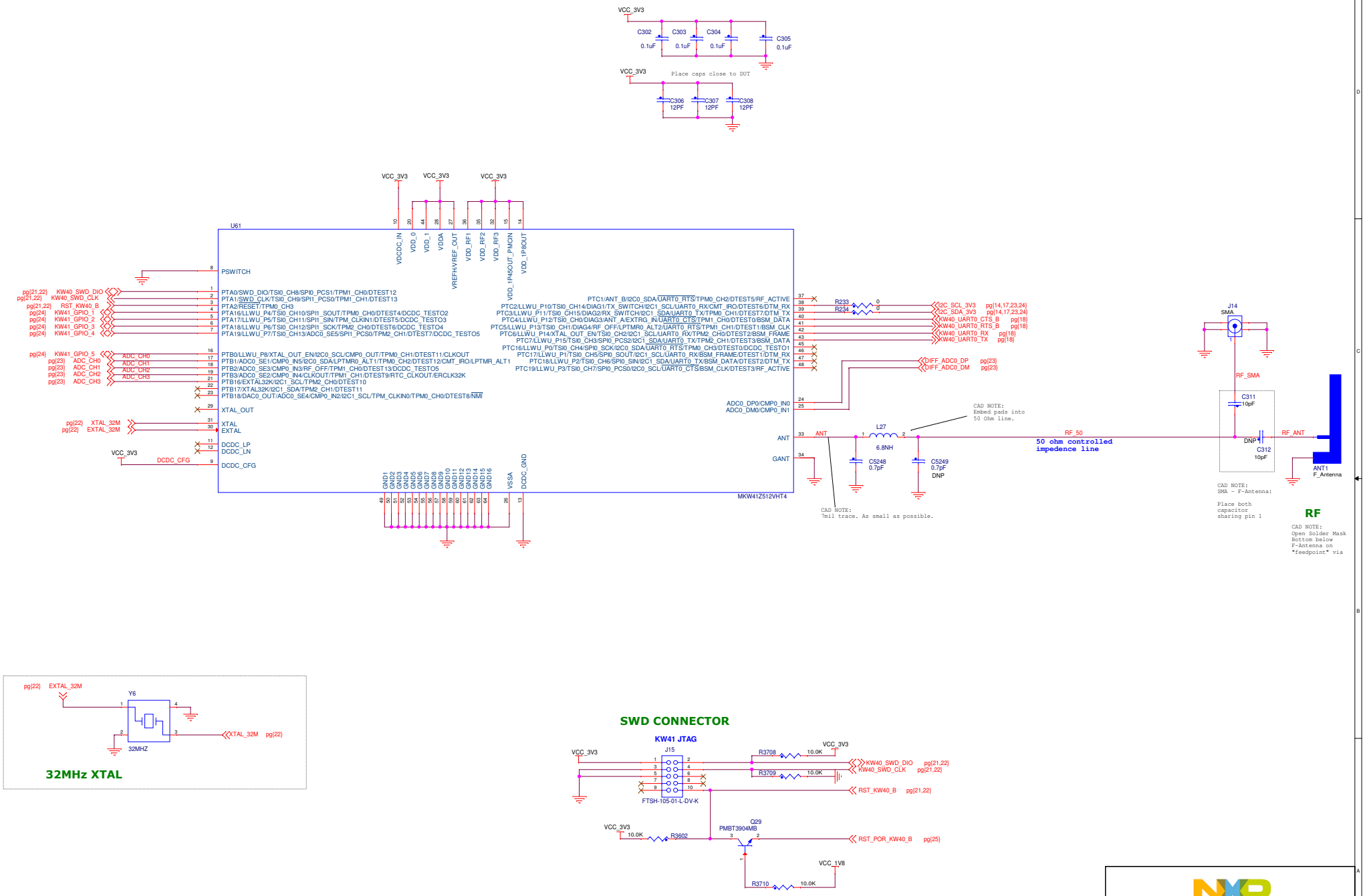

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Drawing Title:	LS1012ARDB		
Page Title:	022_KW41 MCU		
Size C	Document Number SCH-28872 PDF: SPF-28872		Rev D
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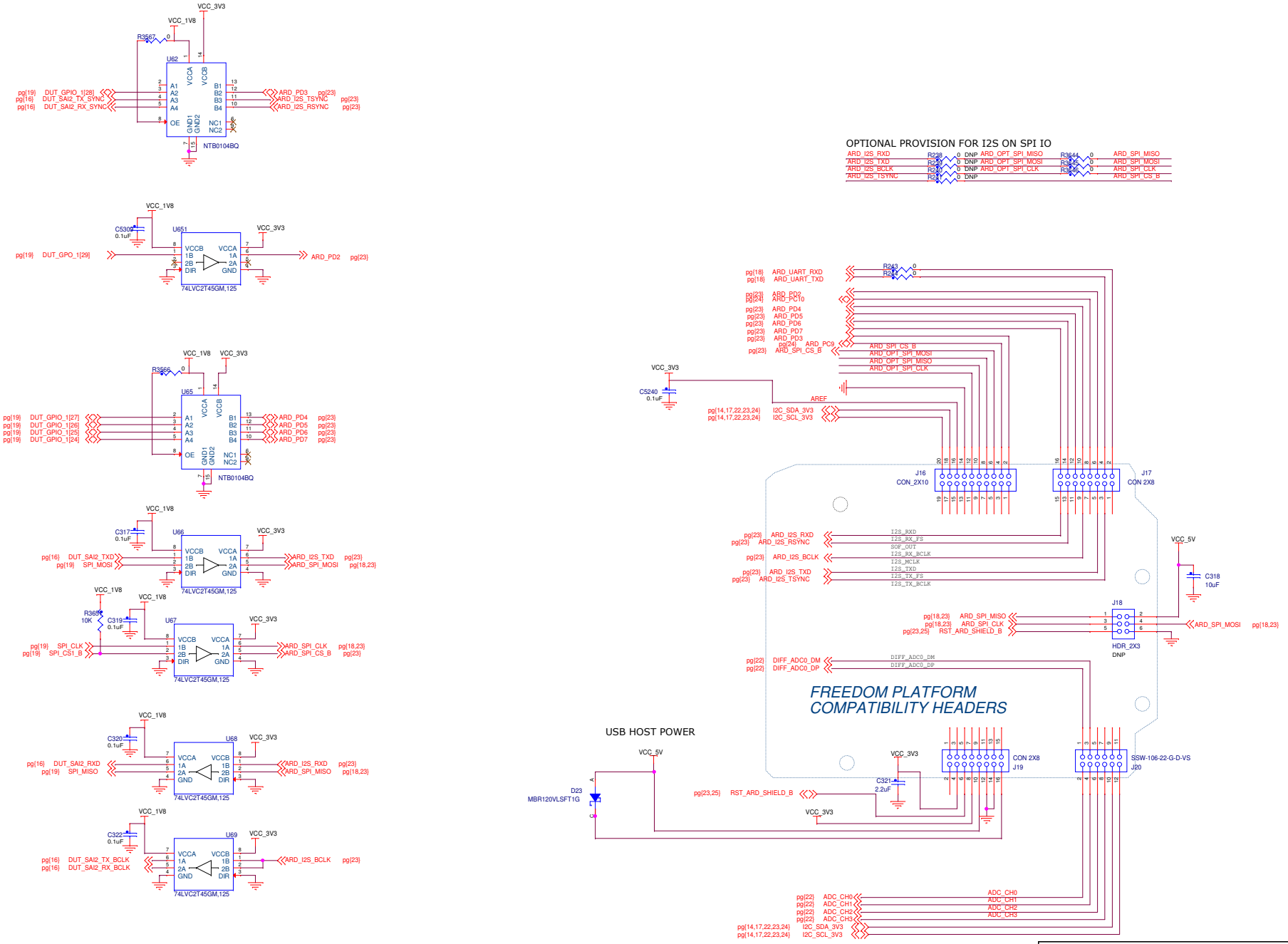

ICAP Classification: CP: X IUO: PUBI: ___

Drawing Title: **LS1012ARDB**

Page Title: **023_Arduino**

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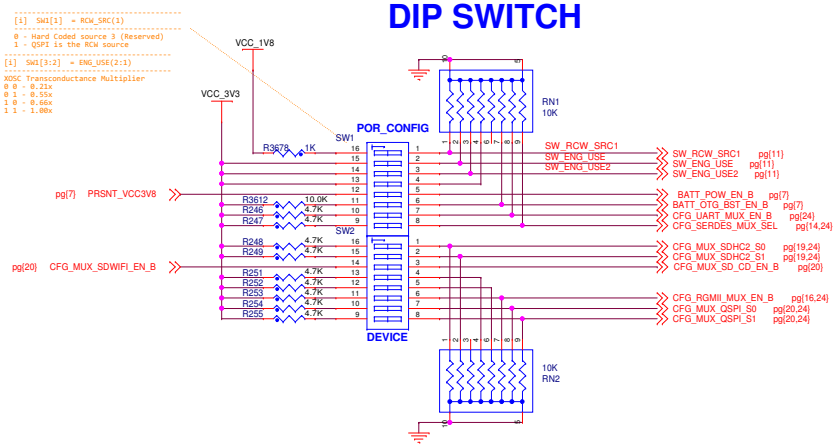
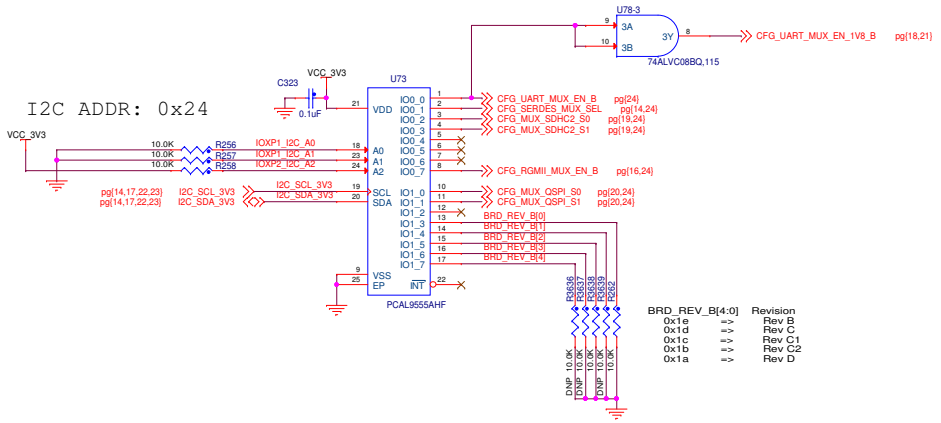
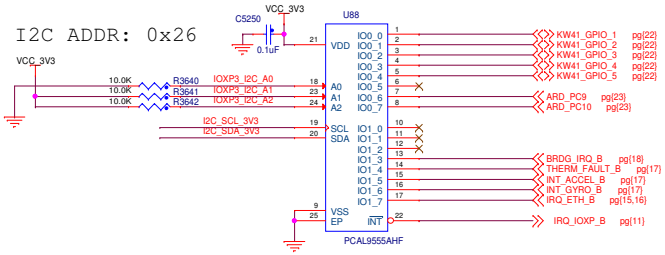
DIP SWITCH



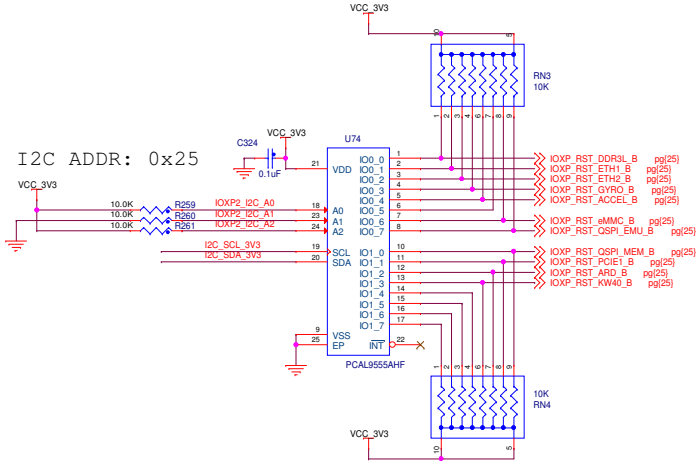
I2C IO-EXPANDER: MUX SEL



I2C IOEXPANDER : INTERRUPT AND GPIO

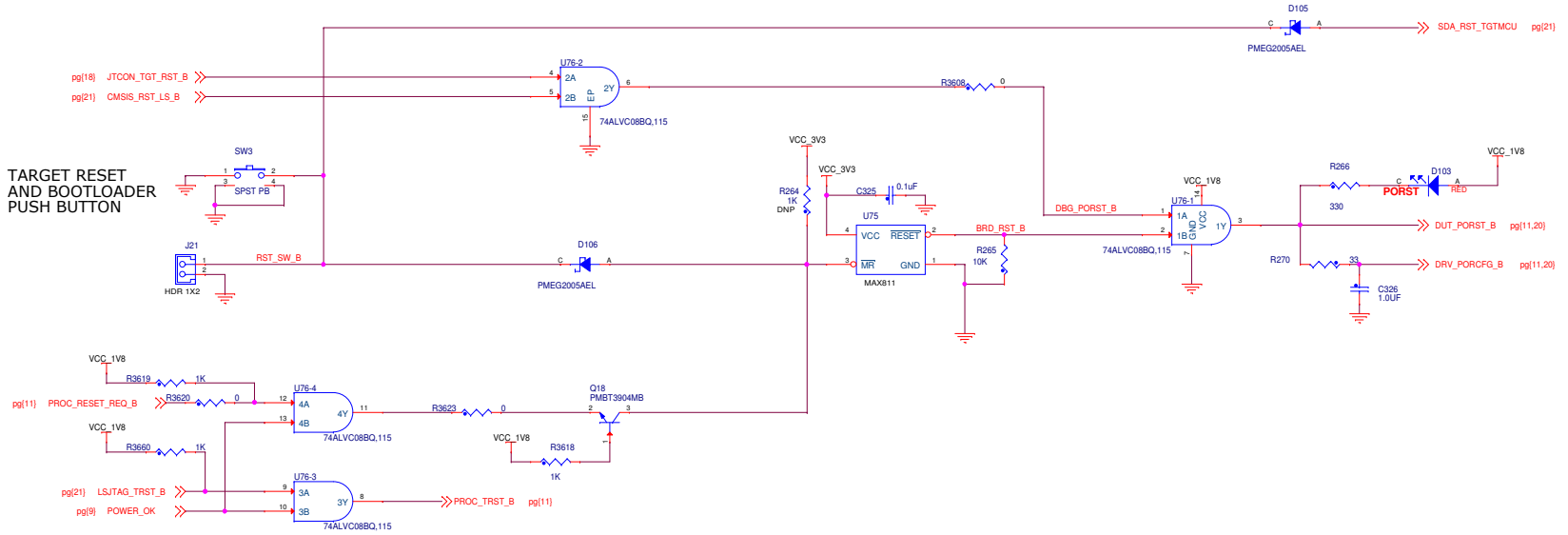


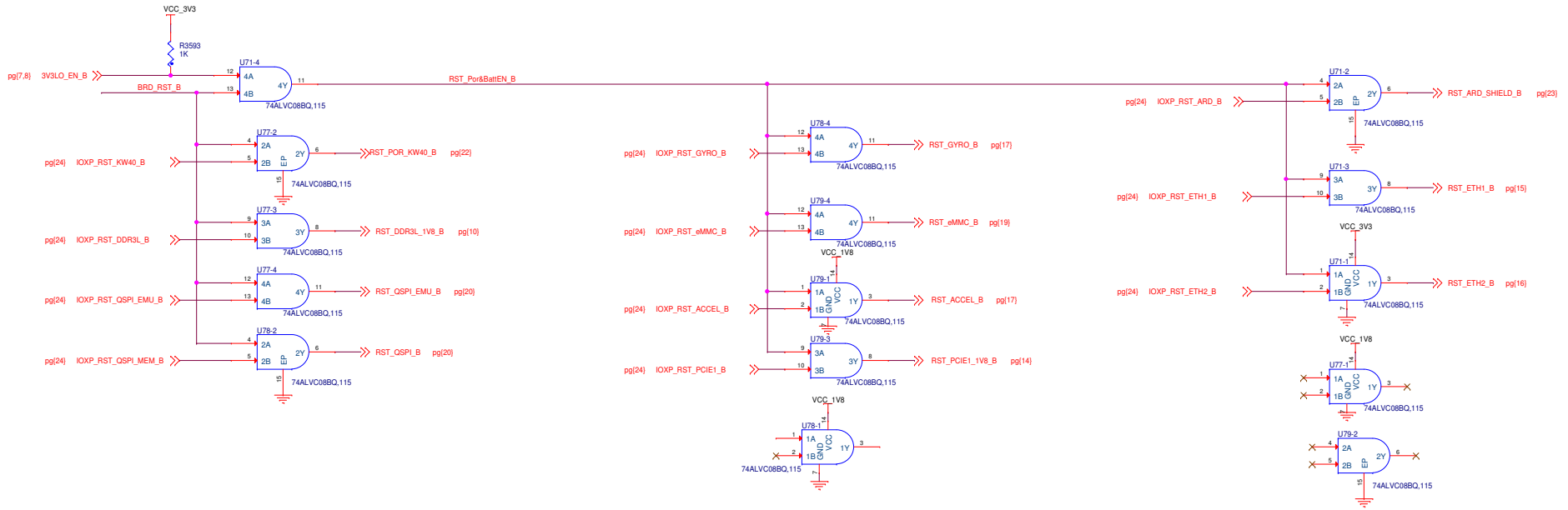
I2C IO-EXPANDER: RESET



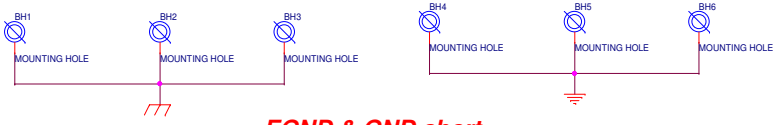
ICAP Classification:	CP: X	IUO:	PUBI:
Drawing Title:	LS1012ARDB		
Page Title:	024_DIP SW, MUX CONTROL		
Size: C	Document Number: SCH-28872 PDF: SPF-28872		Rev: D
Date: Wednesday, October 26, 2016	Sheet 24 of 25		

RESET



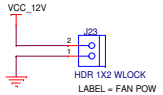


MOUNTING HOLES



EGND & GND short through chassis.

FAN POWER (OPTIONAL)



ICAP Classification:	CP: X	IUO:	PUBI:
Drawing Title:	LS1012ARDB		
Page Title:	025_RESET & MOUNTING HOLES		
Size C	Document Number SCH-28872 PDF: SPF-28872		Rev D
Date: Wednesday, October 26, 2016	Sheet 25 of 25		