NXP Semiconductors
Application Note

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Hardware and Layout Design Considerations for DDR4 SDRAM Memory Interfaces

1 About this document

This document provides general hardware and layout considerations and guidelines for hardware engineers implementing a DDR4 memory subsystem.

The rules and recommendations in this document serve as an initial baseline for board designers to begin their specific implementations, such as fly-by memory topology.

NOTE

It is strongly recommended that the board designer verifies that all aspects, such as signal integrity, electrical timings, and so on, are addressed by using simulation models before board fabrication.

Contents

2 Recommended resources

The following documentation may provide additional, important information:

- The DDR chapter of the applicable device reference manual
- Micron's website: http://www.micron.com
- JEDEC's website: http://www.jedec.com (a good example is *DDR4 SDRAM Specification*)

3 DDR4 design checklist

Table 1. DDR4 design checklist

No.	Task	Completed
	Simulation	
1	Ensure that optimal termination values, signal topology, and trace lengths are determined through simulation for each signal group in the memory implementation. The unique signal groups are as follows: • **Data group:** MDQS(8:0), $\overline{\text{MDQS}}$(8:0), MDM(8:0), MDQ(63:0), MECC(7:0) **NOTE:** In a x4 DRAM mode, the MDM(8:0) signals are no longer available as mask signals but configured in a secondary function as MDQS(17:9) signals. Therefore, the full Data Group for a x4 DRAM mode: MDQS(17:0), MDQS(17:0), MDQ(63:0), MECC(7:0) • **Address/CMD group:** MBG(1:0) MBA(1:0), MA(13:0), $\overline{\text{MRAS}}$/MA16, $\overline{\text{MCAS}}$/MA15, $\overline{\text{MWE}}$/MA14, $\overline{\text{MACT}}$ • **Control group:** $\overline{\text{MCS}}$(3:0), MCKE(3:0), MODT(3:0), $\overline{\text{MAPAR\_ERR}}$/ALERT_n, MAPAR_OUT/PAR • **Clock group:** MCK(3:0) and $\overline{\text{MCK}}$(3:0) **NOTE:** These groupings assume a full, 72-bit data implementation (64-bit + 8 bits of ECC). For 32-bit DDR bus mode (32-bit + 8 bits of ECC), you may choose to have fewer MCK, $\overline{\text{MCK}}$, $\overline{\text{MCS}}$, MCKE, and MODT signals.	
2	Ensure to consider the following 3 points in read timing budget simulation: • No Slew Rate Derating should be done for the FSL DDR4 controllers on reads. • Timing budgets for reads can be done with customer's simulation tool by adding the setup and hold margins rather than looking at the setup or hold margins by themselves (to account for the DQS-DQ calibration). • Read timing should be taken at Vref rather than Vin levels. (i.e. ALL read timing measurements for DQ shall be taken at Vref. No read timing measurements are taken at Vih(ac), Vil(ac), Vih(dc), or Vil(dc)). Ensure the selected termination scheme meets the AC signaling parameters (voltage levels, slew rate, and overshoot/undershoot) across all memory chips in the design.	
	Termination scheme **NOTE:** It is assumed that the designer is using the mainstream termination approach as found in JEDEC standards. Specifically, it is assumed that on-die termination is used for the data groups and that external parallel resistors tied to V_{TT} are used for the address/CMD and control groups. **NOTE:** Different termination techniques may also prove valid and useful, but are left to the designer to validate through simulation.	
3	Ensure the worst-case power dissipation for the termination resistors are within the manufacturer's rating for the selected devices. See Selecting termination resistors.	
4	Ensure the V_{TT} resistors are properly placed by tying the R_T terminators into the V_{TT} island at the end of the memory bus.	
5	Ensure the differential termination is present on the clock lines for discrete memory populations, as shown in item 55 of this table. **NOTE:** The DIMM modules already contain this termination.	

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Table 1. DDR4 design checklist (continued)

No.	Task	Completed
6	Ensure the worst-case current for the V_{TT} plane is calculated based on the design termination scheme. See Selecting termination resistors.	
7	Ensure the V_{TT} regulator can support the steady state and transient current needs of the design.	
8	Ensure the V_{TT} island is properly decoupled with high frequency decoupling: • Use at least one low ESL cap or two standard decoupling caps for each four-pack resistor network (or every four discrete resistors). • Use at least one 4.7 µF cap at each end of the V_{TT} island. **NOTE:** This recommendation is based on a top-layer V_{TT} surface island (lower inductance). If an internal split is used, more capacitors may be needed to handle the transient current demands.	
9	Ensure the V_{TT} island is properly decoupled with bulk decoupling. At least one bulk cap (47–220 µF) capacitor should be at each end of the island.	
10	Ensure the V_{TT} island is placed at the end of the memory channel and as closely as possible to the last memory bank. Ensure the V_{TT} regulator is placed in close proximity to the island.	
11	Ensure a wide surface trace (~150 mils) is used for the V_{TT} island trace.	
V_{REF} **NOTE:** In DDR4, V_{REF} is only used for address/command bus of DDR4 DRAM. Memory controller V_{REF} is generated internally.		
12	Ensure that V_{REF} is routed with appropriate trace width.	
13	Ensure that V_{REF} is isolated from noisy aggressors. Maintain at least a 20–25 mils clearance from V_{REF} to other traces; if possible, isolate V_{REF} with adjacent ground traces.	
14	Ensure that V_{REF} is properly decoupled by decoupling the source and each destination pin with 0.1 µf caps.	
15	Ensure the V_{REF} source tracks variations in V_{DD}, temperature, and noise, as required by the JEDEC specification.	
16	Ensure the V_{REF} source supplies the minimal current required by the DDR4 DRAM.	
17	For QorIQ products with DDR3L and DDR4 memory options, there is an external V_{REF} pin available for DDR3L mode. When DDR4 mode is used the external V_{REF} pin needs to be grounded. For QorIQ products with DDR4 only option there is no external V_{REF} pin.	
18	If a resistor divider network is used to generate V_{REF}, ensure that both resistors have the same value and 1% tolerance.	
GV_{DD}, V_{PP} power supplies		
19	Ensure the V_{PP} supply is ramped before or at the same time as GV_{DD} supply.	
Routing		
20	The recommended routing order within the DDR4 interface is as follows: • Data • Address/command • Control • Clocks • Power	

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Table 1. DDR4 design checklist (continued)

No.	Task	Completed
	NOTE: The fly-by routing is recommended for address, command, control, and clock signal bus.	
21	Complete the following global routing items: • Do not route any DDR4 signals over splits or voids. • Ensure that traces routed near the edge of a reference plane maintain at least 30–40 mils gap to the edge of the reference plane. • Allow no more than 1/2 of a trace width to be routed over via antipad.	
22	Ensure the max lead-in trace length for data/address/command signals are no longer than 7 inches.	
	Routing data bus	
23	When routing the data lanes, route the outer-most (that is, the longest lane) first, because this determines the amount of trace length to add on the inner data lanes.	
24	Route all signals within a given byte lane on the same critical layer with the same via count. Assuming ECC is used, the DDR4 data bus consists of nine data byte lanes. **NOTE:** The byte ordering below is not a requirement; byte lanes can be routed in the order that best fits the customer design. • Byte lane 0—MDQ(7:0), MDM(0), MDQS(0), $\overline{\text{MDQS}}$(0) • Byte lane 1—MDQ(15:8), MDM(1), MDQS(1), $\overline{\text{MDQS}}$(1) • Byte lane 2—MDQ(23:16), MDM(2), MDQS(2), $\overline{\text{MDQS}}$(2) • Byte lane 3—MDQ(31:24), MDM(3), MDQS(3), $\overline{\text{MDQS}}$(3) • Byte lane 4—MDQ(39:32), MDM(4), MDQS(4), $\overline{\text{MDQS}}$(4) • Byte lane 5—MDQ(47:40), MDM(5), MDQS(5), $\overline{\text{MDQS}}$(5) • Byte lane 6—MDQ(55:48), MDM(6), MDQS(6), $\overline{\text{MDQS}}$(6) • Byte lane 7—MDQ(63:56), MDM(7), MDQS(7), $\overline{\text{MDQS}}$(7) • Byte lane 8—MECC(7:0), MDM(8), MDQS(8), $\overline{\text{MDQS}}$(8) To facilitate fan-out of the DDR4 data lanes (if needed), alternate adjacent data lanes onto different critical layers (see Figure 1 and Figure 2). **NOTE:** Some product implementations may only implement a 32-bit wide interface. **NOTE:** If the device supports ECC, NXP highly recommends that the user implements ECC on the initial hardware prototypes.	
25	Choose one of the following options to select the impedances and spacings for the DDR4 data group. Option #1 (wider traces—lower trace impedance): • Single-ended impedance = 40 Ω. The lower impedance allows traces to be slightly closer with less cross-talk. • Spacing >= 2-3x distance from signal to adjacent ground plane in PCB stack-up Option #2 (smaller traces—higher trace impedance): • Single-ended impedance = 50 Ω • Spacing >= 2-3x distance from signal to adjacent ground plane in PCB stack-up	
26	Across all DDR4 data lanes: • Ensure that all the data lanes are matched to within 2.0 inches.	
27	Ensure bit and byte swapping rules are applied: • Byte-swap is allowed in any order that would best fit the customer's design. • No specific byte ordering is enforced or required. • Bit-swap is only allowed within a nibble. • Bit-swap across two nibbles is not allowed. • Bit-swap across byte lanes is not allowed. • Swapping of nibbles within a byte lane is allowed.	

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Table 1. DDR4 design checklist (continued)

No.	Task	Completed
	• When DDR4 Discrete DRAM is soldered on the board and two chip selects are used, and the second chip select is bit swizzling (meaning bit mapping from CS0 is additionally swapped in CS1 by swapping DQ0 with DQ1, DQ2 with DQ3, DQ4 with DQ5, and DQ6 with DQ7),then bit map orders of 0x10 (2 1 3 0) and 0x30 (6 5 7 4) are not allowed. • For 32-bit or 16-bit DDR4 data bus, the bit 0 (DQ[0]) and bit 1 (DQ[1]) of ECC byte lane, bit-swap is not allowed.	
28	Ensure that each data lane properly is trace-matched to within 20 mils of its respective differential data strobe. • Ensure the trace matching for parts with operational data rates of higher than 1600 MT/s is within +/-5 mils.	
29	When adding trace lengths to any of the DDR4 signal groups, ensure that there is at least 25 mils between serpentine loops that are in parallel.	
30	MDQS/$\overline{\text{MDQS}}$ considerations: • Match all segment lengths between differential pairs along the entire length of the pair. Trace match the MDQS/$\overline{\text{MDQS}}$ pair to be within +/-5 mils. • Maintain constant line impedance along the routing path by maintaining the required line width and trace separation for the given stackup. • Avoid routing differential pairs adjacent to noisy signal lines or high-speed switching devices such as clock chips. • Data bus can be routed at 50 Ω impedance with ~100 Ω differential impedance. It may benefit from 40-50 Ω impedance and 75-95 Ω differential impedance. • Trace separation between unlike buses should be > 3x distance from signal to adjacent ground plane.	
Routing address/command/control/clock bus		
31	Ensure fly-by topology is used for address/command/control and clock groups. The routing in fly-by topology should go from chip 0 to chip *n* and can be in the order that is most convenient for the board design. The fly-by topology routing of address/command/control and clock groups must end at the termination resistors that are after chip *n*. Choose one of the following options to select the impedances and spacings for the DDR4 address/command/control group. Can route at 50 Ω impedance with 100 Ω differential impedance. However, there may be some benefit seen from routing Address/Command/Control bus at ~40 Ω for traces to connector or from CPU to first memory on a discrete DDR design. Trace separation between unlike buses should be > 3x distance from signal to adjacent ground plane. Tune signals to +/-10 mils of the clock at each device.	
32	Ensure clocks are routed as a differential pair, with the following recommendation: • P-to-N tuning = +/-5 mils **NOTE:** The clock signal trace length from the memory controller to any given DDR4 chip should be longer than its corresponding strobe trace length.	
33	Ensure one clock pair is used for each rank of memory in fly-by topology following the address/command bus routing.	
34	Ensure that all clock pairs are routed on the same critical layer (one referenced to a solid ground plane).	
35	Ensure the clock pair assignments are optimized to allow break-out of all pairs on a single critical layer.	

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Table 1. DDR4 design checklist (continued)

No.	Task	Completed
36	Ensure all clock pairs are properly trace matched to address/command/control signals within 20 mils.	
37	Ensure space from one differential pair to any other trace (this includes other differential pairs) should be at least 25 mils.	
38	If unbuffered DIMM modules are used, are all required clock pairs per DIMM slot connected? **NOTE:** Single ranked DIMM requires one clock pair; dual ranked DIMM requires two clock pairs.	
39	Check the skew between the clock and corresponding strobe for each byte lane. The clock and strobe trace lengths should be measured from the memory controller pin to the DDR4 DRAM chip pin. After obtaining the MCK to DQS skew for each byte lane, ensure max skew is less than 10 inches.	
40	Ensure the MAPAR_OUT and $\overline{\text{MAPAR\_ERR}}$ signals are properly connected: • MAPAR_OUT (from the controller) => PAR (at the DIMM/DRAM) • ALERT_n (from the DIMM/DRAM) => $\overline{\text{MAPAR\_ERR}}$ (at the controller)	
41	Ensure that a 50 Ω to 100 Ω pull up resistor to 1.2 V is present on MALERT / MAPAR_ERR pin. Discrete DRAM chips soldered on the board or RDIMM used 50 to 100 Ω pull up resistor is required. No board pull up is required for UDIMM/SoDIMM, because a 50 Ω termination already exist on the UDIMM/SoDIMM ALERT pin.	
MODT-/MDIC-related items		
42	Connect each of the MODT signals that are in the same group to the same physical memory bank: • MODT(0), $\overline{\text{MCS}}$(0), MCKE(0) • MODT(1), $\overline{\text{MCS}}$(1), MCKE(1) • MODT(2), $\overline{\text{MCS}}$(2), MCKE(2) • MODT(3), $\overline{\text{MCS}}$(3), MCKE(3)	
43	• Ensure that MDIC0 is connected to ground via an 162-Ω precision 1% resistor. • Ensure that MDIC1 is connected to DDR power via an 162-Ω precision 1% resistor. **NOTE:** For exact MDIC resistor value, see the device's data sheet.	
44	For QorIQ products that support more than one type of DDR type, for example DDR3L and DDR4, ensure the power-on reset configuration pin (cfg_dram_type) is properly set for the correct DDR type selection.	
Registered DIMM topologies **NOTE:** All previous tasks still apply.		
45	Ensure the DIMM reset pin has been considered and connected to the proper reset logic. Registered DIMM requires clock to be present when DRAM reset is released/ negated. This means the reset signal needs to be held low independent of the SoC reset signal, until the clock to RDIMM is present by configuring/enabling the corresponding chip selects in the memory controller registers. **NOTE:** The reset pin to the DRAM is 1.2 V LVCMOS. **NOTE:** LX2 devices have a dedicated DRAM reset pin which should be connected directly from controller to each DRAM reset pin with no additional logic or termination.	
46	Although registered DIMMs require only a single clock per bank, attach all DDR4 clock pairs at the DIMM connector (analogous to unbuffered DIMMs) so the design can also support unbuffered DIMMs with minimal changes.	

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Table 1. DDR4 design checklist (continued)

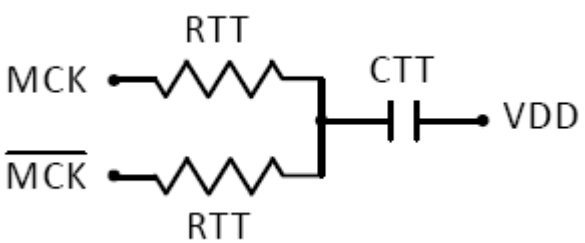
No.	Task	Completed
47	When using RDIMM, the CS, RAS, CAS, WE signals may need series termination to prevent an excessive overshoot.	
	Discrete memory topologies **NOTE:** All previous tasks still apply.	
48	Construct the signal routing topologies for the groups like those found on unbuffered DIMM modules (that is, proven JEDEC topologies). Ensure the address/command/control/clock signals are routed in fly-by topology.	
49	When placing components, optimize placement of the discrete DRAM chips to favor the data bus (analogous to DIMM topologies). Ensure the bit and byte swapping rules listed in item 27 of this table are implemented **NOTE:** Do not swap individual data bits across different nibbles within a byte lane.	
50	Ensure one clock pair is used for each chip-select. The clock pair should follow the address/command/control signal groups in fly-by topology.	
51	If multiple physical banks are needed, double stack (top and bottom) the banks to prevent lengthy and undesirable address/cmd topologies. **NOTE:** Consider implementing address bus mirroring when two-chip select is use.	
52	Properly decouple the DDR4 chips per manufacturer recommendations. Typically, five low ESL capacitors per device are sufficient. For further information (see *Decoupling Capacitor Calculation for a DDR Memory Channel* on Micron's website).	
53	To support expandability into larger devices, ensure that extra NC pins (future address pins) are connected.	
54	Ensure access/test points are available for signal integrity probing. This is especially critical if using blind and buried vias within the memory channel. If through-hole vias are used under the BGA devices, then generally these sites can be used for probing. **NOTE:** Consider adding access to MCK0 and MDQS0 signals for SI problem investigation.	
55	Ensure R_T, resistors on the address/command/control, and clock groups are located after the last DRAM chip in the fly-by topology.	
56	Ensure differential MCK/nMCK pair is terminated at the end of signal trace with two resistors equivalent to PCB characteristic impedance and center-tap-terminated to 0.1 uF cap and cap connects to DRAM V_{DD}. 	
57	Ensure the proper ZQ termination of 240 Ω ± 1% is provided to DRAM chips.	
58	Ensure the reset pin has been considered and connected to the proper reset logic. **NOTE:** The reset pin to the DRAM operates at DRAM V_{DD}.	

Table continues on the next page...

Table 1. DDR4 design checklist (continued)

No.	Task	Completed
	NOTE: LX2 devices have a dedicated DRAM reset pin which should be connected directly from controller to each DRAM reset pin with no additional logic or termination.	
59	Ensure the following pin connection for 8-stacked 3DS DDR4 DRAM: • $\overline{MCS}$(2) -> C(0) • $\overline{MCS}$(3) -> C(1) • MODT(1) -> C(2) For 2-stacked 3DS devices, only C(0) is needed. For 4-stacked 3DS devices, C(1:0) is needed. **NOTE:** When using 3DS devices, only two physical ranks of memory are supported ($\overline{MCS}$(0:1)).	
60	When 16-bit DRAM is used for ECC byte lane, ensure the eight unused DQ pins are pulled up. Strobes DQS,nDQS and DM inputs should be tied via resistor to their non-active power levels (GND or V_{DD}).	
61	TEN connectivity test is not supported. Ensure the DRAM TEN pin is pulled down.	
62	Ensure that ALERT_n signal is routed along with the address bus and is pulled up to V_{DD} after the last DRAM connection. **NOTE:** For devices that support DDR data rates higher than 2133 MT/s, ensure that ALERT_n signal is routed in opposite the direction of the fly-by topology used. For example, if C/A bus in fly-by topology is connecting from controller --> U0 --> U1 — U6 --> U7 --> termination. Then the ALERT signal will connect from controller --> U7 --> U6 — U1 --> U0 --> termination.	
63	If more than one chip-select/rank is implemented, ensure the same clock-to-strobe skews used for CS0 byte lanes are applied for other chip selects. For example: If the clock-to-strobe skew of byte lane 1 of CS0 is 2 inches, then clock-to-strobe skew of byte lane 1 of CS1/CS2/CS3 should also be 2 inches. If the clock-to-strobe skew of a byte lane cannot be the same among all chip-selects, then the maximum variation among all chip-selects/ranks must be less than 0.5 inches.	
64	In fly-by topology, for a given byte lane, the clock trace length must be at least as long as the strobe trace length. In the case that the clock trace length is shorter, the following limits must be observed: • The clock trace length can be a maximum of 2.0 inches shorter than the strobe trace length for a given byte lane.	
65	For LX2xxx products, when only one byte lane of x16 DRAM is used, it must connect to the lower byte lane. For example, if ECC byte lane is the only byte lane used on x16 DRAM then it must connect to the lower byte lane (i.e. DQ[0:7], LDQS_t, LDQS_c, LDMn).	

4 Selecting termination resistors

Sink and source currents flow through the parallel R_T resistors on the address and control groups. The worst case power dissipation for these resistors is as follows:

Power = I^2 x R_T = $(13\ mA)^2$ x $(47\ \Omega)$ = 7.9 mW.

Small resistors that provide dissipation of up to 1/16 W are ideal. Calculating V_{TT} current for assumptions made for current calculations.

5 Avoiding V_{REF} noise problems

V_{REF} is a reference voltage that provides a DC bias of 0.6 V (V_{DD}/2) for the differential receivers at the address/command/control bus of the DDR4 devices. Noise or deviation in the V_{REF} voltage can lead to potential timing errors, unwanted jitter, and erratic behavior on the memory bus.

To avoid these problems, V_{REF} noise must be kept within the JEDEC specification:

- V_{REF} and the V_{TT} cannot be on the same plane because of the DRAM V_{REF} buffer sensitivity to the termination plane noise.
- Both V_{REF} and V_{TT} must share a common source supply to ensure that both are derived from the same voltage plane.
- Adhere to the layout considerations in Table 1 (see V_{REF}) and ensure proper decoupling at each V_{REF} pin (at each DIMM/discrete and at the V_{REF} source).

Numerous off-the-shelf power IC solutions are available that provide both the V_{REF} and V_{TT} from a common source. Regardless of the generation technique, V_{REF} must track variations in V_{DDQ} over voltage, temperature, and noise margins as required by the JEDEC specifications.

6 Calculating V_{TT} current

For a given topology, the worst-case V_{TT} current must be calculated. Calculate sink and source currents using a typical R_T parallel termination resistor and the worst-case parameters listed in this table.

Table 2. Worst-case parameters for V_{TT} current calculation

Parameter	Values	Comment
V_{PP}(max)	2.5 V+ 0.25 V	From JEDEC spec
V_{DDQ}(max)	1.2 V + 0.06 V	From JEDEC spec
V_{TT}(max)	0.76 V	From JEDEC spec
V_{TT}(min)	0.6 V	From JEDEC spec
R_{DRVR}	20 Ω	Nominally, full strength is ~ 20 Ω
R_T	47 Ω	Can vary. Typically 25-47 Ω.
V_{OL}	0 V	Assumes driver reaches 0 V in the low state.

The driver sources (V_{TT} plane sink) the following based on this termination scheme:

$(V_{DD\_max} - V_{TT\_min})/(R_T + R_{DRVR}) = (1.26\ V - 0.594\ V)/(47 + 20) = 10\ mA$

The driver sinks (V_{TT} plane source) the following based on this termination scheme:

$(V_{TT\_max} - V_{OL} / (R_T + R_S + R_{DRVR}) = (0.76\ V - 0\ V)/(47+ 20) = 11.3\ mA$

A bus with a balanced number of high and low signals places no real demand on the V_{TT} supply. However, a bus with all DDR address/command/control signals low (~ 28 signals) causes a transient current demand of approximately 350 mA on the V_{TT} rail. The V_{TT} regulator must provide a relatively tight voltage regulation of the rail per the JEDEC specification. Besides a tight tolerance, the regulator must also allow V_{TT} along with V_{REF} (if driven from a common IC) to track variations in V_{DDQ} over voltage, temperature, and noise margins.

7 Layout guidelines for DDR signal groups

7.1 DDR data group background information

The data group is listed before the command, address, and control group because it operates at twice the clock speed, and its signal integrity is of higher concern. The data group also constitutes the largest portion of the memory bus and comprises most of the trace matching requirements (those of the data lanes).

7.2 Routing DDR memory channel

To help ensure the DDR interface is properly optimized, NXP recommends routing the DDR memory channel in this specific order:

1. Data
2. Address/command/control
3. Clocks

NOTE

The address/command, control, and data groups all have a relationship to the routed clock. Therefore, the effective clock lengths used in the system must satisfy multiple relationships. It is recommended that the designer perform simulation and construct system timing budgets to ensure that these relationships are properly satisfied.

7.3 Routing DDR data signals

The DDR interface data signals (MDQ[0:63], MDQS[0:8], MDM[0:8], and MECC[0:7]) are source-synchronous signals by which memory and the controller capture the data using the data strobe rather than the clock itself. When transferring data, both edges of the strobe are used to achieve the 2x data rate.

An associated data strobe (DQS and $\overline{\text{DQS}}$) and data mask (DM) comprise each data byte lane. This 11-bit signal lane relationship is crucial for routing (see Table 3). When length matching, the critical item is the variance of the signal lengths within a given byte lane to its strobe. Length matching across all bytes lanes is also important and must meet the t_{DQSS} parameter as specified by JEDEC. This is also commonly referred to as the write data delay window. Typically, this timing is considerably more relaxed than the timing of the individual byte lanes themselves.

Table 3. Byte lane to data strobe and data mask mapping

Data	Data strobe	Data mask	x4 mode data strobe	Lane number
MDQ[0:7]	MDQS0, $\overline{\text{MDQS0}}$	MDM0	MDQS9, $\overline{\text{MDQS9}}$	Lane 0
MDQ[8:15]	MDQS1, $\overline{\text{MDQS1}}$	MDM1	MDQS10, $\overline{\text{MDQS10}}$	Lane 1
MDQ[16:23]	MDQS2, $\overline{\text{MDQS2}}$	MDM2	MDQS11, $\overline{\text{MDQS11}}$	Lane 2
MDQ[24:31]	MDQS3, $\overline{\text{MDQS3}}$	MDM3	MDQS12, $\overline{\text{MDQS12}}$	Lane 3
MDQ[32:39]	MDQS4, $\overline{\text{MDQS4}}$	MDM4	MDQS13, $\overline{\text{MDQS13}}$	Lane 4

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Table 3. Byte lane to data strobe and data mask mapping (continued)

Data	Data strobe	Data mask	x4 mode data strobe	Lane number
MDQ[40:47]	MDQS5, $\overline{\text{MDQS5}}$	MDM5	MDQS4, $\overline{\text{MDQS14}}$	Lane 5
MDQ[48:55]	MDQS6, $\overline{\text{MDQS6}}$	MDM6	MDQS5, $\overline{\text{MDQS15}}$	Lane 6
MDQ[56:63]	MDQS7, $\overline{\text{MDQS7}}$	MDM7	MDQS6, $\overline{\text{MDQS16}}$	Lane 7
MECC[0:7]	MDQS8, $\overline{\text{MDQS8}}$	MDM8	MDQS7, $\overline{\text{MDQS17}}$	Lane 8

NOTE

When routing, each row (that is, the 11-bit signal group) must be treated as a trace-matched group.

When x4 DRAM mode is available and used, the data mask signals are not available. Instead the strobe signals listed under the x4 Mode Data Strobe column are the strobes for the second nibble of each byte lane.

7.4 DDR signal groups layout recommendations

This table lists the layout recommendations for DDR signal groups and the benefit of following each recommendation.

Table 4. DDR signal groups layout recommendations

Recommendation	Benefit
Route each data lane adjacent to a solid ground reference for the entire route to provide the lowest inductance for the return currents.	Provides the optimal signal integrity of the data interface **NOTE:** This concern is especially critical in designs that target the top-end interface speed, because the data switches at 2x the applied clock.
When the byte lanes are routed, route signals within a byte lane on the same critical layer as they traverse the PCB motherboard to the memories.	Helps minimize the number of vias per trace and provides uniform signal characteristics for each signal within the data group.
Alternate the byte lanes on different critical layers (see Figure 1 and Figure 2).	Facilitates ease of break-out from the controller perspective and keeps the signals within the byte group together.

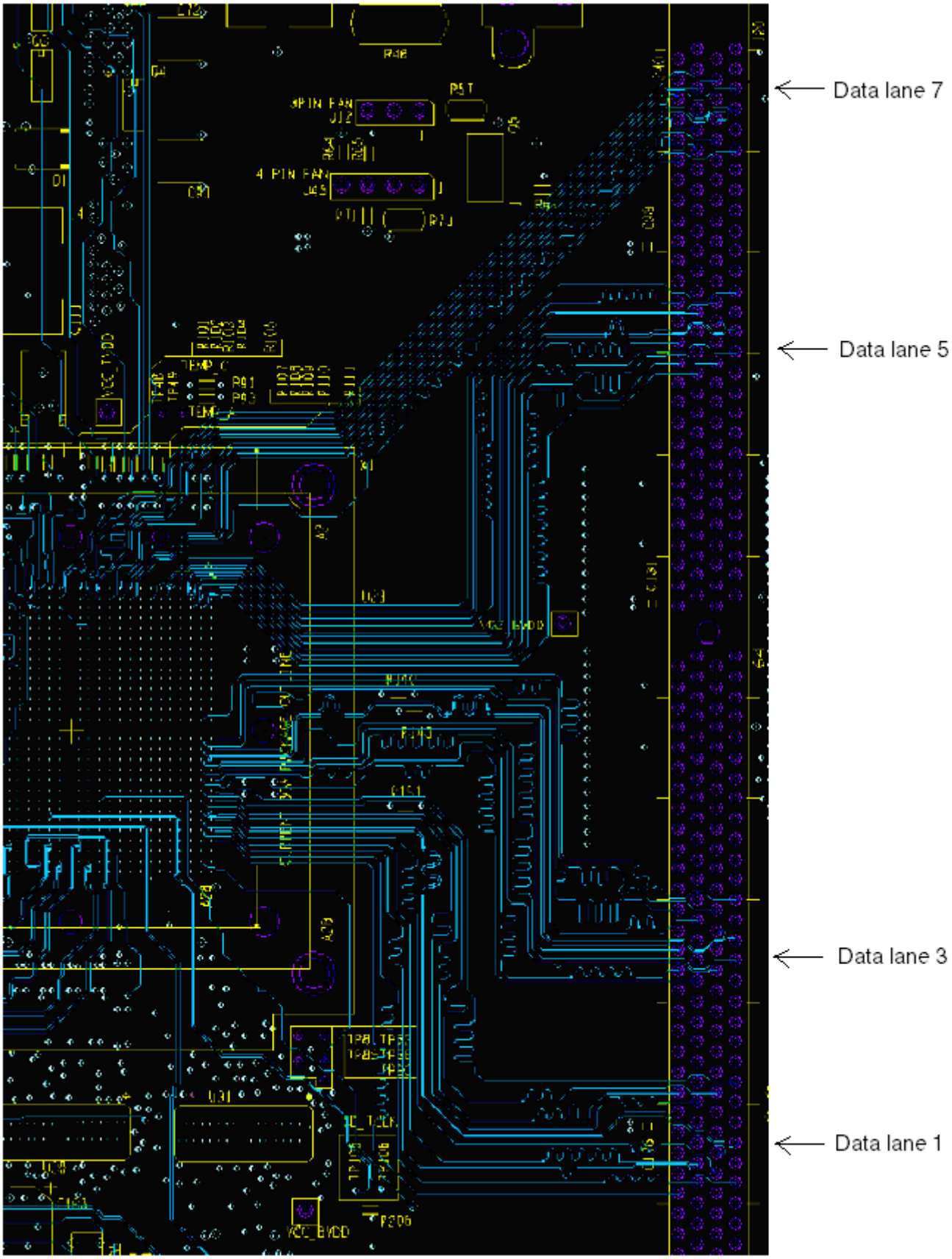

Figure 1. Alternating data byte lanes on different critical layers—Part 1

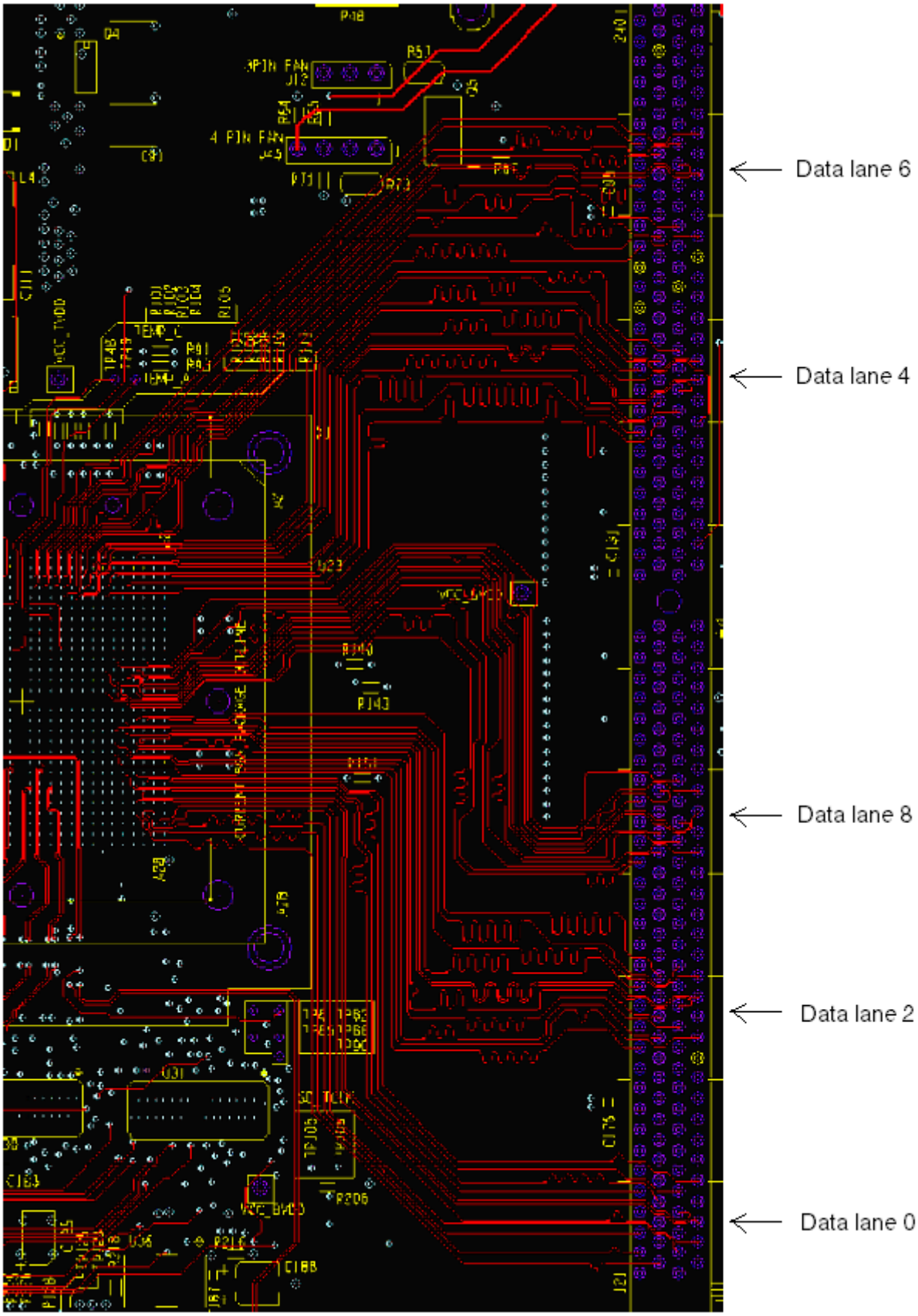

Figure 2. Alternating data byte lanes on different critical layers Part2

8 Using simulation models

NXP provides IBIS models for simulation in tandem with memory vendors. The board designer can realize a key advantage in the form of extra noise margins and extra timing margins by taking the following actions:

- Optimize the clock-to-signal group relationships to maximize setup and hold times.
- Optimize termination values. During board simulation, verify that all aspects of the signal eye (see Figure 3) are satisfied, which includes the following (at a minimum):
  - Sufficient signal eye opening meeting both timing and AC input voltage levels
  - Vswing max not exceeded (or alternatively, max overshoot/max undershoot)
  - Signal slew rate within specifications

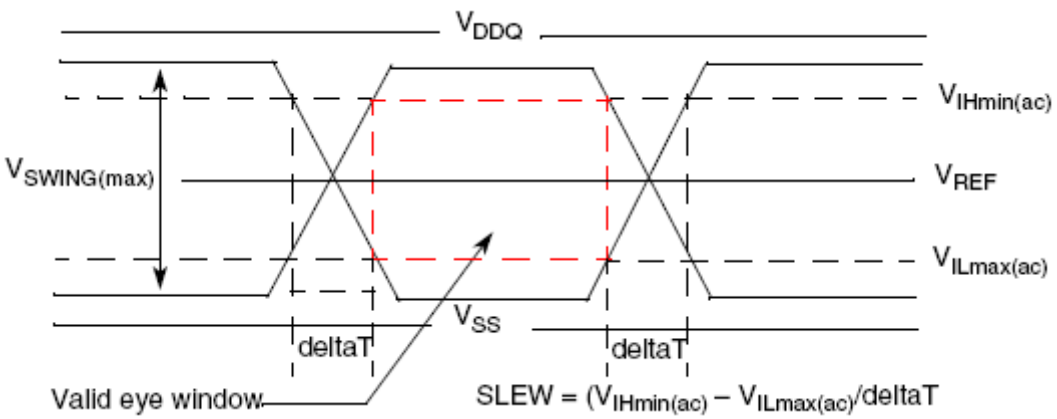

Figure 3. SSTL signal waveform eye diagram

8.1 Important read timing budget simulation considerations

Consider the following:

- Do not perform slew-rate derating for the NXP DDR4 controllers on reads.
- Timing budgets for reads can be done with customer's simulation tool by adding the setup and hold margins rather than looking at the setup or hold margins by themselves (to account for the DQS-DQ calibration).
- Read timing should be taken at Vref rather than Vin levels (that is, read timing measurements for DQ shall be taken at Vref. No read timing measurements are taken at Vih(ac), Vil(ac), Vih(dc), or Vil(dc)).

8.2 Simulation results for QorIQ memory controller receiver during a read cycle

This figure shows the simulation results.

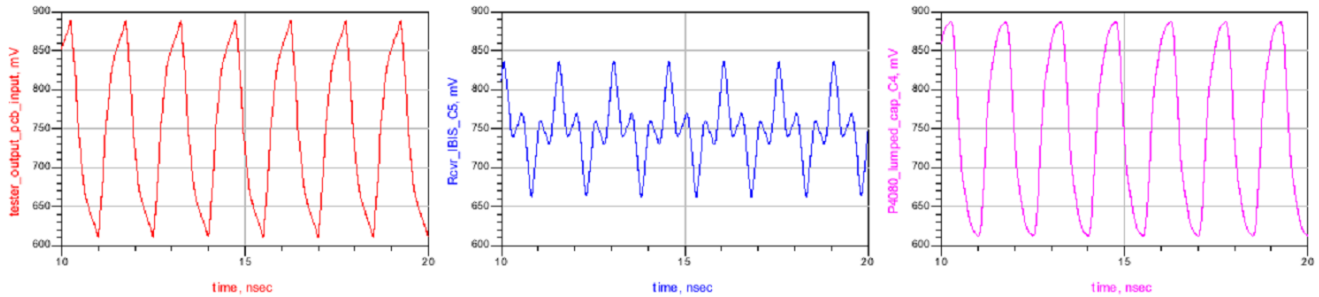

Figure 4. QorIQ memory controller receiver simulation results

From left to right:

- Sent strobe (DQS) signal by DRAM during a read cycle
- Same DQS signal observed at the QorIQ memory controller pin
- Same DQS signal observed at the QorIQ memory controller die

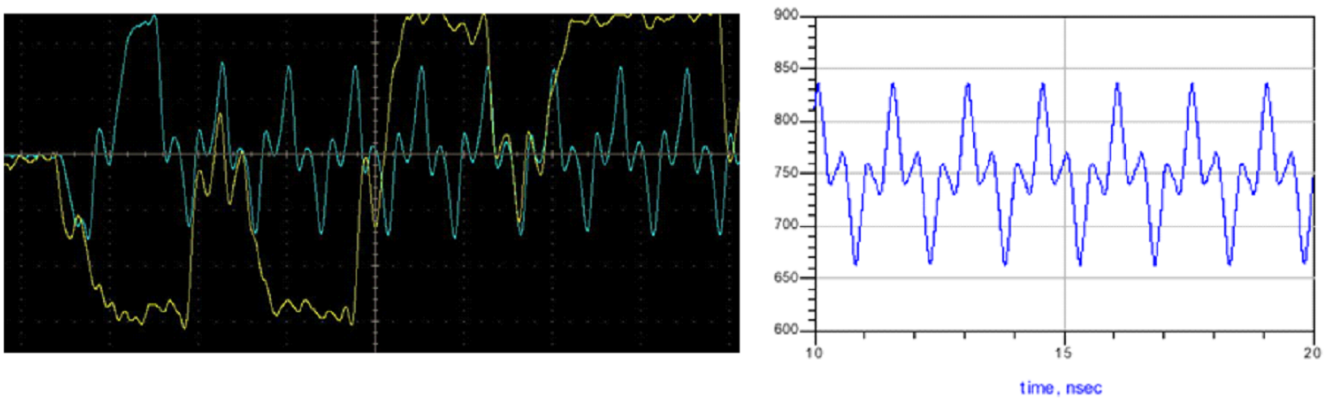

Figure 5. Measurement vs. simulation

From left to right:

- Measured DQS (blue signal in scope shot) at QorIQ memory controller pin during a read cycle with ODT off
- Simulated DQS at QorIQ memory controller pin during a read cycle with ODT off

9 Revision history

This table provides a revision history for this application note.

Table 5. Document revision history

Rev. number	Date	Description
2	07/2019	• In Table 1 :

Table continues on the next page...

Table 5. Document revision history (continued)

Rev. number	Date	Description
		• Added tasks #47 and #65 • Updated tasks #1, #25, #27, #30, #31, #32, #36, #41, #45, #58, #59, and #62 • Added a note in DRAM reset signal considerations
1	07/2016	Rebranded to NXP. Added Appendix A: LS1088A DDR layout routing break out and Appendix B: DRAM reset signal considerations.
0	04/2015	Initial public release

Appendix A LS1088A DDR layout routing break out

The goal of this appendix is to provide an example break out for signal, power, and ground layers and split planes. It is important to note that this is not the only way or the recommended way for the DDR layout. This is simply a break out example.

A.1 32-bit + ECC discrete DRAM break out

This section provides figures that show the 32-bit + ECC discrete DRAM break out.

In the following figure, white lines represent add/control and yellow lines represent data lane 0.

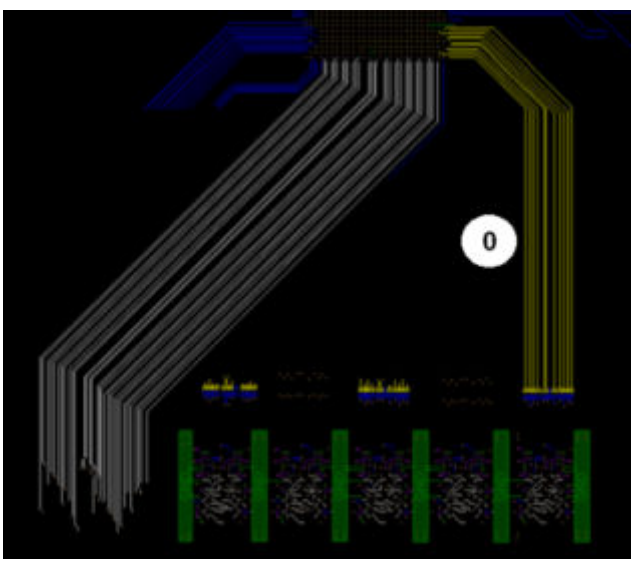

Figure A-1. Top layer 1 with discrete memory

In the following figure, purple areas represent $G2V_{DD}$ and green areas represent GND.

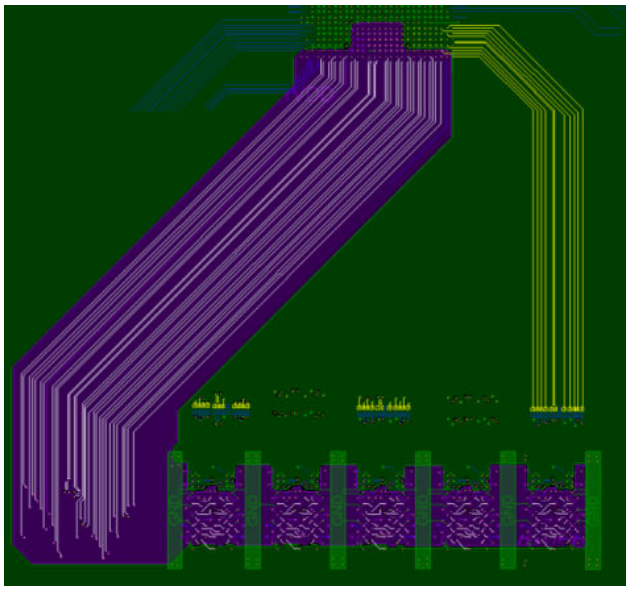

Figure A-2. GND layer 2 with discrete memory

In the following figure, white lines represent add/control and gray lines represent data lines.

Figure A-3. Signal layer 3 with discrete memory

In the following figure, white lines represent add/control; yellow lines represent data lanes 1 and 3; purple lines represent data byte lanes not used in the 32-bit data bus.

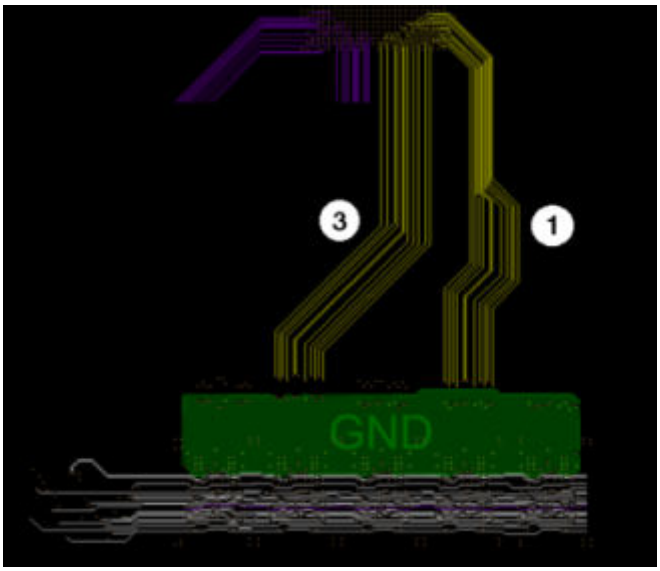

Figure A-4. Signal layer 4 with discrete memory

In the following figure, purple areas represent $G1V_{DD}$.

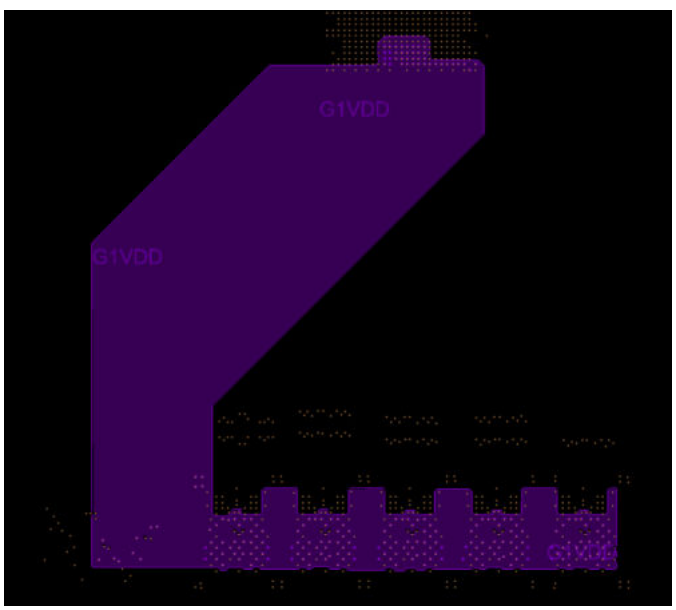

Figure A-5. PWR layer 5 with discrete memory

In the following figure, white lines represent add/control; yellow lines represent data lane 2 and ECC; red lines represent data byte lanes not used in the 32-bit data bus.

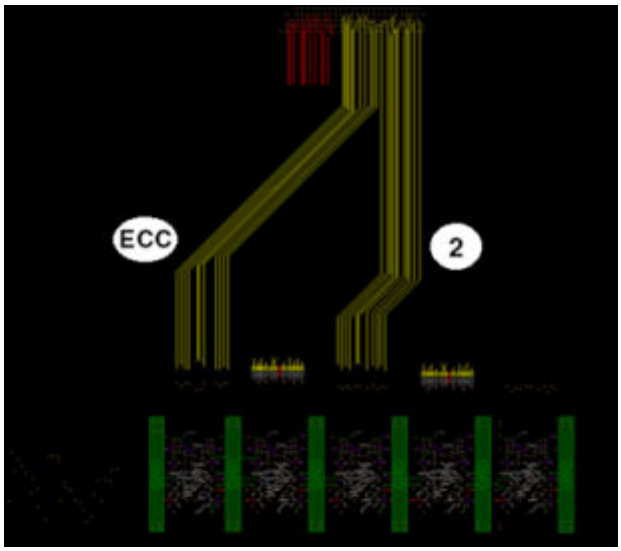

Figure A-6. Bottom layer 6 with discrete memory

A.2 64-bit + ECC UDIMM break out

This section provides figures that show the 64-bit + ECC UDIMM break out.

In the following figure, white lines represent add/control and yellow lines represent data lanes 0 and 7.

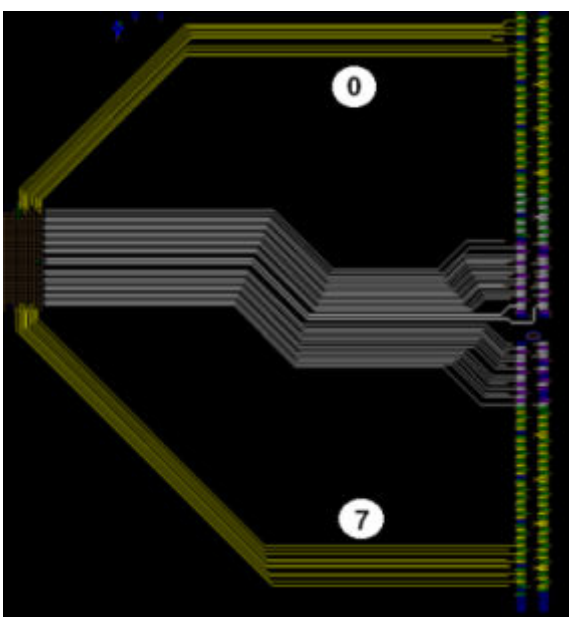

Figure A-7. Top layer 1 with UDIMM memory

In the following figure, purple areas represent $G2V_{DD}$ and green areas represent GND.

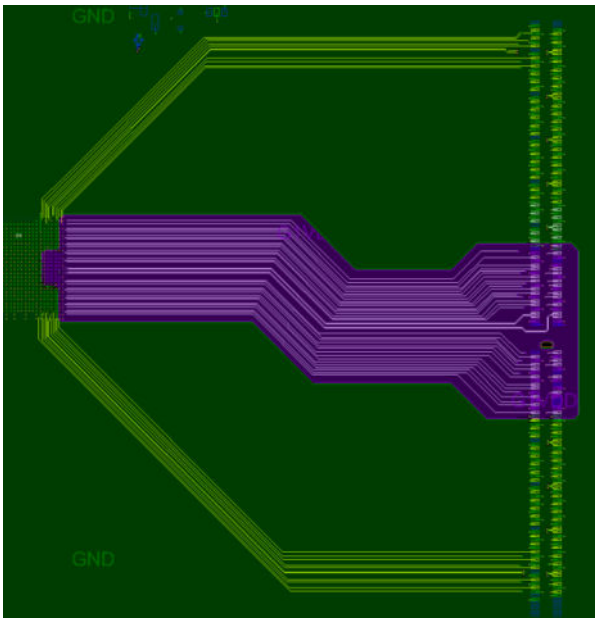

Figure A-8. GND layer 2 with UDIMM memory

There is no address/control and data routing on layer 3, as shown in the following figure.

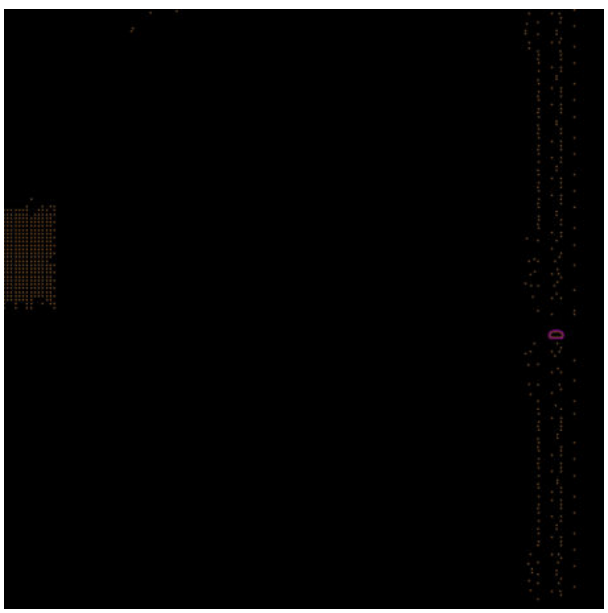

Figure A-9. Signal layer 3 with UDIMM memory

In the following figure, white lines represent add/control and yellow lines represent data lanes 1, 3, 4, and 6.

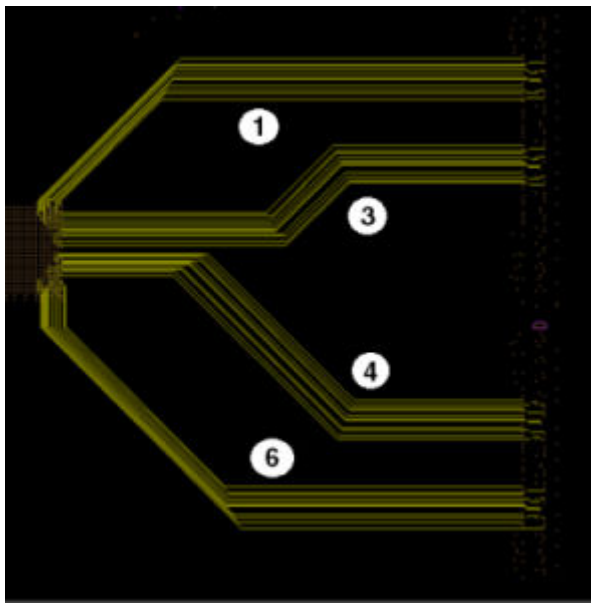

Figure A-10. Signal layer 4 with UDIMM memory

In the following figure, purple areas represent $G1V_{DD}$ and green areas represent GND.

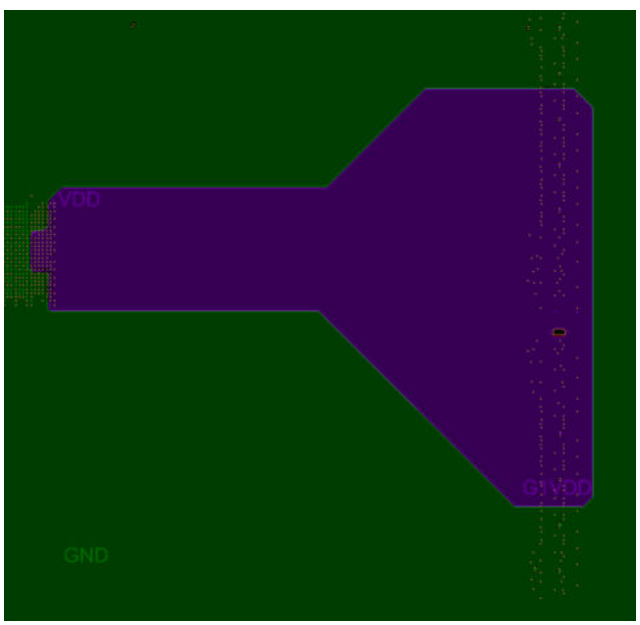

Figure A-11. PWR layer 5 with UDIMM memory

In the following figure, yellow lines represent data lanes 2 5 and ECC.

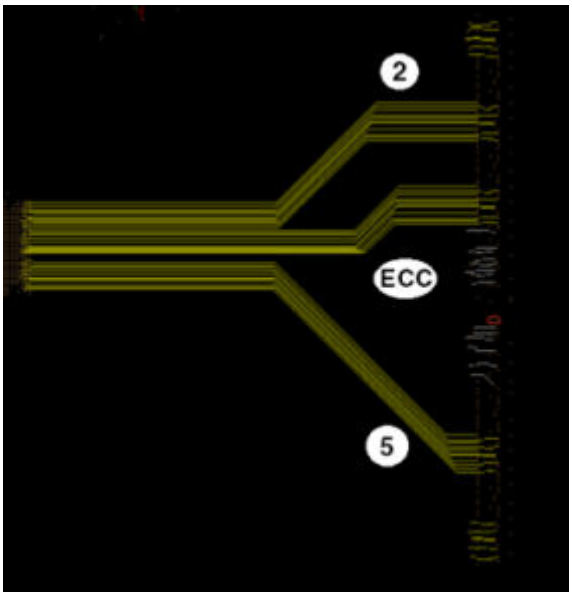

Figure A-12. Bottom layer 6 with UDIMM memory

Appendix B DRAM reset signal considerations

Every DDR3/3L/4 DRAM chip has a reset pin. JEDEC defines the requirements for the DRAM reset signal. The DDR interface in QorIQ products does not have a DRAM reset pin. This means the DRAM reset signal must be controlled by logic in the board.

There are two main cases of the DRAM reset requirements. Case #1 is for unbuffered DIMM (UDIMM, SoDIMM) or discrete DRAM. Case #2 is for Registered DIMM (RDIMM). The following sections describe the DRAM reset signal requirements for each case.

NOTE

LX2 devices have a dedicated DRAM reset pin which should be connected directly from controller to each DRAM reset pin. All the required timing for DRAM reset signal is managed by the LX2 memory controller for any UDIMM/RDIMM/ or discrete DRAM. No additional board logic or termination is required for the DRAM reset signal.

B.1 Case #1

JEDEC specifications for DDR3/3L/4 UDIMM or discrete DRAM require:

1. DRAM reset signal is asserted for a minimum of 200 µs.
2. CKE signal is in logic level low for a minimum of 10 ns before the DRAM reset signal is de-asserted.
3. CKE signal remains low for a minimum of 500 µs after the DRAM reset signal is de-asserted.

This figure illustrates these signal timing requirements.

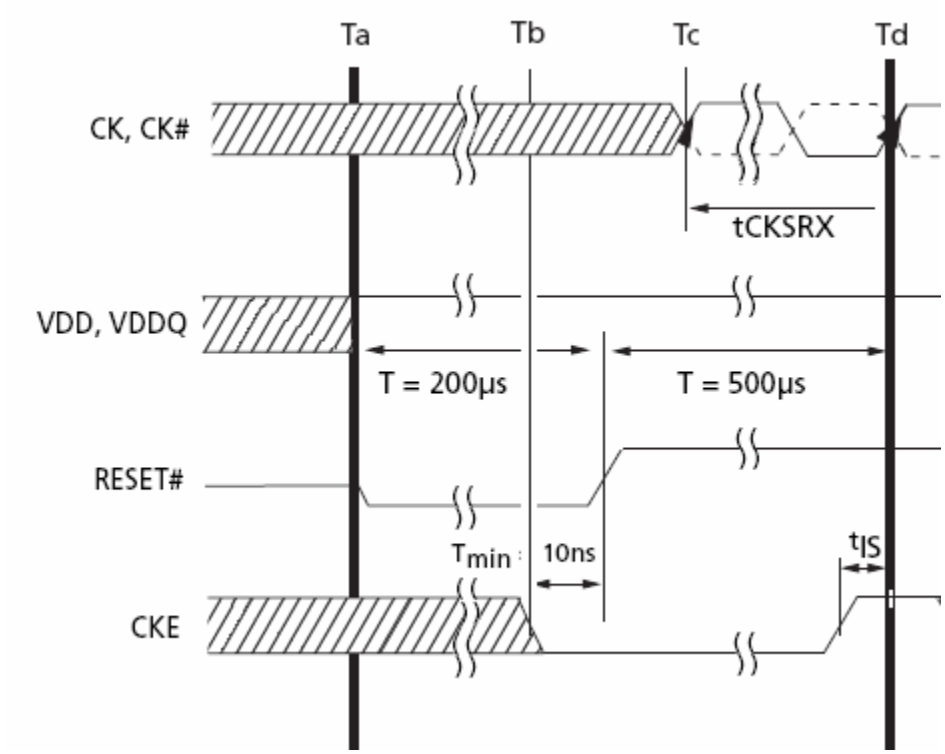

Figure B-1. Signal timing requirements for UDIMM or discrete DRAM

These conditions can be met in QorIQ products (except LS1012A and LS1024A) by simply asserting and de-asserting the DRAM signal with HRESET signal.

B.2 Case #2

JEDEC specifications for DDR3/3L/4 RDIMM require:

- DRAM reset signal is asserted for a minimum of 200 µs.
- Clock must be present before the DRAM reset signal is de-asserted.
- CKE signal is in logic level low for a minimum of 16 clock cycles before the DRAM reset signal is de-asserted.
- CKE signal remains low for a minimum of 500 µs after the DRAM reset signal is de-asserted.

This figure illustrates these signal timing requirements.

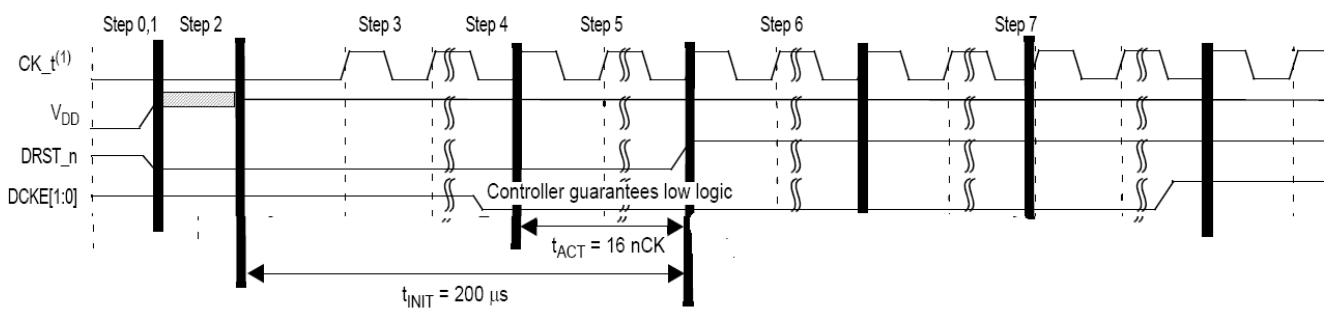

Figure B-2. Signal timing requirements for RDIMM or discrete DRAM

Implementation of these DRAM reset requirements for RDIMM can be achieved via some combination of software and hardware. Below is an example of implementing the DRAM reset requirements for RDIMM. It is important to note that this is not the only way to implement the required DRAM reset timing or the recommended way. This is simply an example.

In QorIQ products (except LS1012A and LS1024A):

- The CKE signal remains low until the memory controller is enabled (DDR_SDRAM_CFG[MEM_EN] = 1).
- Before the memory controller is enabled, all DDR registers must be configured.
- The DDR clock starts running when any chip select is enabled (CSn_CONFIG[CSn_EN] = 1).

Assert the DRAM reset signal at the same time the HRESET signal is asserted. De-asserting the DRAM rest signal needs to be timed to occur after clocks are present while the CKE signal is low. In other words, the DRAM reset signal must be de-asserted after software enables any chip select (CSn_CONFIG[CSn_EN] = 1) and before software enables the memory controller (DDR_SDRAM_CFG[MEM_EN] = 1). Apply a large enough delay between chip select enable and memory controller enable. Then observe the HRESET, DRAM reset, MCK*n*, and CKE*n* signals on an oscilloscope, and time the de-assertion of the DRAM reset to fall after MCK*n* is present and before the CKE*n* signal goes to logic high level.

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