Description

The 6V49205B is a main clock for Freescale P10xx and P20xx-based systems. It has a selectable System CCB clock and 2 DDRCLK speeds – 100M or 66.66M. The 6V49205B also provides LP-HCSL PCIe outputs for low-power and reduced board space.

Output Features

- 1 – Sys_CCB 3.3V LVCMOS output at 100M/83.33M/80M/66.66M
- 1 – DDRCLK 3.3V LVCMOS output at 100M or 66.66M [1]
- 1 – 125M 3.3V LVCMOS output
- 6 – LP-HCSL PCIe pairs selectable at 100M or 125M
- 6 – 25MHz 3.3V LVCMOS outputs
- 2 – 2.048M 3.3V LVCMOS outputs
- 2 – USB 3.3V LVCMOS outputs at 12M or 24M

Key Specifications

- PCIe Gen1-2-3 compliant
- < 3p rms phase noise on REF outputs

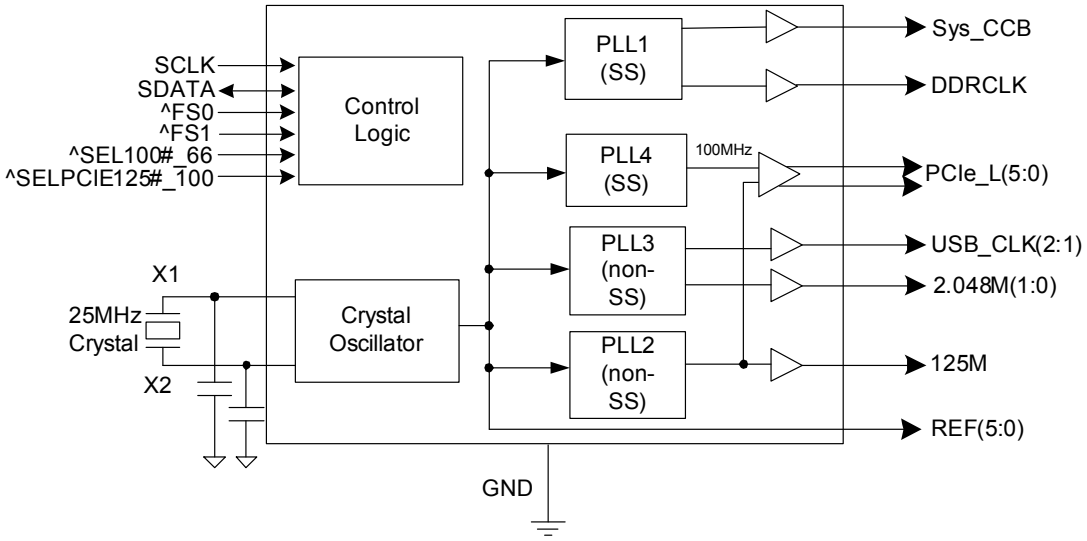
Typical Applications

System Clock for Freescale P10xx and P20xx-based designs

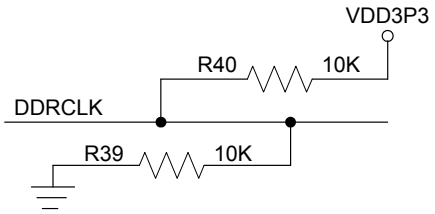
Features

- Replaces 11 crystals, 2 oscillators and 3 clock generators; lowers cost, power and area
- Integrated terminations on LP-HCSL PCIe outputs; eliminate 24 resistors, saving 41mm^2 of board area
- Industrial temperature range operation; supports demanding environmental conditions
- Advanced 3.3V CMOS process; high-performance, low-power
- Supports independent spread spectrum on Sys_CCB/DDRCLK and PCIe outputs
- Available in space-saving 7 x 7 mm 48-VFQFPN with 0.5mm pad pitch; reduced board space without the need for fine-pitch assembly techniques

Block Diagram



Note 1: For DDR Clock: Processor core and I/O supply rails must be ramped with VDD3P3 or earlier. Clock signal will be clamped LOW and output clock will be 100MHz if this is not followed (see diagram below).



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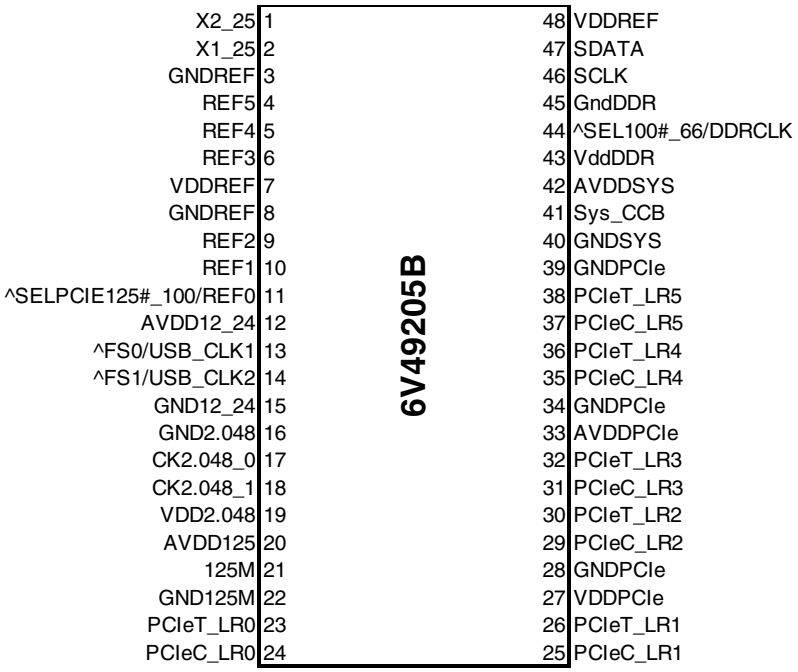
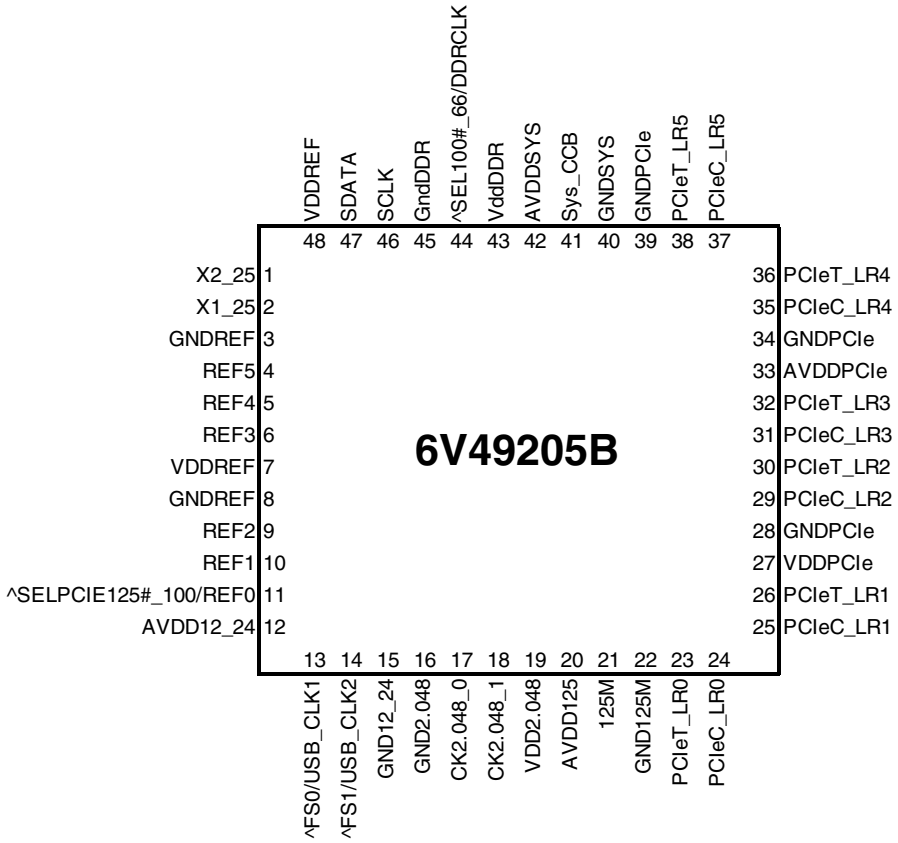
Pin Assignments



48-Pin TSSOP

^ Indicates Internal 100kohm pull up resistor



48-Pin VFQFPN

^ Indicates Internal 100kohm pull up resistor

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Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	X2_25	OUT	Crystal output, Nominally 25.00MHz.
2	X1_25	IN	Crystal input, Nominally 25.00MHz.
3	GNDREF	PWR	Ground pin for the REF outputs.
4	REF5	OUT	Copy of crystal input
5	REF4	OUT	Copy of crystal input
6	REF3	OUT	Copy of crystal input
7	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
8	GNDREF	PWR	Ground pin for the REF outputs.
9	REF2	OUT	Copy of crystal input
10	REF1	OUT	Copy of crystal input
11	^SELPCIE125#_100/REF0	I/O	Latched input to select the PCIe output frequency/REF0 output. 0 = 125M 1 = 100M
12	AVDD12_24	PWR	Power for 12_24MHz PLL core, and outputs. Nominal 3.3V
13	^FS0/USB_CLK1	I/O	Frequency select latch for Sys_CCB / 12 or 24MHz USB clock output. 3.3V. This pin has an internal pull up resistor.
14	^FS1/USB_CLK2	I/O	Frequency select latch for Sys_CCB / 12 or 24MHz USB clock output. 3.3V. This pin has an internal pull up resistor.
15	GND12_24	PWR	Ground pin for 12_24M outputs.
16	GND2.048	PWR	Ground pin for 2.048M outputs.
17	CK2.048_0	OUT	2.048M output, nominal 3.3V.
18	CK2.048_1	OUT	2.048M output, nominal 3.3V.
19	VDD2.048	PWR	Power supply for 2.048M outputs, nominal 3.3V.
20	AVDD125	PWR	Power for 125MHz PLL core and output, nominal 3.3V
21	125M	OUT	125M output, nominal 3.3V.
22	GND125M	PWR	Ground pin for 125M outputs.
23	PCIeT_LR0	OUT	True clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor
24	PCIeC_LR0	OUT	Complement clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor
25	PCIeC_LR1	OUT	Complement clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor
26	PCIeT_LR1	OUT	True clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor
27	VDDPCIe	PWR	Power supply for PCI Express outputs, nominal 3.3V
28	GNDPCIe	PWR	Ground pin for the PCIe outputs.
29	PCIeC_LR2	OUT	Complement clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor
30	PCIeT_LR2	OUT	True clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor
31	PCIeC_LR3	OUT	Complement clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor
32	PCIeT_LR3	OUT	True clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor
33	AVDDPCIe	PWR	Analog Power supply for PCI Express clocks, nominal 3.3V
34	GNDPCIe	PWR	Ground pin for the PCIe outputs.
35	PCIeC_LR4	OUT	Complement clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor
36	PCIeT_LR4	OUT	True clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor
37	PCIeC_LR5	OUT	Complement clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor
38	PCIeT_LR5	OUT	True clock of 0.8V differential push-pull PCI_Express pair with integrated 33ohm series resistor
39	GNDPCIe	PWR	Ground pin for the PCIe outputs.
40	GNDSYS	PWR	Ground pin for the Sys_CCB output
41	Sys_CCB	OUT	System CCB clock output
42	AVDDSYS	PWR	Analog Power supply for Sys_CCB clock and outputs, nominal 3.3V
43	VddDDR	PWR	Power supply for DDR Clock output, nominal 3.3V
44	^SEL100#_66/DDRCLK	I/O	Latched input to select the DDR output frequency/DDRCLK output. See note regarding system power sequencing. 0 = 100M 1 = 66.666M
45	GndDDR	PWR	Ground pin for the DDR outputs.
46	SCLK	IN	Clock pin of SMBus circuitry.
47	SDATA	I/O	Data pin for SMbus circuitry.
48	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V

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Table 1: PCIEX Spread Table (selectable via SMBUS)

SELPCIE125#_100 B6b4	B0b4	B0b3	Spread %
0 (125MHz)	x	x	No Spread
1 (100MHz)	0	0	No Spread (default)
1 (100MHz)	0	1	Down -0.5%
1 (100MHz)	1	0	Down -0.75%
1 (100MHz)	1	1	No Spread

*Once in spread mode, do not return to non spread without reset

Table 2: Sys_CCB and DDR Spread Table (selectable via SMBUS)

B0b7	B0b6	B0b5	Spread %
0	0	0	No Spread (default)
0	0	1	Down -0.5%
0	1	0	Down -0.75%
0	1	1	Down -0.25%
1	0	0	Down -1%
1	0	1	Down -1.25%
1	1	0	Down -1.5%
1	1	1	Down -2%

Table 3: Sys_CCB Frequency Select Table (Latched and selectable via SMBUS)

FS1 / B4b3	FS0 / B4b2	Sys_CCB (MHz)
0	0	66.66
0	1	100
1	0	80
1	1	83.33

Table 4: PCI Express Amplitude Control

B6b7	B6b6	PCIe Amplitude
0	0	700mV
0	1	800mV
1	0	900mV
1	1	1000mV

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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 6V49205B. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Maximum Supply Voltage	VDDxxx	Supply Voltage			4.6	V	1
Maximum Input Voltage	V_{IH}	Referenced to GND			VDD + 0.5	V	1
Minimum Input Voltage	V_{IL}	Referenced to GND	GND - 0.5			V	1
Storage Temperature	Ts	-	-65		150	°C	
Junction Temperature	Tj	-			125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

NOTES on Absolute Max Parameters

[1] Operation under these conditions is neither implied, nor guaranteed.

Electrical Characteristics - Input/Supply/Common Output DC Parameters

T_{AMB} = -40 to +85°C; V_{DD} = 3.3 V +/-5%, All outputs driving test loads (unless noted otherwise).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Ambient Operating Temp	T_{AMB}	-	-40	25	85	°C	
Supply Voltage	VDDxxx	Supply Voltage	3.135	3.3	3.465	V	
Power supply Ramp Time	T_{PWRRMP}	Power supply ramp must be monotonic			4	ms	
Latched Input High Voltage	V_{IH_LI}	Single-ended Latched Inputs	2.1		V_{DD} + 0.3	V	
Latched Input Low Voltage	V_{IL_LI}	Single-ended Latched Inputs	V_{SS} - 0.3		0.8	V	
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	uA	2
Operating Supply Current	$I_{DDOP3.3}$	All outputs loaded and running		119	155	mA	
Input Frequency	F_i		23	25	27	MHz	3
Pin Inductance	L_{pin}			5	7	nH	
Input Capacitance	C_{IN}	Logic Inputs	1.5	3	5	pF	
	C_{OUT}	Output pin capacitance		5	6	pF	
	C_{INX}	X1 & X2 pins		5	6	pF	
Clk Stabilization	T_{STAB}	From VDD Power-Up or de-assertion of PD to 1st clock		3.2	5	ms	
Tfall_SE	T_{FALL}	Fall/rise time of all 3.3V control inputs from 20-80%			10	ns	1
Trise_SE	T_{RISE}				10	ns	1
SMBus Voltage	V_{DD}		2.7		3.3	V	
Low-level Output Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	
Current sinking at V_{OLSMB} = 0.4 V	I_{PULLUP}	SMB Data Pin	4			mA	
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	
SMBus Operating Frequency	F_{SMBUS}				400	kHz	

NOTES on DC Parameters: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

[1] Signal is required to be monotonic in this region.

[2] Input leakage current does not include inputs with pull-up or pull-down resistors.

[3] For margining purposes only. Normal operation should have Fin =25MHz.

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AC Electrical Characteristics - Low Power HCSL-Compatible PCIe Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f	Spread off		100.00		MHz	2,3
				125.00		MHz	2,3
Synthesis error	ppm_{SSoff}	PCIe 100MHz or 125MHz		0		ppm	1,2
	ppm_{SSon}	PCIe @ -0.5% spread, 100MHz only		+/-100		ppm	1,2
Rising/Falling Edge Slew Rate	t_{SLEW}	Differential Measurement	2.2	4.1	5.7	V/ns	1,3,6
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement		1	20	%	1,6
Maximum Output Voltage	V_{HIGH}	Includes overshoot		793	1150	mV	6,7
Minimum Output Voltage	V_{LOW}	Includes undershoot	-300	-22		mV	6,7
Differential Voltage Swing	V_{SWING}	Differential Measurement	300			mV	1,6
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	300	419	550	mV	1,4,6
Crossing Point Variation	$V_{XABSVAR}$	Single-ended Measurement		115	140	mV	1,4,5
Duty Cycle	D_{CYC}	Differential Measurement	45	50.1	55	%	1
PCIe Jitter - Cycle to Cycle	$PCIe_{JC2C}$	Differential Measurement		36	125	ps	1
PCIe[5:0] Skew	$T_{SKEwPCIe50}$	Differential Measurement		1172	1500	ps	1,6,8
Spread Spectrum Modulation Frequency	f_{SSMOD}	Triangular Modulation	30	31.5	33	kHz	

Notes for PCIe Clocks:

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Clock Frequency specifications are guaranteed assuming that REF is at 25MHz.

[3] Slew rate measured through V_swing voltage range centered about differential zero.

[4] Vcross is defined at the voltage where Clock = Clock#.

[5] Only applies to the differential rising edge (Clock rising, Clock# falling.)

[6] At default SMBus settings.

[7] The Freescale P-series CPU's have internal terminations on their SerDes Reference Clock inputs. The resulting amplitude at these inputs will be 1/2 of the values listed, which are well within the 800mV Freescale specification for these inputs.

[8] This value includes an intentional output-to-output skew of approximately 250ps.

Electrical Characteristics - Phase Jitter, PCIe Outputs at 100MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY SPEC LIMIT	UNITS	NOTES
Jitter, Phase	$t_{jphPCIe1}$	PCIe Gen 1 phase jitter		35	56	86	ps	1,2,3
	$t_{jphPCIe2Lo}$	PCIe Gen 2 phase jitter Lo-band content		1.6	2.4	3	ps (RMS)	1,2,3
	$t_{jphPCIe2Hi}$	PCIe Gen 2 phase jitter Hi-band content		1.9	2.8	3.1	ps (RMS)	1,2,3
	$t_{jphPCIe3}$	PCIe Gen 3 phase jitter		0.5	0.83	1	ps (RMS)	1,2,3

Notes on Phase Jitter:

[1] See http://www.pcisig.com for complete specs. Guaranteed by design and characterization, not tested in production.

[2] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1^{-12}.

[3] Applies to PCIe outputs @ default amplitude and 100MHz with spread off or at -0.5%.

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Electrical Characteristics - DDR Clock

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
DDR Clock Frequency	$f_{DDR66.66}$	SEL100#_66 = 1, V_T = OVDD/2 V		66.666		MHz	2,3,6
	f_{DDR100}	SEL100#_66 = 0, V_T = OVDD/2 V		100.00		MHz	2,3,6
Synthesis error	ppm_{SSoff}	Spread off		0		ppm	1,2,5
	ppm_{SSon}	Spread on		+/-150		ppm	1,2,5
Output High Voltage	V_{OH}	V_{OH} at the selected operating frequency	2.4			V	1
Output Low Voltage	V_{OL}	V_{OL} at the selected operating frequency			0.4	V	1
Slew Rate VDDO = 3.3V	t_{SLEW00}	'00' = Hi-Z		Hi-Z		V/ns	
	t_{SLEW01}	'01' Slow Slew Rate (Averaging on)	1.1	1.6	2.3	V/ns	1,3,8
	t_{SLEW10}	'10' Fast Slew Rate (Averaging on)	1.6	2.3	3.2	V/ns	1,3,8
	t_{SLEW11}	'11' Fastest Slew Rate (Averaging on)	1.8	2.7	3.7	V/ns	1,3,8
Duty Cycle	d_{t1}	V_T = OVDD/2 V	40	51.4	60	%	1,6
Jitter, Peak period jitter	t_{jpeak}	V_T = OVDD/2 V		±96	±150	ps	1,6
Phase Noise	$t_{phasenoise}$	-56dBc		10	500	kHz	1,7
AC Input Swing Limits @ 3.3V OV_{DD}	$_{T}V_{AC}$	This is the difference between VOL and VOH at the selected operating frequency.	1.9	3.4		V	1
Spread Spectrum Modulation Frequency	f_{SSMOD}	Triangular Modulation	30	32.3	60	kHz	

Electrical Characteristics - Sys_CCB

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f_{Sys_CCB}	FS(1:0) = 00, VT = OVDD/2 V		66.666		MHz	2,3,6
		FS(1:0) = 01, VT = OVDD/2 V		100.00		MHz	2,3,6
		FS(1:0) = 10, VT = OVDD/2 V		80.00		MHz	2,3,6
		FS(1:0) = 11, VT = OVDD/2 V		83.333		MHz	2,3,6
Synthesis error	ppm_{SSoff}	Spread off		0		ppm	1,2,5
	ppm_{SSon}	Spread on		+/-150		ppm	1,2,5
Output High Voltage	V_{OH}	V_{OH} at the selected operating frequency	2.4			V	1
Output Low Voltage	V_{OL}	V_{OL} at the selected operating frequency			0.4	V	1
Slew Rate VDDO = 3.3V	t_{SLEW00}	'00' = Hi-Z		Hi-Z		V/ns	
	t_{SLEW01}	'01' Slow Slew Rate (Averaging on)	0.8	1.4	2.1	V/ns	1,3,8
	t_{SLEW10}	'10' Fast Slew Rate (Averaging on)	0.9	1.6	2.5	V/ns	1,3,8
	t_{SLEW11}	'11' Fastest Slew Rate (Averaging on)	1.1	1.9	3.1	V/ns	1,3,8
Duty Cycle	d_{t1}	V_T = OVDD/2 V	40	51.4	60	%	1,6
Jitter, Peak period jitter	t_{jpeak}	V_T = OVDD/2 V, SSC < 0.75%		±116	±150	ps	1
Phase Noise	$t_{phasenoise}$	-56dBc		10	500	kHz	1,7
AC Input Swing Limits @ 3.3V OV_{DD}	$_{T}V_{AC}$	This is the difference between VOL and VOH at the selected operating frequency.	1.9			V	1
Spread Spectrum Modulation Frequency	f_{SSMOD}	Triangular Modulation	0	31.5	60	kHz	

Electrical Characteristics - 125M

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Clock frequency	f_{125M}	V_T = OVDD/2 V		125.00		ns	2,3,6
Synthesis error	ppm			0		ppm	1,2,5
Output High Voltage	V_{OH}	V_{OH} at the selected operating frequency	2.2			V	1
Output Low Voltage	V_{OL}	V_{OL} at the selected operating frequency			0.5	V	1
Rise/Fall time VDDO = 3.3V	$t_{RF125M3.3V}$	Measured between 0.6V and 2.7V		0.7	1	ns	1,3
Duty Cycle	d_{t1}	V_T = OVDD/2 V	47	52	53	%	1
Jitter, Peak period jitter	t_{jpeak}	V_T = OVDD/2 V			±150	ps	1

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Electrical Characteristics - REF(5:0)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f	V_T = OVDD/2 V		25.00		MHz	2,3
Crystal Frequency Error	ppm	Including all aging and tuning effects	-50		50	ppm	1,2
Output High Voltage	V_{OH}	V_{OH} at the selected operating frequency	2.2			V	1
Output Low Voltage	V_{OL}	V_{OL} at the selected operating frequency			0.4	V	1
Slew Rate	t_{SLEW}	'00' = Hi-Z	1.0	1.7	2.7	V/ns	1,3,4
Duty Cycle	d_{t1}	V_T = OVDD/2 V	40	51	60	%	1
Pin to Pin Skew	t_{skew}	V_T = 1.5 V, odd/even outputs have an intentional 180degree phase shift.		N/A		ps	1
Jitter, Peak period jitter	t_{jpeak}	V_T = OVDD/2 V		±78	±200	ps	1
Jitter, Phase	t_{jphase}	(12kHz-5MHz), V_T = 1.5 V		1.7	3	ps rms	1

Electrical Characteristics - USB_CLK(2:1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f_{USB_CLK}	V_T = OVDD/2 V		12.00		MHz	2,3
				24.00		MHz	2,3
Synthesis error	ppm			0		ppm	1,2,5
Output High Voltage	V_{OH}	V_{OH} at the selected operating frequency	2.2			V	1
Output Low Voltage	V_{OL}	V_{OL} at the selected operating frequency			0.4	V	1
Slew Rate VDDO = 3.3V	t_{SLEW00}	'00' = Hi-Z		Hi-Z		V/ns	
	t_{SLEW01}	'01' Slow Slew Rate (Averaging on)	1.0	1.4	1.8	V/ns	1,3,4
	t_{SLEW10}	'10' Fast Slew Rate (Averaging on)	1.5	2.0	2.7	V/ns	1,3,4
	t_{SLEW11}	'11' Fastest Slew Rate (Averaging on)	1.8	2.3	3.1	V/ns	1,3,4
Duty Cycle	d_{t1}	V_T = OVDD/2 V	45	50.3	55	%	1
Jitter, RMS	t_{jRMS}	12kHz to Nyquist		23	120	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = OVDD/2 V		142	350	ps	1

Electrical Characteristics - 2.048M(1:0)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f_{USB_CLK}	V_T = OVDD/2 V		2.048		MHz	2,3,6
Synthesis error	ppm			0		ppm	1,2,5
Output High Voltage	V_{OH}	V_{OH} at the selected operating frequency	2.2			V	1
Output Low Voltage	V_{OL}	V_{OL} at the selected operating frequency			0.4	V	1
Slew Rate VDDO = 3.3V	t_{SLEW00}	'00' = Hi-Z		Hi-Z		V/ns	
	t_{SLEW01}	'01' Slow Slew Rate (Averaging on)	1.1	1.7	2.5	V/ns	1,3,4
	t_{SLEW10}	'10' Fast Slew Rate (Averaging on)	1.6	2.3	3.2	V/ns	1,3,4
	t_{SLEW11}	'11' Fastest Slew Rate (Averaging on)	1.8	2.6	3.6	V/ns	1,3,4
Duty Cycle	d_{t1}	V_T = OVDD/2 V	45	46.7	55	%	1
Pin to Pin Skew	t_{skew}	V_T = OVDD/2 V		108	250	ps	1
Jitter, RMS	t_{jRMS}	12kHz to Nyquist		47	70	ps	1
Jitter, Peak period jitter	t_{jpeak}	V_T = OVDD/2 V		±170	±250	ps	1

Notes for single-ended clocks:

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Clock Frequency specifications are guaranteed assuming that REF is at 25MHz.

[3] At default SMBus settings.

[4] Measured between 20% and 80% of OVDD.

[5] This is the frequency error with respect to the crystal frequency.

[6] Measured at the rising and/or falling edge at OVDD/2 V.

[7] Phase noise is calculated as the FFT of the TIE jitter.

[8] Slew rate is measured from $\pm 0.3\Delta V_{AC}$ at the center of peak to peak voltage at the clock input.

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General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will ***acknowledge***
- Controller (host) sends the beginning byte location = N
- IDT clock will ***acknowledge***
- Controller (host) sends the byte count = X
- IDT clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N+X-1***
- IDT clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Note: I²C compatible. Native mode is SMBus Block mode protocol. To use I²C Byte mode set the 2^7 bit in the command Byte. No Byte count is used.

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will ***acknowledge***
- Controller (host) sends the beginning byte location = N
- IDT clock will ***acknowledge***
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will ***acknowledge***
- IDT clock will send the data byte count = X
- IDT clock sends ***Byte N+X-1***
- IDT clock sends ***Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

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Byte 0 Frequency and Spread Select Register

Bit	Name	Description	Type	0	1	Default
7	SS4	Sys_CCB and DDRCLK Spread Selection Table	RW	See Table 2: Sys_CCB and DDRCLK Spread Table		0
6	SS3		RW			0
5	SS2		RW			0
4	SS1	PCIE Spread Selection Table	RW	See Table 1: PCIE Spread Table		0
3	SS0		RW			0
2	REF_5_EN	Output enable for REF_5	RW	Output Disabled	Output Enabled	1
1	REF_4_EN	Output enable for REF_4	RW	Output Disabled	Output Enabled	1
0	REF_3_EN	Output enable for REF_5	RW	Output Disabled	Output Enabled	1

Byte 1 Output Enable Register

Bit	Name	Description	Type	0	1	Default
7	REF_2_EN	Output enable for REF_2	RW	Output Disabled	Output Enabled	1
6	REF_1_EN	Output enable for REF_1	RW	Output Disabled	Output Enabled	1
5	REF_0_EN	Output enable for REF_0	RW	Output Disabled	Output Enabled	1
4	USB_CLK1_EN	Output enable for USB_CLK1	RW	Output Disabled	Output Enabled	1
3	USB_CLK2_EN	Output enable for USB_CLK2	RW	Output Disabled	Output Enabled	1
2	CK2.048_0_EN	Output enable for CK2.048_0	RW	Output Disabled	Output Enabled	1
1	CK2.048_1_EN	Output enable for CK2.048_1	RW	Output Disabled	Output Enabled	1
0	DDRCLK_EN	Output enable for DDRCLK	RW	Output Disabled	Output Enabled	1

Byte 2 Output Enable Register

Bit	Name	Description	Type	0	1	Default
7	Sys_CCB_EN	Output enable for Sys_CCB	RW	Output Disabled	Output Enabled	1
6	PCIe5_EN	Output enable for PCIe5	RW	Output Disabled	Output Enabled	1
5	PCIe4_EN	Output enable for PCIe4	RW	Output Disabled	Output Enabled	1
4	PCIe3_EN	Output enable for PCIe3	RW	Output Disabled	Output Enabled	1
3	PCIe2_EN	Output enable for PCIe2	RW	Output Disabled	Output Enabled	1
2	PCIe1_EN	Output enable for PCIe1	RW	Output Disabled	Output Enabled	1
1	PCIe0_EN	Output enable for PCIe0	RW	Output Disabled	Output Enabled	1
0	125M_EN	Output enable for 125M	RW	Output Disabled	Output Enabled	1

Byte 3 Slew Rate Control Register

Bit	Name	Description	Type	0	1	Default
7	USB1_SLEW1	USB_CLK1 Slew Rate Control	RW	See USB Electrical Tables		0
6	USB1_SLEW0		RW			1
5	USB2_SLEW1	USB_CLK2 Slew Rate Control	RW	See USB Electrical Tables		0
4	USB2_SLEW0		RW			1
3	CK2.048_SLEW1	CK2.048_0 and CK2.048_1 Slew Rate Control	RW	See CK2.048 Electrical Tables		1
2	CK2.048_SLEW0		RW			1
1	Sys_CCB_SLEW1	Sys_CCB Slew Rate Control	RW	See Sys_CCB Electrical Tables		0
0	Sys_CCB_SLEW0		RW			1

Byte 4 Slew Rate Control Register

Bit	Name	Description	Type	0	1	Default
7	DDR_Slew1	DDRCLK Slew Rate Control	RW	See DDR Electrical Tables		0
6	DDR_Slew0		RW			1
5	Reserved					0
4	Reserved					1
3	FS1	Sys_CCB Frequency Select Latch	RW	See Table 3: Sys_CCB Frequency Selection		Latch
2	FS0		RW			Latch
1	USB1_fSel	USB_CLK1 Clock Frequency Select	RW	12MHz	24MHz	0
0	USB2_fSel	USB_CLK2 Clock Frequency Select	RW	12MHz	24MHz	1

Byte 5 is Reserved

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Byte 6 PCI Express Amplitude Control Register

Bit	Name	Description	Type	0	1	Default
7	PCIE_AMP1	PCI Express Amplitude Control	RW	See Table 4: PCIe Amplitude Selection Table		0
6	PCIE_AMP0		RW			1
5	SEL100#_66	DDRCLK latch select	R	100MHz	66MHz	latch
4	SELPCIE125#_100	PCI Express latch select	R	125MHz	100MHz	latch
3	Reserved	Reserved	RW	-	-	0
2	Reserved	Reserved	RW	-	-	1
1	Reserved	Reserved	RW	-	-	0
0	Reserved	Reserved	RW	-	-	1

Byte 7 Revision and Vendor ID Register

Bit	Name	Description	Type	0	1	Default
7	REV ID	Revision ID	R	-	-	0
6	REV ID		R	-	-	0
5	REV ID		R	-	-	0
4	REV ID		R	-	-	1
3	Vendor ID	Vendor ID	R	-	-	0
2	Vendor ID		R	-	-	0
1	Vendor ID		R	-	-	0
0	Vendor ID		R	-	-	1

Byte 8 Byte Count Register

Bit	Name	Description	Type	0	1	Default
7	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back.		0
6	BC6		RW			0
5	BC5		RW			0
4	BC4		RW			0
3	BC3		RW			0
2	BC2		RW			1
1	BC1		RW			0
0	BC0		RW			1

Recommended Crystal Characteristics

PARAMETER	VALUE	UNITS	NOTES
Frequency	25	MHz	1
Resonance Mode	Fundamental	-	1
Frequency Tolerance @ 25°C	±20	PPM Max	1
Frequency Stability, ref @ 25°C Over Operating Temperature Range	±20	PPM Max	1
Temperature Range (commercial)	0~70	°C	1
Temperature Range (industrial)	-40~85	°C	1
Equivalent Series Resistance (ESR)	50	Ω Max	1
Shunt Capacitance (C_O)	7	pF Max	1
Load Capacitance (C_L)	8	pF Max	1
Drive Level	0.1	mW Max	1
Aging per year	±5	PPM Max	1

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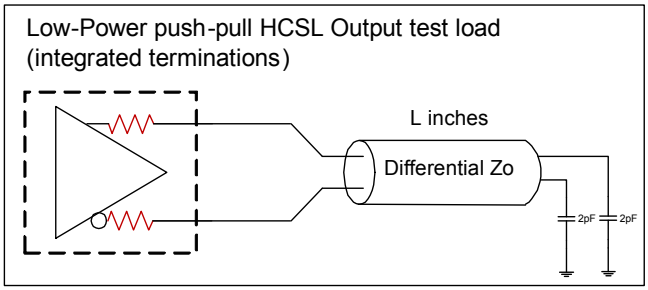
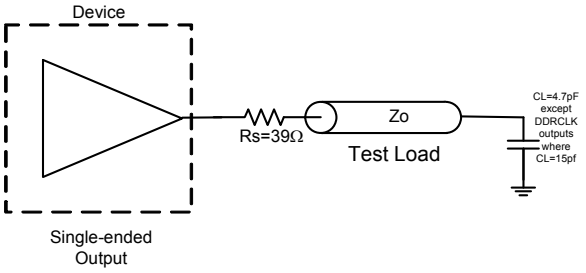
Test Loads





Differential Test Load, Zo = 100ohm, L = 5 inches

Thermal Characteristics (48-TSSOP)

PARAMETER	SYMBOL	CONDITIONS	PKG	TYP VALUE	UNITS	NOTES
Thermal Resistance	θ_{JC}	Junction to Case	PAG48	28	°C/W	1
	θ_{Jb}	Junction to Base		42	°C/W	1
	θ_{JA0}	Junction to Air, still air		62	°C/W	1
	θ_{JA1}	Junction to Air, 1 m/s air flow		54	°C/W	1
	θ_{JA3}	Junction to Air, 3 m/s air flow		51	°C/W	1

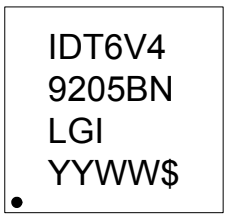
Thermal Characteristics (48-VFQFPN)

PARAMETER	SYMBOL	CONDITIONS	PKG	TYP VALUE	UNITS	NOTES
Thermal Resistance	θ_{JC}	Junction to Case	NLG48	25	°C/W	1
	θ_{Jb}	Junction to Base		3.1	°C/W	1
	θ_{JA0}	Junction to Air, still air		32	°C/W	1
	θ_{JA1}	Junction to Air, 1 m/s air flow		25	°C/W	1
	θ_{JA3}	Junction to Air, 3 m/s air flow		22	°C/W	1

[1]ePad soldered to board

Marking Diagrams

48TSSOP



48VFQFPN

Notes:
1. “$” is the mark code.
2. “YYWW” is the last two digits of the year, and the week number that the part was assembled.
3. “G” after the two-letter package code denotes Pb free package.
4. “I” denotes industrial temperature range.
5. Bottom marking for TSSOP: country of origin if not USA.

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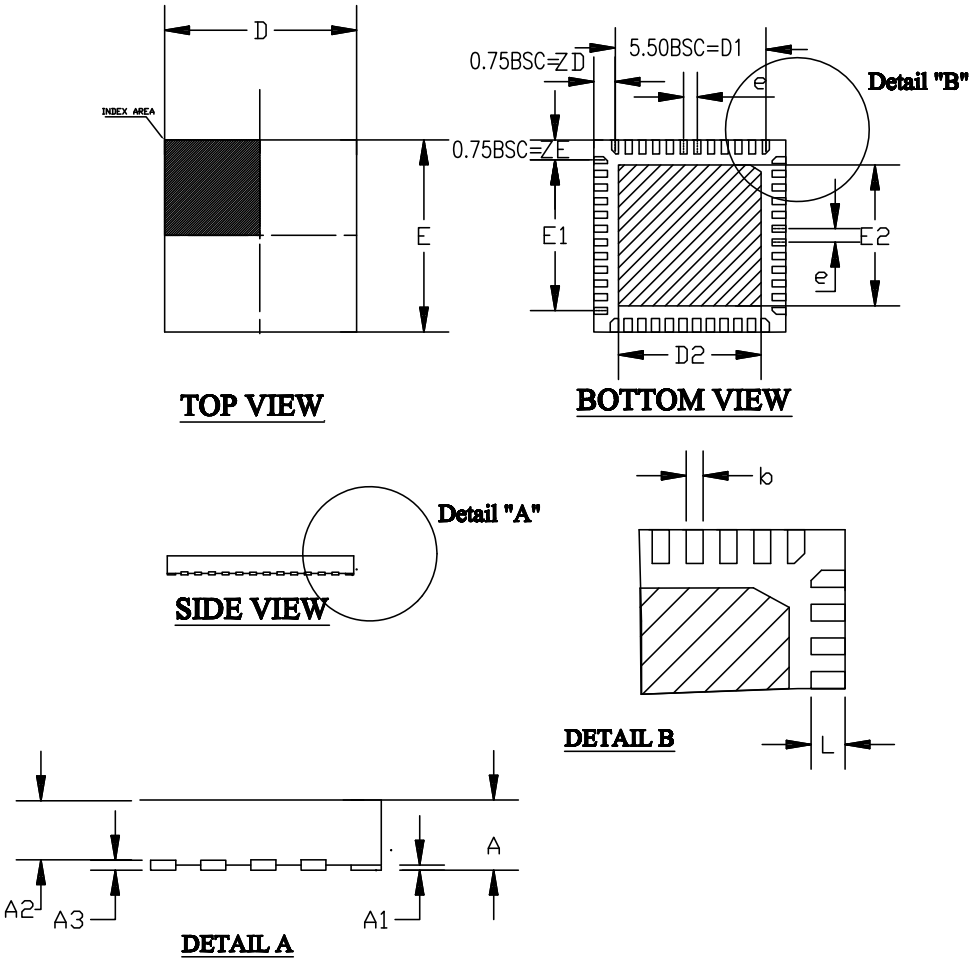
Package Outline and Dimensions (7 x 7mm 48-VFQFPN)

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	11/20/15	JH



SYMBOL	DIMENSION		
D	7.00 BSC		
E	7.00 BSC		
D2	5.50	5.65	5.80
E2	5.50	5.65	5.80
L	0.35	0.40	0.45
e	0.50 BSC		
N	48		
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.2 REF		
b	0.18	0.25	0.30

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX±
ANGULAR ±

IDT™ www.IDT.com
6024 Silver Creek Valley Road
San Jose, CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-8591

APPROVALS	DATE
DRAWN RAC	10/18/07
CHECKED	

TITLE NL/NLG48 PACKAGE OUTLINE 7.0 x 7.0 mm BODY, EPAD 5.65 mm SQ. 0.5 mm PITCH QFN (SAWN)

SIZE C | DRAWING No. PSC-4203-01 | REV 00

DO NOT SCALE DRAWING | SHEET 1 OF 2

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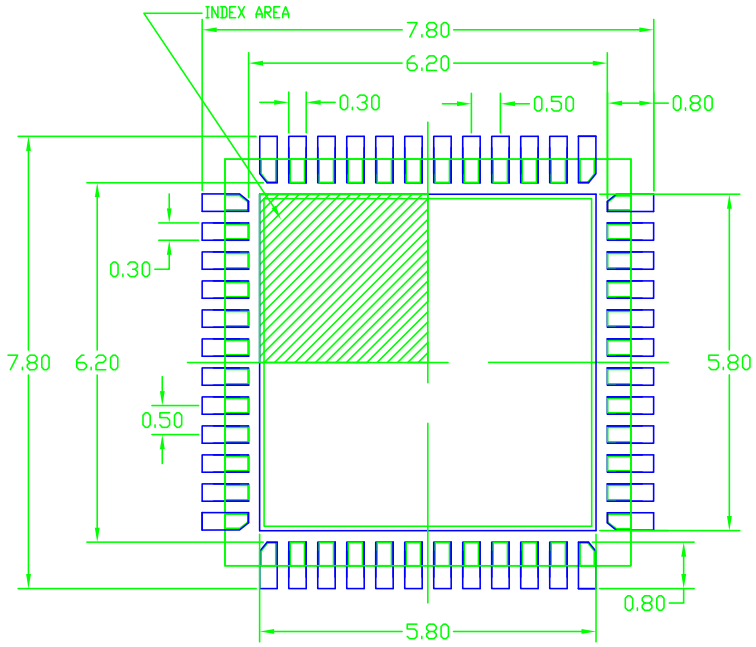
Package Outline and Dimensions (7 x 7mm 48-VFQFPN), cont.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	11/20/15	JH



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN BLACK.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX±
ANGULAR ±

APPROVALS	DATE
DRAWN RAC	10/18/07
CHECKED	

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TITLE NL/NLG48 PACKAGE OUTLINE 7.0 x 7.0 mm BODY, EPAD 5.65 mm SQ. 0.5 mm PITCH QFN (SAWN)

SIZE	DRAWING No.	REV
C	PSC-4203-01	00

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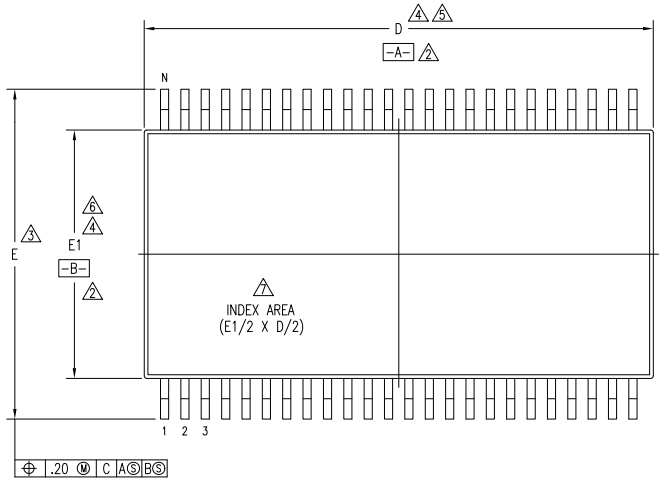
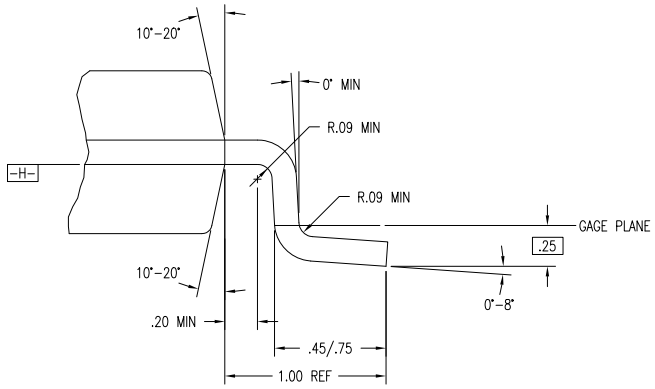
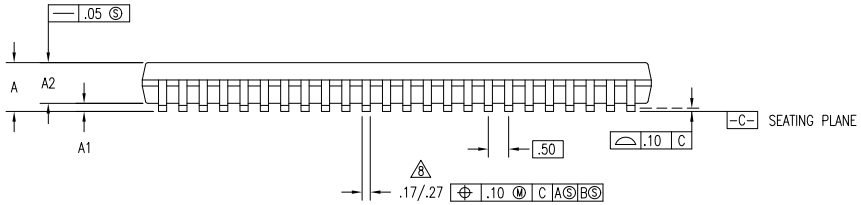
Package Outline and Dimensions (6.10 mm Body 48-TSSOP)

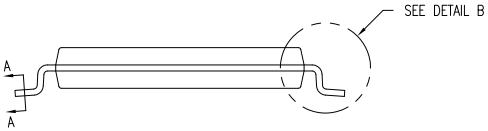
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
26490	02	CHANGE DIM A1	07/21/94	T. VU
27494	03	REDRAW TO JEDEC FORMAT	03/08/95	T. VU
61767	04	ADD 64 LD	01/15/99	
	05	ADD "GREEN" PAG NOMENCLATURE	10/14/04	TU VU
	06	CHANGE SOME COMMON DIMENSION	03/14/07	TU VU

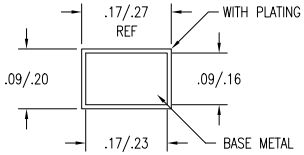




DETAIL B







SECTION A-A

TOLERANCES UNLESS SPECIFIED		IDT™ www.IDT.com	2975 Stender Way Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674
DECIMAL XX± XXX± XXXX±	ANGULAR ±		
APPROVALS	DATE	TITLE	PA/PAG PACKAGE OUTLINE 6.10 mm BODY WIDTH TSSOP .50 mm PITCH
DRAWN			
CHECKED		SIZE C	DRAWING No. PSC-4039 / REV 06
		DO NOT SCALE DRAWING	SHEET 1 OF 2

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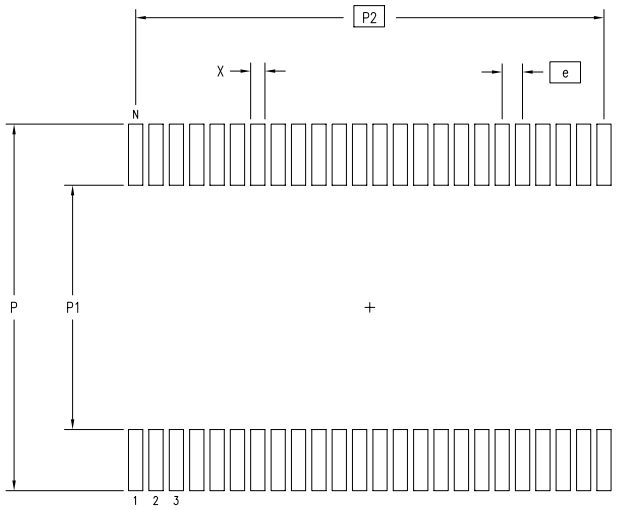
Package Outline and Dimensions (6.10 mm Body 48-TSSOP), cont.

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
26490	02	CHANGE DIM A1	07/21/94	T. VU
27494	03	REDRAW TO JEDEC FORMAT	03/08/95	T. VU
61767	04	ADD 64 LD	01/15/99	
	05	ADD "GREEN" PAG NOMENCLATURE	10/14/04	TU VU
	06	CHANGE SOME COMMON DIMENSION	03/14/07	TU VU

SYMBOL	JEDEC VARIATION ED			NOTE	JEDEC VARIATION EE			NOTE	JEDEC VARIATION EF			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	–	–	1.20		–	–	1.20		–	–	1.20	
A1	.05	–	.15		.05	–	.15		.05	–	.15	
A2	.80	1.00	1.05		.80	1.00	1.05		.80	1.00	1.05	
D	12.40	12.50	12.60	4,5	13.90	14.00	14.10	4,5	16.90	17.00	17.10	4,5
E	7.95	8.10	8.25	3	7.95	8.10	8.25	3	7.95	8.10	8.25	3
E1	6.00	6.10	6.20	4,6	6.00	6.10	6.20	4,6	6.00	6.10	6.20	4,6
N	48				56				64			

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX
P	8.90	9.10	8.90	9.10	8.90	9.10
P1	5.90	6.10	5.90	6.10	5.90	6.10
P2	11.50 BSC		13.50 BSC		15.50 BSC	
X	.30	.40	.30	.40	.30	.40
e	.50 BSC		.50 BSC		.50 BSC	
N	48		56		64	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-
4. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-
5. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
6. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
7. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
8. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–153, VARIATION ED, EE & EF

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX±
ANGULAR ±

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Santa Clara, CA 95054
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APPROVALS	DATE
DRAWN	
CHECKED	

TITLE PA/PAG PACKAGE OUTLINE 6.10 mm BODY WIDTH TSSOP .50 mm PITCH

SIZE	DRAWING No.	REV
C	PSC–4039	06

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Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
6V49205BPAGI	see page 12	Tubes	48-pin TSSOP	-40 to +85°C
6V49205BPAGI8		Tape and Reel	48-pin TSSOP	-40 to +85°C
6V49205BNLGI	see page 12	Tray	48-pin VFQFPN	-40 to +85°C
6V49205BNLGI8		Tape and Reel	48-pin VFQFPN	-40 to +85°C

"G" after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History

Rev.	Issue Date	Issuer	Description	Page #
M	12/9/2013	R. Wade	1. Extensive overhaul of Electrical tables to more closely align with Freescale published specifications. 2. Updated electrical tables with characterization data. 3. Clarified SMBus registers for Slew Rate Controls 4. Moved electrical tables in front of SMBus for consistency with other data sheets. 5. Updated Thermal Data and added test loads for clarity. 6. Updated front page text 7. Minor updates to pin names (mainly power and ground) for consistency and clarity 8. Move to Final	Various
N	6/2/2014	R. Wade	1. Corrected pin description for pin 44.	3
P	8/10/2015	R. Wade	1. Updated SMBus operating frequency from 100KHz minimum to 400KHz maximum.	5
Q	5/11/2016	RDW	1. Correct PCIeT_LRn and PCIeC_LRn to be PCIeT_Ln and PCIeC_Ln to indicate that the Rs for the PCIe outputs is outside the part and to correct the pin description accordingly. The test loads for the device are correct. 2. Update block diagram PCIe pin names to be consistent.	1-3
R	11/22/2016	RDW	1. Undo Revision Q 2. PCIe outputs have integrated terminations for 100ohm differential Zo. 3. Update Test Loads 4. Update Features/Benefits	1-3, 12
S	5/5/2017	RDW	1. Updated bit values in the "Sys_CCB Frequency Select" table. 2. Updated 48-TSSOP and 48-VFQFPN package outline drawings. 3. Updated legal disclaimer.	3, 13-16

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(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
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www.renesas.com

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