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15	2D-ACE

Revision History

Rev	
X1	TWR-LS1021A draft revision for Rev2.0 LS1021A/LS1020A silicon 1. Change PWR Solution by FSL parts 2. Support deep-sleep 3. Changed NOR flash to MT28EW01GABA1HJS-0SIT 4. Changed IFC_ADDR[16:18] connection from SOC to NOR directly. 5. Added IFC_ADDR[15] to ELEV D76 pin 6. Added C363 for USB_HVDD filter circuit.
A	No circuit change only upgrade document revision.
B	1. Remove mux part U39, U38 and C331, C348; 2. Change SATA connector to Molex 67800-5025. 3. Add J24 SATA PWR. 4. Add U54, U55 INA220 instead of LTC2945 current monitor. 5. RGMII_PHY_INT_N_18 go through CPLD then to SOC INT. 6. Asleep LED driver changed to always ON +3V3_PMIC 7. Connect IRQ_C from ELEV to CPLD. 8. R746 changed to 47ohm.

Revisions

Rev	Description	Date	Approved
X1	Original Release	Dec 05, 2014	Tom Sun
A	RevA Final Release	Jan 20, 2015	Tom Sun
B	RevB Final Release	May 29, 2015	Tom Sun

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TWR-LS1021A-PB

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ICAP Classification: FCP: FIUO: PUBI: X

Designer: Gan Fulian/B27268	Drawing Title: TWR-LS1021A-PB	
Drawn by: Gan Fulian/B27268	Page Title: COVER PAGE	
Approved: Tom Sun	Size: C	Document Number: SCH-28673 PDF: SPF-28673 — Rev: B
	Date: Sunday, May 31, 2015	Sheet 1 of 15

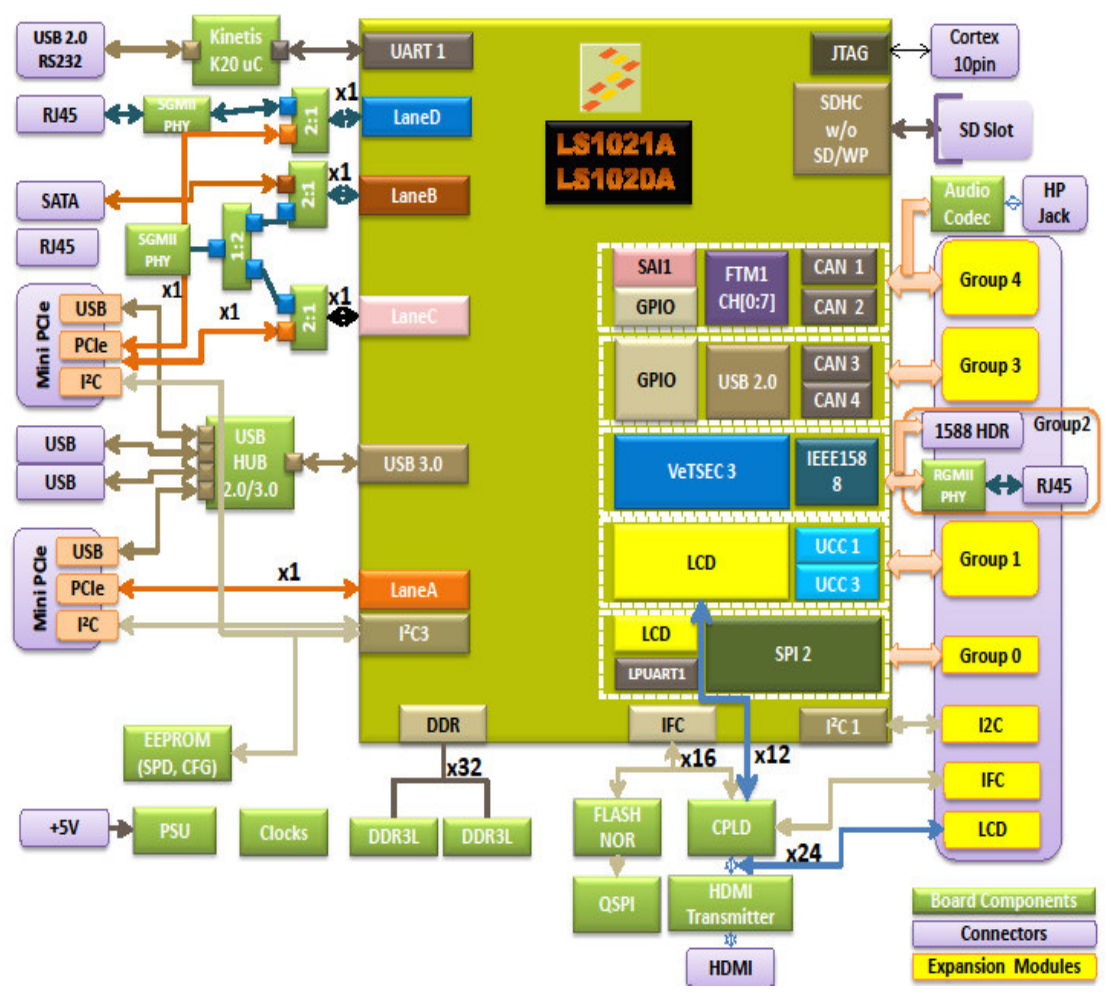
1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/8 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted Lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.



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ICAP Classification: FCP: ___ FIUO: PUBI: X

Drawing Title: **TWR-LS1021A-PB**

Page Title: **NOTES**

Size	Document Number	Rev
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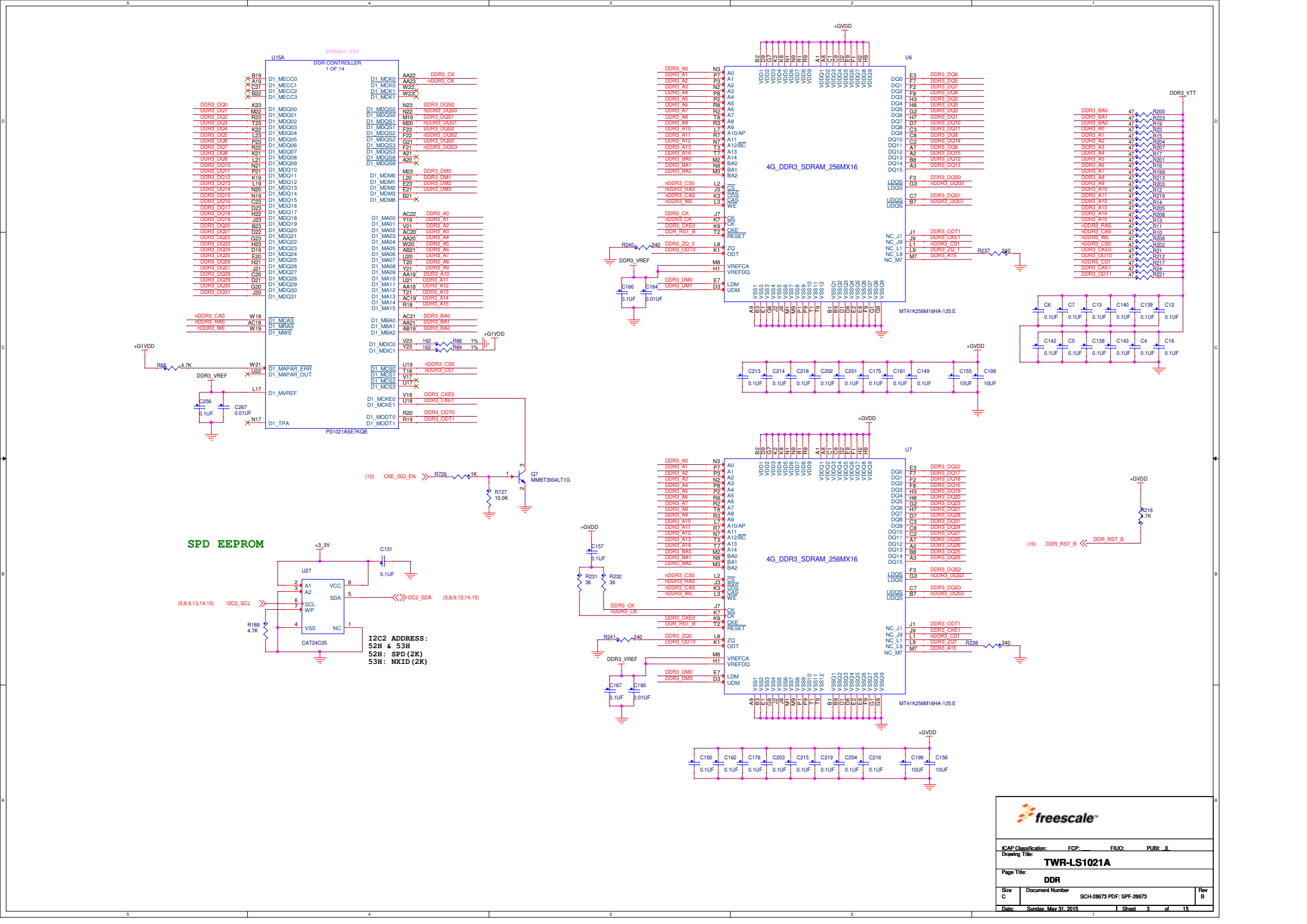
Date: Sunday, May 31, 2015 Sheet 2 of 15



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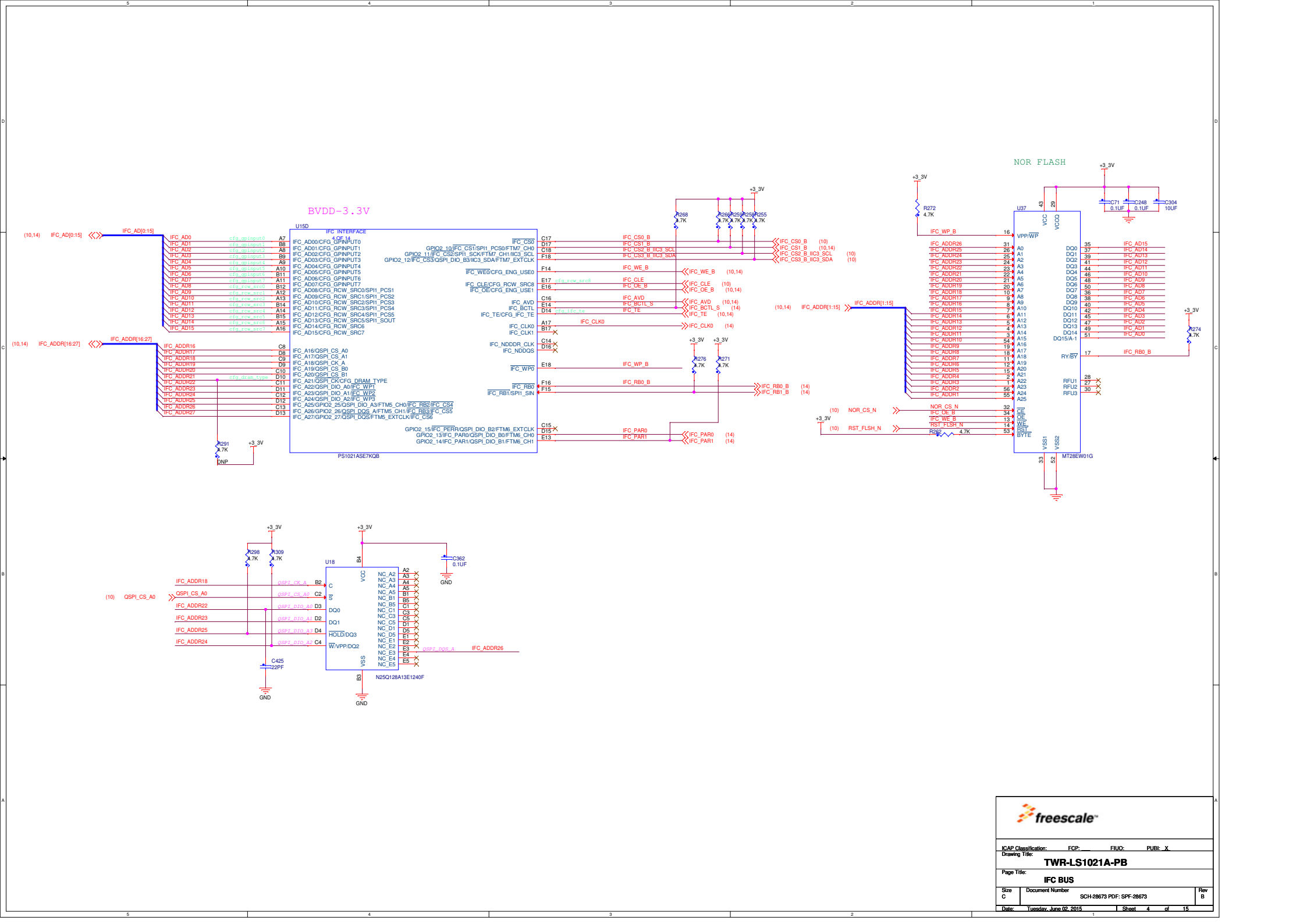
Drawing Title:	TWR-LS1021A		
Page Title:	DDR		
Size: C	Document Number: SCH-28673 PDF: SPF-28673		Rev: B
Date: Sunday, May 31, 2015		Sheet 3 of 15	



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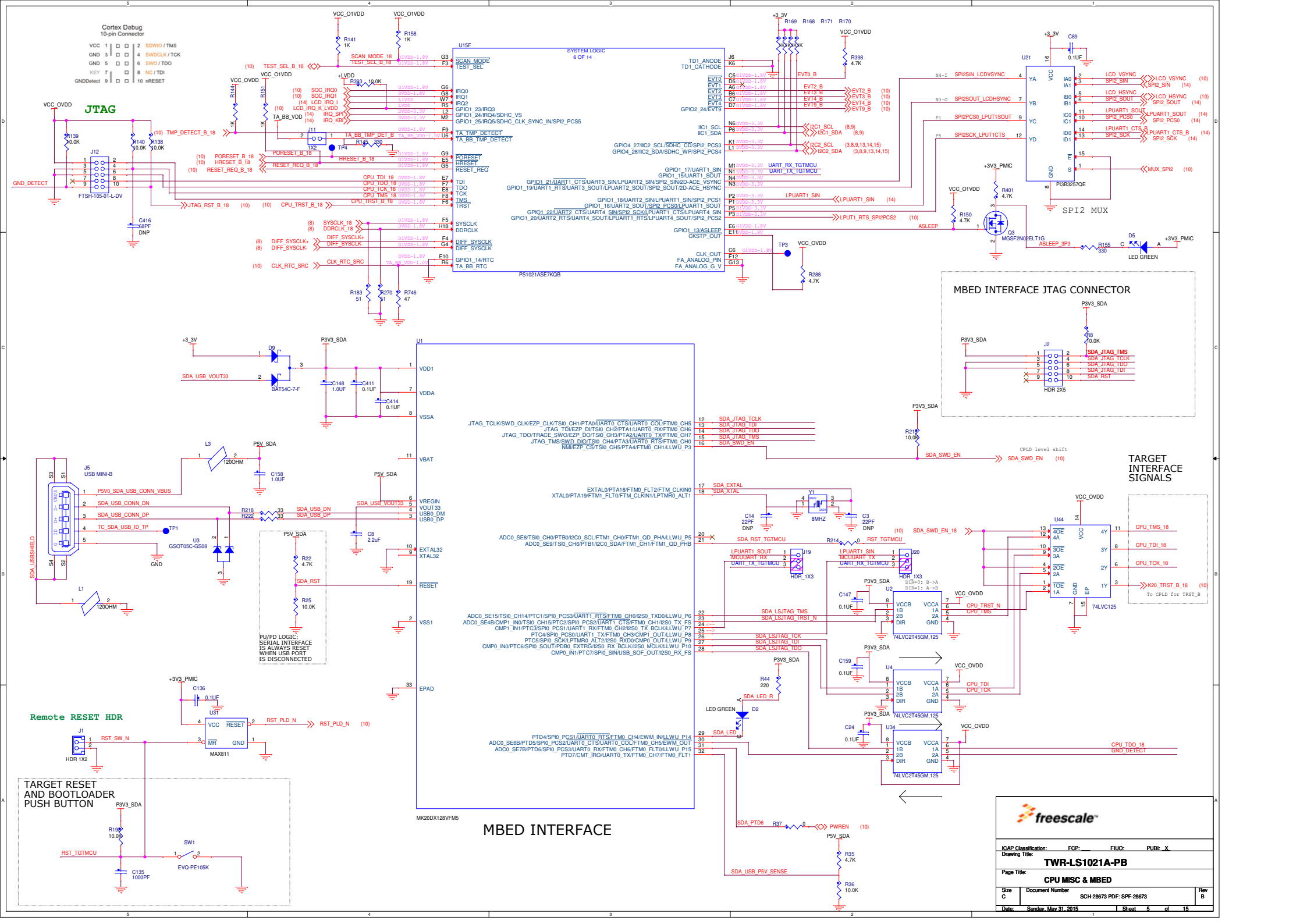
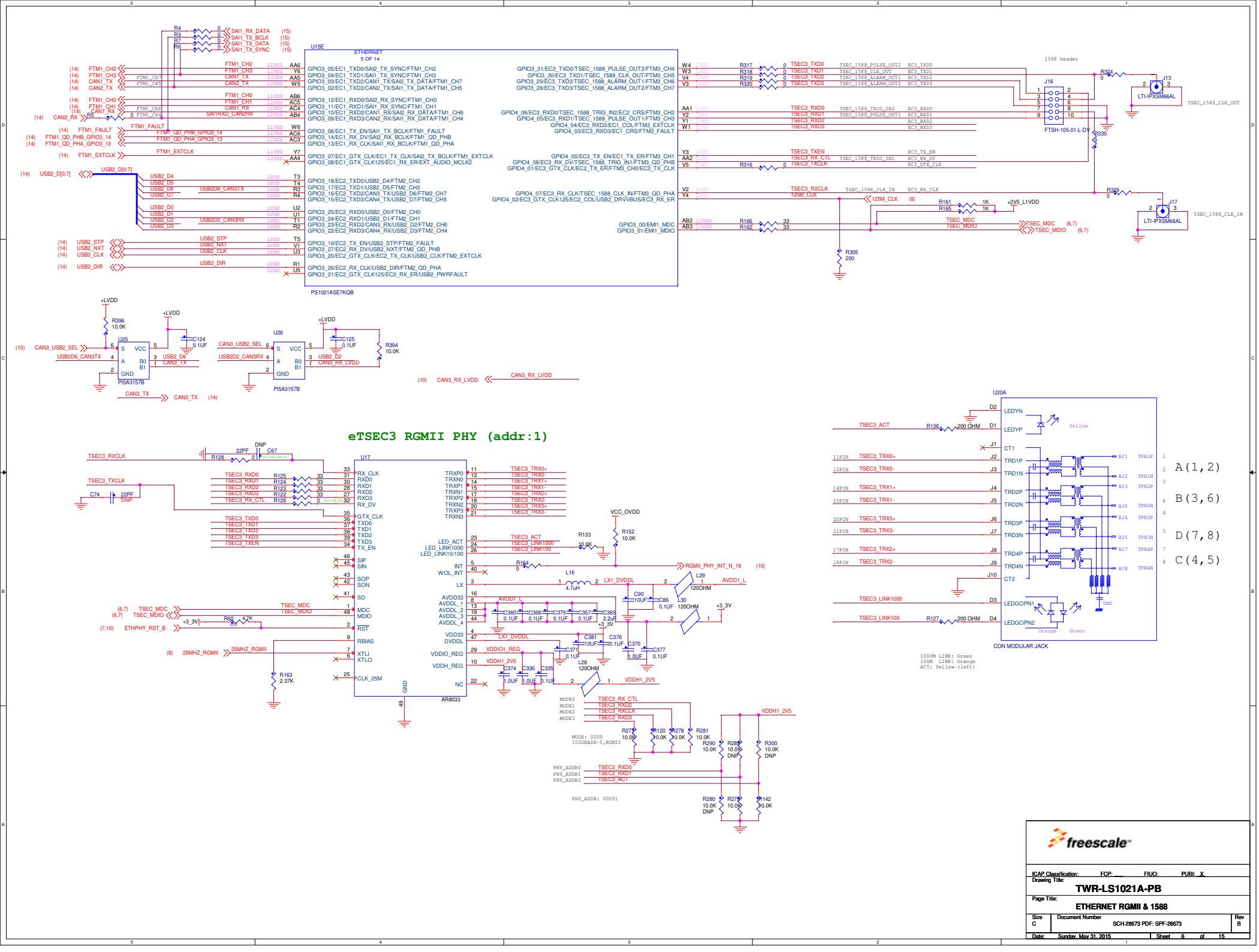
Drawing Title:	TWR-LS1021A-PB
Page Title:	IFC BUS
Size: C	Document Number: SCH-28673 PDF: SPF-28673 Rev: B
Date: Tuesday, June 02, 2015	Sheet 4 of 15


JTAG
MBED INTERFACE JTAG CONNECTOR
TARGET INTERFACE SIGNALS
SPI2 MUX
MBED INTERFACE
Remote RESET HDR
TARGET RESET AND BOOTLOADER PUSH BUTTON
PU/PD LOGIC: SERIAL INTERFACE IS ALWAYS RESET WHEN USB PORT IS DISCONNECTED
PS1021ASE7KQB
MK20DX128VFM5
TWR-LS1021A-PB
CPU MISC & MBED
SCH-28673 PDF: SPF-28673
Sunday, May 31, 2015



ICAP Classification:	FCP: ___ FIUO: PUBI: X
Drawing Title:	TWR-LS1021A-PB
Page Title:	ETHERNET RGMII & 1588
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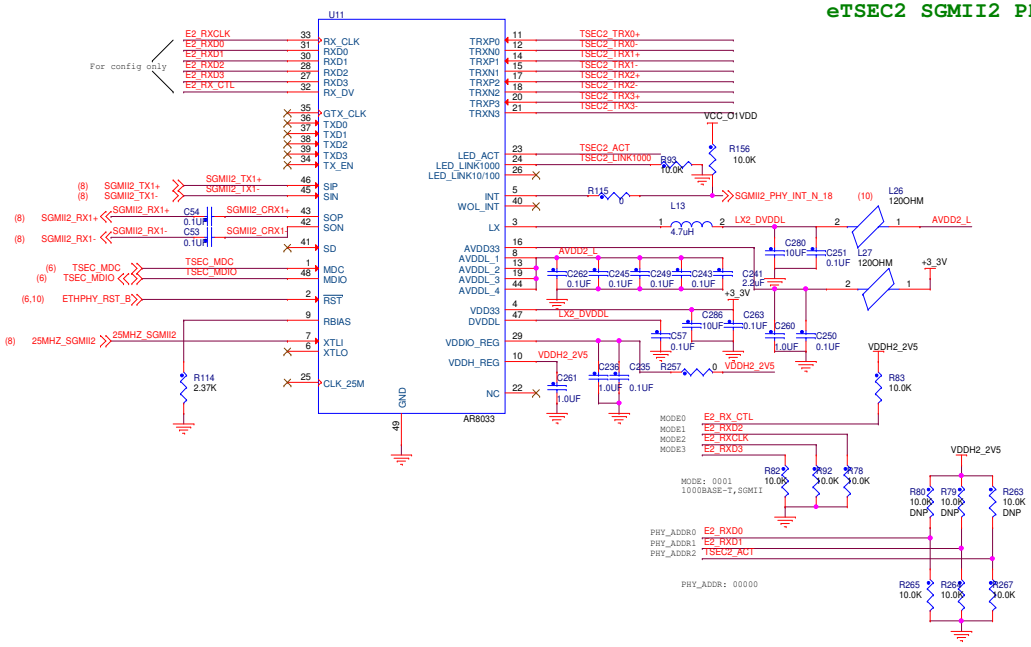
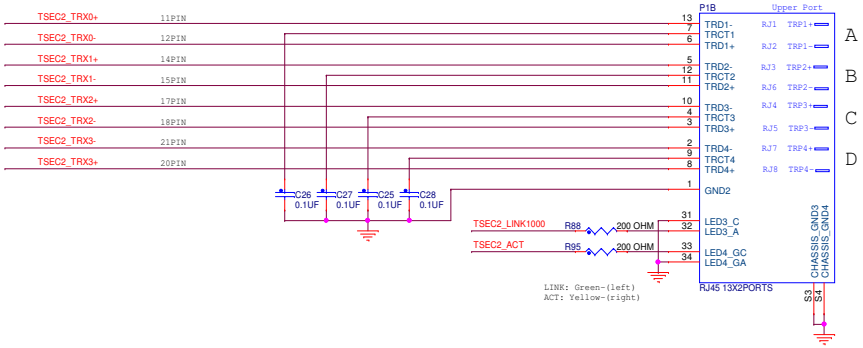
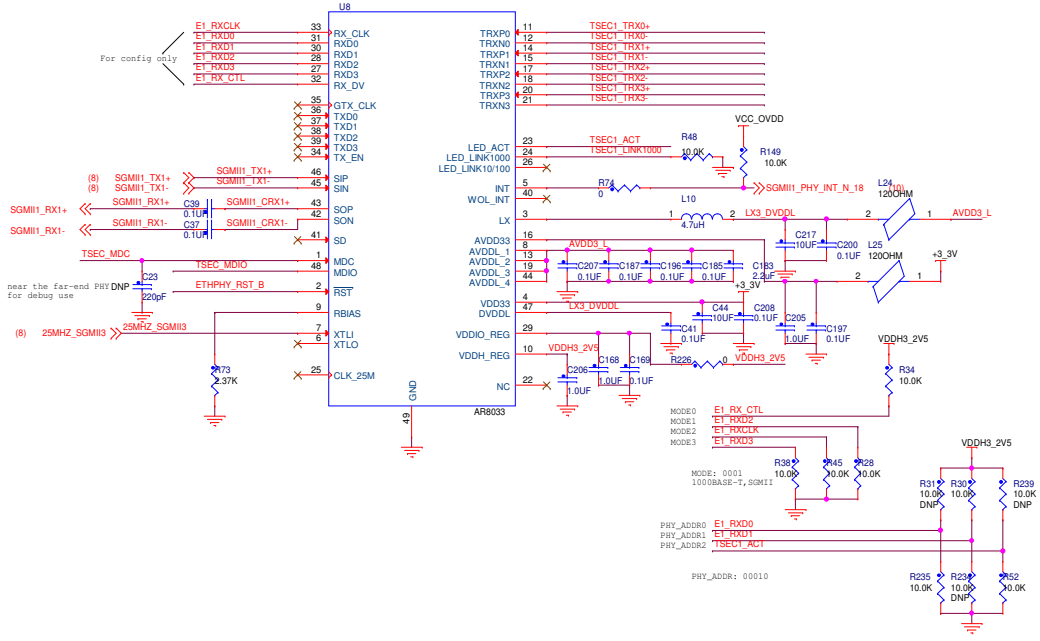
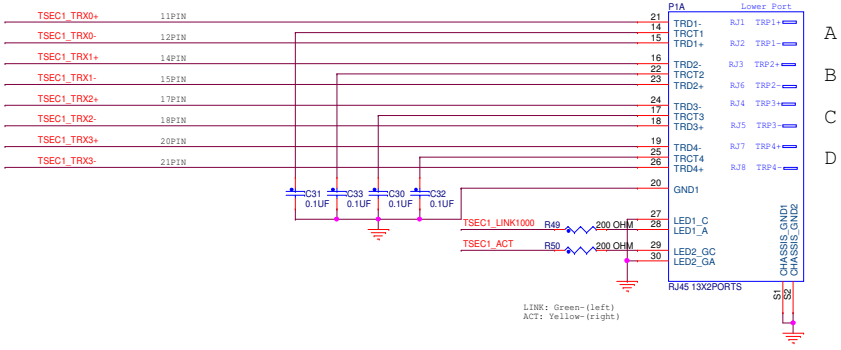
eTSEC2 SGMII2 PHY (addr:0)





eTSEC1 SGMII1 PHY (addr:2)





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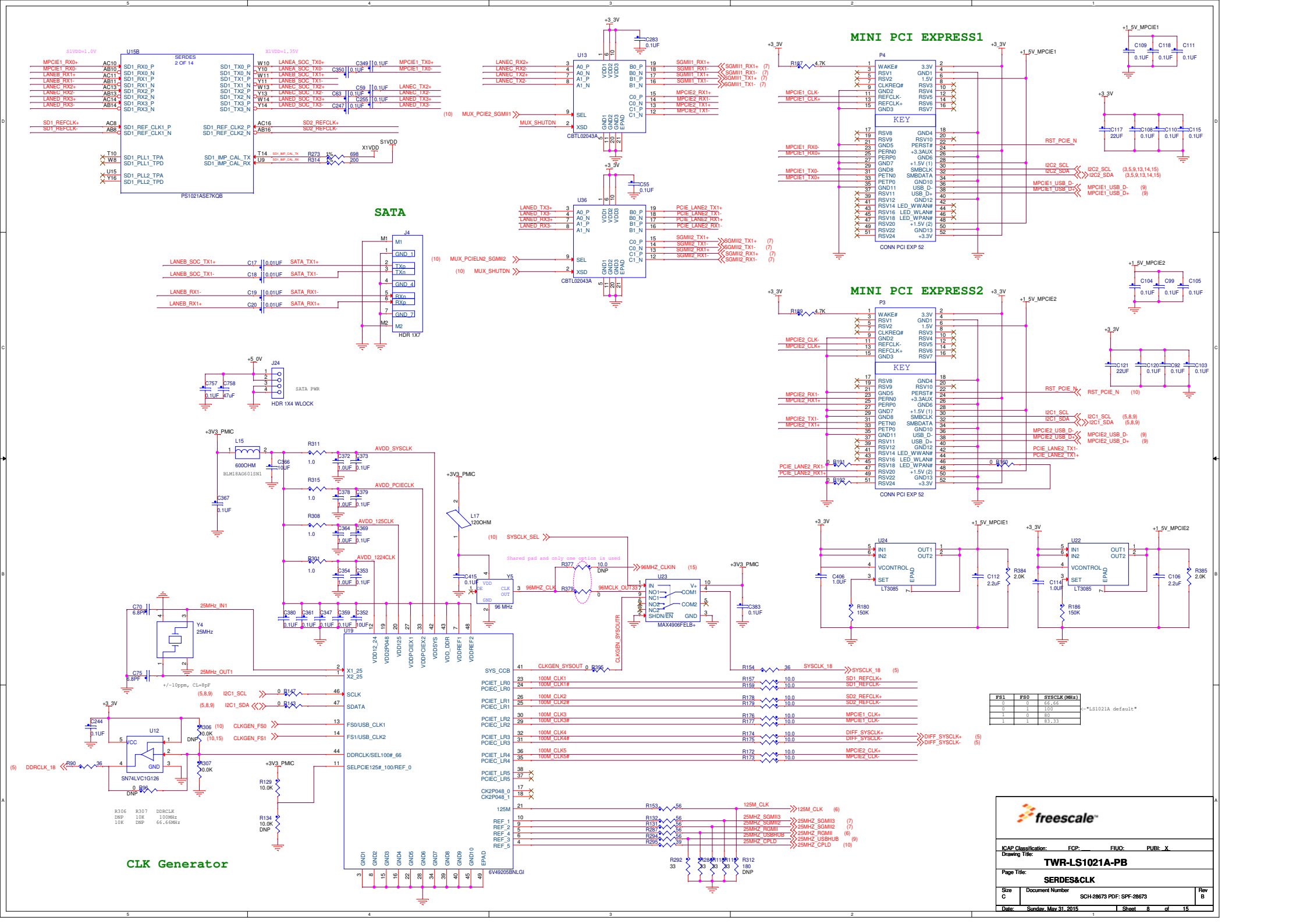
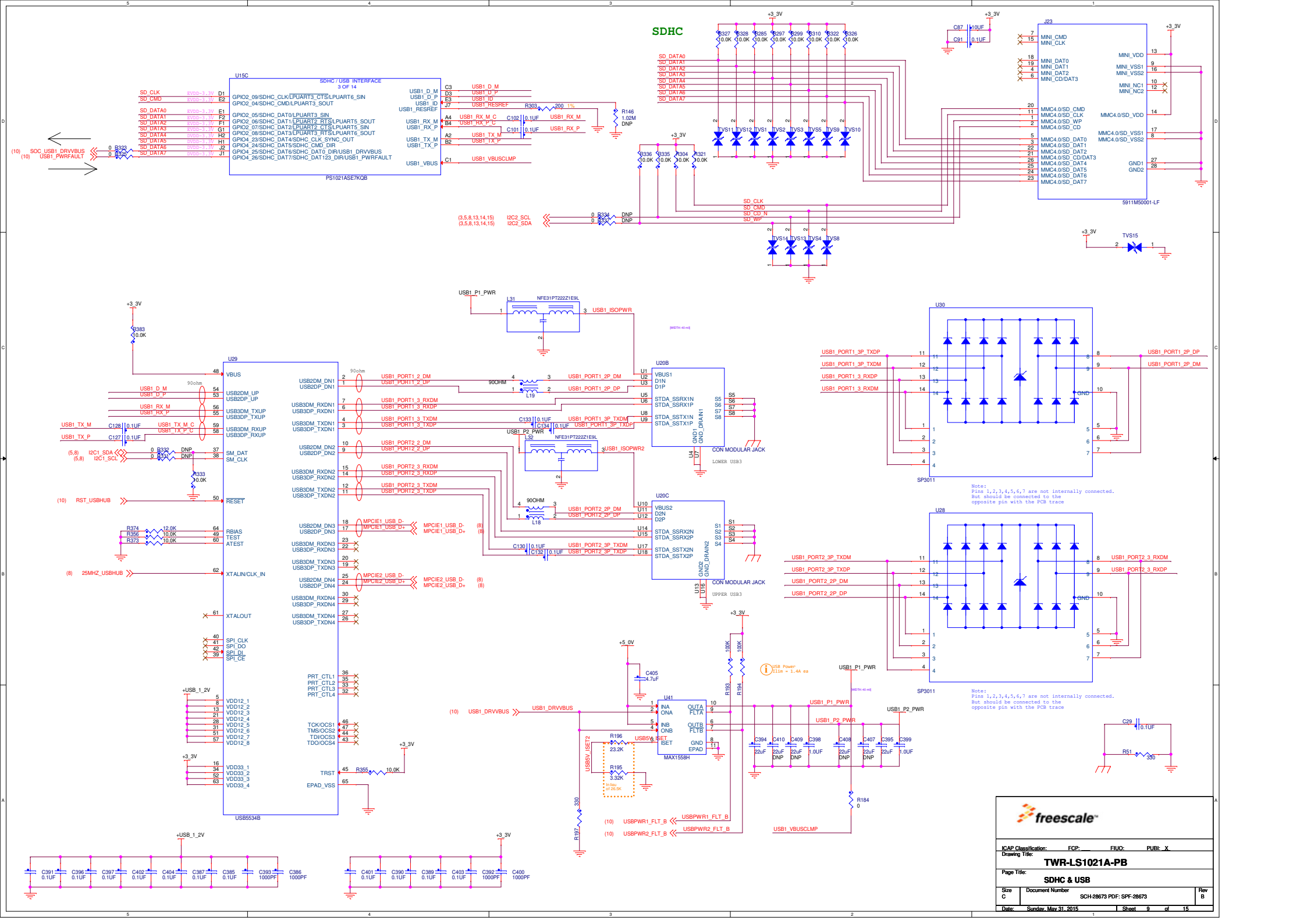
ICAP Classification:	FCP: ___ FIUO:	PUBI: X
Drawing Title:	TWR-LS1021A-PB	
Page Title:	ETHERNET SGMII	
Size: C	Document Number: SCH-28673 PDF: SPF-28673	Rev: B
Date: Sunday, May 31, 2015	Sheet 7 of 15	



FS1	FS0	SYSCLK (MHz)	
0	0	66.66	
0	1	100	<-"LS1021A default"
1	0	80	
1	1	83.33	


SDHC
U15C
SDHC / USB INTERFACE
3 OF 14
PS1021ASE7KQB
J23
5911M50001-LF
U29
USB5534B
U20B
U20C
CON MODULAR JACK
LOWER USB3
UPPER USB3
U30
U28
SP3011
MAX1558H
U41
TVS15
Note:
Pins 1,2,3,4,5,6,7 are not internally connected.
But should be connected to the
opposite pin with the PCB trace
freescale
ICAP Classification:
FCP:
FIUO:
PUBI: X
Drawing Title:
TWR-LS1021A-PB
Page Title:
SDHC & USB
Size
C
Document Number
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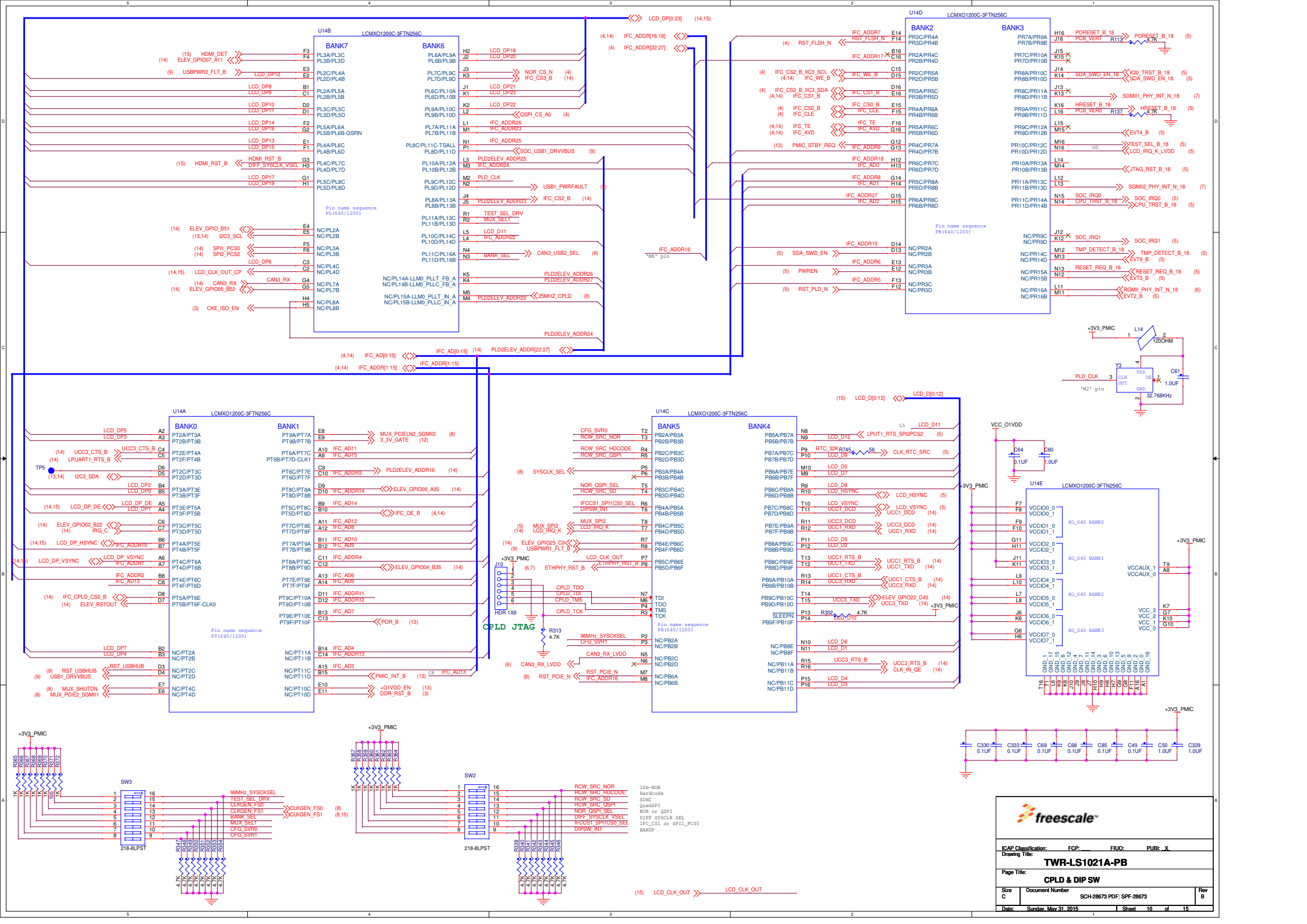
U14B
LCMXO1200C-3FTN256C
BANK7
BANK6
U14D
BANK2
BANK3
U14A
BANK0
BANK1
U14C
BANK5
BANK4
U14E
LCMXO1200C-3FTN256C
Pin name sequence PL(640/1200)
Pin name sequence PR(640/1200)
Pin name sequence PT(640/1200)
Pin name sequence PB(640/1200)
CPLD JTAG
HDR 1X6
SW3
SW2
218-8LPST
freescale
ICAP Classification:
FCP:
FIUO:
PUBI: X
Drawing Title:
TWR-LS1021A-PB
Page Title:
CPLD & DIP SW
Size C
Document Number
SCH-28673 PDF: SPF-28673
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Date: Sunday, May 31, 2015
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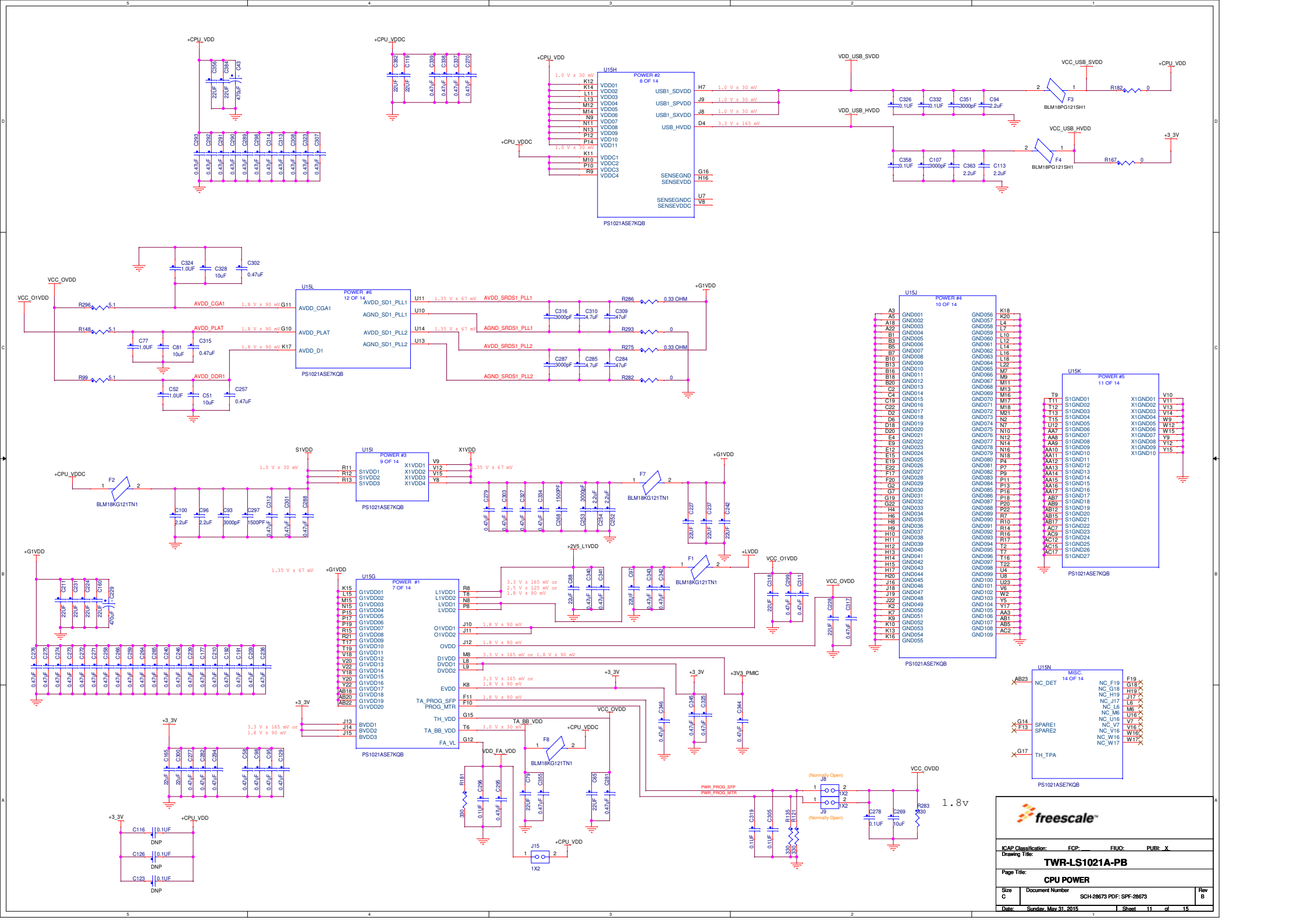
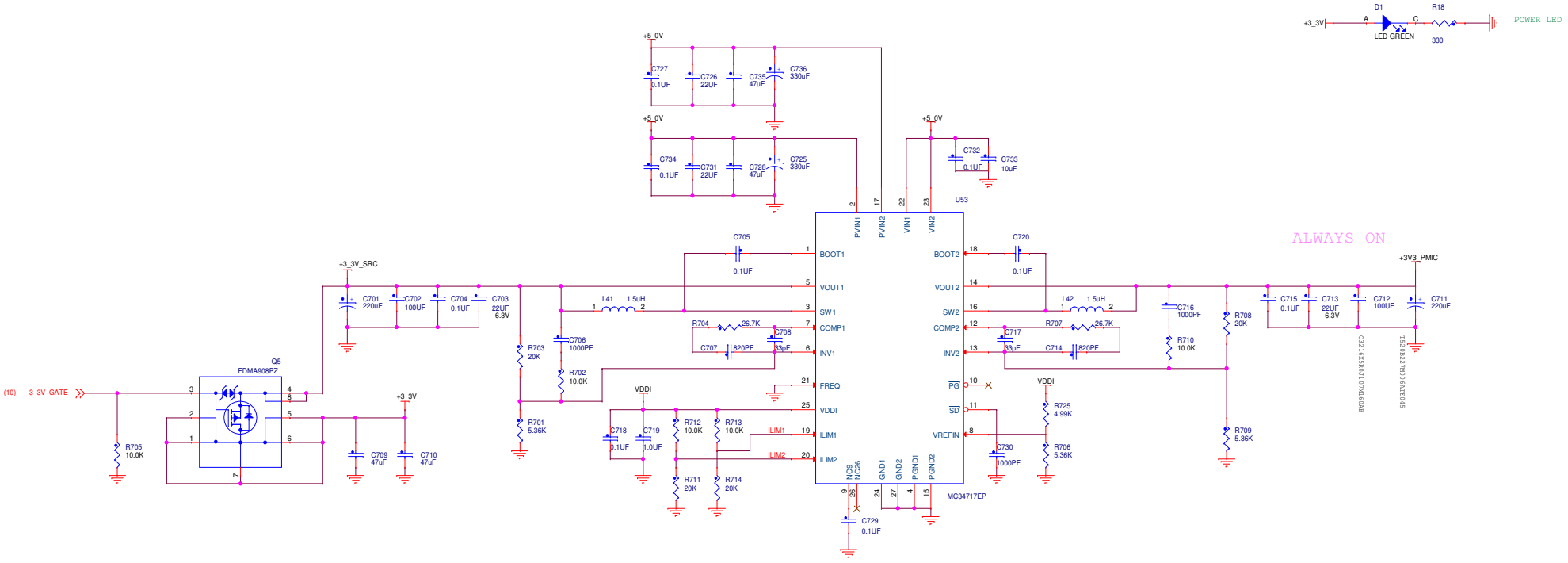


ICAP Classification:	FCP:	FIUO:	PUBI: X
Drawing Title:	TWR-LS1021A-PB		
Page Title:	CPU POWER		
Size: C	Document Number: SCH-28673 PDF: SPF-28673		Rev: B
Date: Sunday, May 31, 2015	Sheet 11 of 15		



AC ADAPTER SPECIFICATIONS

DC Voltage Output: 5VDC

Current Output: ~ 5A (depending on application)

Polarity:

Inner Diameter: 2.1mm

Outer Diameter: 5.5mm

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ICAP Classification: FCP: ___ FIUO: PUBI: X

Drawing Title: **TWR-LS1021A-PB**

Page Title: **POWER SUPPLY (3.3V &MISC)**

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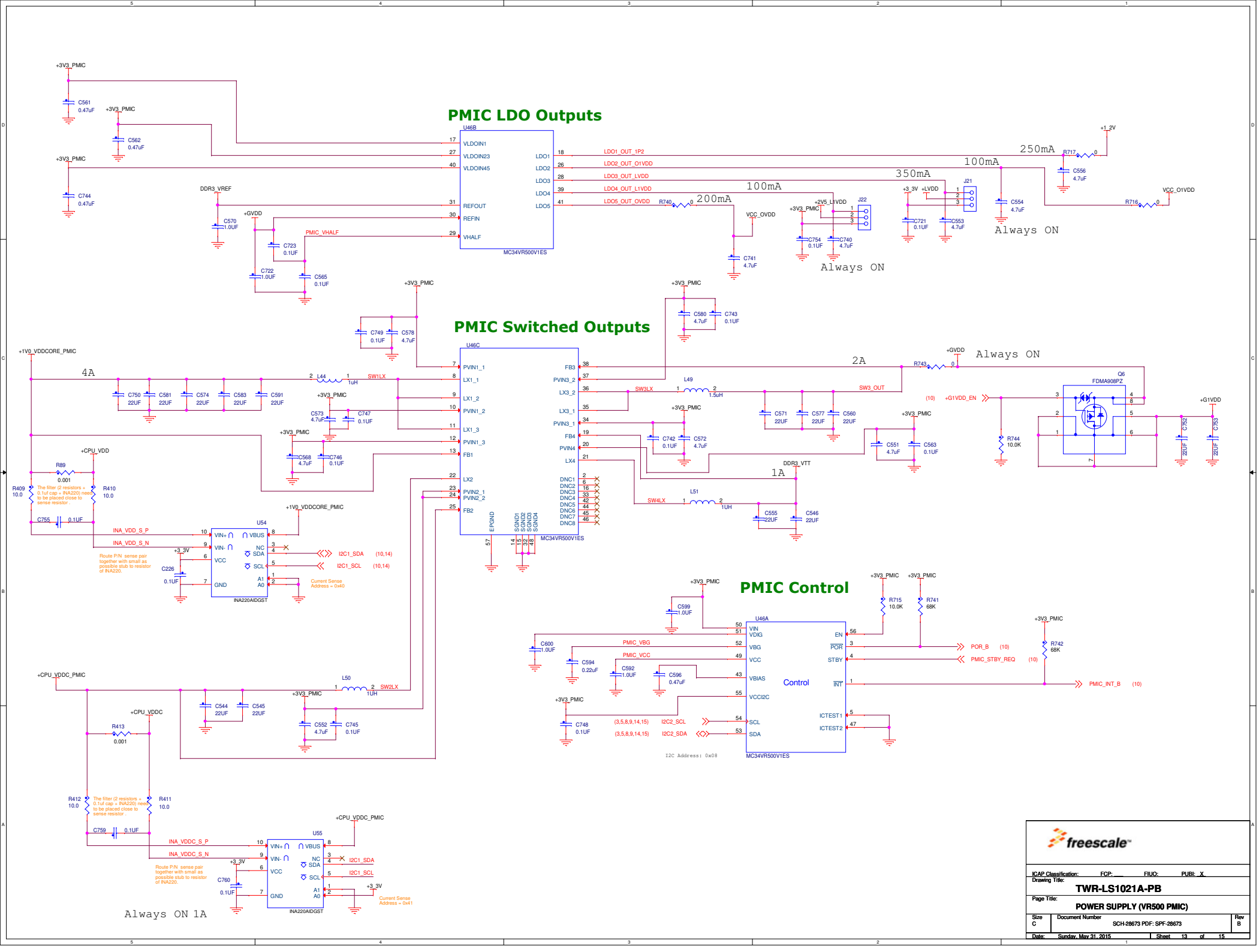
PMIC LDO Outputs
PMIC Switched Outputs
PMIC Control
U46B
MC34VR500V1ES
VLDOIN1
VLDOIN23
VLDOIN45
REFOUT
REFIN
VHALF
LDO1
LDO2
LDO3
LDO4
LDO5
LDO1_OUT_1P2
LDO2_OUT_O1VDD
LDO3_OUT_LVDD
LDO4_OUT_L1VDD
LDO5_OUT_OVDD
250mA
100mA
350mA
100mA
200mA
Always ON
Always ON
U46C
PVIN1_1
LX1_1
LX1_2
PVIN1_2
LX1_3
PVIN1_3
FB1
LX2
PVIN2_1
PVIN2_2
FB2
FB3
PVIN3_2
LX3_2
LX3_1
PVIN3_1
FB4
PVIN4
LX4
EPGND
SGND1
SGND2
SGND3
SGND4
SW1LX
SW3LX
SW4LX
SW3_OUT
2A
1A
Always ON
U46A
VIN
VDIG
VBG
VCC
VBIAS
VCCI2C
SCL
SDA
EN
POR
STBY
INT
ICTEST1
ICTEST2
Control
PMIC_VBG
PMIC_VCC
I2C2_SCL
I2C2_SDA
I2C Address: 0x08
U54
U55
INA220AIDGST
VIN+
VIN-
VCC
GND
VBUS
NC
SDA
SCL
A1
A0
INA_VDD_S_P
INA_VDD_S_N
INA_VDDC_S_P
INA_VDDC_S_N
I2C1_SDA
I2C1_SCL
Current Sense Address = 0x40
Current Sense Address = 0x41
Route P/N sense pair together with small as possible stub to resistor of INA220.
The filter (2 resistors + 0.1uf cap + INA220) need to be placed close to sense resistor .
Always ON 1A
Q6
FDMA908PZ
+3V3_PMIC
+1V0_VDDCORE_PMIC
+CPU_VDD
+CPU_VDDC_PMIC
+GVDD
+G1VDD
+1_2V
+3_3V
+LVDD
+2V5_LIVDD
VCC_O1VDD
VCC_OVDD
DDR3_VREF
DDR3_VTT
PMIC_VHALF
+G1VDD_EN
POR_B
PMIC_STBY_REQ
PMIC_INT_B
I2C1_SDA
I2C1_SCL
I2C2_SDA
I2C2_SCL
ICAP Classification:
FCP:
FIUO:
PUBI: X
Drawing Title:
TWR-LS1021A-PB
Page Title:
POWER SUPPLY (VR500 PMIC)
Size
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Document Number
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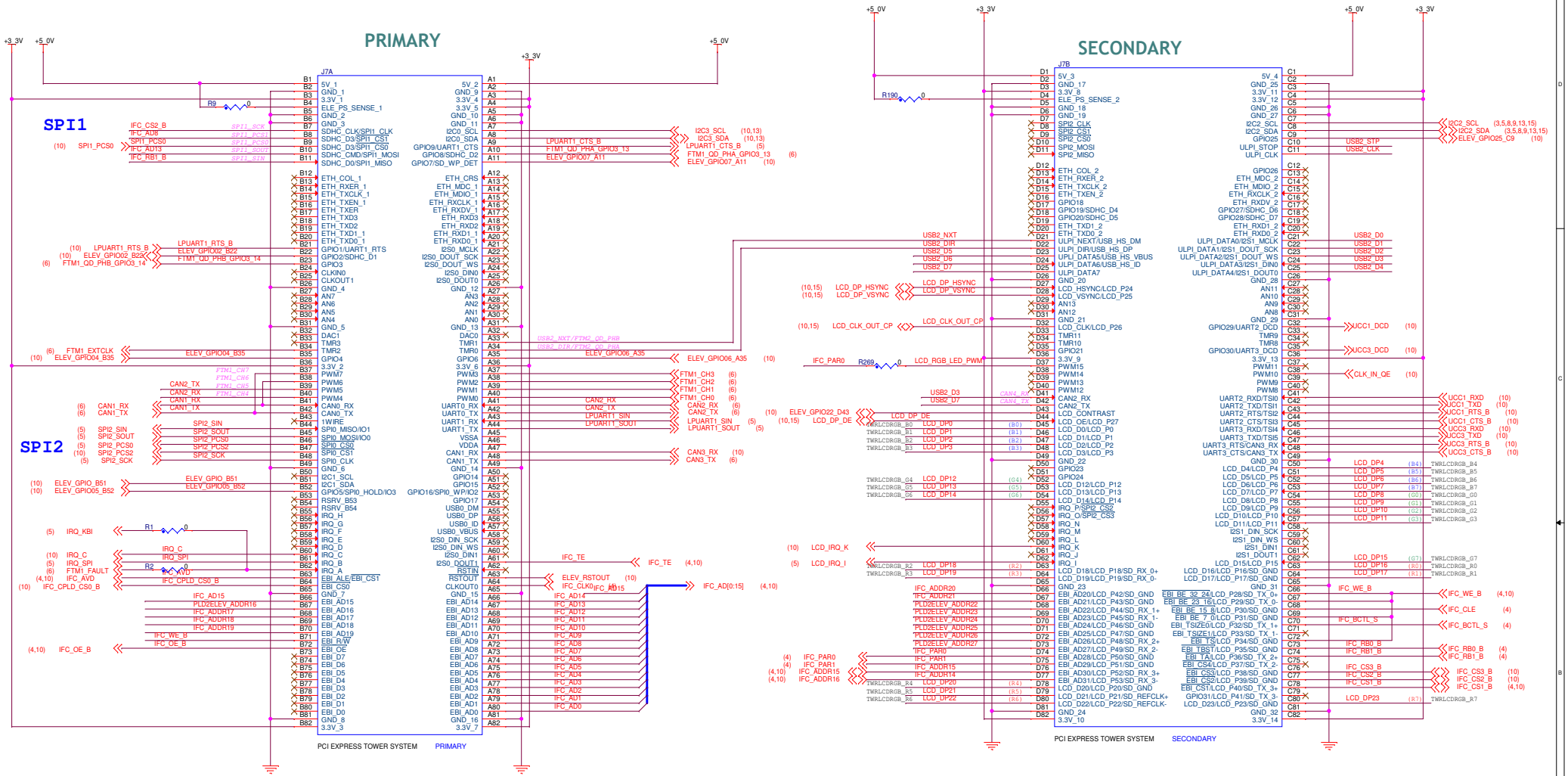
PRIMARY
SECONDARY
SPI1
SPI2
J7A
J7B
PCI EXPRESS TOWER SYSTEM PRIMARY
PCI EXPRESS TOWER SYSTEM SECONDARY
+3_3V
+5_0V
R9 0
R190 0
R269 0
R1 0
R2 0
IFC_CS2_B
IFC_AD8
SPI1_PCS0
IFC_AD13
IFC_RB1_B
SPI1_SCK
SPI1_PCS1
SPI1_PCS2
SPI1_SOUT
SPI1_SIN
LPUART1_RTS_B
ELEV_GPIO02_B22
FTM1_QD_PHB_GPIO3_14
FTM1_EXTCLK
ELEV_GPIO04_B35
CAN2_TX
CAN2_RX
CAN1_RX
CAN1_TX
FTM1_CH7
FTM1_CH6
FTM1_CH5
FTM1_CH4
SPI2_SIN
SPI2_SOUT
SPI2_PCS0
SPI2_PCS2
SPI2_SCK
ELEV_GPIO_B51
ELEV_GPIO05_B52
IRQ_KBI
IRQ_C
IRQ_SPI
FTM1_FAULT
IFC_AVD
IFC_CPLD_CS0_B
IFC_AD15
PLD2ELEV_ADDR16
IFC_ADDR17
IFC_ADDR18
IFC_ADDR19
IFC_WE_B
IFC_OE_B
IFC_RB0_B
IFC_RB1_B
IFC_CS3_B
IFC_CS2_B
IFC_CS1_B
IFC_BCTL_S
IFC_CLE
IFC_TE
IFC_CLK0
IFC_AD15
IFC_AD14
IFC_AD13
IFC_AD12
IFC_AD11
IFC_AD10
IFC_AD9
IFC_AD8
IFC_AD7
IFC_AD6
IFC_AD5
IFC_AD4
IFC_AD3
IFC_AD2
IFC_AD1
IFC_AD0
IFC_AD[0:15]
I2C3_SCL
I2C3_SDA
LPUART1_CTS_B
FTM1_QD_PHA_GPIO3_13
ELEV_GPIO07_A11
ELEV_GPIO06_A35
FTM1_CH3
FTM1_CH2
FTM1_CH1
FTM1_CH0
CAN2_RX
CAN2_TX
LPUART1_SIN
LPUART1_SOUT
CAN3_RX
CAN3_TX
USB2_NXT/FTM2_QD_PHB
USB2_DIR/FTM2_QD_PHA
I2C2_SCL
I2C2_SDA
ELEV_GPIO25_C9
USB2_STP
USB2_CLK
USB2_D0
USB2_D1
USB2_D2
USB2_D3
USB2_D4
UCC1_DCD
UCC3_DCD
CLK_IN_QE
UCC1_RXD
UCC1_TXD
UCC1_RTS_B
UCC1_CTS_B
UCC3_RXD
UCC3_TXD
UCC3_RTS_B
UCC3_CTS_B
LCD_DP_HSYNC
LCD_DP_VSYNC
LCD_CLK_OUT_CP
LCD_RGB_LED_PWM
LCD_DP_DE
LCD_IRQ_K
LCD_IRQ_I
LCD_DP0
LCD_DP1
LCD_DP2
LCD_DP3
LCD_DP4
LCD_DP5
LCD_DP6
LCD_DP7
LCD_DP8
LCD_DP9
LCD_DP10
LCD_DP11
LCD_DP12
LCD_DP13
LCD_DP14
LCD_DP15
LCD_DP16
LCD_DP17
LCD_DP18
LCD_DP19
LCD_DP20
LCD_DP21
LCD_DP22
LCD_DP23
LCD_DP[0:23]
PLD2ELEV_ADDR[22:27]
IFC_ADDR[17:21]
USB2_D[0:7]
IFC_PAR0
IFC_PAR1
IFC_ADDR15
IFC_ADDR16
IFC_ADDR20
IFC_ADDR21
freescale
ICAP Classification: FCP: ___ FIUO: PUBI: X
Drawing Title:
TWR-LS1021A-PB
Page Title:
TWR-ELEV Connectivity
Size C
Document Number SCH-28673 PDF: SPF-28673
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Date: Sunday, May 31, 2015
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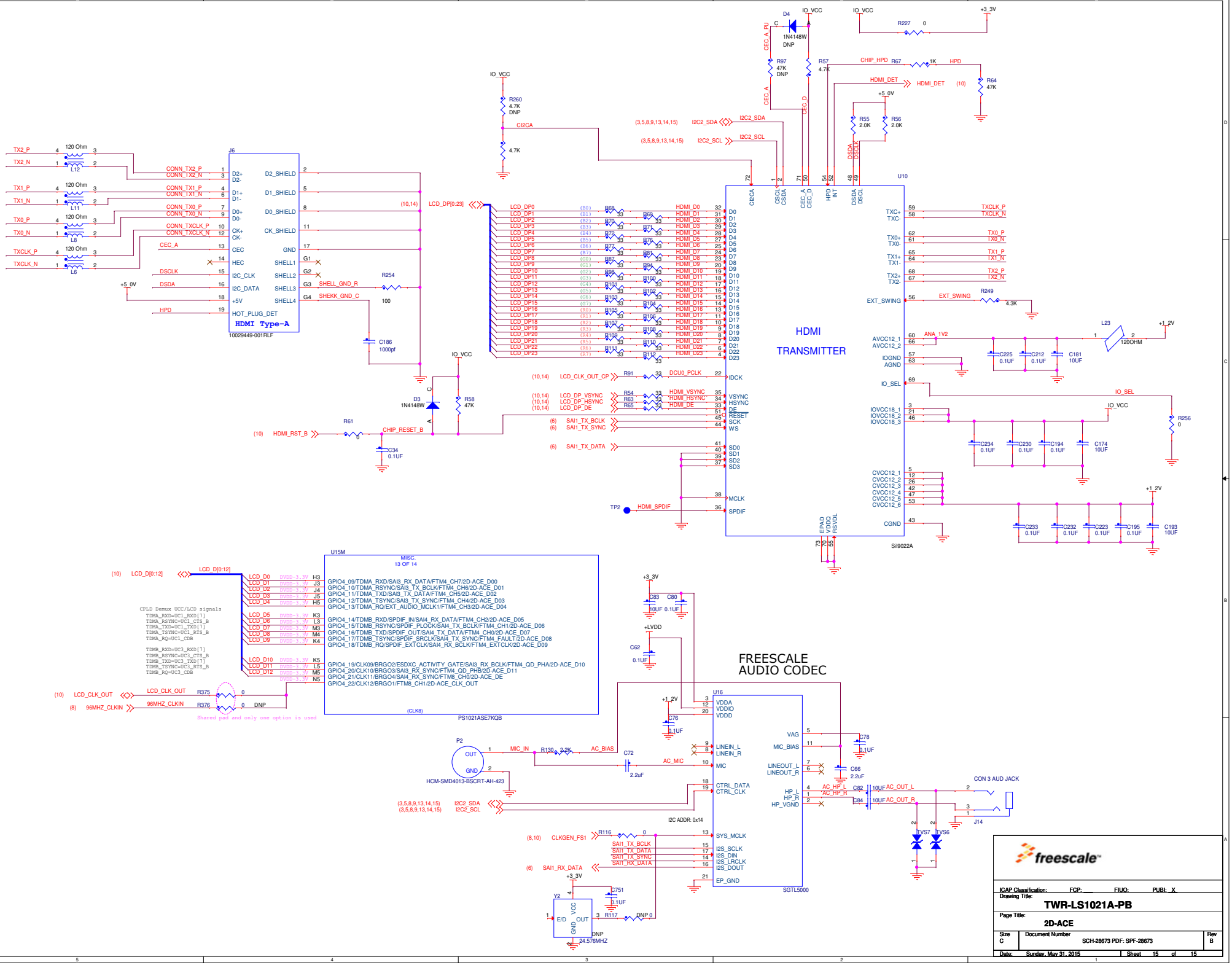
HDMI Type-A
HDMI TRANSMITTER
Sil9022A
FREESCALE AUDIO CODEC
SGTL5000
PS1021ASE7KQB
HCM-SMD4013-BSCRT-AH-423
CON 3 AUD JACK
TWR-LS1021A-PB
2D-ACE
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