# DIANA analog core modeling

This project aims to develop a black-box model as a look-up table for the analog core of the DIANA chip. The model can be used to train the neural network or understand the SoC limitations.

Unit time [50, 140, 10], activation value [-63, 63, 1], and VCSbias [0.61, 0.73, 0.5] are the inputs to the model, and the output is the column readout value. First, a plain model of DIANA’s normal behavior will be delivered. In this model, according to exploration experiments, a look-up table is proposed in which having the input values, the output is determined. This naive model is called the zero-order model in this document. In experiments, an n-row section of the analog array is provided by inputs. The inputs are swept across their valid values, and the average value of 512 columns is stored as the output value. Thus, although the output values are integers [-63,63], the model’s output can be a float number. This is in a probabilistic manner, 20.3 is more likely to be 20, but it may also be 21. In the zero-order model, the differences between the readouts of the columns are due to noise and on-chip variation; modeling the former is not possible, and the latter is different from sample to sample, so considering it is not feasible for a generic model of DIANA.

The n-row sections for each VCSbias are selected in a way to have the maximum output swing for values of unit time and activation without output saturation. A higher dynamic range helps for higher resolution in the model, considering that the accumulation in a column is relatively linear (Figure 1). Also, more rows increase the model’s accuracy by lowering the effect of noises and variations.

Chart, line chart

Description automatically generated

Figure 1 Linear accumulation in columns. The number of inputs with constant value increases causes a relative increase in the output.