Application Note

mifare® Interface Platform

Type Identification Procedure

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CONTENTS

1 ABBREVIATIONS

ATQA	Answer to Request, Type A (2 bytes)
n.a.	not applicable
PCD	13.56MHz Proximity **Reader** (Proximity Coupling Device according to the ISO/IEC 14443)
PICC	Proximity Integrated Circuit Card
REQA	Request Command, Type A
SAK	Select Acknowledge, Type A
SELECT	Select Command, Type A
UID	Unique Identifier

2 INTRODUCTION

This document describes how to differentiate between the members of the MIFARE® interface card IC family. ISO/IEC 14443A-3 describes the initialisation and anticollision procedure, which delivers the chip type information for all MIFARE® chips.

All MIFARE® chips are ISO/IEC 14443A-3 compatible. Therefore already existing applications can easily be extended to operate with newer MIFARE® chips respectively all other ISO/IEC 14443A-3 compatible chips.

This document provides an easy guideline how an ISO/IEC 14443 compatible PCD should handle the MIFARE® chips and how it can distinguish between the different available MIFARE® chip types.

3 MIFARE® AND ISO/IEC 14443

All MIFARE® ICs are compliant to the ISO/IEC 14443 A part 1, part 2 and part3. The T=CL protocol as defined in the ISO/IEC 14443-4 is supported by MIFARE® DESFire, MIFARE® Pro and MIFARE® ProX.

MIFARE® 1K, MIFARE® 4K and MIFARE® ultralight use the MIFARE® Classic Protocol.

The ISO/IEC 14443 consists of:

Part 1: Physical characteristics (physical size of the ISO/IEC 14443 PICC)

Part 2: RF signal & power interface (13.56 MHz, modulation, min. field-strength)
split up into type A (= MIFARE®)and type B

Part 3: Initialisation & anti-collision (Start of communication and PICC select)
split up into type A (= MIFARE®)and type B

Part 4: Transmission protocol (data exchange between PCD and PICCs)

Please refer to the ISO/IEC 14443 for details.

4 MIFARE® CHIP TYPES

4.1 Philips MIFARE® Product Portfolio with its features

	MIFARE® ultralight	MIFARE® Standard 1K	MIFARE® Standard 4K	MIFARE® DESFire	MIFARE® ProX Platform	SmartMX Platform
	MF0 U10/U11	MF1 S50	MF1 S70	MF3 IC D40	P8RF…	P5xD(T)…
CPU	-	-	-	Tangram 80C51	Tangram 80C51	Tangram 80C51
HW Crypto		MIFARE® CRYPTO		DES / 3DES	MIFARE® CRYPTO, DES / 3DES, PKI	MIFARE® CRYPTO, DES,3DES, AES, PKI
EEPROM	512 bit	1 KByte	4 KByte	4 KByte	4/8/16 KByte	4-72 KByte
Contact Interface	n.a.	n.a.	n.a.	n.a.	ISO 7816	ISO 7816
C'less Interface	ISO 14443A					

4.2 Supported ISO layers of the MIFARE® Product Portfolio

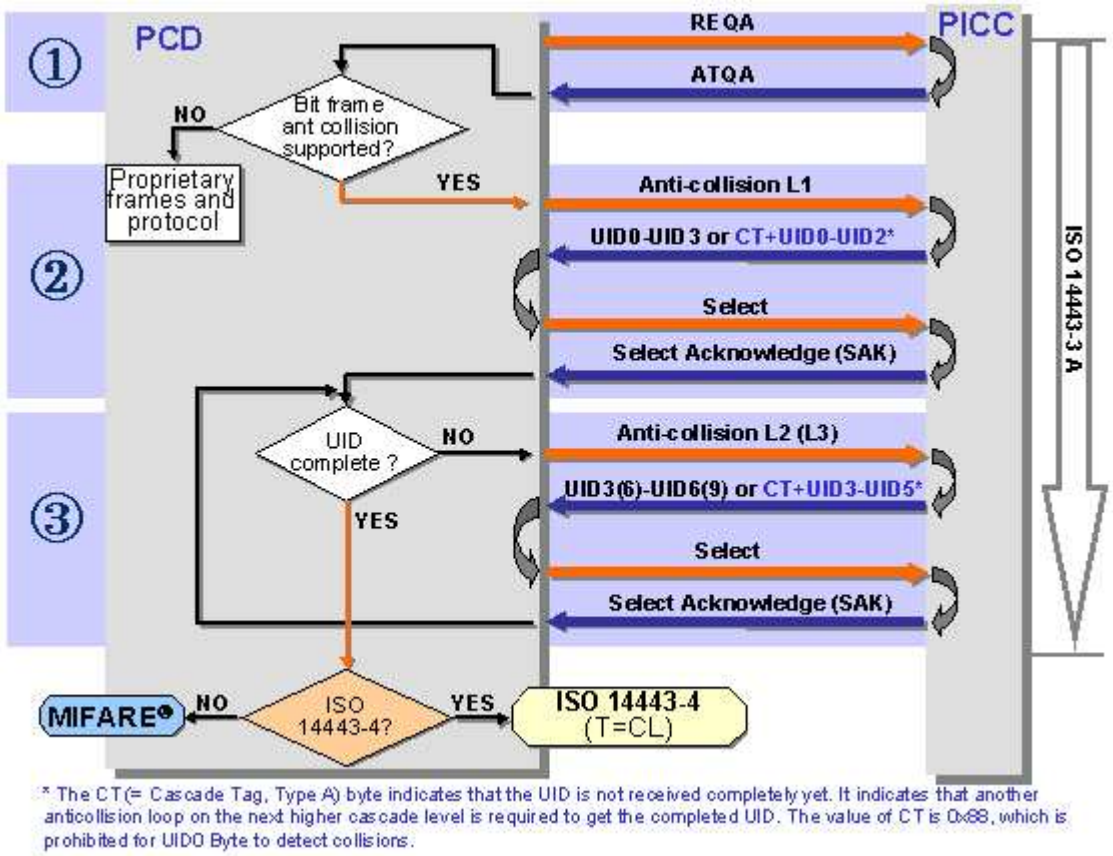
	MIFARE® ultralight	MIFARE® Standard 1K	MIFARE® Standard 4K	MIFARE® DESFire	MIFARE® Pro X Platform	SmartMX Platform
ISO 14443-4 Transmission Protocol	-	-	-	✓ T = CL	✓ T = CL	✓ T = CL
ISO 14443-3 Initialization & Anticollision	✓	✓	✓	✓	✓	✓
ISO 14443-2 RF - Power & Signal Interface	✓	✓	✓	✓	✓	✓
SO 14443-1 Physical Characteristics	✓[1]	✓[1]	✓[1]	✓[1]	✓[1]	✓[1]

[1] Depends on the card manufacturer, as the IC cannot fulfil the physical CARD characteristics of ISO.

5 CHIP TYPE IDENTIFICATION PROCEDURE

The chip type identification has to be handled by the PCD software. As already mentioned the ISO/IEC 144443A-3 defines an initialisation & anticollision procedure according to all existing MIFARE® PICCs, which delivers the necessary information to distinguish between different chip types.

The below mapped flowchart illustrates the initialisation and anticollision procedure.



① The PCD starts the communication with a 'REQA' (Request Command, Type A). The PICC answers with an 'ATQA' (Answer to Request, Type A), which includes

- information whether the PICC supports the bit frame anticollision or not
- information about the UID size
- some proprietary coded information (to be ignored).

② Afterwards the anticollision & select procedure of the first cascade level is handled by the PCD. The PCD sends the 'ANTICOLLISION' command to which the PICC answers with its whole UID in case of a single UID or with a cascade byte plus the first 3 UID bytes in case of a double or triple UID. Subsequently the PCD sends a 'SELECT' command and the PICC answers with a 'SAK' (Select Acknowledge, Type A) which includes

- information whether the UID is already received completely or not
- information whether the PICC supports the ISO/IEC 14443-4 protocol or not
- proprietary coded information
  (indicating the MIFARE® chip type, pls. refer to 5.2)

In case of a single UID the UID is already completely received and the PCD can start a communication according to the supported protocol.
In case of double or triple UIDs a second anticollision & select loop is necessary, see point ③.

③ In case of a double or triple UID another anticollision & select procedure is initiated by the PCD.
The PCD sends the 'ANTICOLLISION' command of the cascade level 2 to which the PICC answers with the rest of its UID in case of a double UID or with a cascade byte plus the second 3 UID bytes in case of a triple UID.
Subsequently the PCD sends a 'SELECT' command and the PICC answers with a 'SAK' which includes

- information whether the UID is already received completely or not
- information whether the PICC supports the ISO/IEC 14443-4 protocol or not
- proprietary coded information
  (indicating the MIFARE® chip type, pls. refer to 5.2)

In case of a double UID the complete UID is received and the PCD can start a communication according to the supported protocol.
In case of a triple UID the PCD finally sends the 'ANTICOLLISION' command of the third cascade level to which the PICC answers with the rest of its UID.
Subsequently the PCD again sends a 'SELECT' command again and the PICC answers with a 'SAK' which includes

- information whether the PICC supports the ISO/IEC 14443-4 protocol or not
- proprietary coded information
  (indicating the MIFARE® chip type, pls. refer to 5.2)

Finally also triple sized UIDs are completely received and the PCD can start a communication according to the supported protocol.

Please also refer to the ISO/IEC 14443-4 and the communication example in the annex for further details.

5.1 Answer to Request, Type A (ATQA)

All MIFARE® chips respond to the ISO/IEC 14443A-3 'REQA' (Request Command, Type A) with the appropriate ATQA (Answer To Request, Type A). The ATQA is two bytes long and contains the information as mapped in the table below.

	MSB ATQA								LSB ATQA							
Bit no.	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
ATQA bit values as defined in the ISO/IEC 14443A-3																
Coding of ATQA according to ISO/IEC 14443A-3	RFU[1]				Proprietary coding				UID size bit frame		RFU[1]	Bit frame anticollision				
Proprietary								1								
Proprietary							1									
Proprietary						1										
Single UID									0	0						
Double UID									0	1						
Triple UID									1	0						
RFU									1	1						
Bit Frame Anticollision supported												1	0	0	0	0
Bit Frame Anticollision supported												0	1	0	0	0
Bit Frame Anticollision supported												0	0	1	0	0
Bit Frame Anticollision supported												0	0	0	1	0
Bit Frame Anticollision supported												0	0	0	0	1
ATQA response values of different MIFARE® chips																
MIFARE® ultralight (0x0044)	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
MIFARE® 1K (0x0004)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
MIFARE® 4K (0x0002)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
MIFARE® DESFire (0x0344)	0	0	0	0	0	0	1	1	0	1	0	0	0	1	0	0
MIFARE® ProX (0xXX08)	0	0	0	0	0	X[2]	X[2]	X[2]	0	0	0	0	1	0	0	0
MIFARE® ProX (0xXX04)	0	0	0	0	0	X[2]	X[2]	X[2]	0	0	0	0	0	1	0	0
MIFARE® ProX (0xXX02)	0	0	0	0	0	X[2]	X[2]	X[2]	0	0	0	0	0	0	1	0
MIFARE® ProX (0xXX48)	0	0	0	0	0	X[2]	X[2]	X[2]	0	1	0	0	1	0	0	0
MIFARE® ProX (0xXX44)	0	0	0	0	0	X[2]	X[2]	X[2]	0	1	0	0	0	1	0	0
MIFARE® ProX (0xXX42)	0	0	0	0	0	X[2]	X[2]	X[2]	0	1	0	0	0	0	1	0
SmartMX xD(T) (0xXX08)	0	0	0	0	0	X[2]	X[2]	X[2]	0	0	0	0	1	0	0	0
SmartMX xD(T) (0xXX04)	0	0	0	0	0	X[2]	X[2]	X[2]	0	0	0	0	0	1	0	0
SmartMX xD(T) (0xXX02)	0	0	0	0	0	X[2]	X[2]	X[2]	0	0	0	0	0	0	1	0
SmartMX xD(T) (0xXX48)	0	0	0	0	0	X[2]	X[2]	X[2]	0	1	0	0	1	0	0	0
SmartMX xD(T) (0xXX44)	0	0	0	0	0	X[2]	X[2]	X[2]	0	1	0	0	0	1	0	0
SmartMX xD(T) (0xXX42)	0	0	0	0	0	X[2]	X[2]	X[2]	0	1	0	0	0	0	1	0

[1] All RFU bits shall be set to '0' according the ISO/IEC 14443A-3.

[2] For the MIFARE® ProX, and SmartMX Dual & Triple Interface ICs any bit combinations in the propriety field are possible.

ISO/IEC 14443A-3 defined bits

Proprietary coded bits

5.2 Select Acknowledge (SAK)

All MIFARE® chips respond to the ISO/IEC 14443A-3 'SELECT' (Select Command, Type A) with the appropriate SAK (Select Acknowledge, Type A). The SAK is one byte long and contains the information as mapped in the table below.

	SAK							
Bit no.	8	7	6	5	4	3	2	1
SAK bit values as defined in the ISO/IEC 14443A-3								
Cascade bit set: UID not complete						1[1]		
UID complete, PICC compliant with ISO/IEC 14443-4			1			0		
UID complete, PICC not compliant with ISO/IEC 14443-4			0			0		
SAK response values of different MIFARE® chips with respect to the ISO/IEC 1443A-3								
MIFARE® ultralight (0x04) – cascade level 1	0	0	0	0	0	1	0	0
MIFARE® ultralight (0x00) – cascade level 2	0	0	0	0	0	0	0	0
MIFARE® 1K (0x08)	0	0	0	0	1	0	0	0
MIFARE® 4K (0x18)	0	0	0	1	1	0	0	0
MIFARE® DESFire (0x24) – cascade level 1	0	0	1	0	0	1	0	0
MIFARE® DESFire (0x20) – cascade level 2	0	0	1	0	0	0	0	0
MIFARE® Pro (0x20) [2]	0	0	1	0[2]	0[2]	0	0	0
MIFARE® Pro (0x08)	0	0	0	0	1	0	0	0
MIFARE® Pro (0x28)	0	0	1	0	1	0	0	0
MIFARE® ProX (0x00)[2]	0	0	0	0[2]	0[2]	X[3]	0	0
MIFARE® ProX (0x20)[2]	0	0	1	0[2]	0[2]	X[3]	0	0
MIFARE® ProX (0x08)	0	0	0	0	1	X[3]	0	0
MIFARE® ProX (0x28)	0	0	1	0	1	X[3]	0	0
MIFARE® ProX (0x18)	0	0	0	1	1	X[3]	0	0
MIFARE® ProX (0x38)	0	0	1	1	1	X[3]	0	0
SmartMX xD(T) (0x00)[2]	0	0	0	0[2]	0[2]	X[3]	0	0
SmartMX xD(T) (0x20)[2]	0	0	1	0[2]	0[2]	X[3]	0	0
SmartMX xD(T) (0x08)	0	0	0	0	1	X[3]	0	0
SmartMX xD(T) (0x28)	0	0	1	0	1	X[3]	0	0
SmartMX xD(T) (0x18)	0	0	0	1	1	X[3]	0	0
SmartMX xD(T) (0x38)	0	0	1	1	1	X[3]	0	0

[1] A set cascade bit within the SAK indicates that the UID is not received completely yet and that another anticollision and select loop using the next higher cascade level has to be executed.

[2] Bit 4 and 5 set to '0' in the 'SAK' of the MIFARE® ProX or SmartMX means that the card does not support the MIFARE® Classic protocol.

[3] Depending on ordered configuration and if applicable on the cascade level.

ISO/IEC 14443A-3 defined bits

Proprietary coded bits

5.3 UID

UID sizes are defined in the ISO/IEC 14443A-3. Double and triple sized UIDs also include the manufacturer code. The manufacturer code itself is defined in the ISO/IEC 7816-6 / AM1 and is 0x04 for Philips.

UID format of double and triple sized UIDs.

UID0	**UID1 – UID6 (resp. UID1 - UID9)**
Manufacturer ID according to the ISO/IEC 7816-6/AM1	Each manufacturer is responsible for the uniqueness of the value of the other bytes of the unique number.

5.4 Overview of the UIDs used for MIFARE®

Overview of UIDs used for MIFARE®		
Single sized UID	**Double sized UID**	**Triple sized UID**
MIFARE® 1K	MIFARE® ultralight	/
MIFARE® 4K	MIFARE® DESFire	/
MIFARE® Pro***X*** (depending on the card OS)	MIFARE® ProX (depending on the card OS)	/
Smart***MX*** (depending on the card OS)	Smart***MX*** (depending on the card OS)	/

6 RELATED INFORMATION

6.1 Additional Documents

Information about the different MIFARE® chips:

- MIFARE® Standard Card IC, MF1ICS50, Functional Specification
- MIFARE® Standard 4 Kbytes Card IC, MF1 IC S70, Functional Specification
- MIFARE® Ultra Light, Contactless Single-trip Ticket IC, MF0 IC U10, Functional Specification
- MIFARE® DESFire, Contactless Multi-Application IC with DES and 3DES Security, MF3 IC D40
- MIFARE® ProX Family Line Sheet and Short Form Specifications
- MIFARE® MF RD700, Command Set, User & Reference Manual
- SmartMX Family Line Sheet and Short Form Specifications

All documents can be downloaded from the Internet at:

www.semiconductors.philips.com/markets/identification/customer/download/

7 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics section of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

8 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so on their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

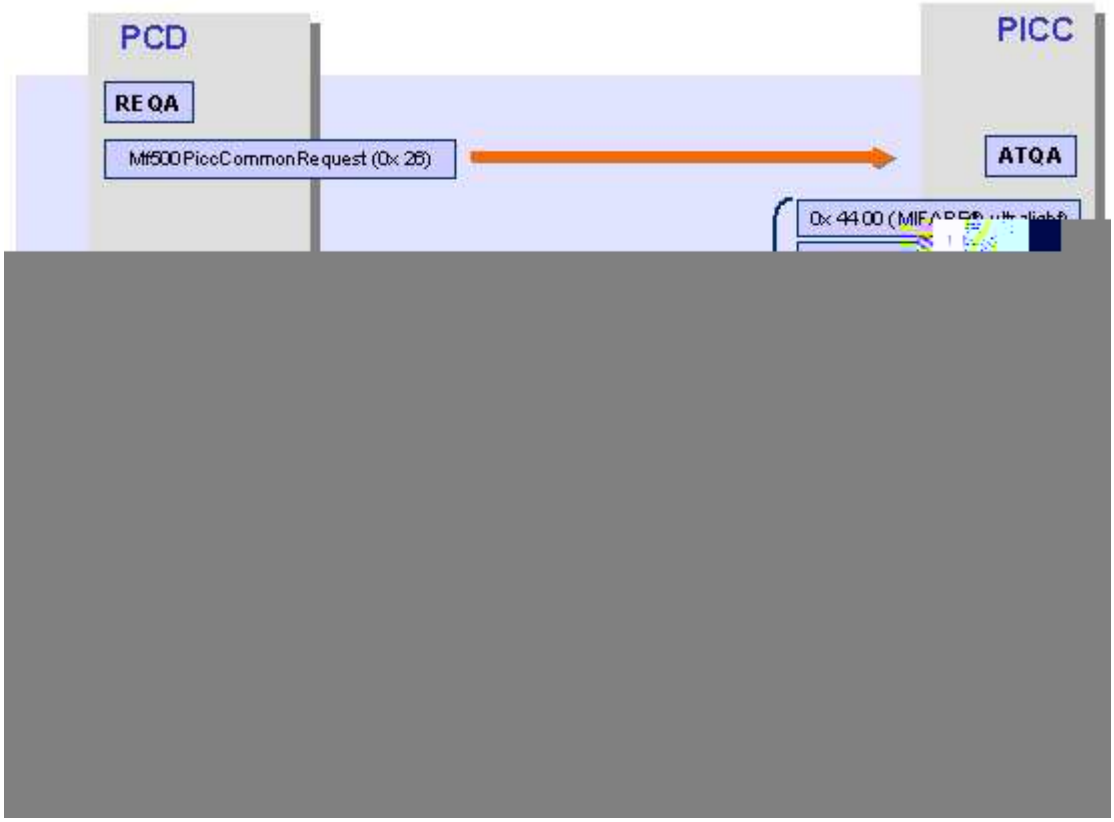
Annex A

This example shows how the Philips MIFARE WND program (using the functions of the MF RD700 of the Pegoda Reader) handles the anticollision & select procedures if following 5 PICCs are in the field:

MIFARE® ultralight (UID: 0x 04 3C B0 00 00 07 00)
MIFARE® 1K (UID: 0x C2 2E 57 32)
MIFARE® 4K (UID: 0x 32 8D A7 9C)
MIFARE® DESFire (UID: 0x 04 00 00 00 00 02 66)
MIFARE® ProX or SmartMX (UID: 0x 20 8E 84 01)

In general the PCD has to poll for PICCs with a 'Request Type A' command. If there are PICCs in the field they answer with their 'Answer to Request, Type A'. The 'ATQA' contains the information whether the bit frame anticollision is supported or not and about the size of the UID.

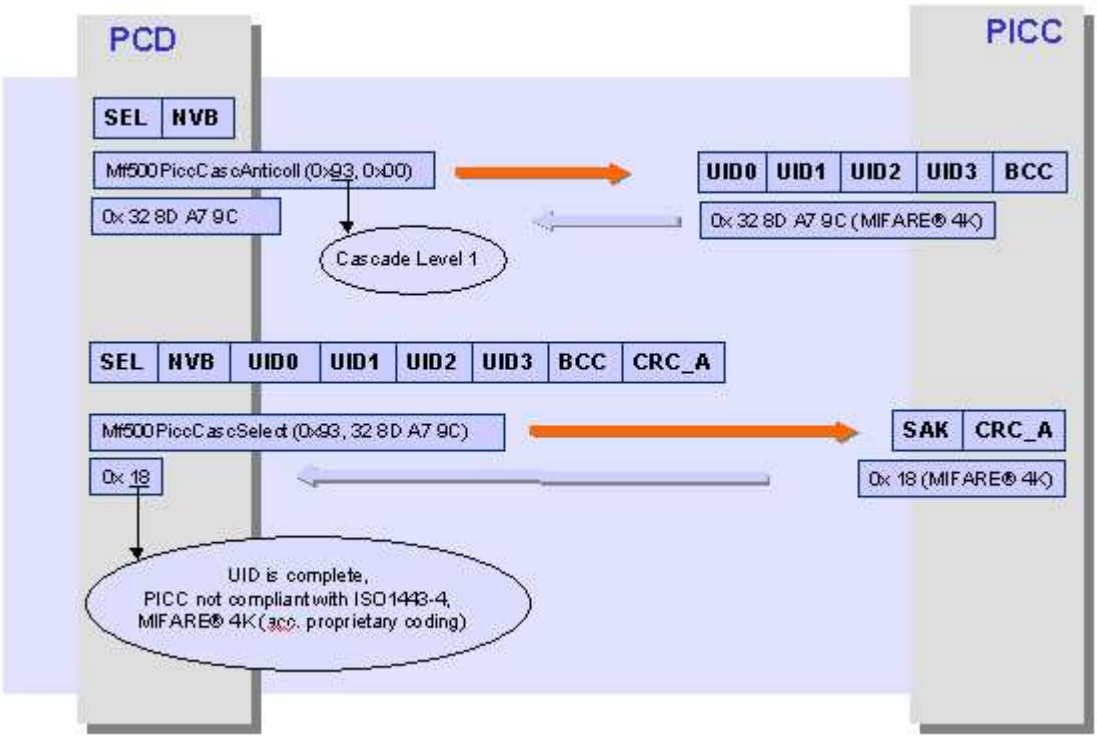
As illustrated below, all five PICCs answer with their 'ATQA'.



The ‘ATQA’ coding indicates that the bit frame anticollision is supported by at least one of the PICCs and therefore a bit frame ‘Anticollision’ can be executed.

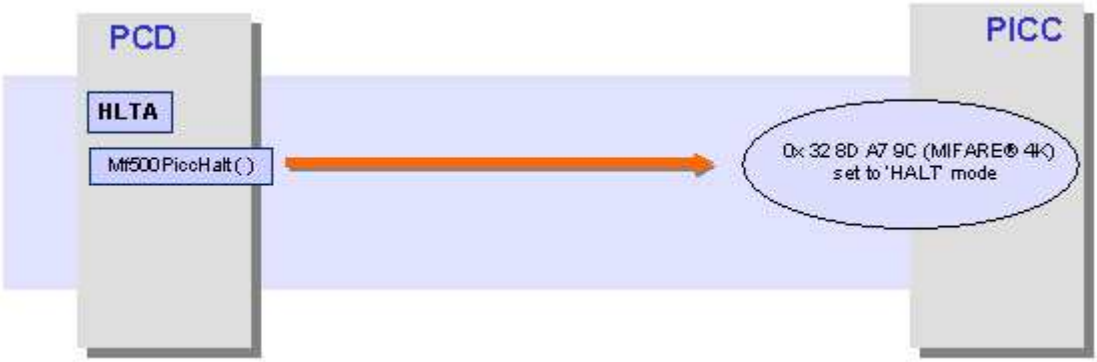
In this example one PICC answers with its whole UID, since the function ‘Mf500PiccAnticoll’ of the MF RD700 solves the whole anticollision procedure automatically.

The PICC has to be selected with its UID.



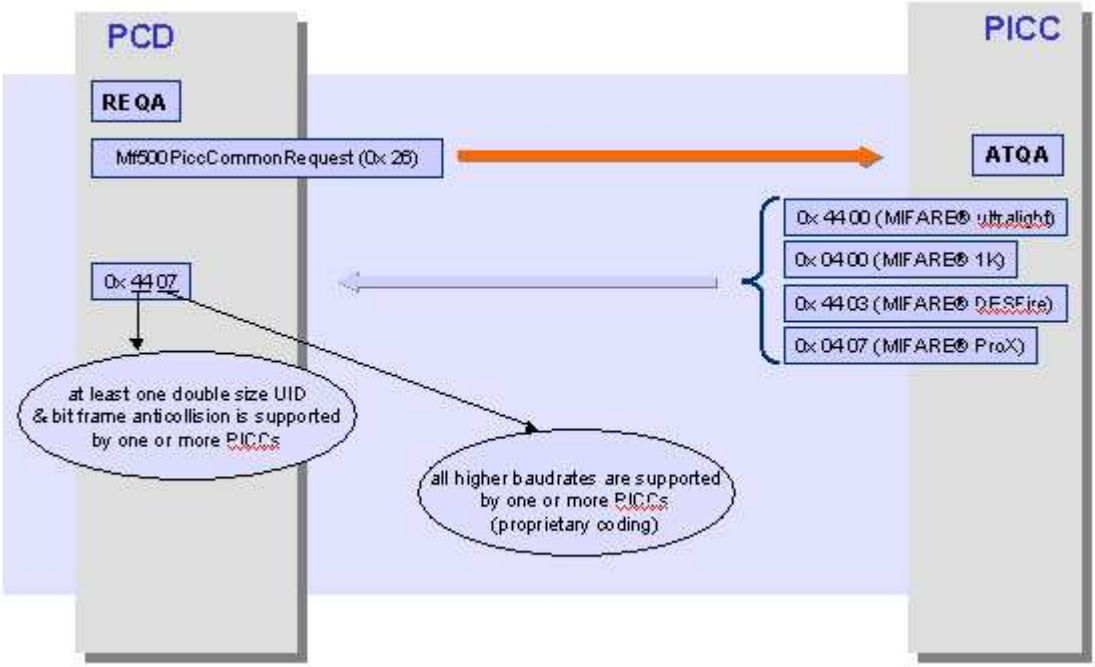
Now it’s up to the PCD to decide whether to further communicate with the PICC or to set it into the ‘HALT’.

In this case the PICC is set into ‘HALT’ mode and it will not respond to following commands anymore.



Now, since the communication with the first PICC is finished another ‘Request Type A’ command is sent to poll for further PICCs.

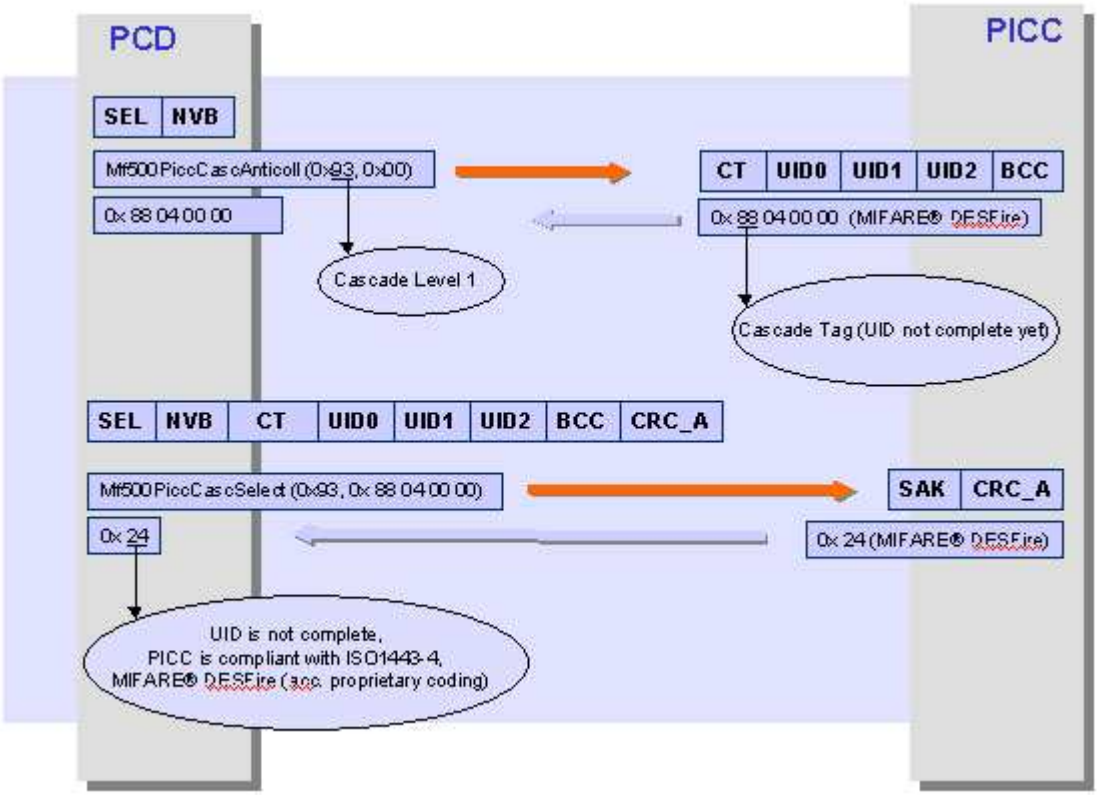
As illustrated below, the remaining four PICCs answer with their ‘ATQA’.



The ‘ATQA’ coding indicates that the bit frame anticollision is supported again and therefore an ‘Anticollision’ can be executed.

One PICC answers with the CT (which indicates that the UID is not completely received yet) and the first part of its UID.

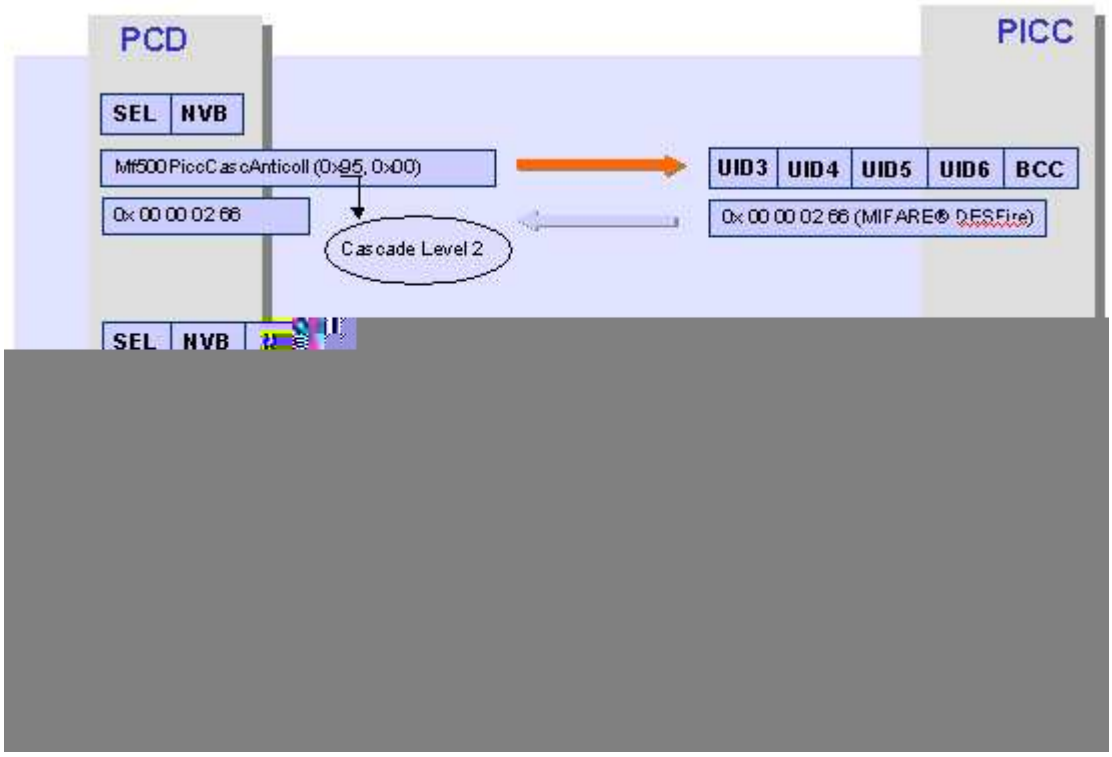
The PICC has to be selected with the first part of its UID.



The ‘SAK’ coding indicates that the UID was not completely received yet and therefore another ‘Anticollision’ loop of the next higher cascade level has to be executed.

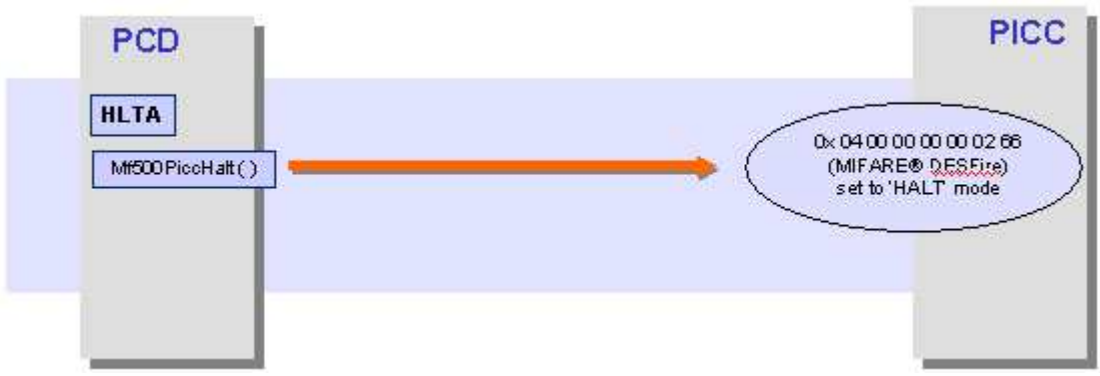
The PICC answers with the rest of its UID.

The PICC has to be selected with the second part of its UID.



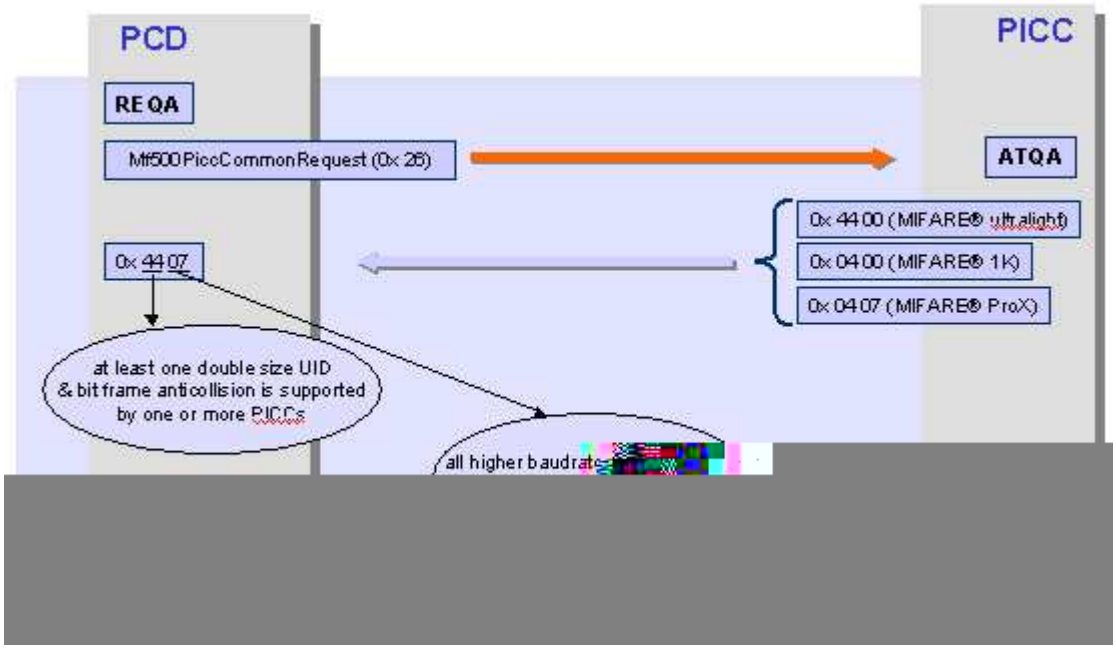
Now it’s up to the PCD to decide whether to further communicate with the PICC or to set it into the ‘HALT’.

In this case the PICC is set into ‘HALT’ mode and it will not respond to following commands anymore.



Now, since the communication with the second PICC is finished another ‘Request Type A’ command is sent to poll for further PICCs.

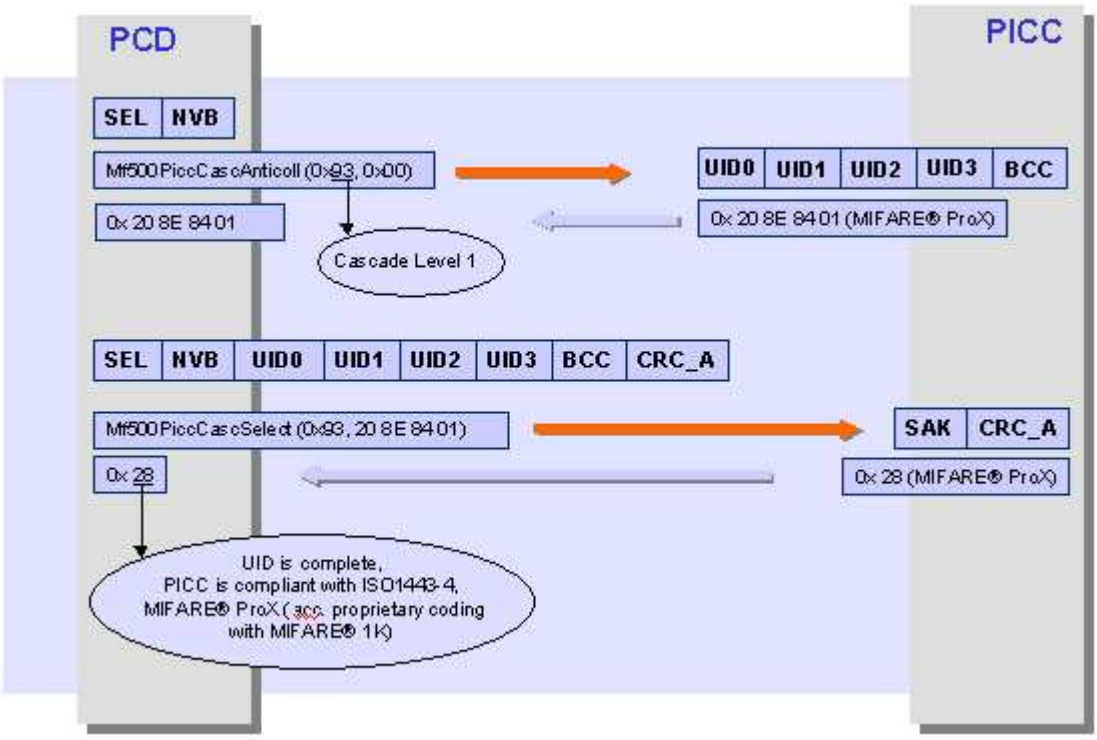
As illustrated below, the remaining three PICCs answer with their ‘ATQA’.



The ‘ATQA’ coding indicates that the bit frame anticollision is supported again and therefore an ‘Anticollision’ can be executed.

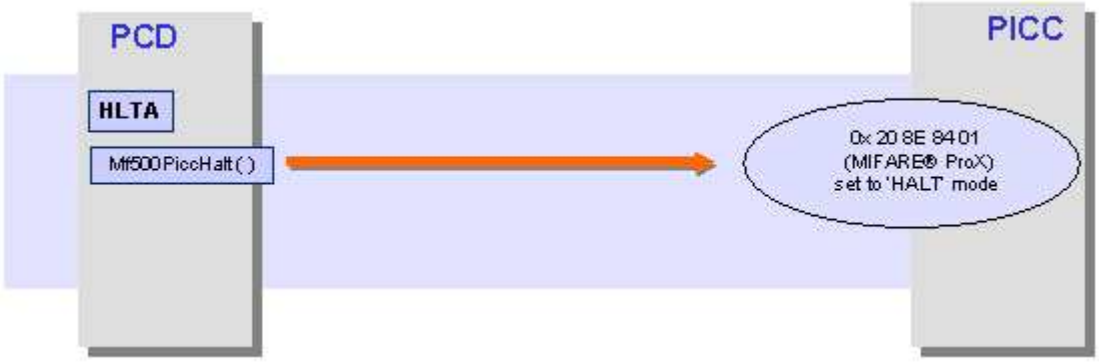
One PICC answers with its whole UID.

The PICC has to be selected with its UID.



Now it’s up to the PCD to decide whether to further communicate with the PICC or to set it into the ‘HALT’.

In this case the PICC is set into ‘HALT’ mode and it will not respond to following commands anymore.



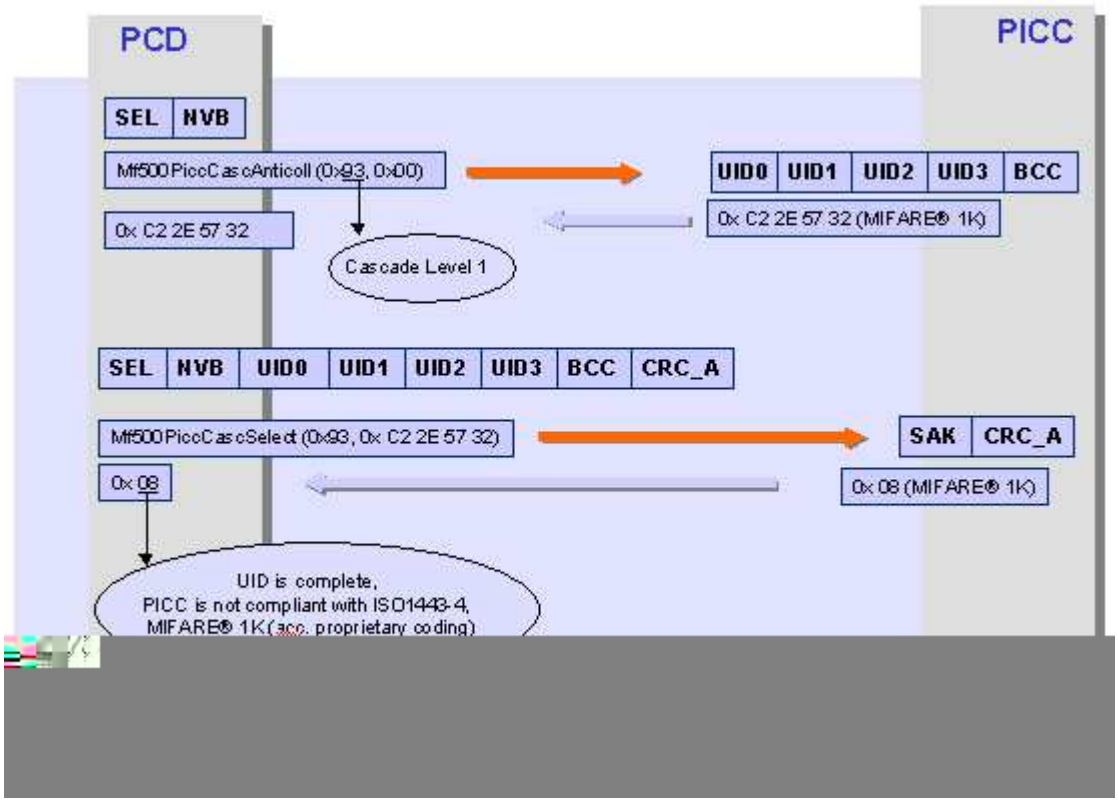
Now, since the communication with the third PICC is finished another ‘Request Type A’ command is sent to poll for further PICCs.

As illustrated below, the remaining two PICCs answer with their ‘ATQA’.

The ‘ATQA’ coding indicates that the bit frame anticollision is supported again and therefore an ‘Anticollision’ can be executed.

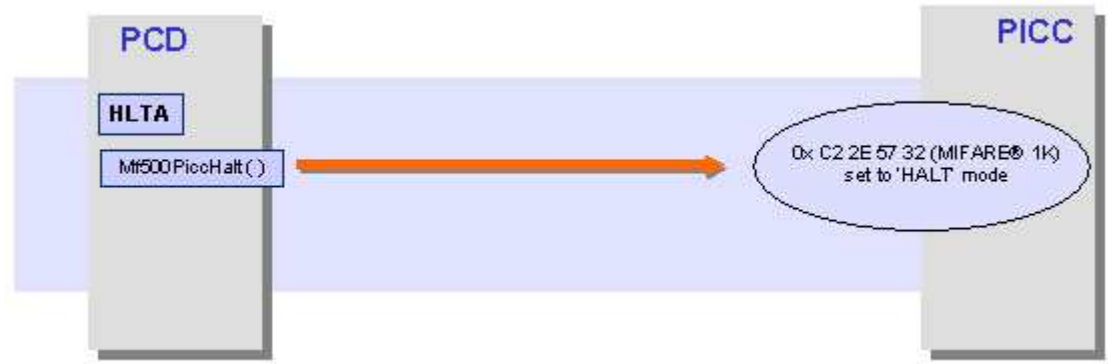
One PICC answers with its whole UID.

The PICC has to be selected with its UID.



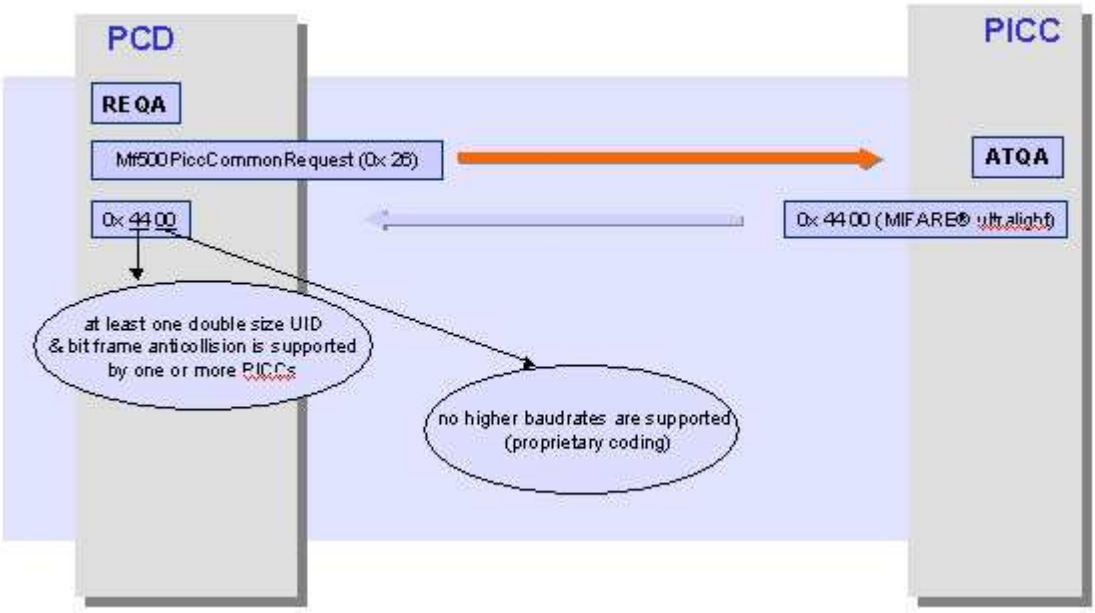
Now it’s up to the PCD to decide whether to further communicate with the PICC or to set it into the ‘HALT’.

In this case the PICC is set into ‘HALT’ mode and it will not respond to following commands anymore.



Now, since the communication with the fourth PICC is finished another ‘Request Type A’ command is sent to poll for further PICCs.

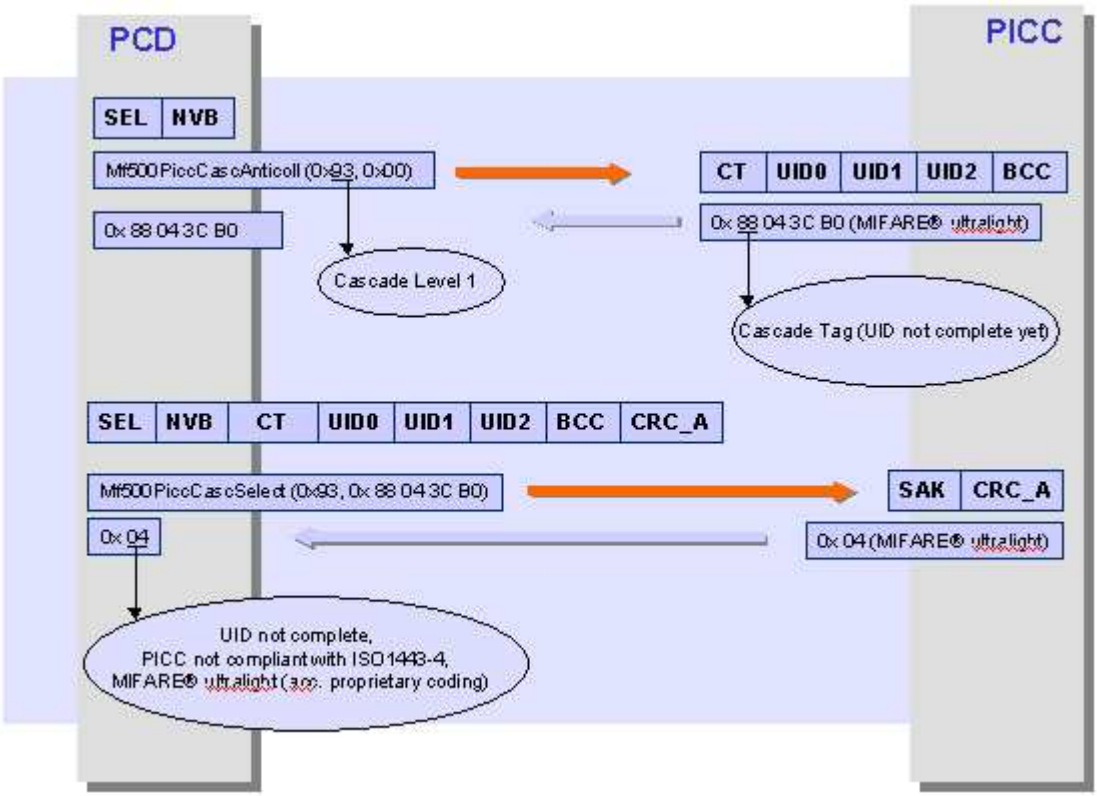
As illustrated below, the remaining PICC answers with its ‘ATQA’.



The ‘ATQA’ coding indicates that the bit frame anticollision is supported again and therefore an ‘Anticollision’ can be executed.

One PICC answers with the CT (which indicates that the UID is not completely received yet) and the first part of its UID.

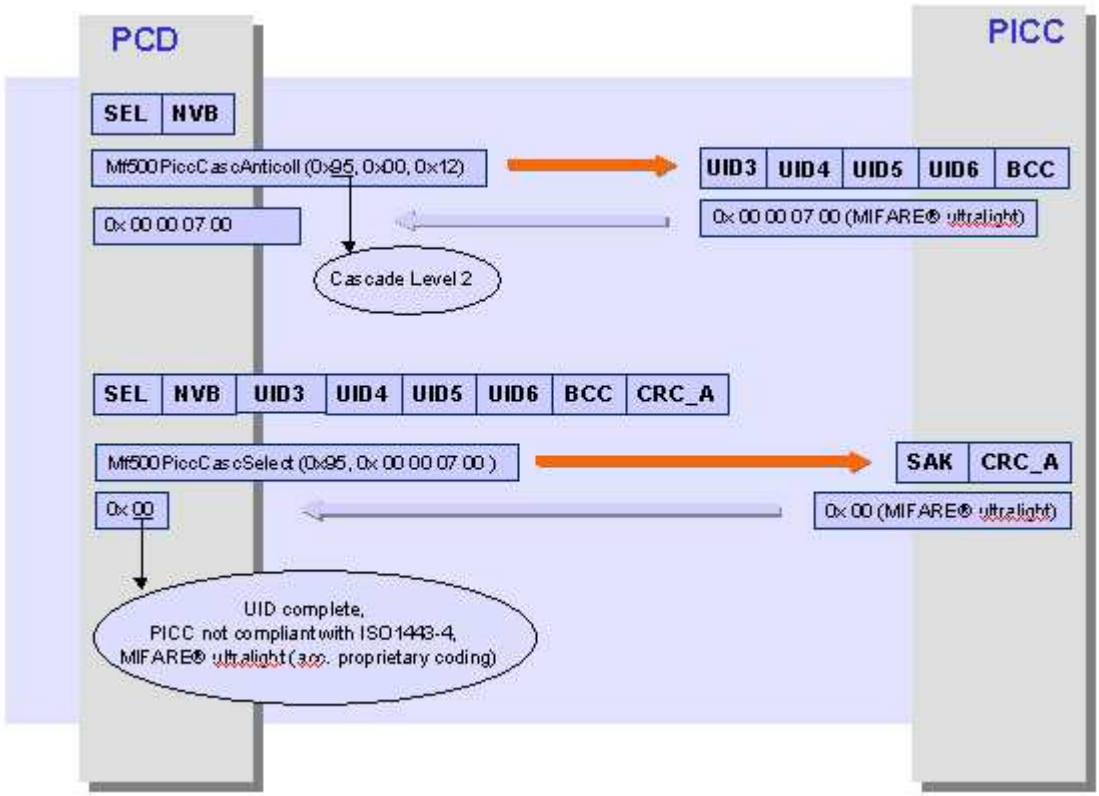
The PICC has to be selected with the first part of its UID.



The ‘SAK’ coding indicates that the UID was not completely received yet and therefore another ‘Anticollision’ loop of the next higher cascade level has to be executed.

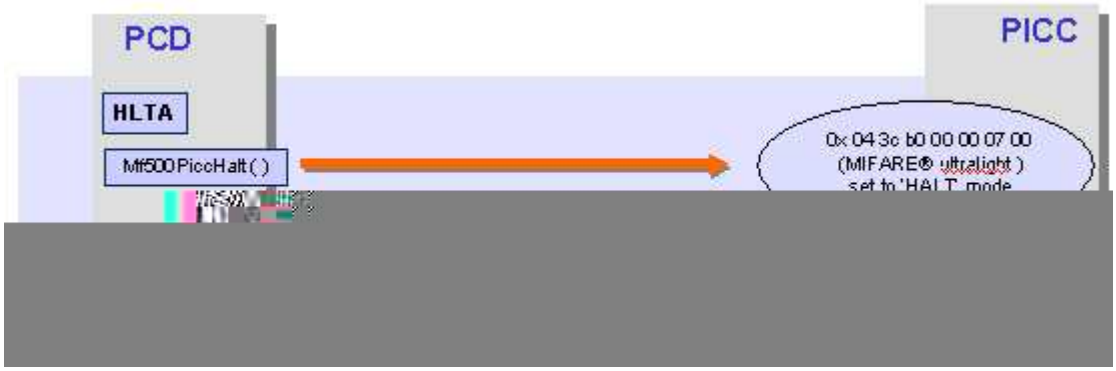
The PICC answers with the rest of its UID.

The PICC has to be selected with the second part of its UID.



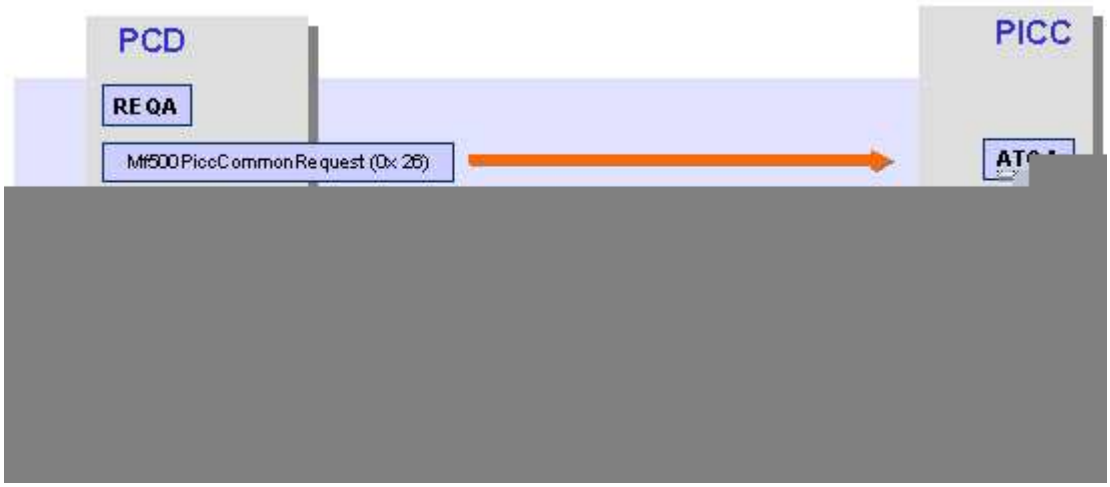
Now it’s up to the PCD to decide whether to further communicate with the PICC or to set it into the ‘HALT’.

In this case the PICC is set into ‘HALT’ mode and it will not respond to following commands anymore.



Now, since the communication with the fifth PICC is finished another ‘Request Type A’ command is sent to poll for further PICCs.

As illustrated below, no PICC is answering since all five PICCs are set to ‘HALT’ and no other PICCs are in the field anymore.



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