### **Control Unit:**

This control unit includes a ROM 32x256.

Each micro operation is set to has at most 8 directed micro programs or more undirected ones.

This structure is architecture to be flexible and to use Mano base computer Assembly language.

### **ROM STRING BITS:**

F1	F2	F3	CD	BR	AD
6	6	6	4	2	8

- 1. This is performed to Mano basic computer (including interrupt and diversity of usable registers).
- 2. Available parts to define new micro operations and micro programs.
- 3.F1, F2 and F3 commands can be used with the minimum conflicts number.

## F1:

000000	NONE
000001	BUS <- M[AR]
000010	BUS <- AR
000011	BUS <- PC
000100	BUS <- DR
000101	BUS <- AC
000110	BUS <- IR
000111	BUS <- TR
001000	CLR AR
001001	CLR PC
001010	CLR DR
001011	CLR TR
001100	INCR AR
001101	INCR PC
001110	INCR DR
001111	INCR TR

The operations are putting on the bus and CLR and INCR registers.

Note that BUS is not a register.

F2:

000000	NONE
000001	M[AR] <- BUS
000010	AR <- BUS
000011	PC <- BUS
000100	DR <- BUS
000101	IR <- BUS
000110	TR <- BUS
000111	FGO <- 1
001000	IEN <- 1
001001	R <- 1
001010	S <- 1
001011	FGO <- 0
001100	IEN <- 0
001101	R <- 0
001110	S <- 0
001111	FGI <- 0

The operations are loading from the bus and changing the value of the flags.

F3:

000000	NONE	
000001	AC <- AC ^ DR	
000010	AC <- AC + DR	
000011	AC <- DR	
000100	AC <- INPR	
000101	AC <- AC'	
000110	AC, E <- SHR(AC, E)	
000111	AC, E <- SHL(AC, E)	
001000	INCR AC	
001001	CLR AC	
001010	E <- 1	
001011	E <- 0	
000101 000110 000111 001000 001001 001010	AC <- AC' AC, E <- SHR(AC, E) AC, E <- SHL(AC, E) INCR AC CLR AC E <- 1	

The operations are related to ALU ,AC and E. Alse changing the value of the E.

## CD:

0000	ALWAYS = 1	
0001	IR(15) = 1	
0010	AC(15) = 1	
0011	AC = 0	
0100	FGI = 1	
0101	R = 1	
0110	S = 1	

It's considered 4 bits to be available to expand conditions.

# BR:

00	JMP	CAR <- AD
01	CALL	CAR <- AD
		SBR <- CAR +1
10	RET	CAR <- SBR
11	MAP	CAR(0-2) <- 0
		CAR(3-8)<-
		OPCODE

Else CAR <- CAR + 1.