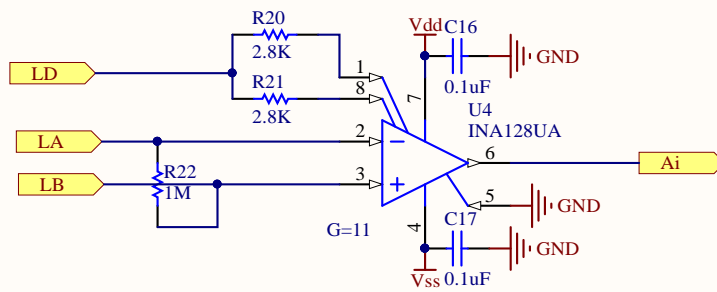
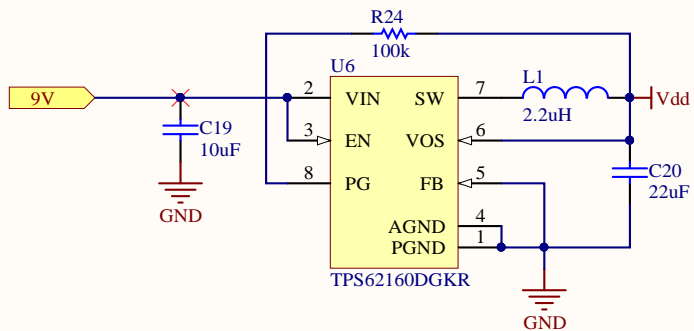


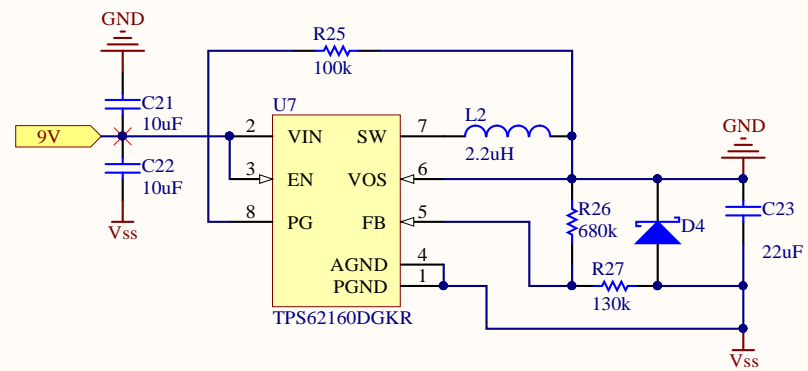
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Date:	10/24/16	Sheet of
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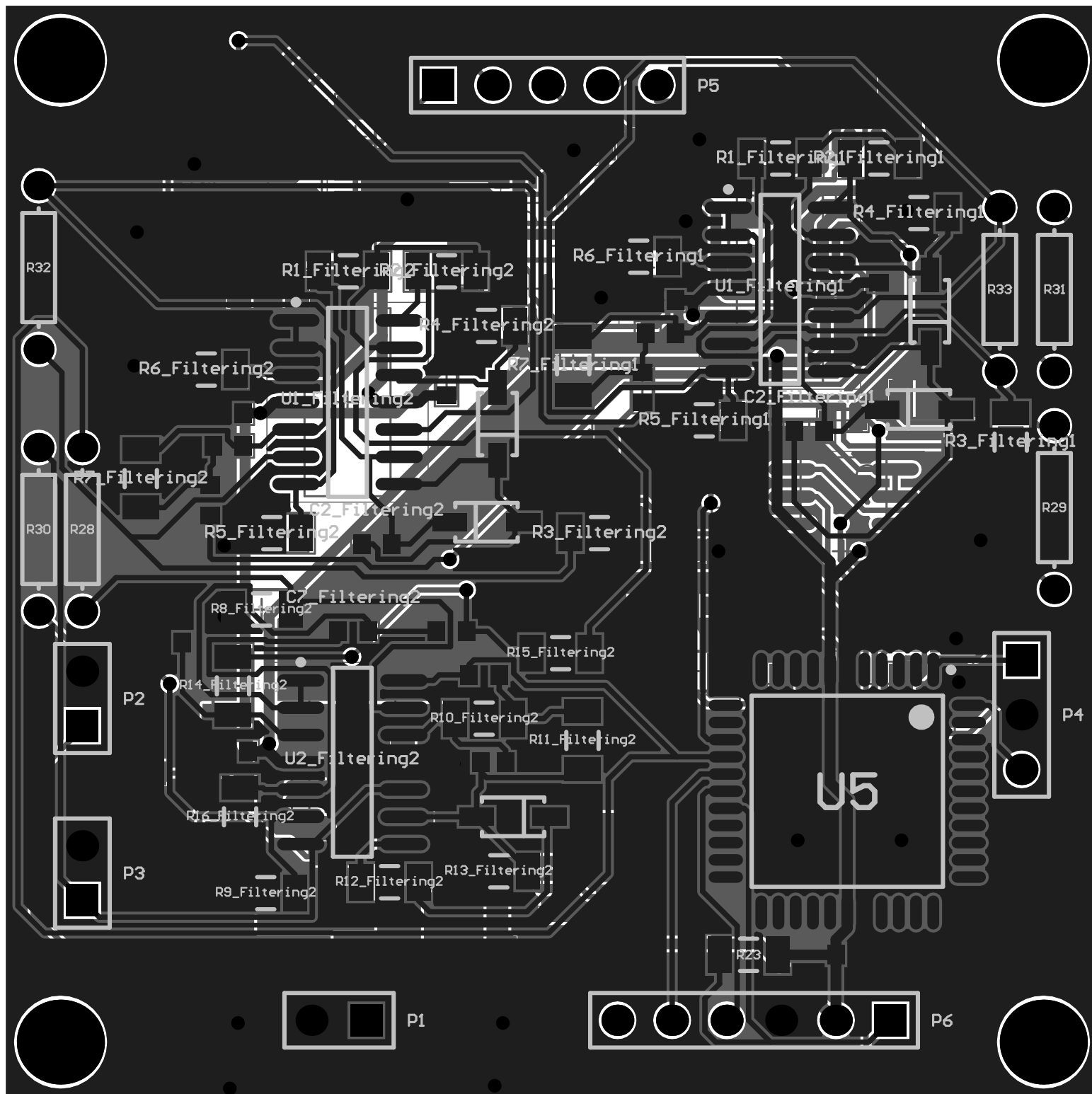
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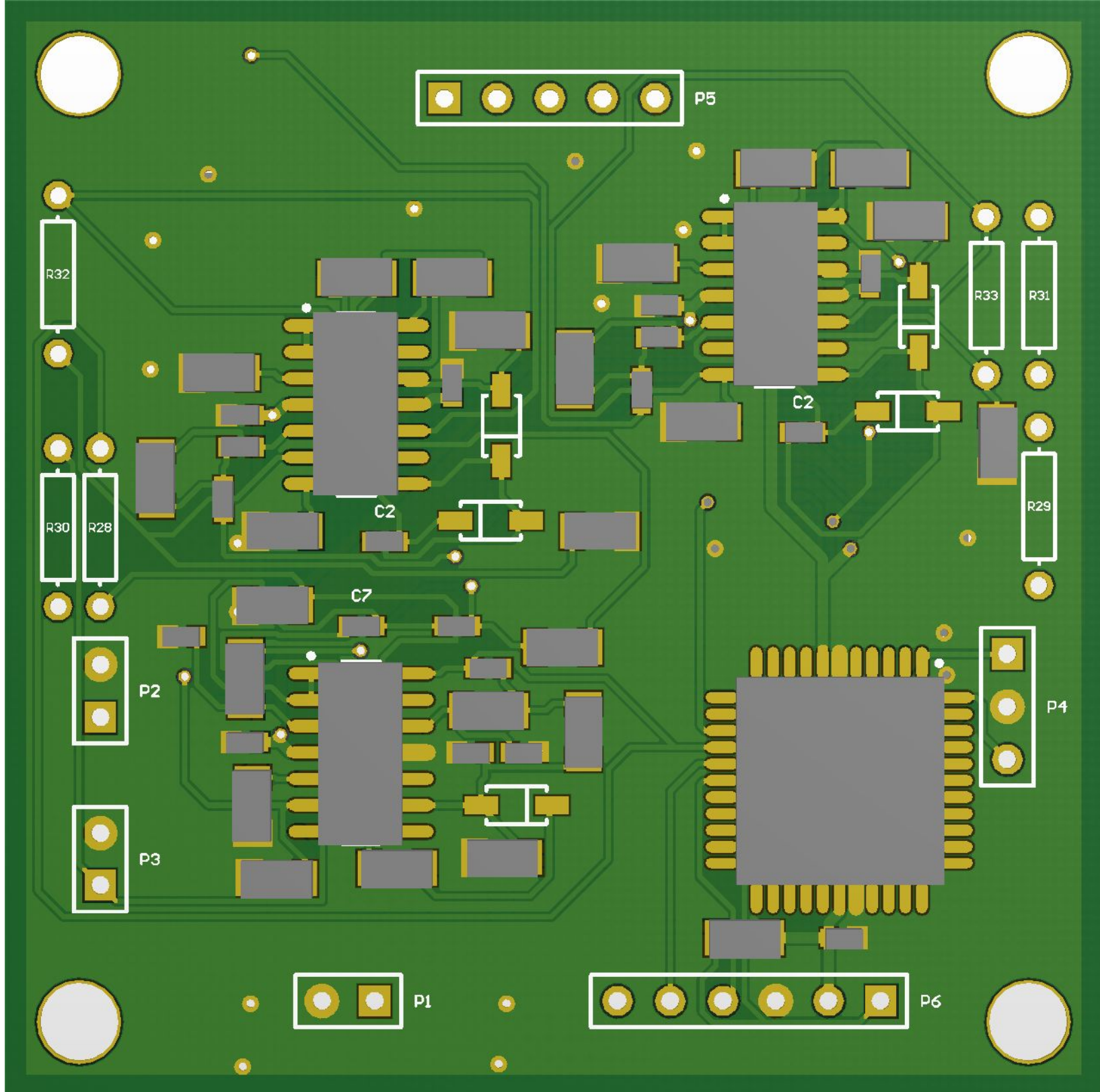


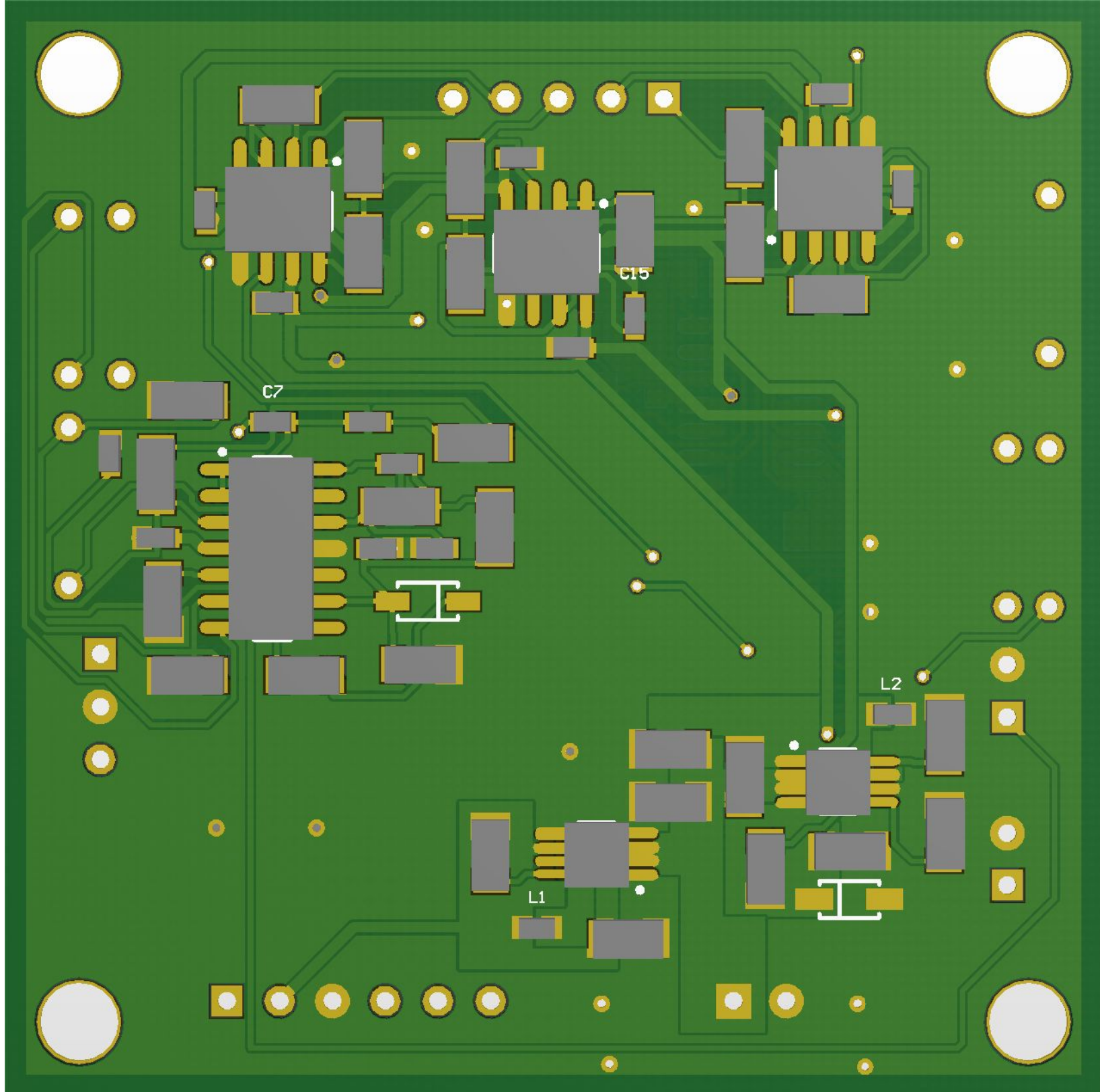
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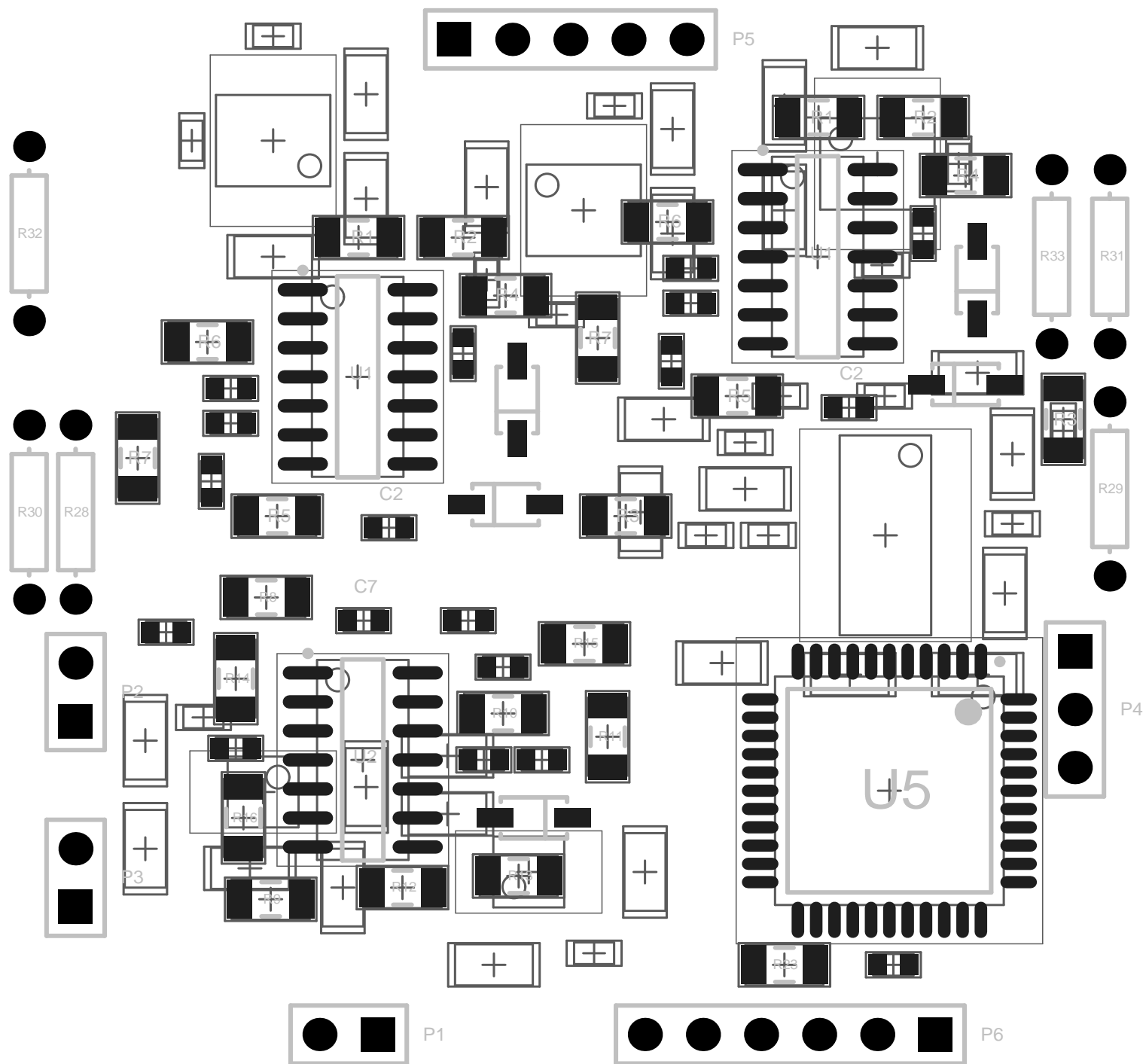


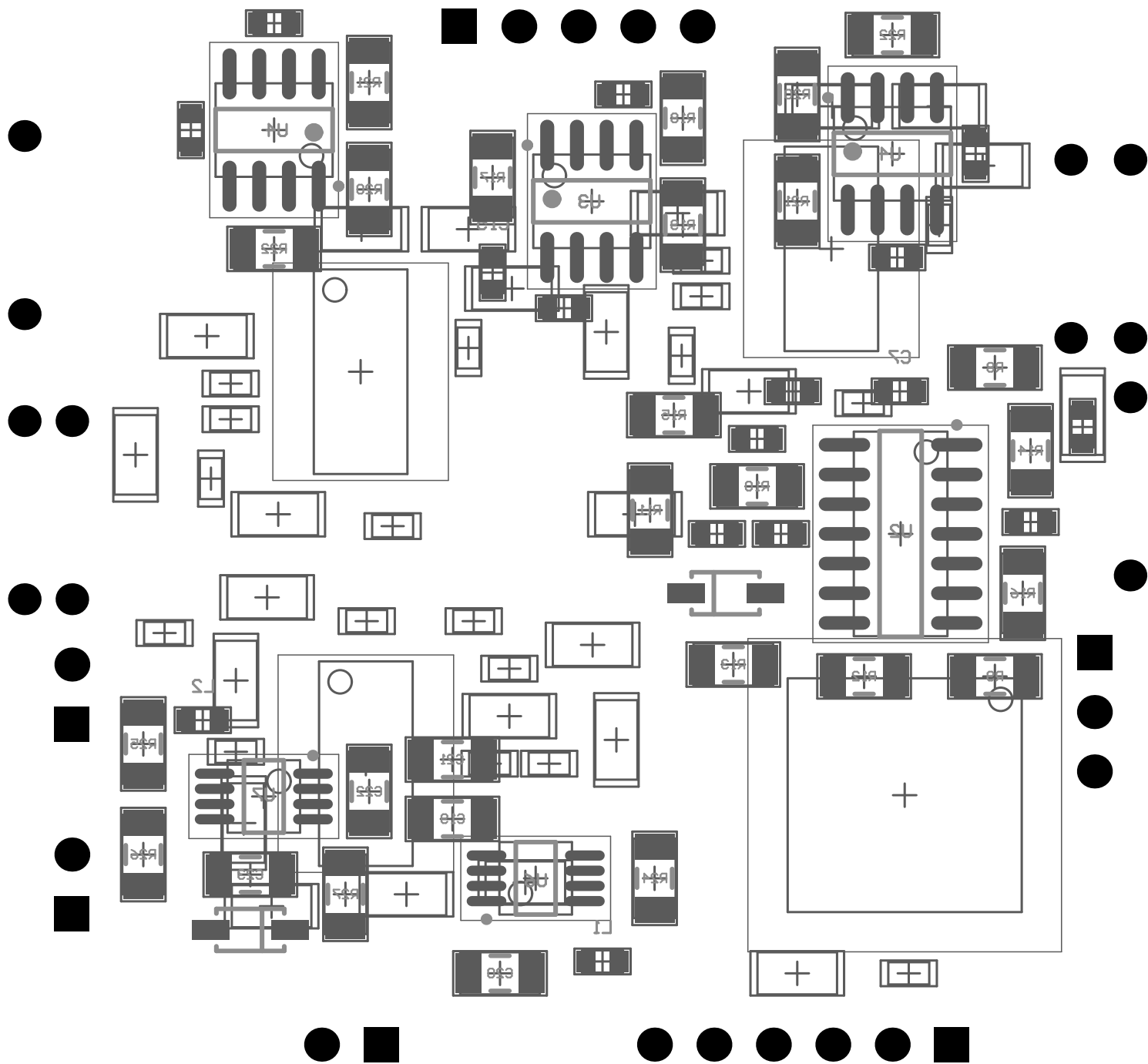
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Size	Number	Revision
A		
Date:	10/24/16	Sheet of
File:	\\.\Vss.SchDoc	Drawn By:











Electrical Rules Check Repor

Class	Document	Message
		Successful Compile for Electronics.PrjPc

Design Rules Verification Report

Filename : \\Mac\Home\Desktop\Duke\BME464\Electronics\Main.PcbDr

Warnings C
Rule Violations C

Warnings	
Total	0

Rule Violations	
Room Neg (Bounding Region = (1200mil, 1280mil, 1880mil, 1773.15m	0
Room Pos (Bounding Region = (1680mil, 1200mil, 2180mil, 1560mi	0
Room Input2 (Bounding Region = (2300mil, 2420mil, 2700mil, 2900m	0
Room Input1 (Bounding Region = (1300mil, 2420mil, 1700mil, 2900m	0
Room Drive (Bounding Region = (1774.409mil, 2340mil, 2227.559mil, 2800m	0
Room Main (Bounding Region = (920mil, 2940mil, 3080mil, 3040mi	0
Room Power2 (Bounding Region = (1153.78mil, 1313.07mil, 2180.001mil, 2613.07m	0
Room Filtering1 (Bounding Region = (1945.591mil, 1680mil, 2971.811mil, 2820m	0
Room Digital (Bounding Region = (2240.709mil, 1180mil, 2820.709mil, 1840m	0
Width Constraint (Min=10mil) (Max=20mil) (Preferred=20mil) (InNet('GND	0
Width Constraint (Min=10mil) (Max=20mil) (Preferred=20mil) (InNet('VDD	0
Width Constraint (Min=10mil) (Max=20mil) (Preferred=20mil) (InNet('VSS	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Net Antennae (Tolerance=0mil) (All)	0
Silk to Silk (Clearance=2mil) (All),(All)	0
Silk To Solder Mask (Clearance=5mil) (Disabled)(IsPad),(All)	0
Minimum Solder Mask Sliver (Gap=1mil) (All),(All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Hole Size Constraint (Min=1mil) (Max=150mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Preferred=500mil) (All)	0
Width Constraint (Min=10mil) (Max=20mil) (Preferred=10mil) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=20mil) (Conductor Width=10mil) (0
Clearance Constraint (Gap=5mil) (All),(All)	0
Un-Routed Net Constraint ((All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
SMD Neck-Down Constraint (Percent=100%) (All)	0
Total	0