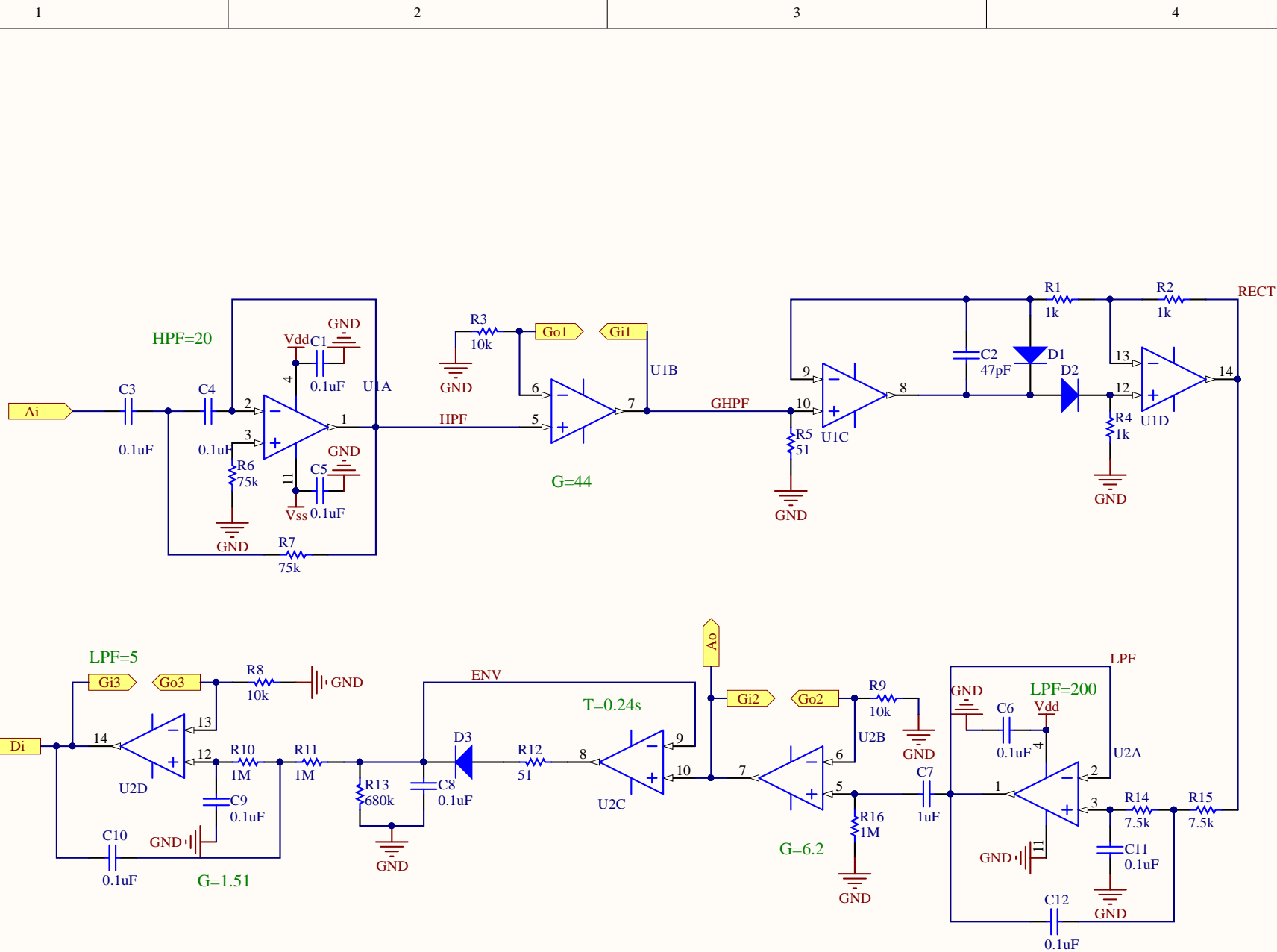
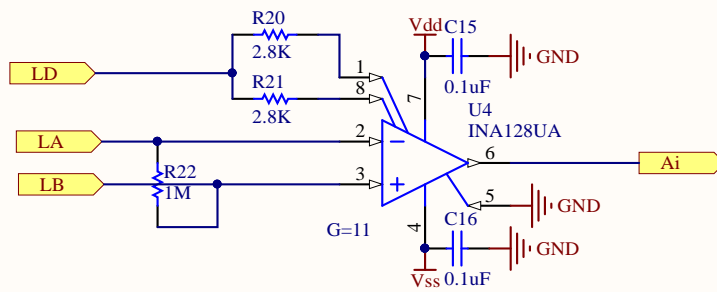


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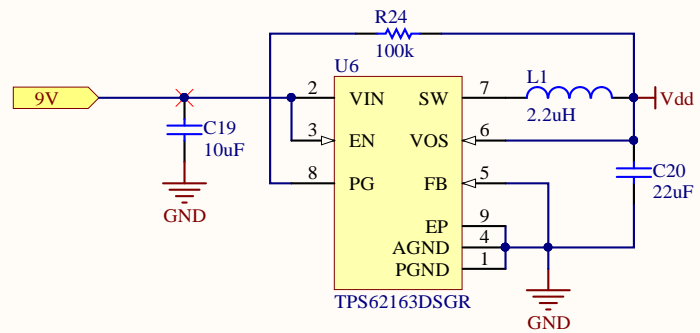


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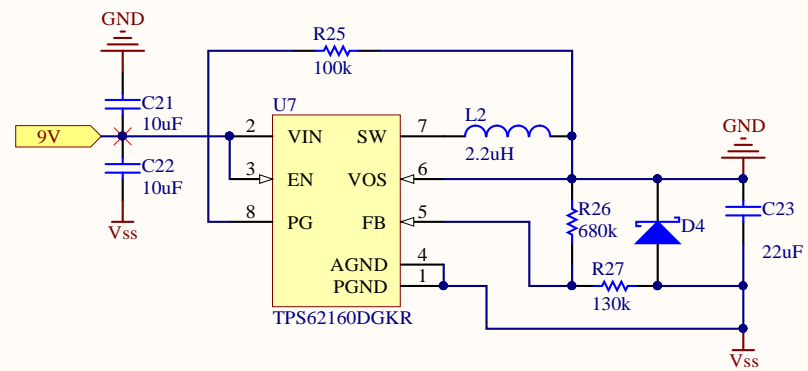


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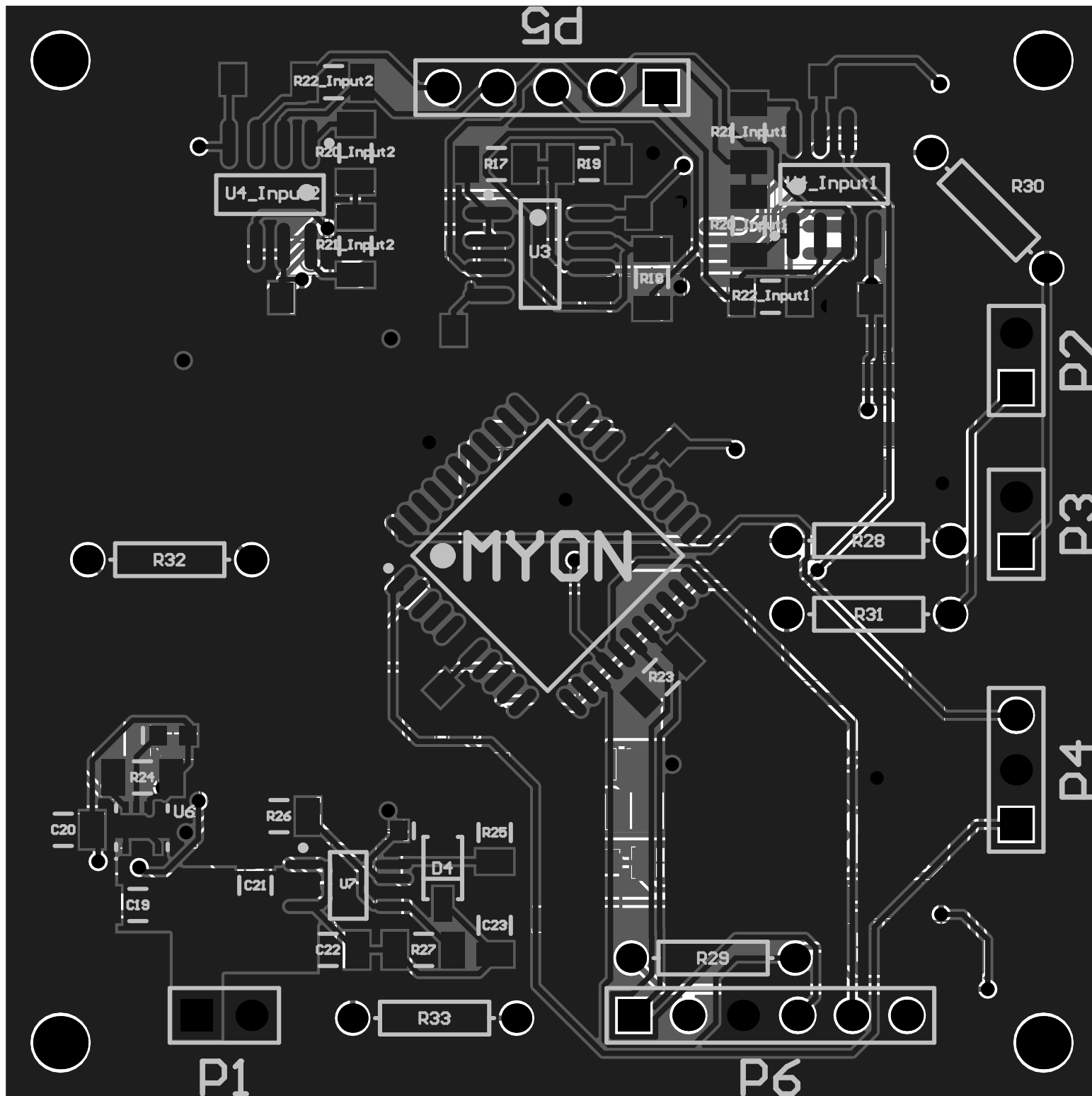




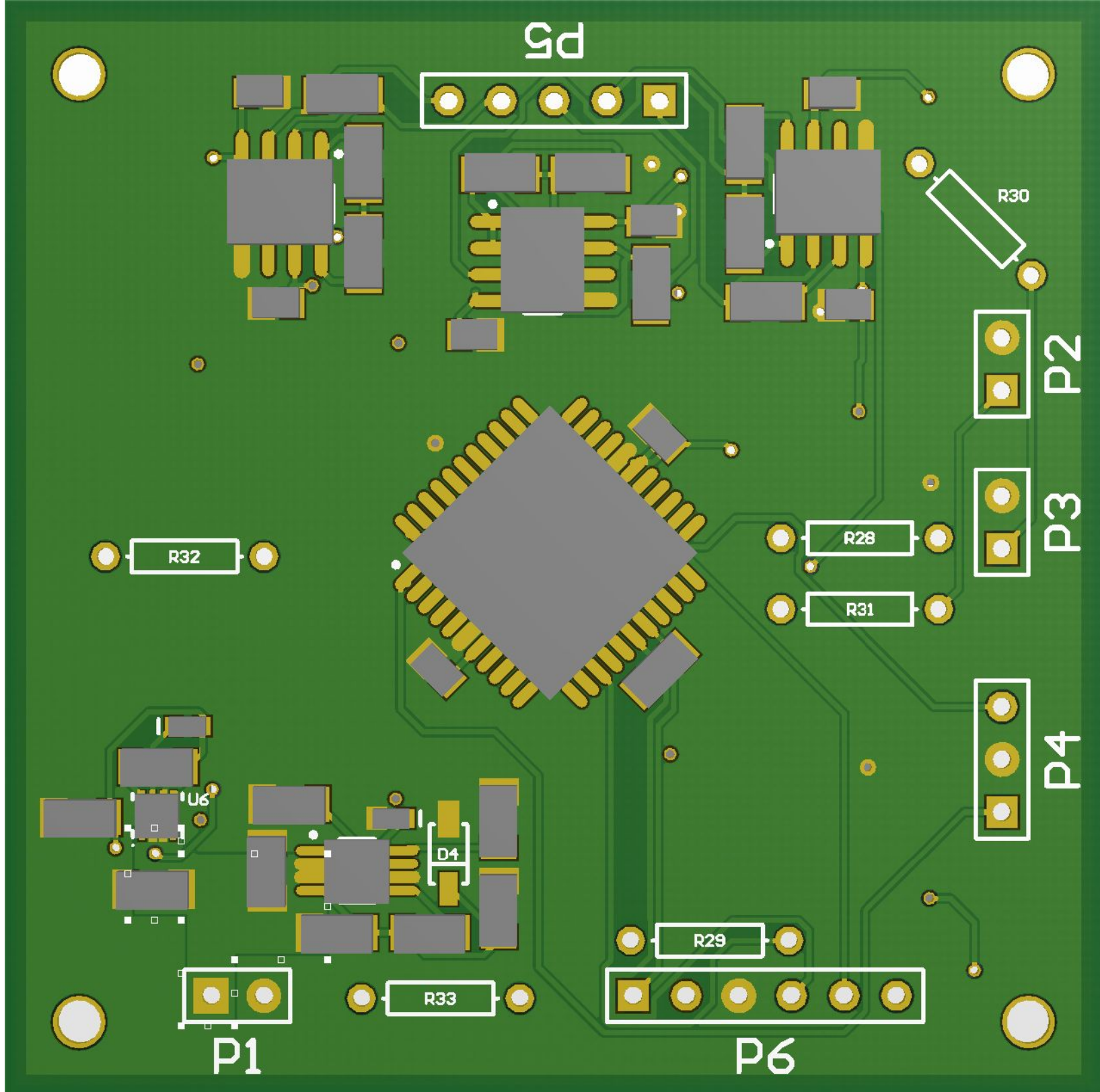
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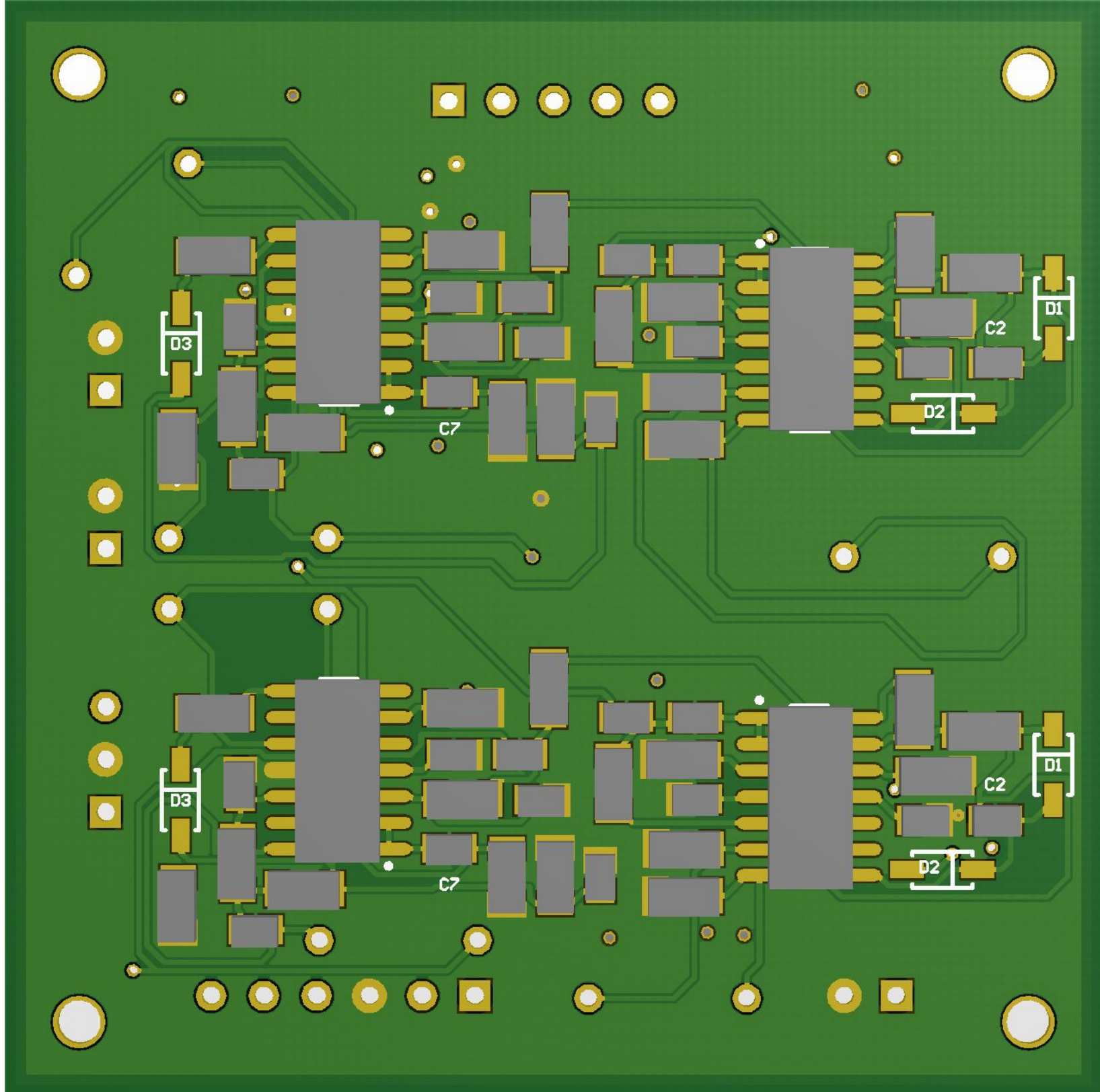


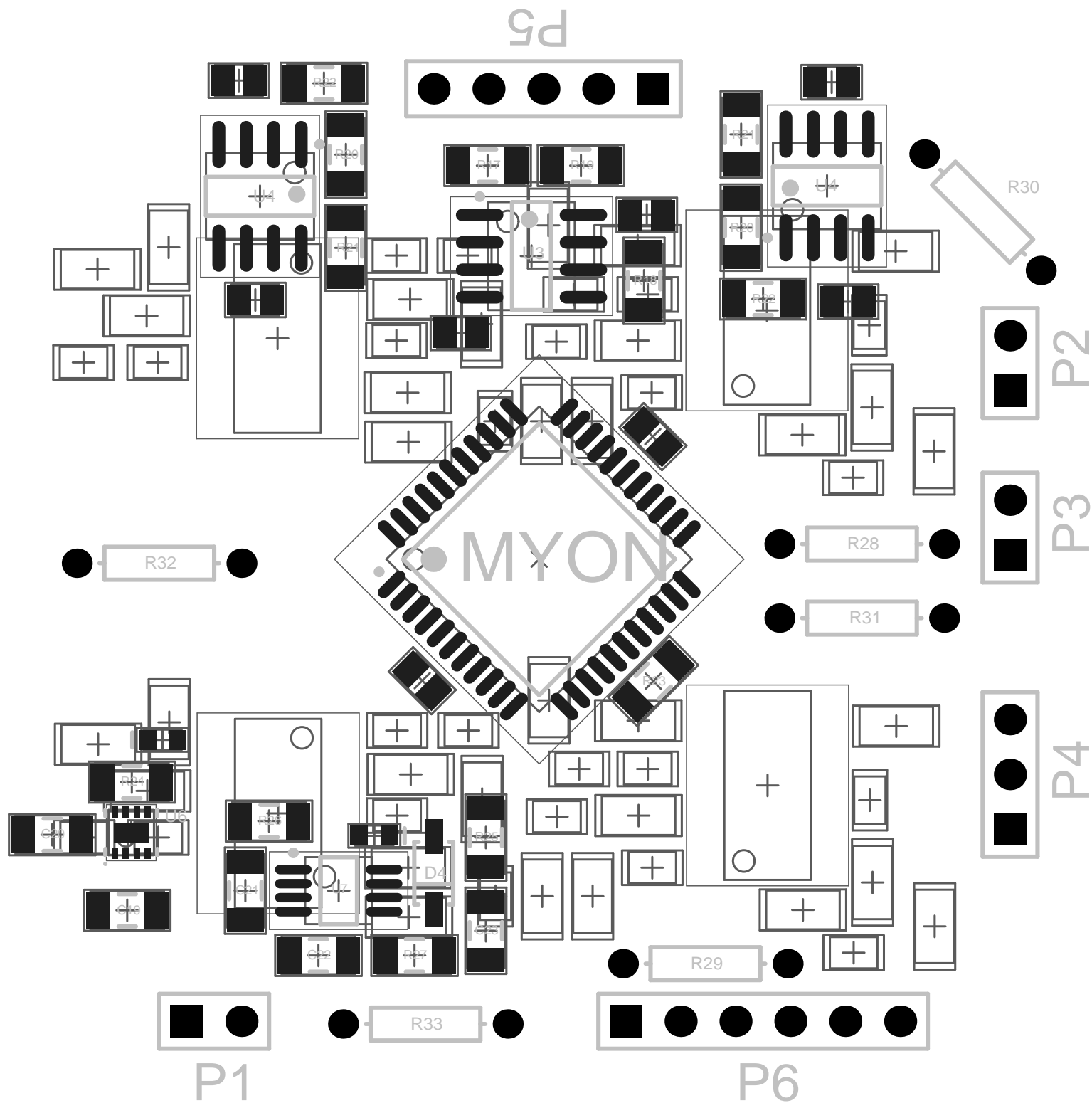
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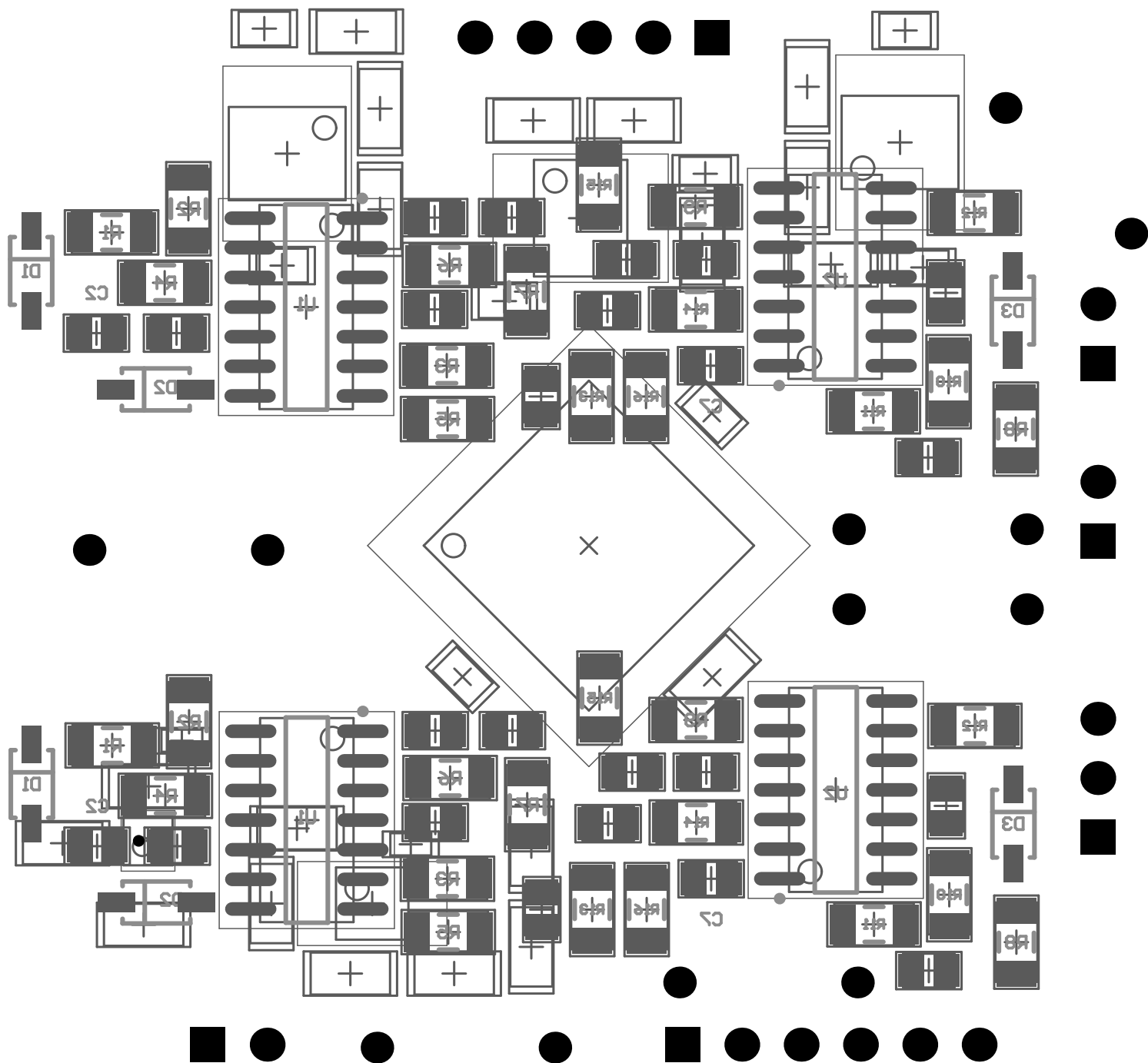












**Electrical Rules Check Repor**

Class	Document	Message
		Successful Compile for Electronics.PrjPc

## Design Rules Verification Report

Filename : \\Mac\Home\Desktop\Duke\BME464\Electronics\Main.PcbDr

Warnings C  
Rule Violations C

Warnings	
Total	0

Rule Violations	
Room Pos (Bounding Region = (1015mil, 1302.323mil, 1392mil, 1719m	0
Room Neg (Bounding Region = (1410mil, 1225mil, 1945mil, 1570mi	0
Room Common (Bounding Region = (3030mil, 2094mil, 3070mil, 2812m	0
Room Input2 (Bounding Region = (1370mil, 2425mil, 1690mil, 2910m	0
Room Input1 (Bounding Region = (2310mil, 2416.85mil, 2630mil, 2901.85m	0
Room Drive (Bounding Region = (1748.15mil, 2360mil, 2253.15mil, 2769m	0
Room Digital (Bounding Region = (1604.121mil, 1610.879mil, 2374.121mil, 2380.879m	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Net Antennae (Tolerance=0mil) (All)	0
Silk to Silk (Clearance=2mil) (All),(All)	0
Silk To Solder Mask (Clearance=5mil) (Disabled)(IsPad),(All)	0
Minimum Solder Mask Sliver (Gap=1mil) (All),(All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Hole Size Constraint (Min=1mil) (Max=150mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Preferred=500mil) (All)	0
Width Constraint (Min=10mil) (Max=20mil) (Preferred=10mil) (All)	0
Power Plane Connect Rule(Direct Connect )(Expansion=20mil) (Conductor Width=10mil) (All)	0
Clearance Constraint (Gap=5mil) (All),(All)	0
Un-Routed Net Constraint (All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
SMD Neck-Down Constraint (Percent=100%) (All)	0
Room Filtering2 (Bounding Region = (993.89mil, 2101mil, 2763.89mil, 2691m	0
Room Filtering1 (Bounding Region = (995mil, 1235mil, 2765mil, 1825m	0
Total	0