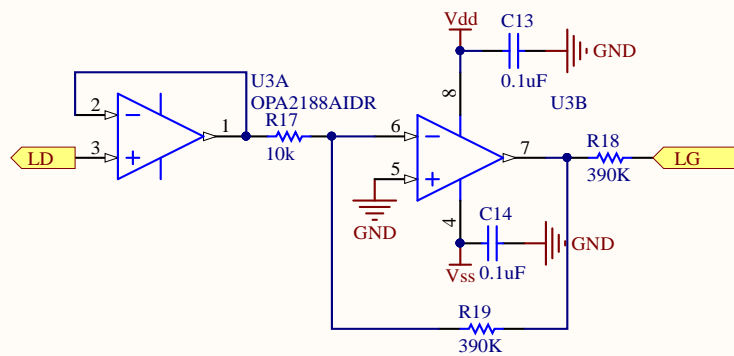
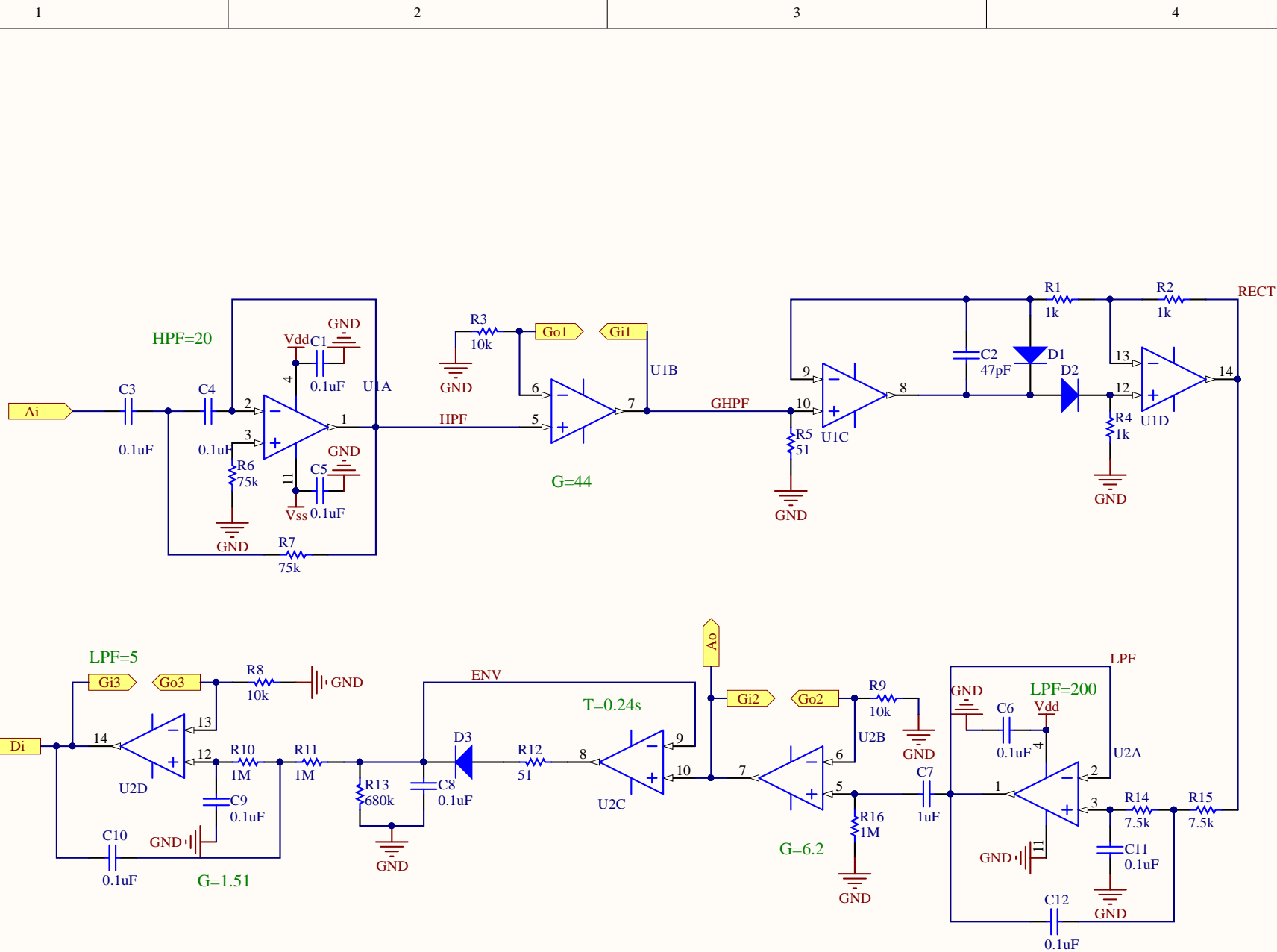


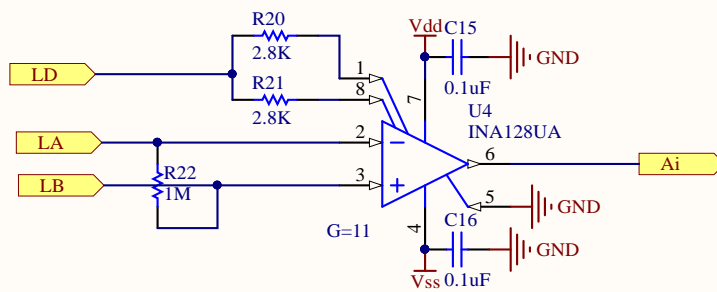
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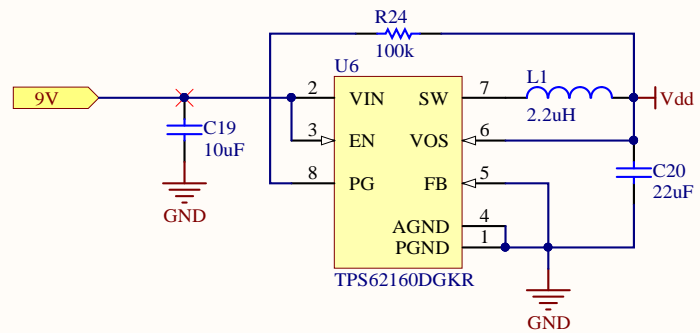
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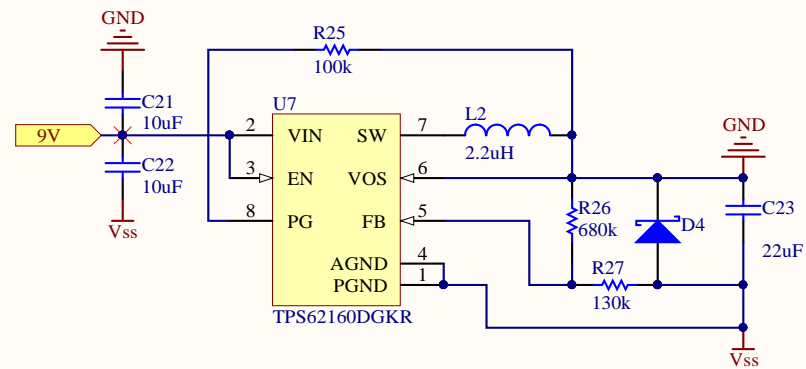
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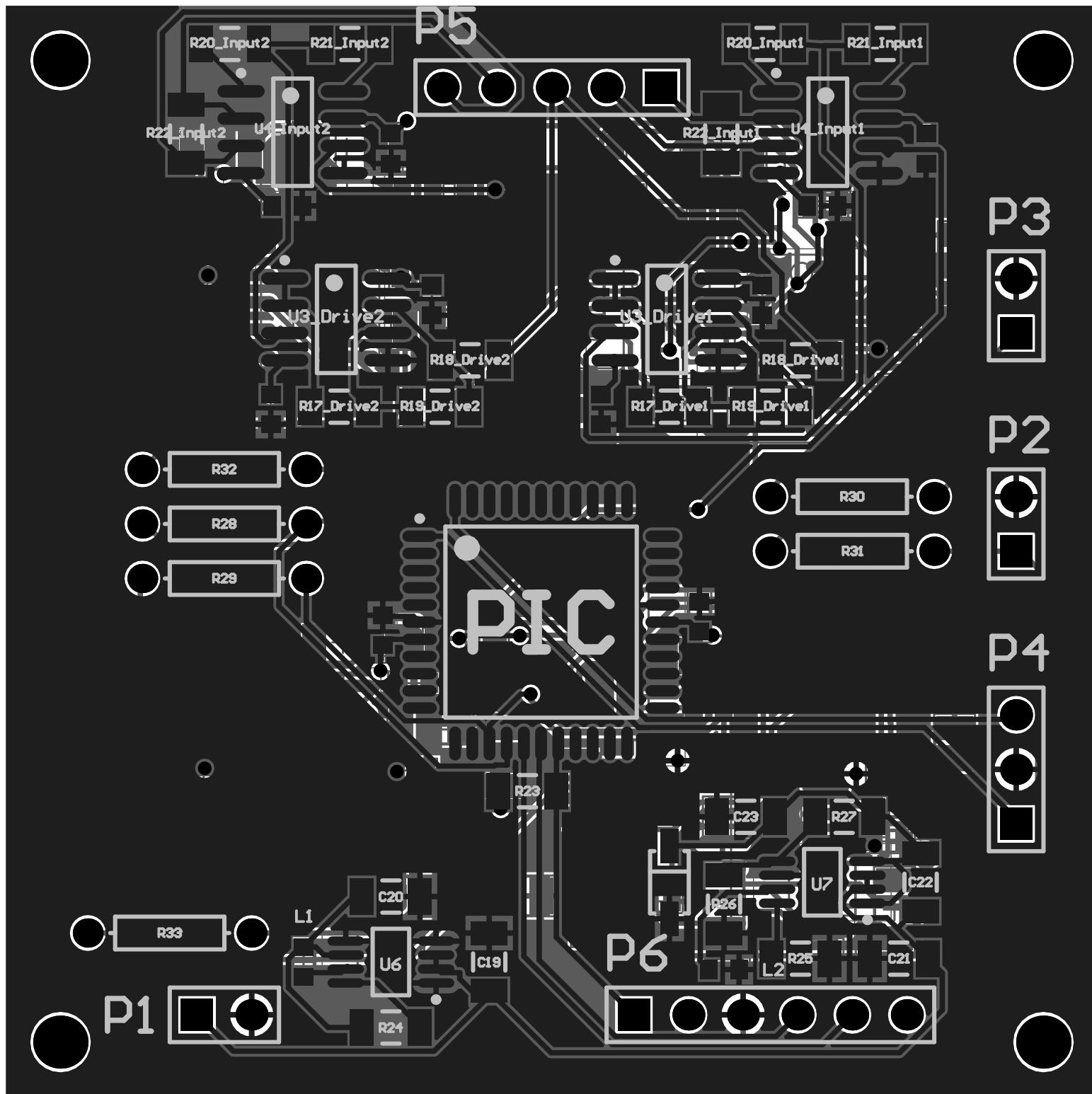
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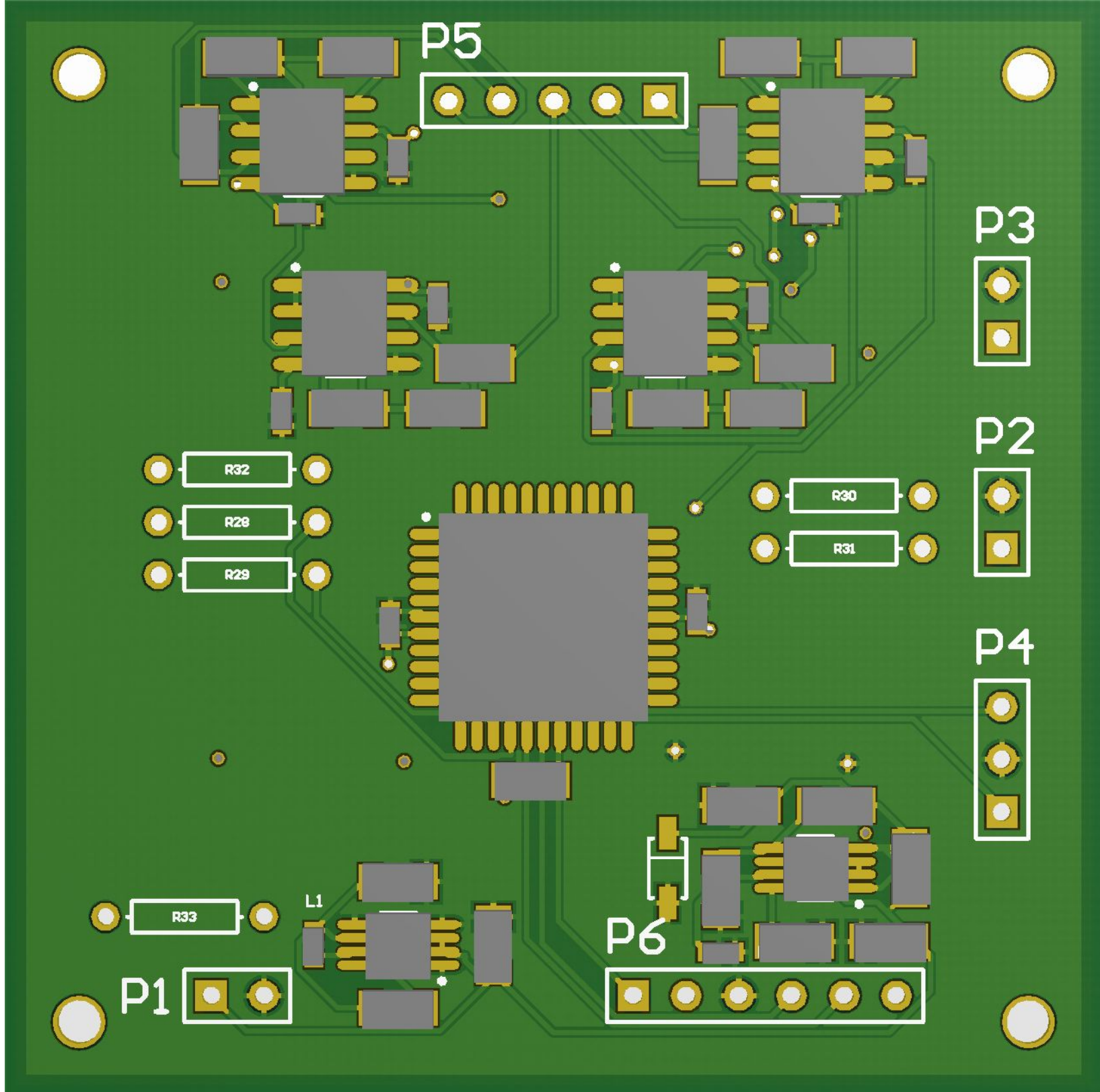


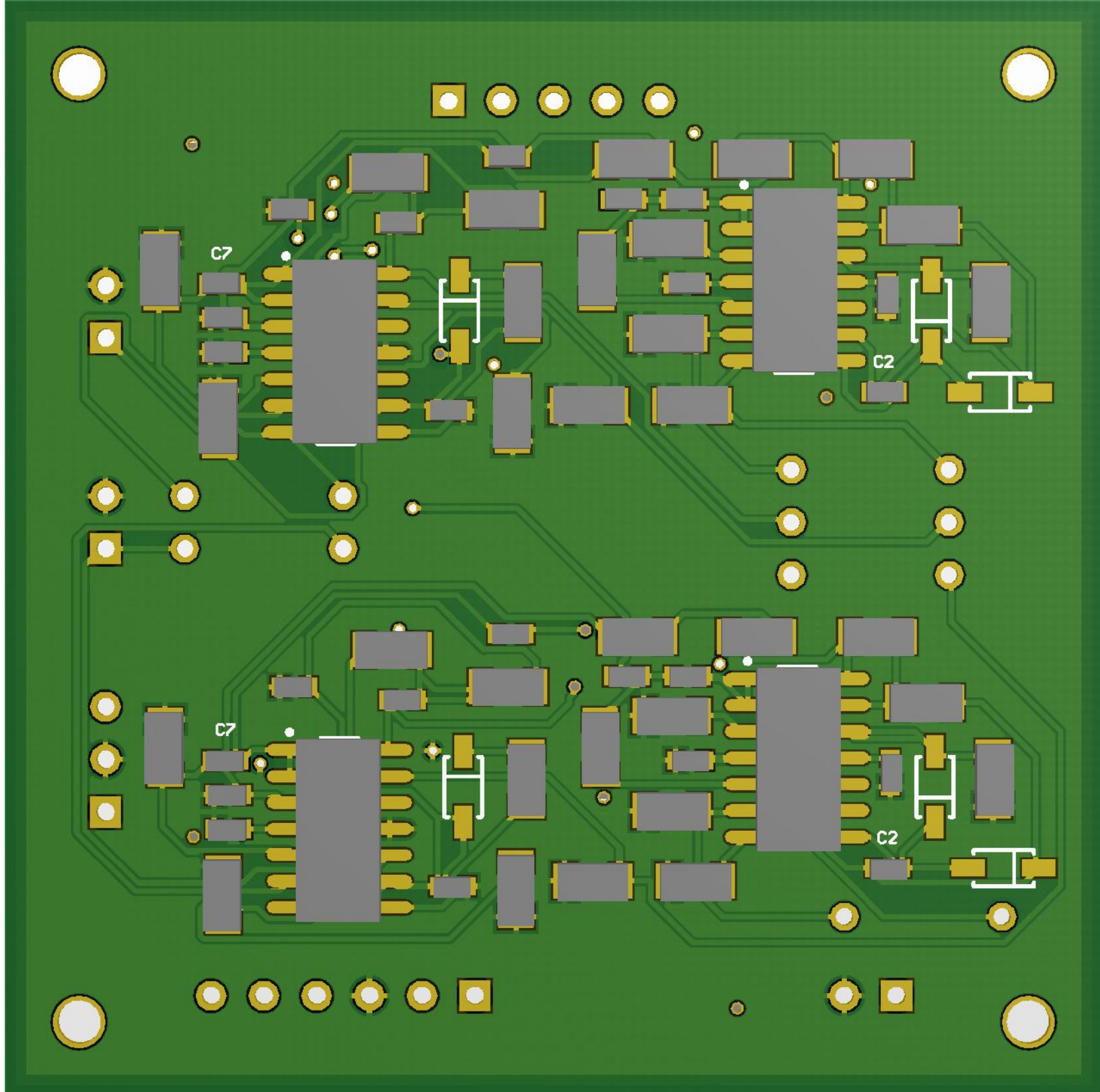
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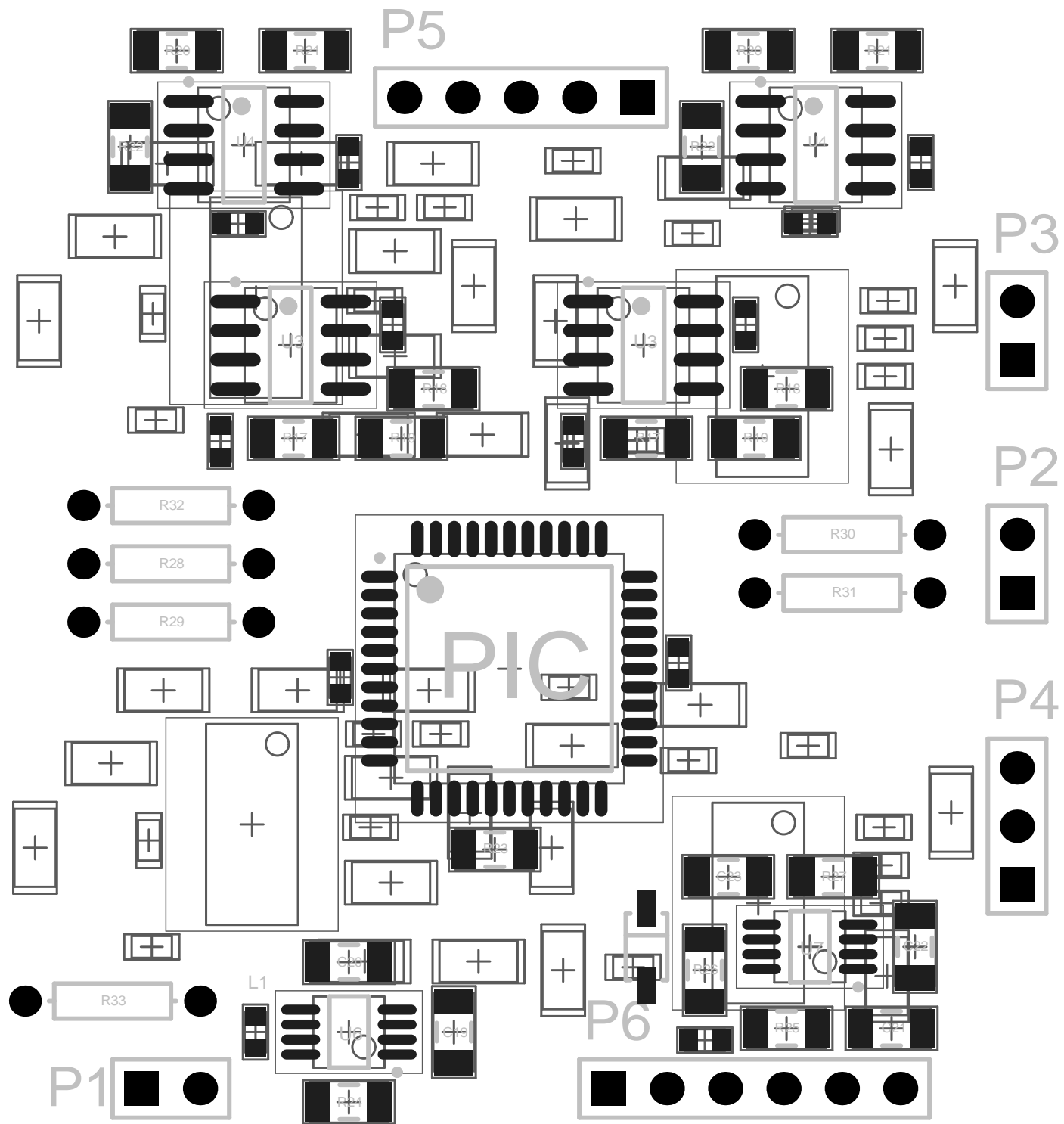


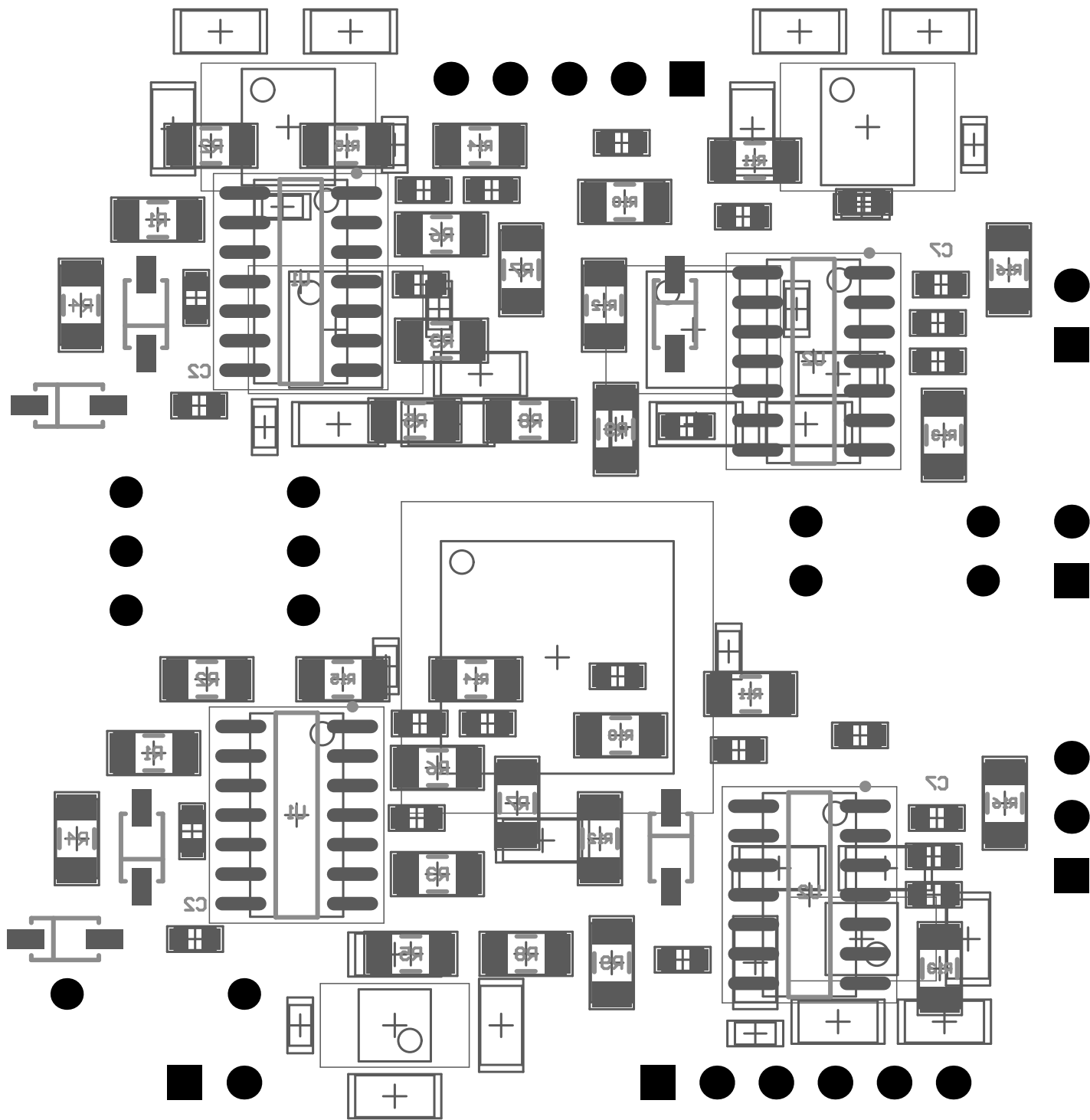
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Electrical Rules Check Repor

Class	Document	Message
		Successful Compile for Electronics.PrjPc

Design Rules Verification Report

Filename : \\Mac\Home\Desktop\Duke\BME464\Electronics\Main.PcbDr

Warnings C
Rule Violations C

Warnings	
Total	0

Rule Violations	
Room Main (Bounding Region = (3000mil, 1715mil, 3050mil, 2435m	0
Room Input2 (Bounding Region = (1270mil, 2600mil, 1750mil, 2993.15m	0
Room Input1 (Bounding Region = (2250mil, 2600mil, 2730mil, 2993.15m	0
Room Drive2 (Bounding Region = (1445mil, 2200mil, 1950mil, 2550m	0
Room Drive1 (Bounding Region = (2050mil, 2200mil, 2555mil, 2550m	0
Room Digital (Bounding Region = (1655mil, 1510mil, 2300mil, 2150m	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Net Antennae (Tolerance=0mil) (All)	0
Silk to Silk (Clearance=2mil) (All),(All)	0
Silk To Solder Mask (Clearance=5mil) (Disabled)(IsPad),(A	0
Minimum Solder Mask Sliver (Gap=1mil) (All),(All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Hole Size Constraint (Min=1mil) (Max=150mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Preferred=500mil) (A	0
Width Constraint (Min=10mil) (Max=20mil) (Preferred=10mil) (A	0
Power Plane Connect Rule(Direct Connect)(Expansion=20mil) (Conductor Width=10mil) (0
Clearance Constraint (Gap=5mil) (All),(All)	0
Un-Routed Net Constraint ((All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
SMD Neck-Down Constraint (Percent=100%) (All)	0
Room Filtering1 (Bounding Region = (1027.15mil, 1238mil, 2792.15mil, 1903m	0
Room Filtering2 (Bounding Region = (1034mil, 2141.409mil, 2799mil, 2806.409m	0
Room Pos (Bounding Region = (1505mil, 1071.85mil, 1945mil, 1441.85m	0
Room Neg (Bounding Region = (2155mil, 1198.071mil, 2735mil, 1568.071m	0
Total	0