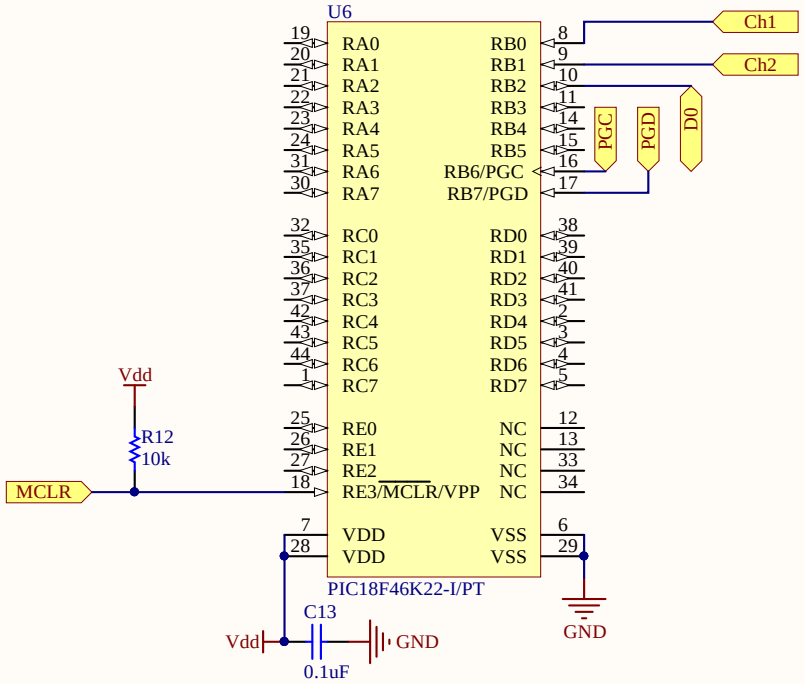

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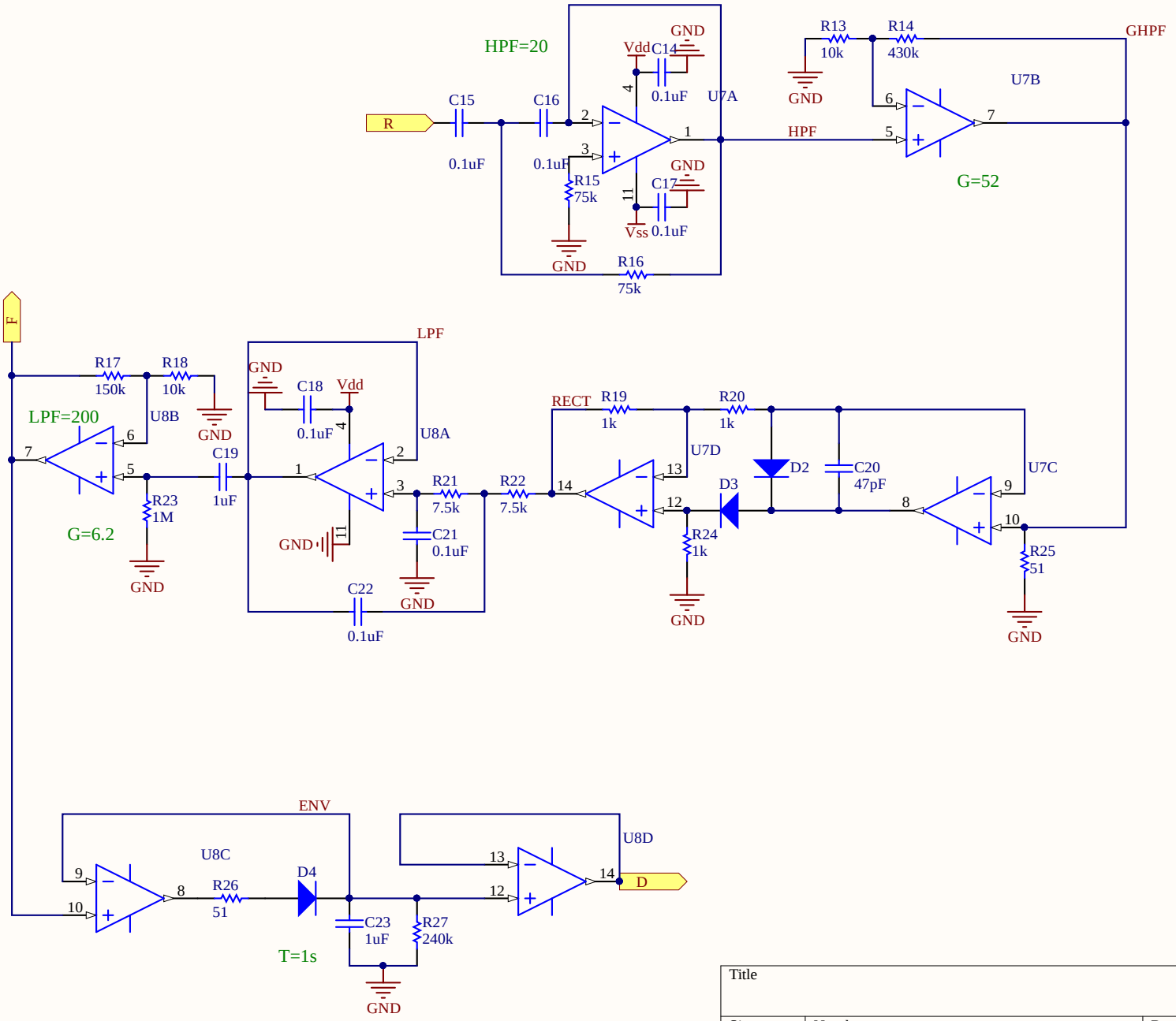

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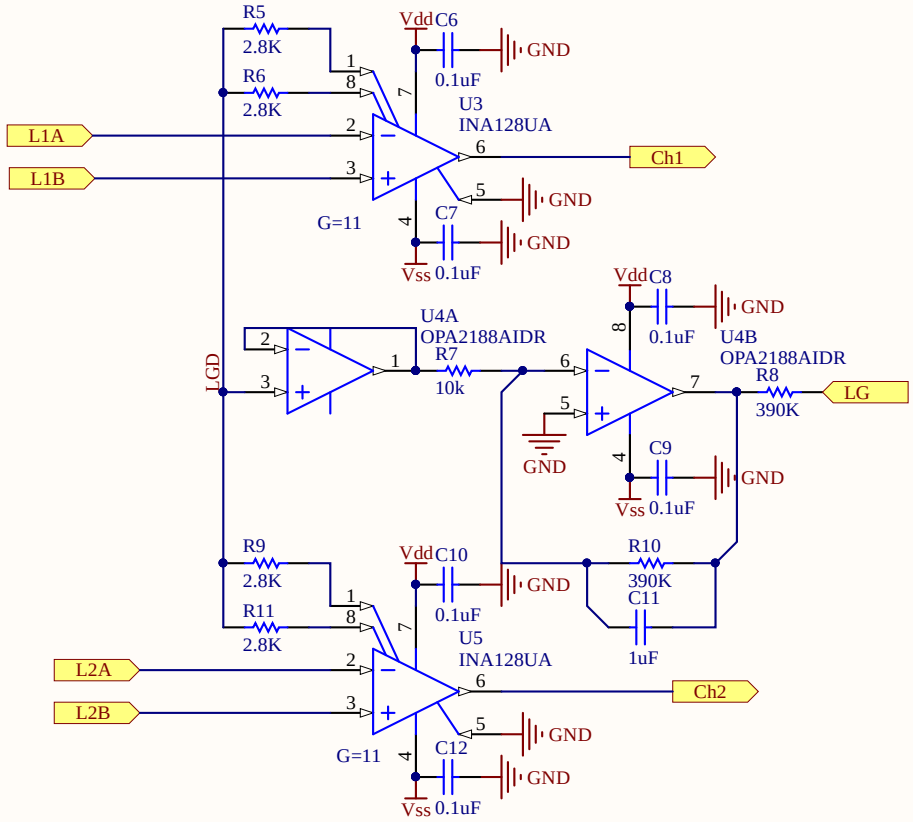

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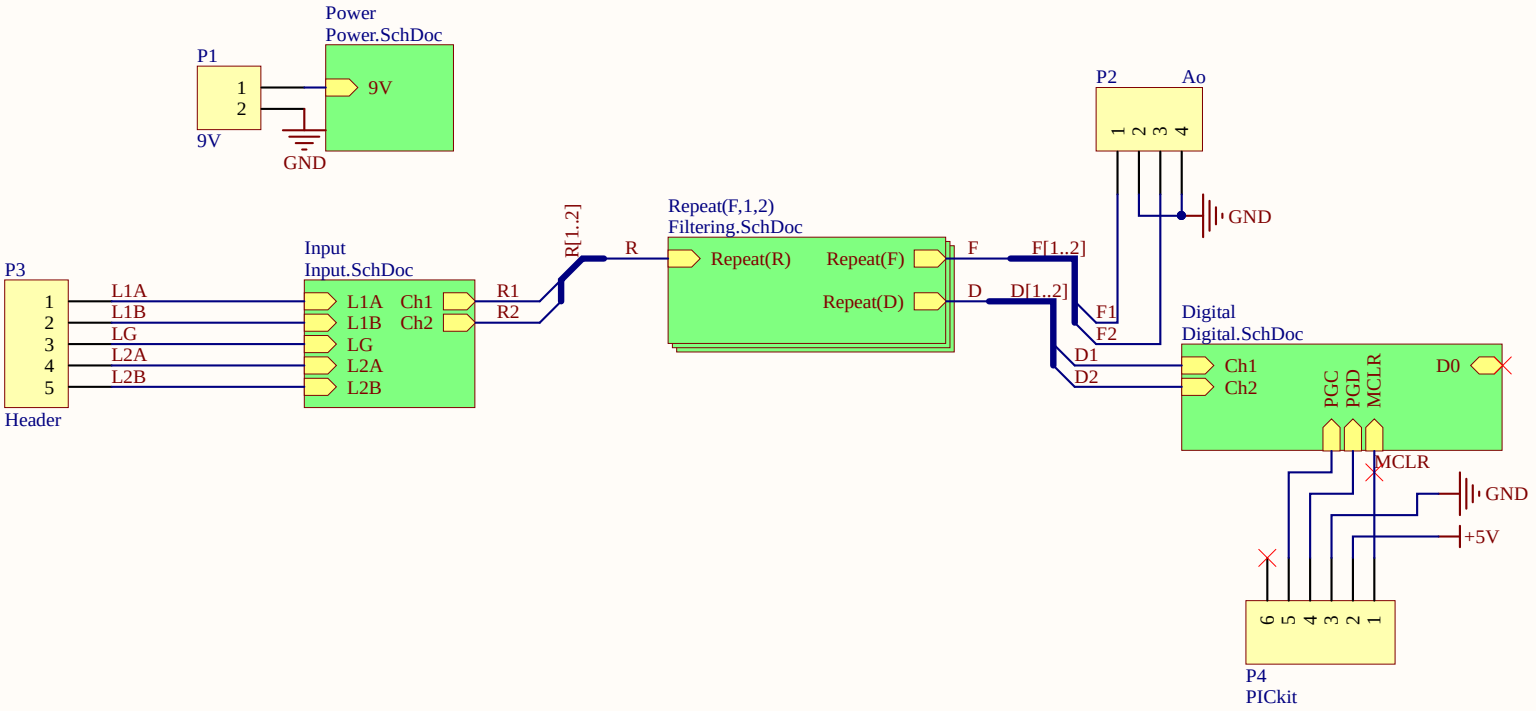

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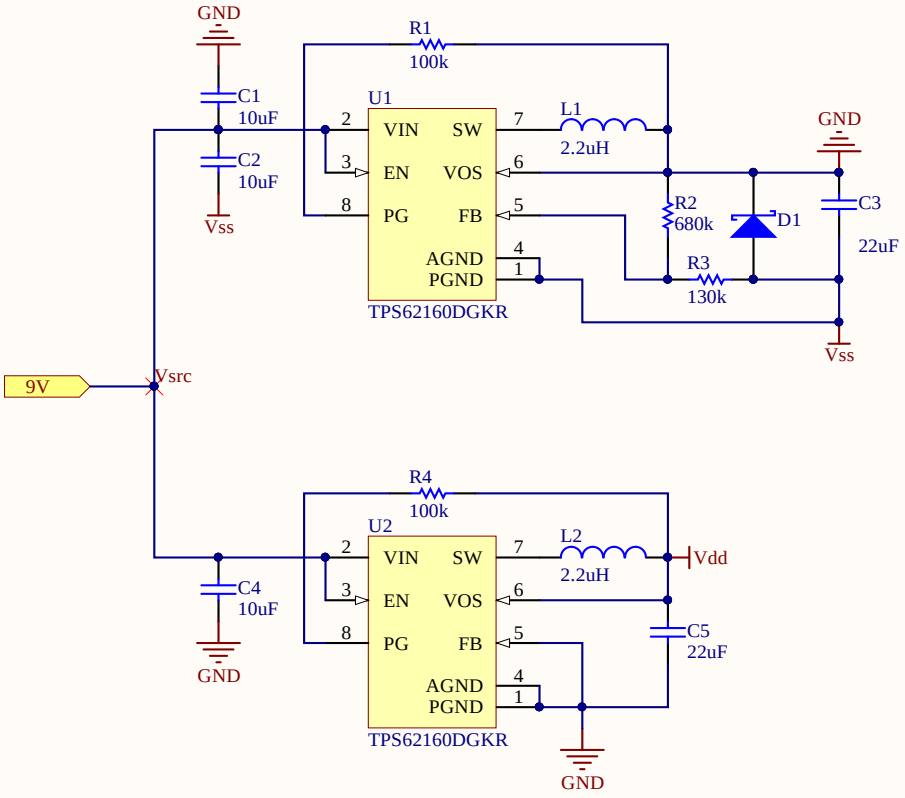

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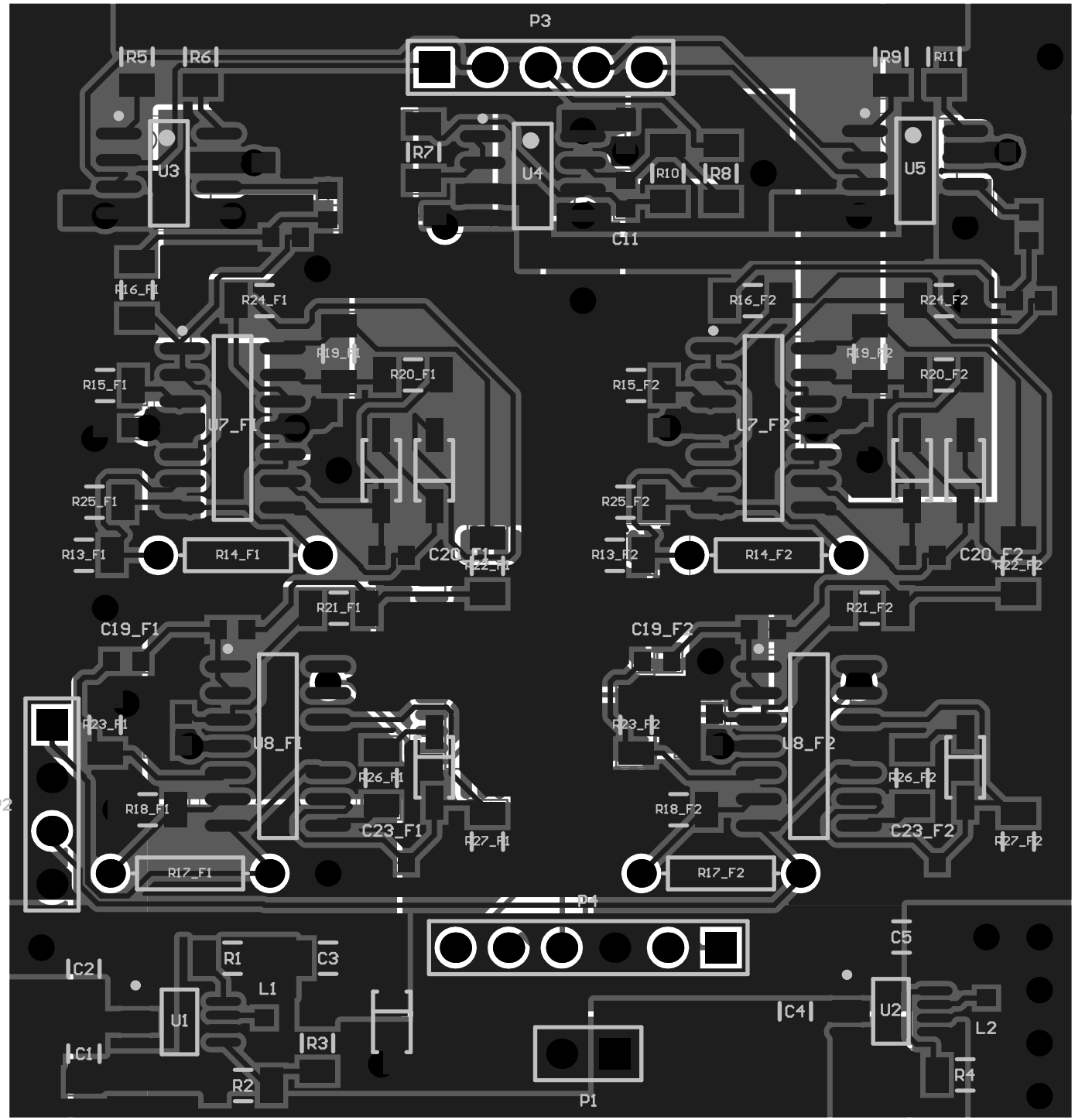
P3
R5
R6
R9
R11
U3
R7
U4
R10
R8
U5
C11
R16_F1
R24_F1
R16_F2
R24_F2
R19_F1
R20_F1
R19_F2
R20_F2
R15_F1
U7_F1
R15_F2
U7_F2
R25_F1
R25_F2
R13_F1
R14_F1
C20_F1
R22_F1
R13_F2
R14_F2
C20_F2
R22_F2
R21_F1
R21_F2
C19_F1
C19_F2
R23_F1
U8_F1
R23_F2
U8_F2
R26_F1
R26_F2
P2
R18_F1
R18_F2
C23_F1
R27_F1
C23_F2
R27_F2
R17_F1
R17_F2
P4
C5
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R1
C3
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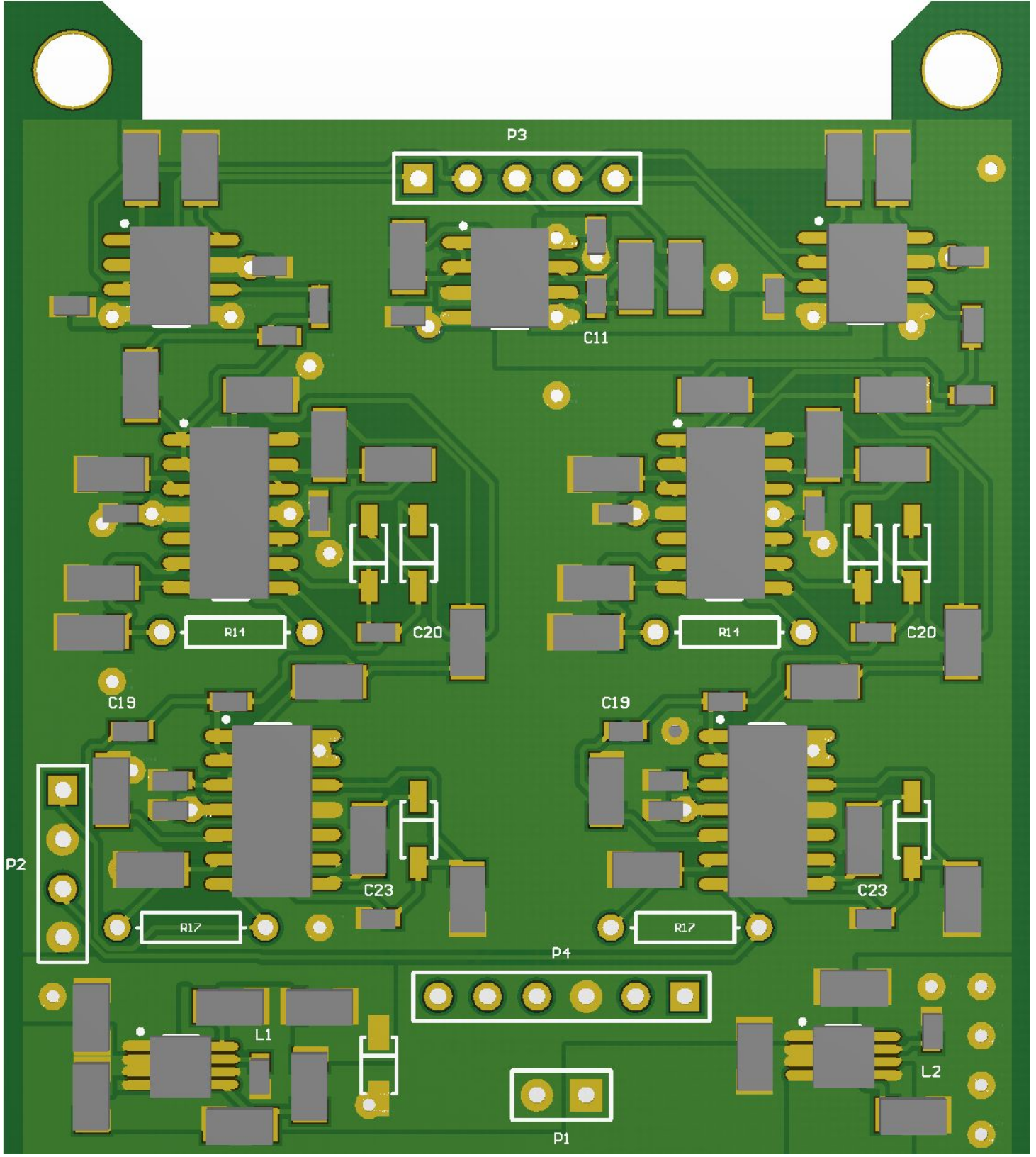
U1
R3
C1
R4
R2
P1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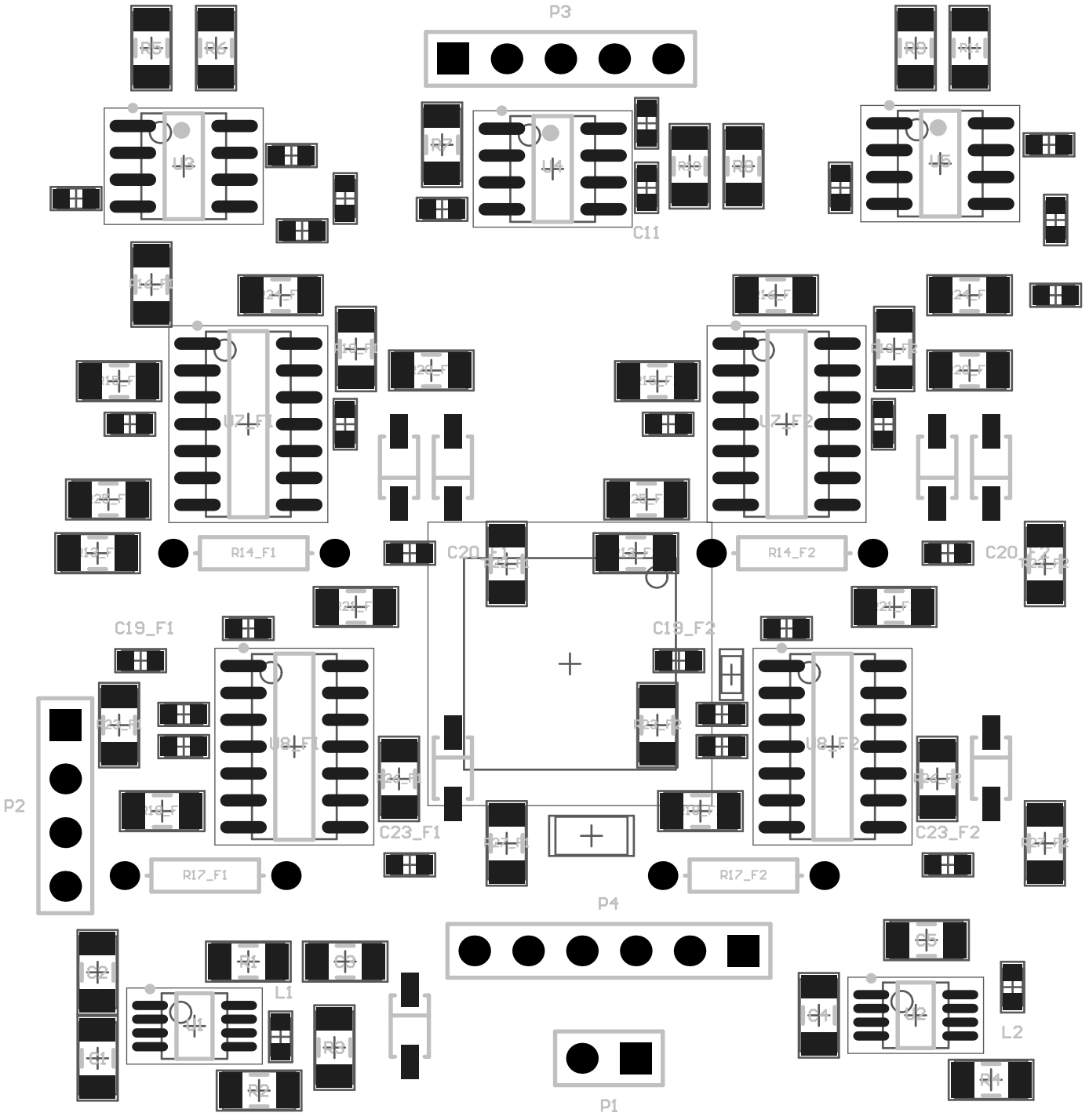
R14
C20
C19
P2
C23
R17
P4
L1
P1
L2


P3
C11
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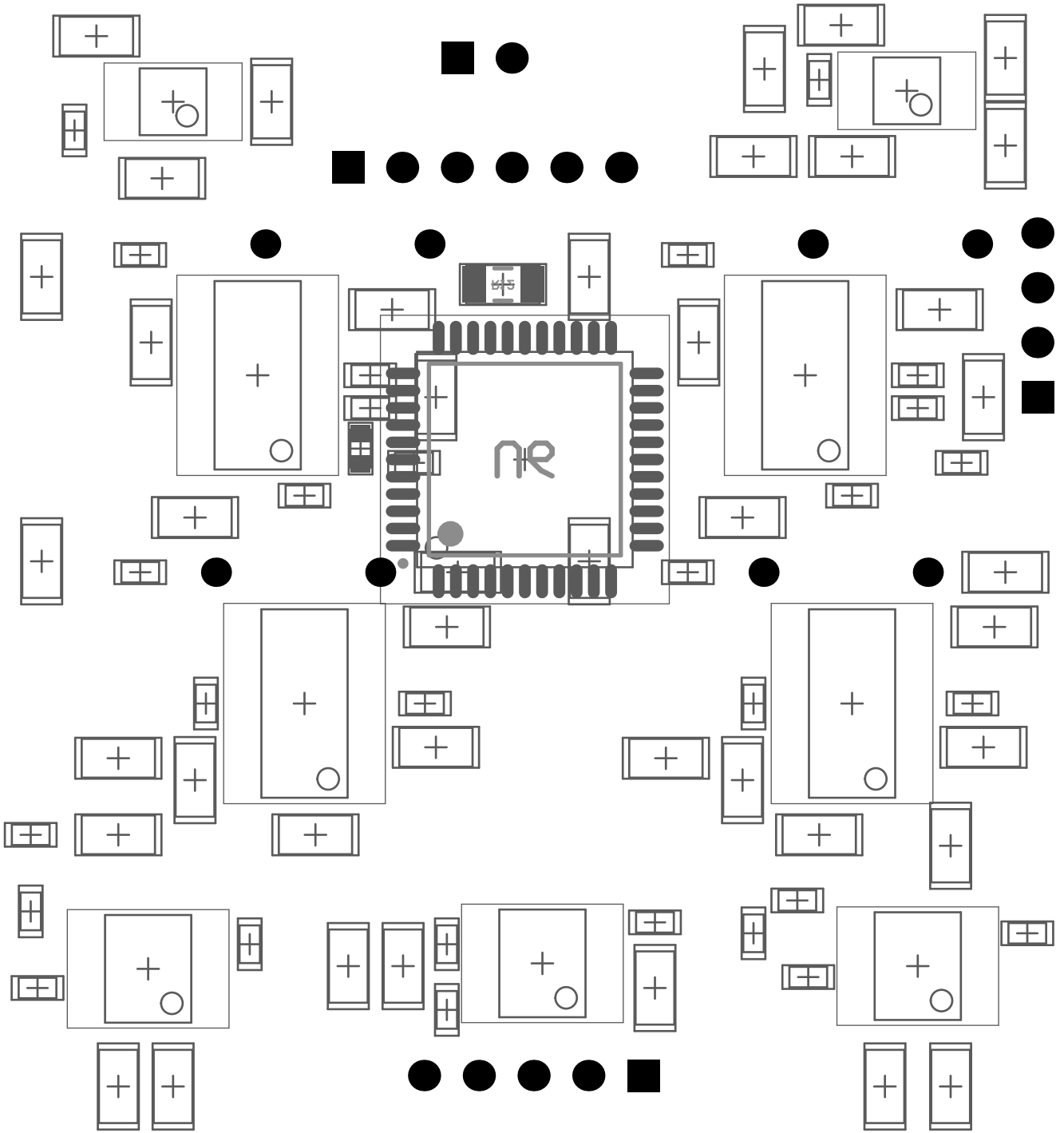
R14_F1
R14_F2
C20_F1
C20_F2
C19_F1
C19_F2
U8_F1
U8_F2
P2
C23_F1
C23_F2
R17_F1
R17_F2
P4
L1
L2
P1



Electrical Rules Check Repor

Class	Document	Message
		Successful Compile for Electronics.PrjPc

Design Rules Verification Repor

Filename : \\Mac\Home\Desktop\Duke\BME464\Electronics\Main.PcbD

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Room Digital (Bounding Region = (1717.559mil, 1434.016mil, 2397.559mil, 2214.016m	0
Room Power (Bounding Region = (1000mil, 1000mil, 3000mil, 1400m	0
Room Input (Bounding Region = (1000mil, 2600mil, 3000mil, 3100m	0
Room F2 (Bounding Region = (2000mil, 1400mil, 3000mil, 2800mil) (InComponentClass('F2	0
Room F1 (Bounding Region = (1000mil, 1400mil, 2000mil, 2800mil) (InComponentClass('F1	0
Width Constraint (Min=10mil) (Max=20mil) (Preferred=20mil) (InNet('GND	0
Width Constraint (Min=10mil) (Max=20mil) (Preferred=20mil) (InNet('VDD	0
Width Constraint (Min=10mil) (Max=20mil) (Preferred=20mil) (InNet('VSS	0
Modified Polygon (Allow modified: No), (Allow shelved: No	0
Net Antennae (Tolerance=0mil) (All	0
Silk to Silk (Clearance=2mil) (All),(All	0
Silk To Solder Mask (Clearance=5mil) (Disabled)(IsPad),(A	0
Minimum Solder Mask Sliver (Gap=1mil) (All),(All	0
Hole To Hole Clearance (Gap=10mil) (All),(All	0
Hole Size Constraint (Min=1mil) (Max=150mil) (All	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (A	0
Width Constraint (Min=10mil) (Max=20mil) (Preferred=10mil) (A	0
Power Plane Connect Rule(Direct Connect)(Expansion=20mil) (Conductor Width=10mil) (	0
Clearance Constraint (Gap=10mil) (All),(All	0
Un-Routed Net Constraint ((All)	0
Short-Circuit Constraint (Allowed=No) (All),(All	0
Room Main (Bounding Region = (1300mil, 1400mil, 2700mil, 2800m	0
Total	0