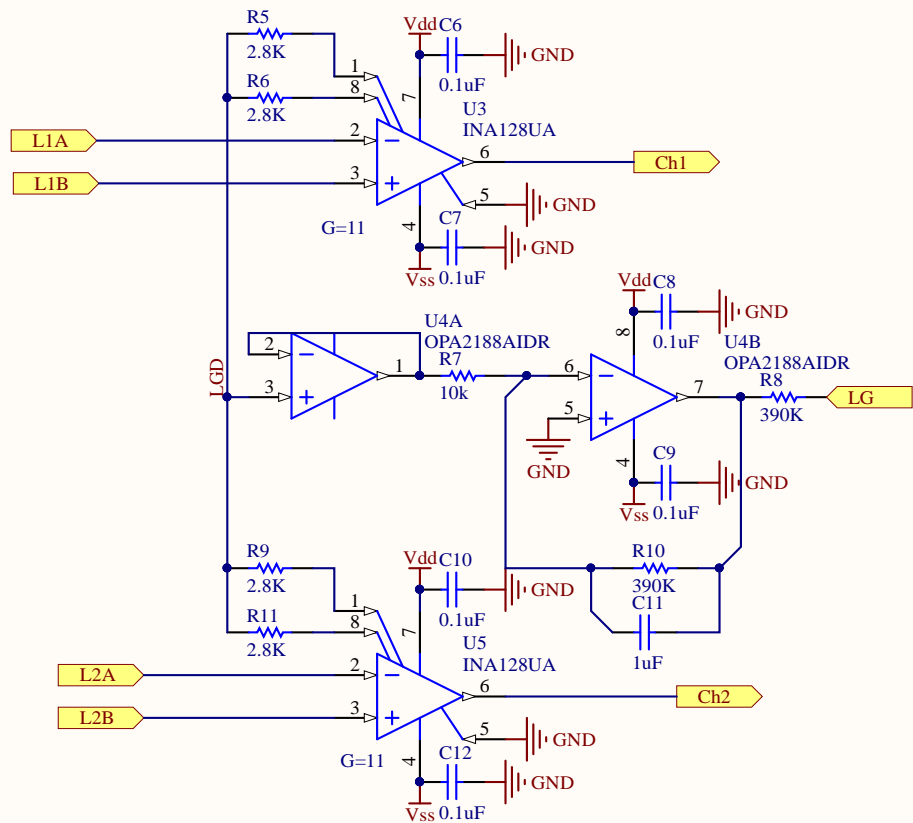
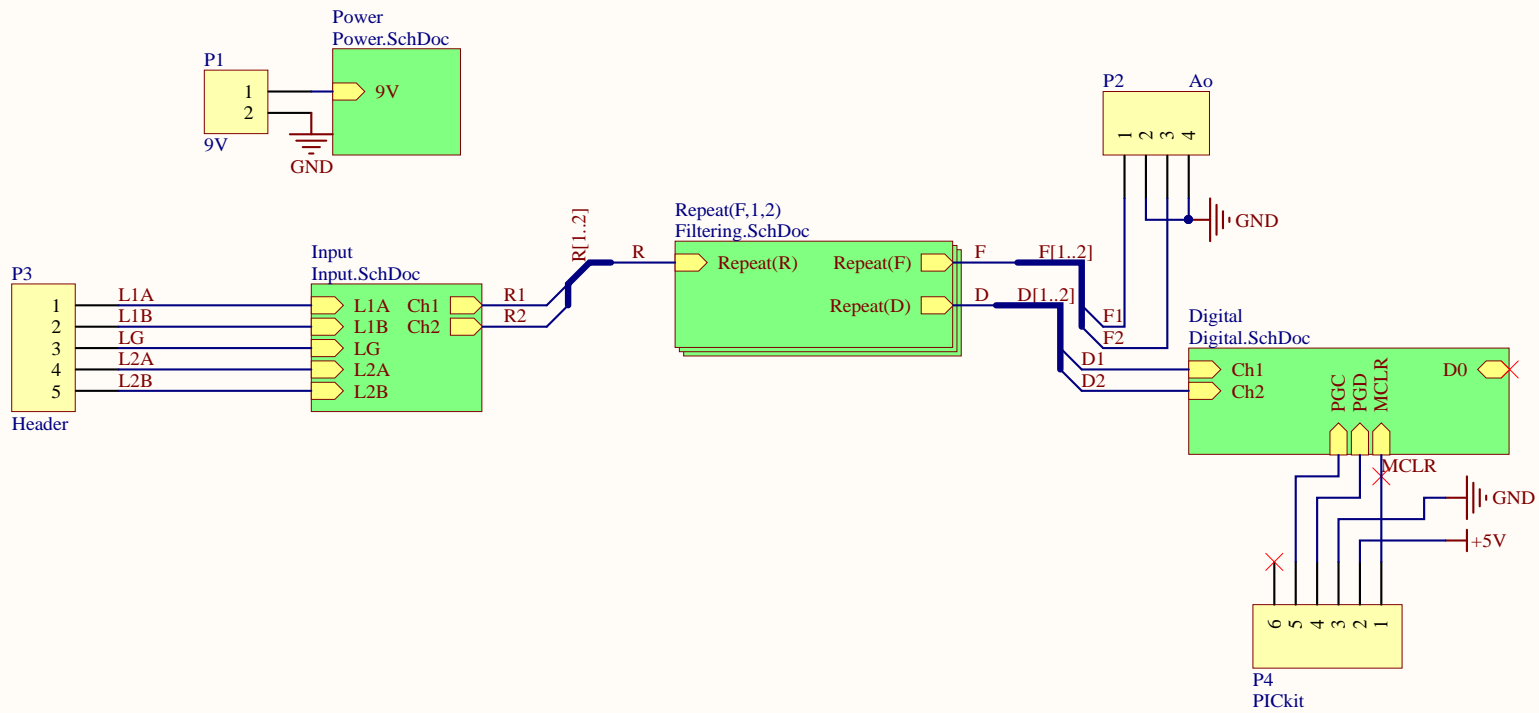


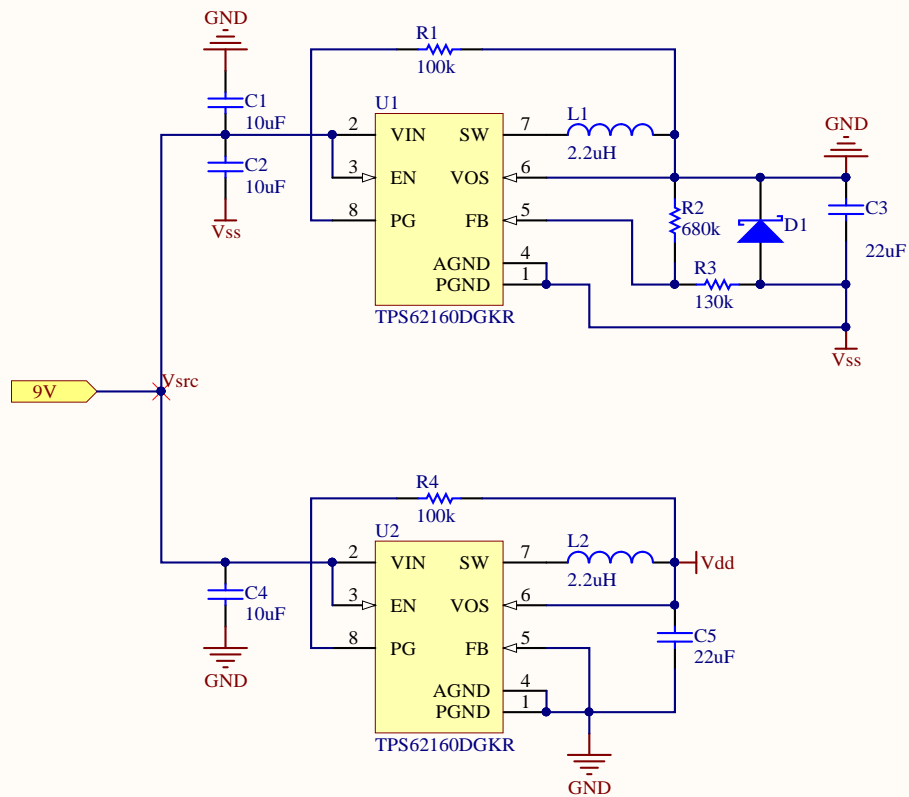
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Size	Number	Revision
A		
Date:	10/20/16	Sheet of
File:	\\.\Filtering.SchDoc	Drawn By:



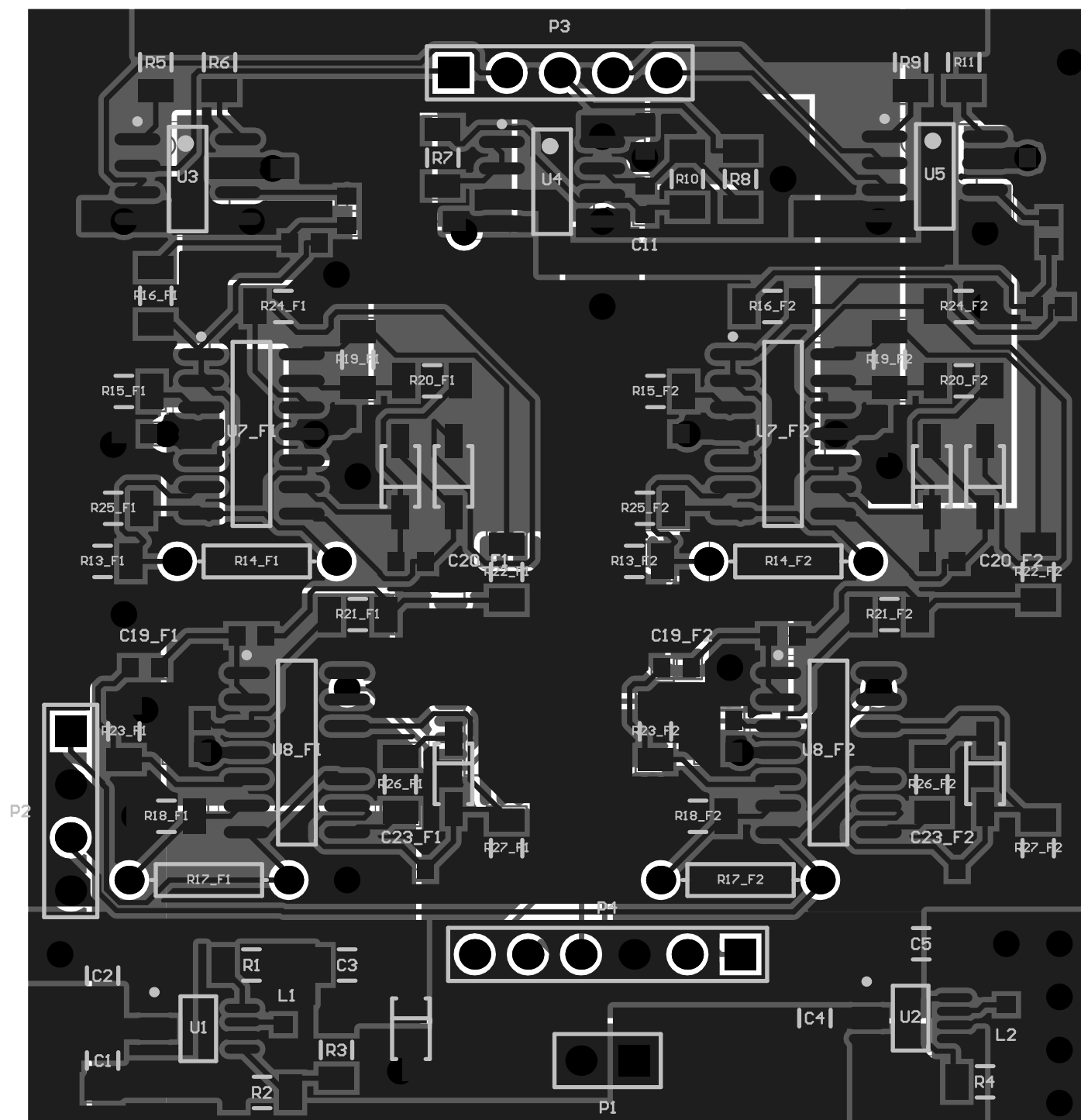
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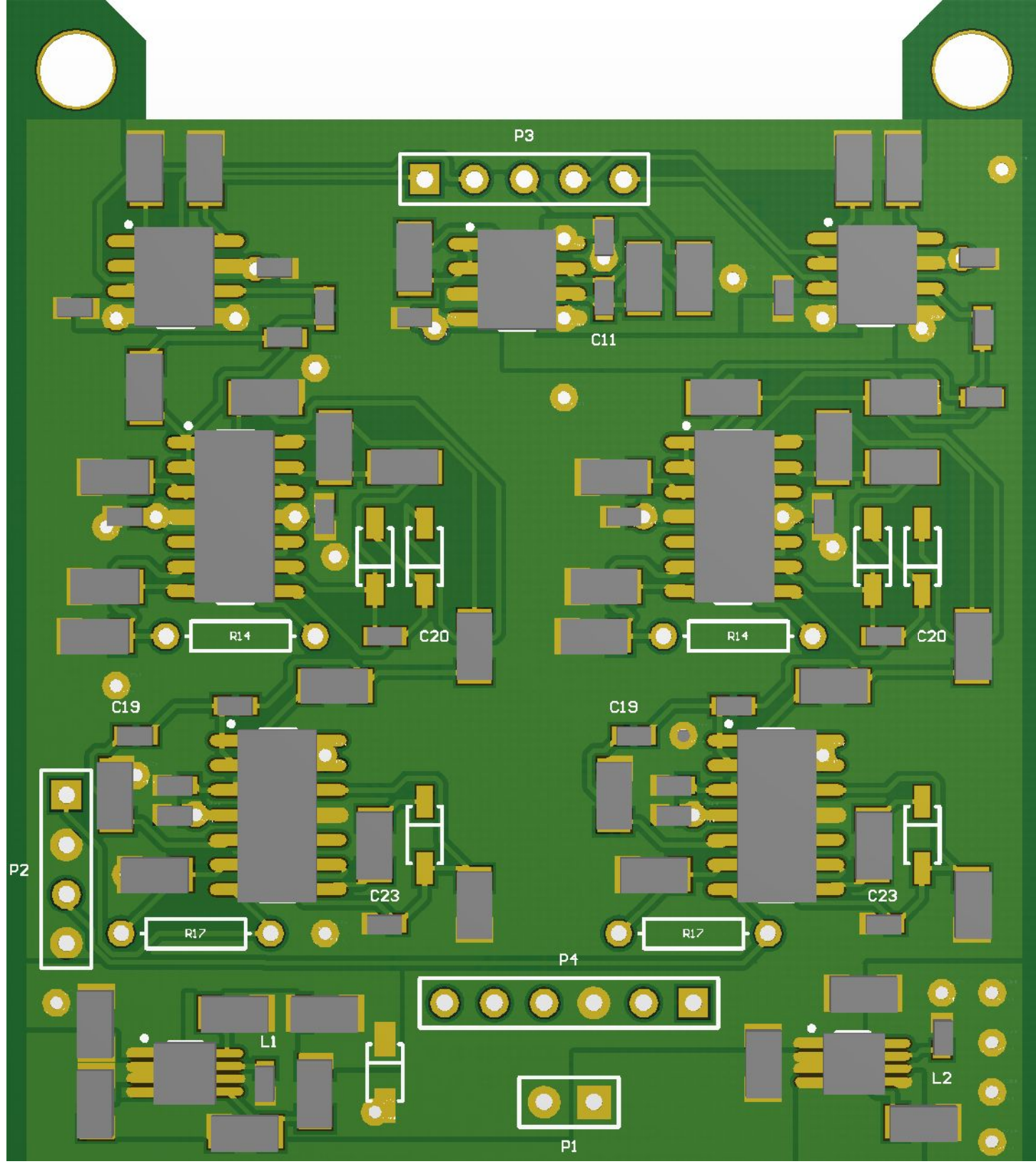


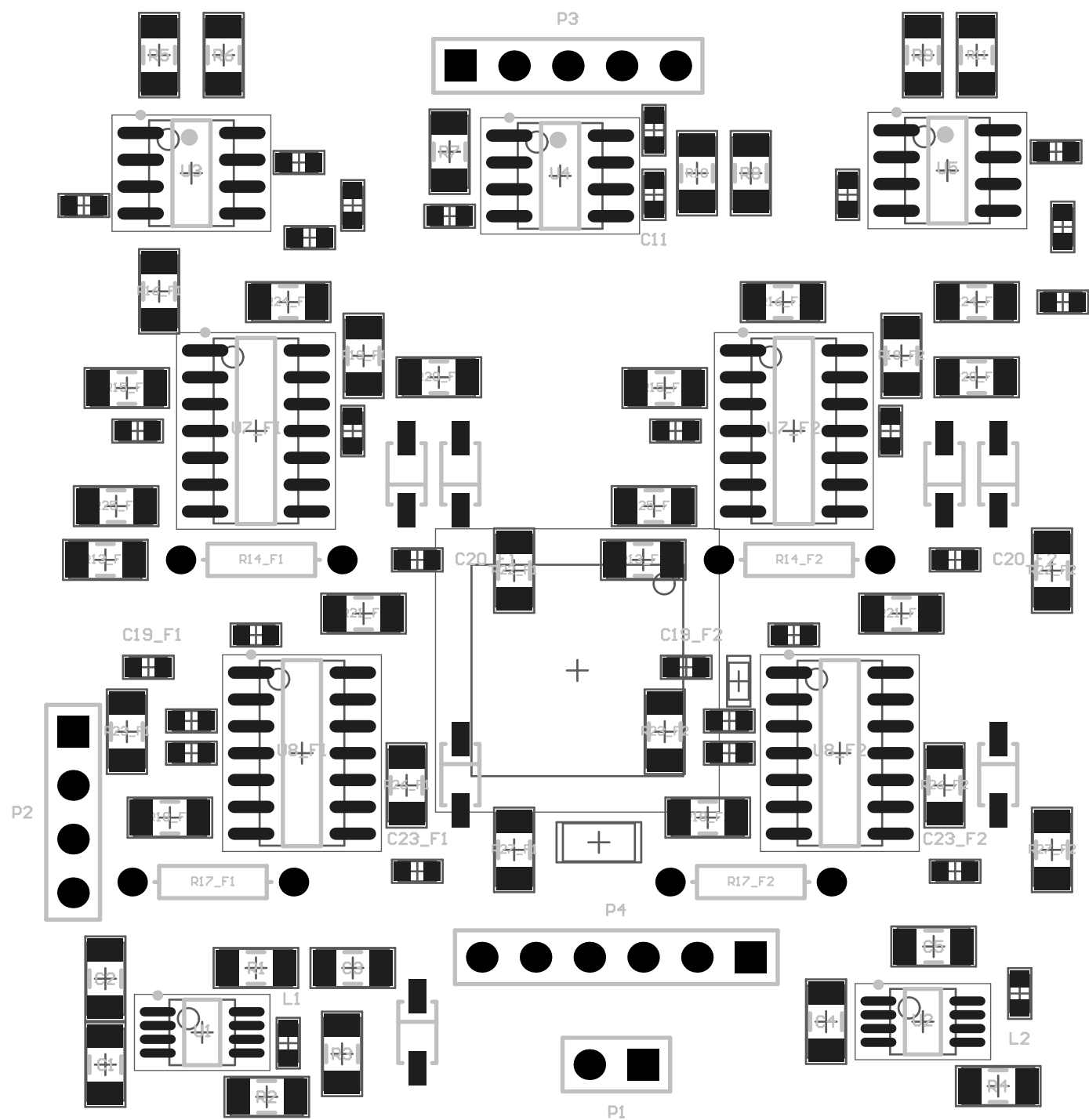
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Date:	10/20/16	Sheet of
File:	\\.\Main.SchDoc	Drawn By:



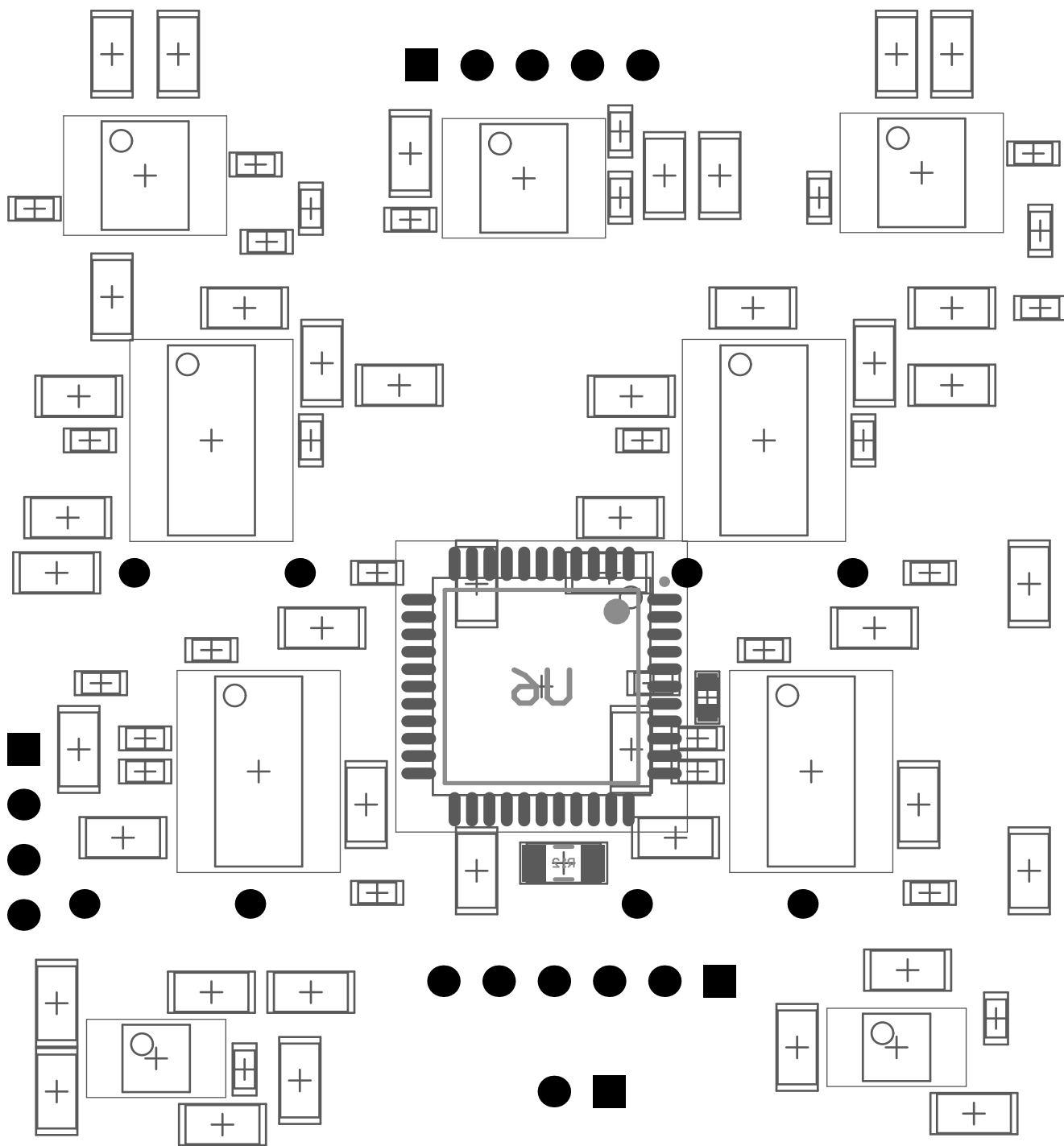
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Size	Number	Revision
A		
Date:	10/20/16	Sheet of
File:	\\..\Power.SchDoc	Drawn By:











**Electrical Rules Check Repor**

Class	Document	Message
		Successful Compile for Electronics.PrjPc

## Design Rules Verification Report

Filename : \\Mac\Home\Desktop\Duke\BME464\Electronics\Main.PcbDr

Warnings C  
Rule Violations C

Warnings	
Total	0

Rule Violations	
Room Main (Bounding Region = (1300mil, 1400mil, 2700mil, 2800m	0
Short-Circuit Constraint (Allowed=No) (All),(Al	0
Un-Routed Net Constraint ( (All)	0
Clearance Constraint (Gap=10mil) (All),(Al	0
Power Plane Connect Rule(Direct Connect )(Expansion=20mil) (Conductor Width=10mil) (	0
Width Constraint (Min=10mil) (Max=20mil) (Preferred=10mil) (A	0
Height Constraint (Min=0mil) (Max=1000mil) (Preferred=500mil) (A	0
Hole Size Constraint (Min=1mil) (Max=150mil) (Al	0
Hole To Hole Clearance (Gap=10mil) (All),(Al	0
Minimum Solder Mask Sliver (Gap=1mil) (All),(Al	0
Silk To Solder Mask (Clearance=5mil) (Disabled)(IsPad),(A	0
Silk to Silk (Clearance=2mil) (All),(All	0
Net Antennae (Tolerance=0mil) (Al	0
Modified Polygon (Allow modified: No), (Allow shelved: No	0
Width Constraint (Min=10mil) (Max=20mil) (Preferred=20mil) (InNet('VSS	0
Width Constraint (Min=10mil) (Max=20mil) (Preferred=20mil) (InNet('VDD	0
Width Constraint (Min=10mil) (Max=20mil) (Preferred=20mil) (InNet('GND	0
Room F1 (Bounding Region = (1000mil, 1400mil, 2000mil, 2800mil) (InComponentClass('F1	0
Room F2 (Bounding Region = (2000mil, 1400mil, 3000mil, 2800mil) (InComponentClass('F2	0
Room Input (Bounding Region = (1000mil, 2600mil, 3000mil, 3100m	0
Room Power (Bounding Region = (1000mil, 1000mil, 3000mil, 1400m	0
Room Digital (Bounding Region = (1717.559mil, 1434.016mil, 2397.559mil, 2214.016m	0
Total	0