2023 ICLAB Fall Syllabus

Instructor:

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TA List:

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Time:

- Lecture: 3EF (13:30 ~ 15:30, Wednesday) @ ED415
- Code Review: 1EF (13:30 ~ 15:30, Monday) @ ED415 for Lab01~Midterm Project

Prerequisites:

- Introduction to VLSI, Logic Design, Digital System Design, Computer Organization (Opt)

Course Objectives:

This course aims to convey the senior and graduated EE students techniques to design the VLSI chips using state-of-the-art CAD tools. In addition to learning CAD tools for performance-driven and cost effective IC designs, a top-down design flow and related environment will also be addressed. Upon completion of the course, the student will be able to design the integrated circuits and systems based on standard cell library as well as full-custom layout approaches. As such he/she will be able to work in a team of designers or stand alone.

Grading Policy

Weekly Lab Exercise x 13	(60%)
Midterm Project	(10%)
Midterm Exam	(6%)
Online Test	(8%)
Final Project	(10%)
Final Exam	(6%)
Bonus (ADFP Lab/Lecture)	(5%)

Course Schedule:

Week	Date	Course Content	TA
1	09/13	00、Introduction + Environment Setting	賴林鴻
2	09/20	01、Cell Based Design Methodology + Verilog Combinational Circuit Programming	賴林鴻
3	09/27	02、Finite State Machine + Verilog Sequential Circuit Programming	莊彥騰
4	10/04	03、Verification & Simulation + Verilog Test Bench Programming	張庭瑜
5	10/11	04、Sequential Circuit Design II (STA + Pipeline) + Synopsys DesignWare IP	李家毓
6	10/18	05、Memory & Coding Style (Memory Compiler)	翁沐昀
7	10/25	06、Synthesis Methodology (Design Compiler + IP Design) Midterm Project Announcement	連紹華 賴林鴻
8	11/01 11/04	No class : Study Days **Midterm Exam + Online Test (Sat.)**	賴林鴻 莊彥騰
9	11/08	07、Timing: Cross Clock Domain + Synthesis Static Time Analysis	張庭瑜
10	11/15	08、Power: Low Power Design Midterm Project Deadline	彭賢齊
11	11/22	09、System Verilog I (Design)	蔡睿煌
12	11/29	10、System Verilog II (Verification)	蔡睿煌
13	12/06	11、System Verilog (Formal Verification)	李家毓
14	12/13	12、APR I : From RTL to GDSII	翁沐昀
15	12/20	13、APR II : IR-Drop Analysis + Advanced IC Design Methodology Final Project Announcement	連紹華 賴林鴻 張庭瑜
16	12/27	**Final Exam**	賴林鴻
17	01/05	TBD	TBD
18	**01/10**	**ADFP Lab/Lecture + Final Project Deadline**	賴林鴻 彭賢齊 李家毓 莊彥騰