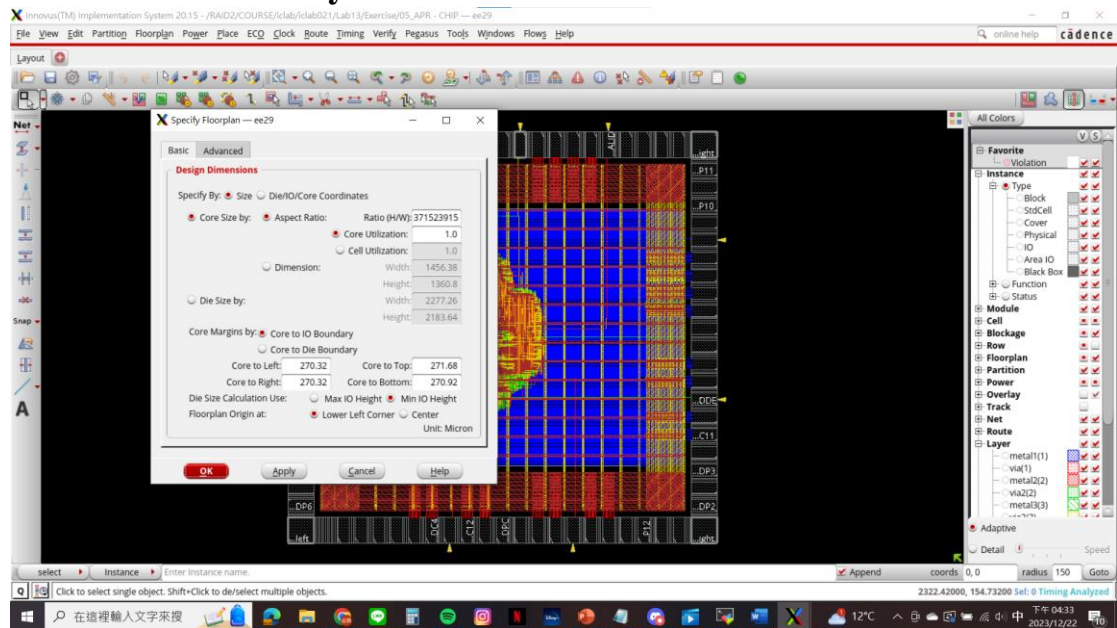
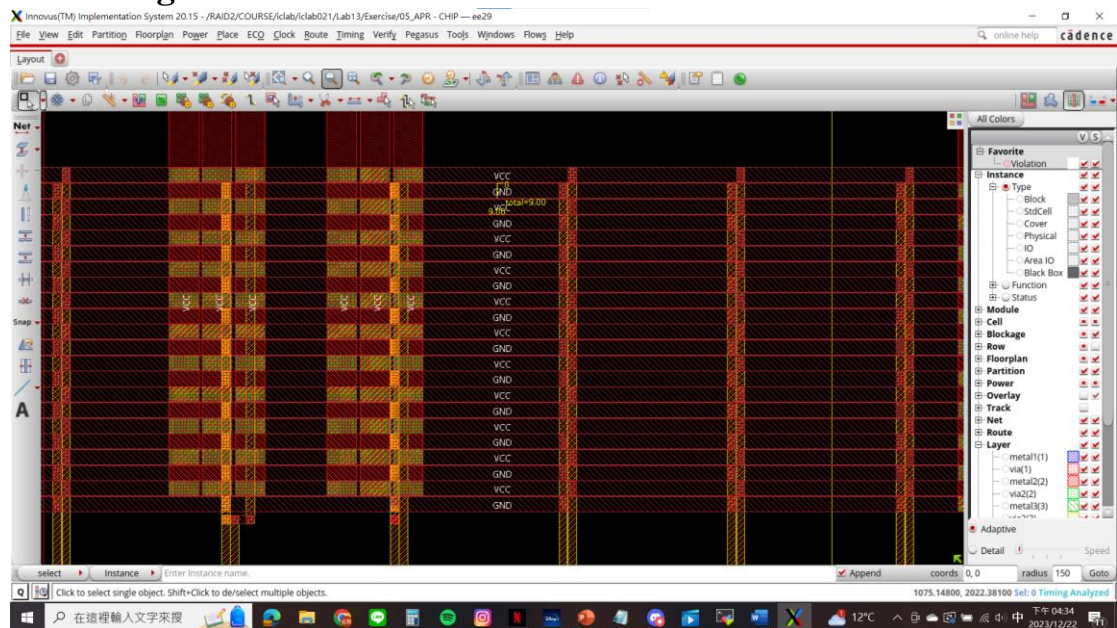


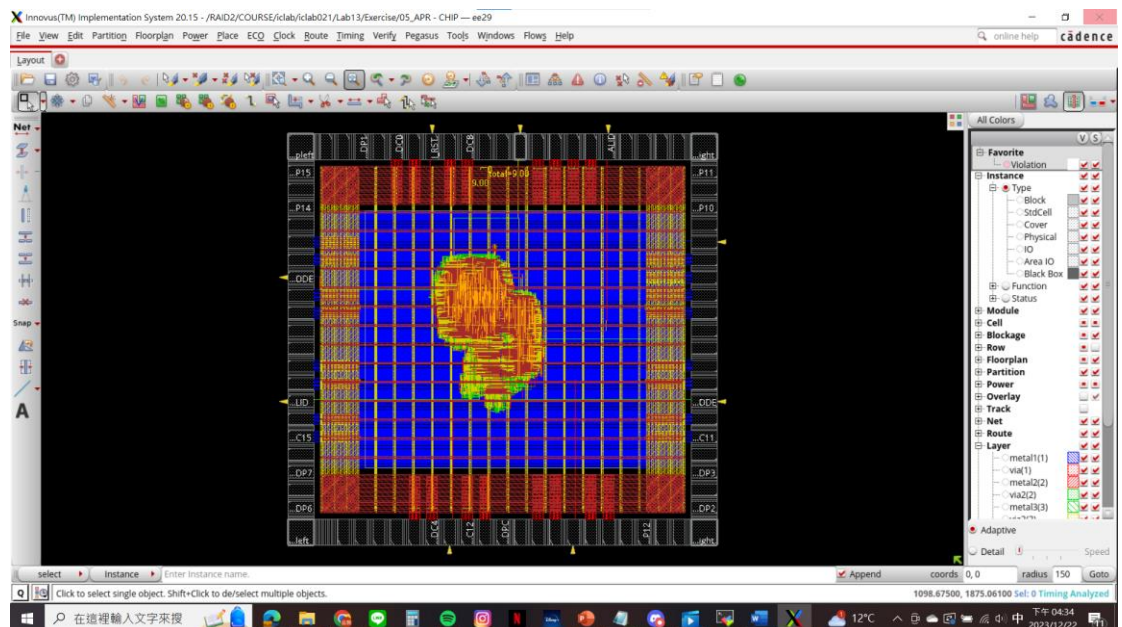
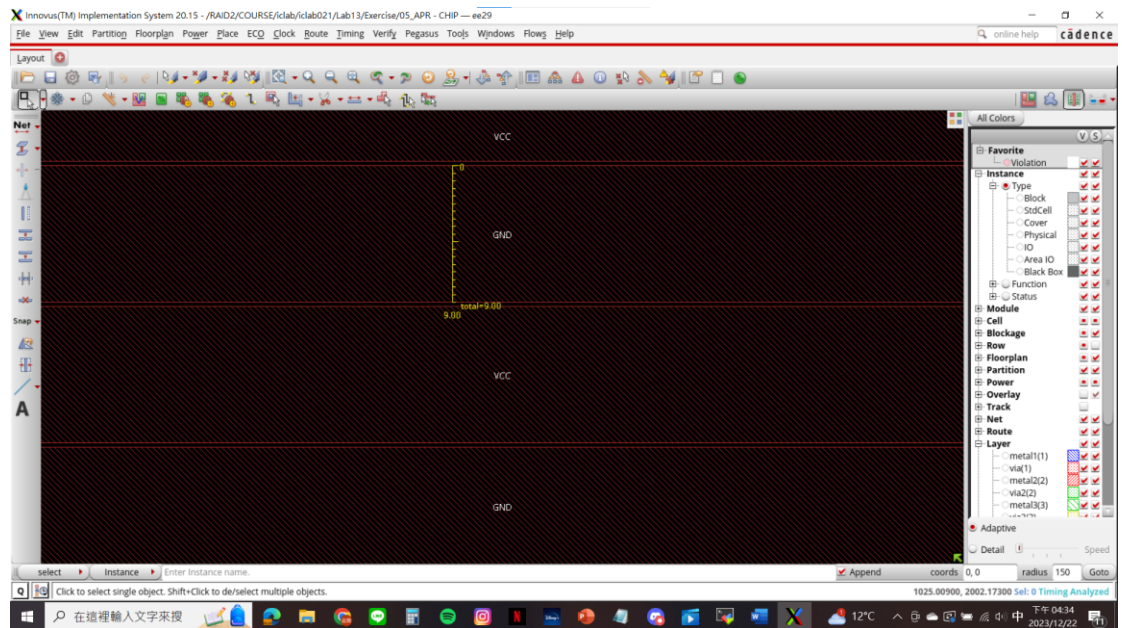
Report

1. Core to IO boundary :



2. Core Ring :





3. Post-Route setup time analysis :

The screenshot displays the Xilinx Vivado IDE interface. On the left, a project tree shows various design files. The main window is divided into two panes. The top pane shows the 'tueDesign Summary' for the 'av_func_mode_max' setup view. The bottom pane shows the 'Setup views included:' section.

End delay calculation (fullDC). (MEM=2980.22 CPU=0:00:00.1 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=2980.22 CPU=0:00:00.1 REAL=0:00:00.0)
*** Done Building Timing Graph (cpus=0:00:02.9 real=0:00:03.0 totSessionCpu=0:05:18 mem=2980.2M)

Setup views included:
av_func_mode_max

Setup mode	all	reg2reg	default
MNS (ns):	0.506	0.506	1.636
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	371	281	370

Reported timing to dir timingReports
Total CPU time: 3.88 sec
Total Real time: 6.0 sec
Total Memory Usage: 2957.496094 Mbytes
Reset AAE Options
*** timeDesign #7 [finish] : cpu/real = 0:00:03.9/0:00:06.0 (0.6), totSession cpu/real = 0:05:18.4/0:22:30.7 (0.2), mem = 2957.5M

4. Post-Route hold time analysis :

The screenshot displays the Xilinx Vivado IDE interface. On the left, a project tree shows various design files. The main window is divided into two panes. The top pane shows the 'tueDesign Summary' for the 'av_func_mode_min' hold view. The bottom pane shows the 'Hold views included:' section.

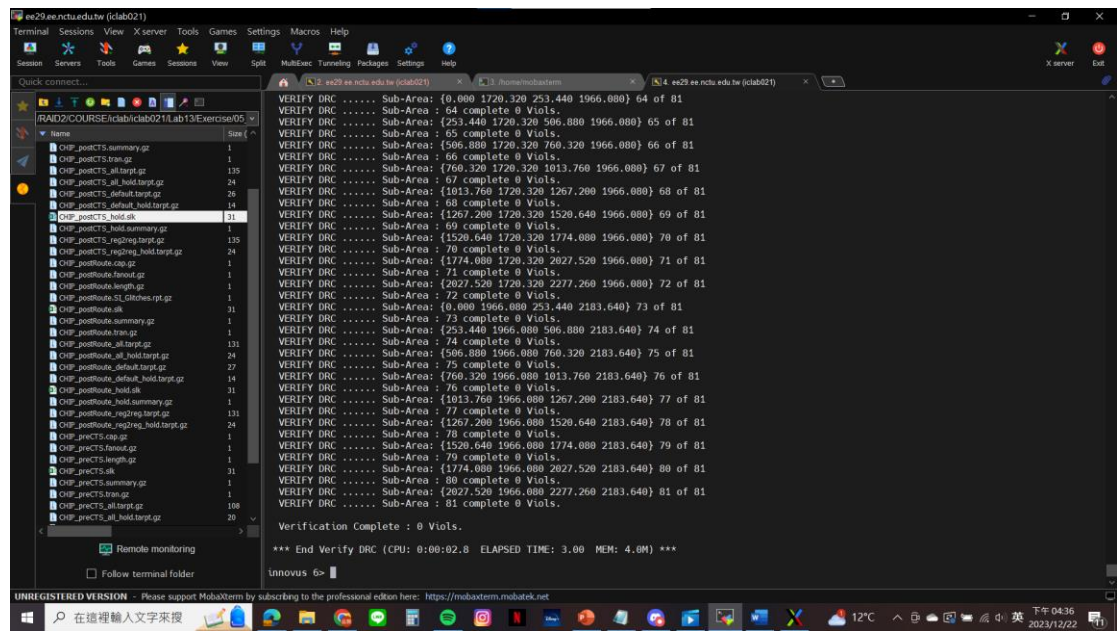
End delay calculation (fullDC). (MEM=2980.69 CPU=0:00:02.1 REAL=0:00:03.0)
End delay calculation (fullDC). (MEM=2980.69 CPU=0:00:02.1 REAL=0:00:03.0)
Loading CTE timing window with Teflowtype 9... (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 2980.7M)
Add other clocks and setupCtoAAEClockMapping during iter 1
Loading CTE timing window is completed (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 2980.7M)
Start delay calculation (fullDC) (1 T). (MEM=2943.81)
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Skipped = 0.
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Analyzed = 8930.
Total number of fetched objects 8930
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
AAE INFO-618: Total number of nets in the design is 8877, 0.0 percent of the nets selected for SI analysis
End delay calculation (fullDC). (MEM=2981.06 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=2981.06 CPU=0:00:00.1 REAL=0:00:00.0)
*** Done Building Timing Graph (cpus=0:00:02.8 real=0:00:03.0 totSessionCpu=0:05:22 mem=2982.0M)

Hold views included:
av_func_mode_min

Hold mode	all	reg2reg	default
MNS (ns):	0.233	0.233	9.819
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	371	281	370

Reported timing to dir timingReports
Total CPU time: 3.5 sec
Total Real time: 4.0 sec
Total Memory Usage: 2915.230469 Mbytes
Reset AAE Options
*** timeDesign #8 [finish] : cpu/real = 0:00:03.5/0:00:04.1 (0.8), totSession cpu/real = 0:05:22.5/0:23:01.6 (0.2), mem = 2915.2M

5. DRC result :



```
ee29.ee.nctu.edu.tw (iclab021)
Terminal Sessions View X server Tools Games Settings Macros Help
Quick connect...
RAID2\COURSE\iclab021\Lab13\Exercise05
Name Size
CHP_postCTS.summary.gz 1
CHP_postCTS.trace.gz 1
CHP_postCTS_all_target.gz 135
CHP_postCTS_all_hold_target.gz 24
CHP_postCTS_default_target.gz 26
CHP_postCTS_defult_hold_target.gz 24
CHP_postCTS_hold.sil 27
CHP_postCTS_hold.summary.gz 1
CHP_postCTS_regreg_target.gz 135
CHP_postCTS_regreg_hold_target.gz 24
CHP_postRoute.cap.gz 1
CHP_postRoute.fanout.gz 1
CHP_postRoute.length.gz 1
CHP_postRoute_SLCatches.rpt.gz 1
CHP_postRoute.sil 31
CHP_postRoute.summary.gz 1
CHP_postRoute.trace.gz 1
CHP_postRoute_all_target.gz 131
CHP_postRoute_all_hold_target.gz 24
CHP_postRoute_default_target.gz 27
CHP_postRoute_defult_hold_target.gz 24
CHP_postRoute_hold.sil 31
CHP_postRoute_hold.summary.gz 1
CHP_postRoute_regreg_target.gz 131
CHP_postRoute_regreg_hold_target.gz 24
CHP_preCTS.cap.gz 1
CHP_preCTS.fanout.gz 1
CHP_preCTS.length.gz 1
CHP_preCTS.sil 31
CHP_preCTS.summary.gz 1
CHP_preCTS.trace.gz 1
CHP_preCTS_all_target.gz 108
CHP_preCTS_all_hold_target.gz 20

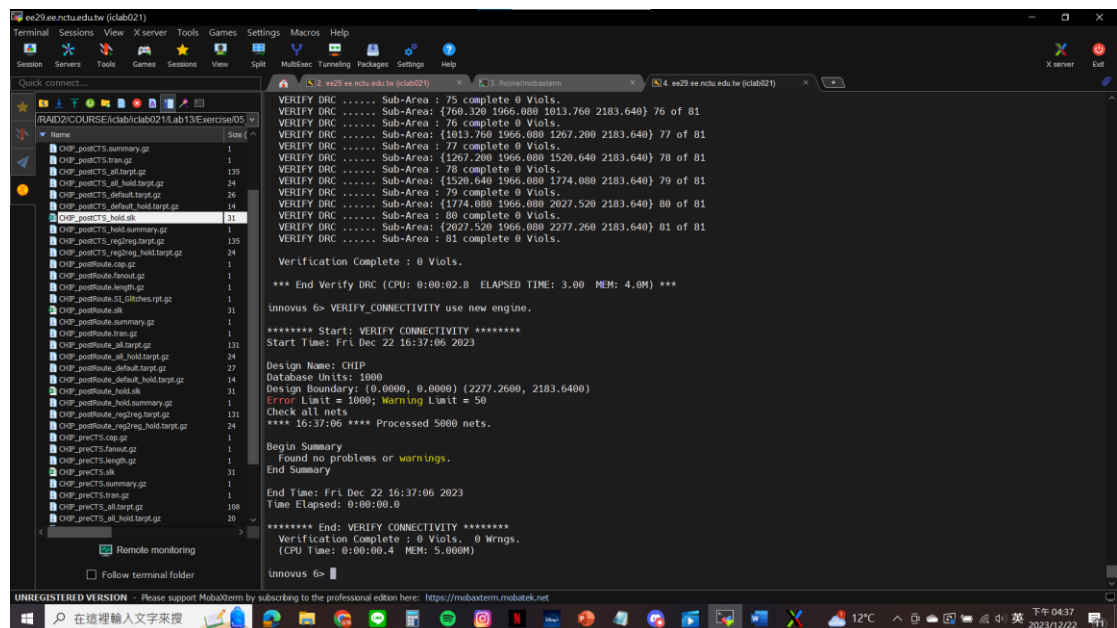
Remote monitoring
Follow terminal folder

UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: https://mobaxterm.mobatek.net

VERIFY DRC ..... Sub-Area: {0.000 1720.320 253.440 1966.080} 64 of 81
VERIFY DRC ..... Sub-Area: {253.440 1720.320 506.880 1966.080} 65 of 81
VERIFY DRC ..... Sub-Area: {506.880 1720.320 760.320 1966.080} 66 of 81
VERIFY DRC ..... Sub-Area: {760.320 1720.320 1013.760 1966.080} 67 of 81
VERIFY DRC ..... Sub-Area: {1013.760 1720.320 1267.200 1966.080} 68 of 81
VERIFY DRC ..... Sub-Area: {1267.200 1720.320 1520.640 1966.080} 69 of 81
VERIFY DRC ..... Sub-Area: {1520.640 1720.320 1774.080 1966.080} 70 of 81
VERIFY DRC ..... Sub-Area: {1774.080 1720.320 2027.520 1966.080} 71 of 81
VERIFY DRC ..... Sub-Area: {2027.520 1720.320 2277.260 1966.080} 72 of 81
VERIFY DRC ..... Sub-Area: {2277.260 1720.320 2530.720 1966.080} 73 of 81
VERIFY DRC ..... Sub-Area: {2530.720 1720.320 2784.160 1966.080} 74 of 81
VERIFY DRC ..... Sub-Area: {2784.160 1720.320 3037.600 1966.080} 75 of 81
VERIFY DRC ..... Sub-Area: {3037.600 1720.320 3291.040 1966.080} 76 of 81
VERIFY DRC ..... Sub-Area: {3291.040 1720.320 3544.480 1966.080} 77 of 81
VERIFY DRC ..... Sub-Area: {3544.480 1720.320 3797.920 1966.080} 78 of 81
VERIFY DRC ..... Sub-Area: {3797.920 1720.320 4051.360 1966.080} 79 of 81
VERIFY DRC ..... Sub-Area: {4051.360 1720.320 4304.800 1966.080} 80 of 81
VERIFY DRC ..... Sub-Area: {4304.800 1720.320 4558.240 1966.080} 81 of 81
Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:02.8 ELAPSED TIME: 3.00 MEM: 4.0M) ***
innovus 6>
```

6. LVS result :



```
ee29.ee.nctu.edu.tw (iclab021)
Terminal Sessions View X server Tools Games Settings Macros Help
Quick connect...
RAID2\COURSE\iclab021\Lab13\Exercise05
Name Size
CHP_postCTS.summary.gz 1
CHP_postCTS.trace.gz 1
CHP_postCTS_all_target.gz 135
CHP_postCTS_all_hold_target.gz 24
CHP_postCTS_default_target.gz 26
CHP_postCTS_defult_hold_target.gz 24
CHP_postCTS_hold.sil 27
CHP_postCTS_hold.summary.gz 1
CHP_postCTS_regreg_target.gz 135
CHP_postCTS_regreg_hold_target.gz 24
CHP_postRoute.cap.gz 1
CHP_postRoute.fanout.gz 1
CHP_postRoute.length.gz 1
CHP_postRoute_SLCatches.rpt.gz 1
CHP_postRoute.sil 31
CHP_postRoute.summary.gz 1
CHP_postRoute.trace.gz 1
CHP_postRoute_all_target.gz 131
CHP_postRoute_all_hold_target.gz 24
CHP_postRoute_default_target.gz 27
CHP_postRoute_defult_hold_target.gz 24
CHP_postRoute_hold.sil 31
CHP_postRoute_hold.summary.gz 1
CHP_postRoute_regreg_target.gz 131
CHP_postRoute_regreg_hold_target.gz 24
CHP_preCTS.cap.gz 1
CHP_preCTS.fanout.gz 1
CHP_preCTS.length.gz 1
CHP_preCTS.sil 31
CHP_preCTS.summary.gz 1
CHP_preCTS.trace.gz 1
CHP_preCTS_all_target.gz 108
CHP_preCTS_all_hold_target.gz 20

Remote monitoring
Follow terminal folder

UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: https://mobaxterm.mobatek.net

VERIFY DRC ..... Sub-Area: {0.000 1720.320 253.440 1966.080} 64 of 81
VERIFY DRC ..... Sub-Area: {253.440 1720.320 506.880 1966.080} 65 of 81
VERIFY DRC ..... Sub-Area: {506.880 1720.320 760.320 1966.080} 66 of 81
VERIFY DRC ..... Sub-Area: {760.320 1720.320 1013.760 1966.080} 67 of 81
VERIFY DRC ..... Sub-Area: {1013.760 1720.320 1267.200 1966.080} 68 of 81
VERIFY DRC ..... Sub-Area: {1267.200 1720.320 1520.640 1966.080} 69 of 81
VERIFY DRC ..... Sub-Area: {1520.640 1720.320 1774.080 1966.080} 70 of 81
VERIFY DRC ..... Sub-Area: {1774.080 1720.320 2027.520 1966.080} 71 of 81
VERIFY DRC ..... Sub-Area: {2027.520 1720.320 2277.260 1966.080} 72 of 81
VERIFY DRC ..... Sub-Area: {2277.260 1720.320 2530.720 1966.080} 73 of 81
VERIFY DRC ..... Sub-Area: {2530.720 1720.320 2784.160 1966.080} 74 of 81
VERIFY DRC ..... Sub-Area: {2784.160 1720.320 3037.600 1966.080} 75 of 81
VERIFY DRC ..... Sub-Area: {3037.600 1720.320 3291.040 1966.080} 76 of 81
VERIFY DRC ..... Sub-Area: {3291.040 1720.320 3544.480 1966.080} 77 of 81
VERIFY DRC ..... Sub-Area: {3544.480 1720.320 3797.920 1966.080} 78 of 81
VERIFY DRC ..... Sub-Area: {3797.920 1720.320 4051.360 1966.080} 79 of 81
VERIFY DRC ..... Sub-Area: {4051.360 1720.320 4304.800 1966.080} 80 of 81
VERIFY DRC ..... Sub-Area: {4304.800 1720.320 4558.240 1966.080} 81 of 81
Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:02.8 ELAPSED TIME: 3.00 MEM: 4.0M) ***
innovus 6> VERIFY CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Fri Dec 22 16:37:06 2023
Design Name: CHIP
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (2277.2600, 2183.6400)
Error Limit = 1000; Warning Limit = 50
**** 16:37:06 **** Processed 5000 nets.

Begin Summary
Found no problems or warnings.
End Summary

End Time: Fri Dec 22 16:37:06 2023
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wngs.
(CPU Time: 0:00:00.4 MEM: 5.000M)
innovus 6>
```

7. Post Layout simulation result :

```
ee29.ee.nctu.edu.tw (iclab021)
PASS PATTERN NO.1973
PASS PATTERN NO.1974
PASS PATTERN NO.1975
PASS PATTERN NO.1976
PASS PATTERN NO.1977
PASS PATTERN NO.1978
PASS PATTERN NO.1979
PASS PATTERN NO.1980
PASS PATTERN NO.1981
PASS PATTERN NO.1982
PASS PATTERN NO.1983
PASS PATTERN NO.1984
PASS PATTERN NO.1985
PASS PATTERN NO.1986
PASS PATTERN NO.1987
PASS PATTERN NO.1988
PASS PATTERN NO.1989
PASS PATTERN NO.1990
PASS PATTERN NO.1991
PASS PATTERN NO.1992
PASS PATTERN NO.1993
PASS PATTERN NO.1994
PASS PATTERN NO.1995
PASS PATTERN NO.1996
PASS PATTERN NO.1997
PASS PATTERN NO.1998
PASS PATTERN NO.1999

-----
Congratulations!
You have passed all patterns!
Your execution cycles = 32000 cycles
Your clock period = 20.0 ns
Total Latency = 640000.0 ns
-----
$finish called from file "PATTERN.v", line 36.
$finish at simulation time      1819638000
VCS Simulation Report
Time: 1819638000 ps
CPU Time: 26.930 seconds;      Data structure size: 2.2M
Fri Dec 22 16:38:06 2023
CPU time: 2.029 seconds to compile + .425 seconds to elab + .696 seconds to link + 26.974 seconds in simulation
16:38 iclab021@ee29[~/Lab13/Exercise/06_POST]$

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```

8. Power result :

```
ee29.ee.nctu.edu.tw (iclab021)
** WARN: (VOLTUS_POWER-2152): Instance GNDP6 (GND100) has no static power.
** WARN: (VOLTUS_POWER-2152): Instance VDDP7 (VCC3100) has no static power.
** WARN: (VOLTUS_POWER-2152): Instance GNDP7 (GND107) has no static power.
** WARN: (VOLTUS_POWER-2152): Instance VDDP8 (VCC3100) has no static power.
** WARN: (VOLTUS_POWER-2152): Instance GNDP8 (GND108) has no static power.
** WARN: (VOLTUS_POWER-2152): Instance VDDP9 (VCC3100) has no static power.
** WARN: (VOLTUS_POWER-2152): Instance GNDP9 (GND109) has no static power.
** WARN: (EMS-27): Message (VOLTUS_POWER-2152) has exceeded the current message display limit of 20.
To increase the message display limit, refer to the product command reference manual.
*

Total Power
-----
Total Internal Power:      0.13013477      43.8394%
Total Switching Power:    10.40634960      56.1133%
Total Leakage Power:      0.00876714      0.0473%
Total Power:              10.54525152

** WARN: (VOLTUS_POWER-2041): There are some instances in the design which are not connected to any power or ground nets.
These instances will be added to default power/ground rail uti files.
Use 'ltoputil list -uti-file' command to get the list of instances.
** WARN: (VOLTUS_POWER-3424): Cell AN2 has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWER-3424): Cell A012S has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWER-3424): Cell 0A12P has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWER-3424): Cell 0A12HS has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWER-3424): Cell INV12CK has no power pin defined in LEF/PGV.

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```

9. IR Drop Results :

使用兩組power ring，每組裡面包含11組VCC和GND，且使用四組stripes(metal 2, 3, 4, 5)，每條stripe的寬度為5。

