# ICLAB, Autumn 2023 (IEE 535224)

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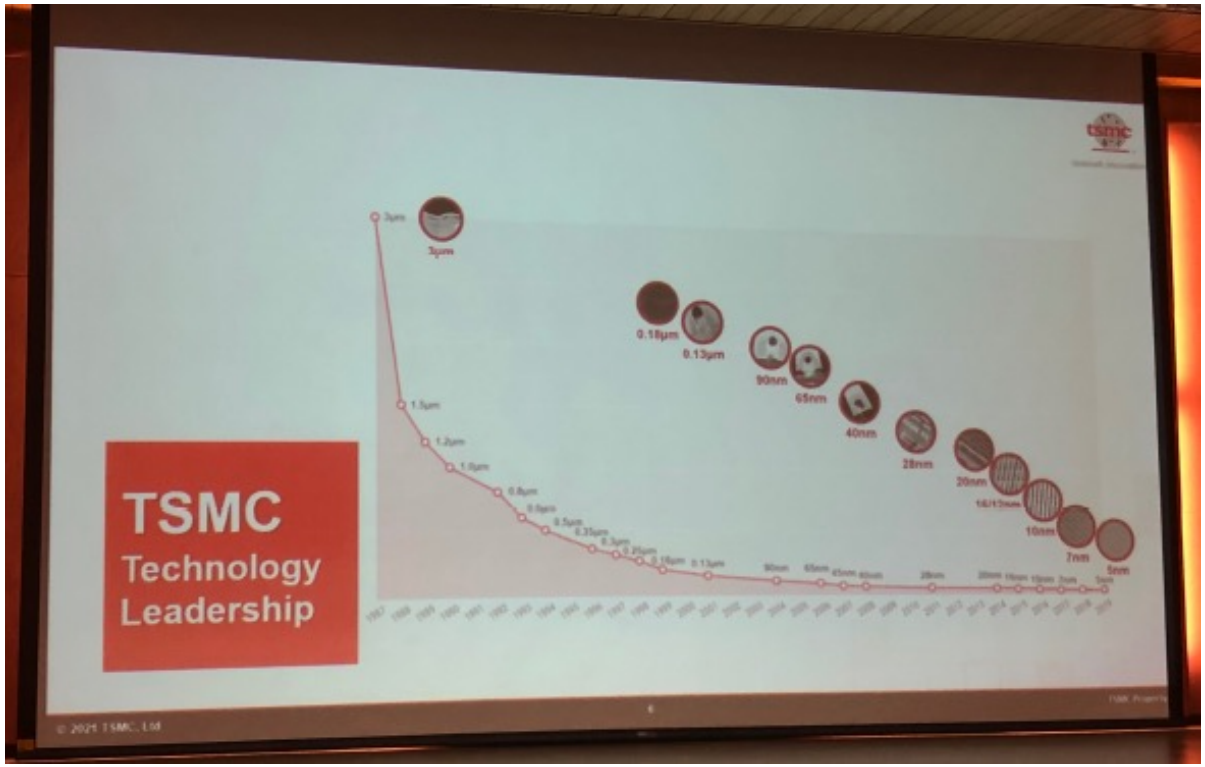
# TSMC Technology Roadmap (1/4)

- Paradigm Shift: from Intel to TSMC
- Who hits the 7nm Wall?



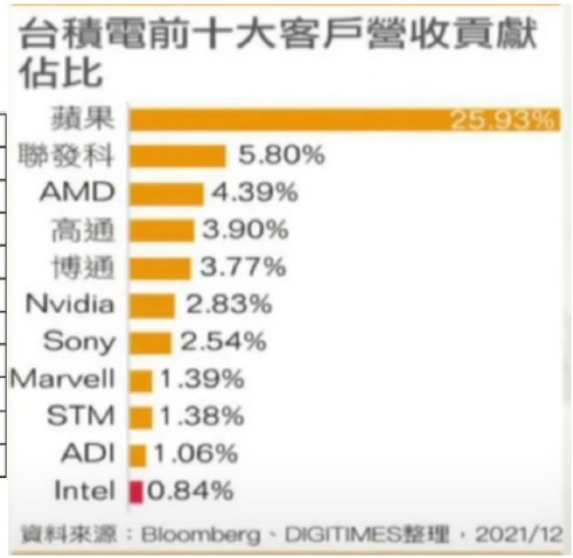
# TSMC Technology Roadmap (2/4)

- Ax processors fabricated in tsmc for iPhones, Mac, Pads, …

# TSMC Technology Roadmap (3/4)

- Top 10 customers in tsmc

| Table 4 – TSMC Customer Share of Revenues 2019-2021 | | | |
|---|---|---|---|
| | 2019 | 2020 | 2021 |
| Apple | 24.0% | 24.2% | 25.4% |
| Hi-Silicon | 15.0% | 12.8% | 0.0% |
| Qualcomm | 6.1% | 9.8% | 7.6% |
| NVIDIA | 7.6% | 7.7% | 5.8% |
| Broadcom | 7.7% | 7.6% | 8.1% |
| AMD | 4.0% | 7.3% | 9.2% |
| Intel | 5.2% | 6.0% | 7.2% |
| Mediatek | 4.3% | 5.9% | 8.2% |
| Source: The Information Network (www.theinformationnet.com) | | | |




**研調：台積電第3季可望超車三星 首登全球半導體龍頭**

1 中央社

2022年9月8日 週四 下午12:42

Over $20B in 2022/Q3

# TSMC Technology Roadmap (4/4)

- Silicon Wafer Cost


Over $20B in 2022/Q3

# Course Outline

- Design Trend
- Lab Contents
- Lab Items
- Scoring Rules
- Other Issues

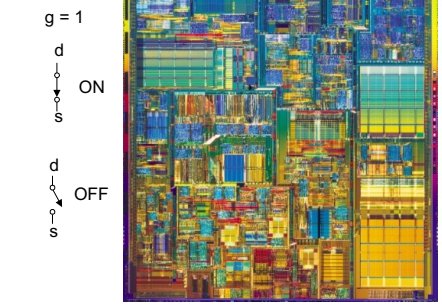

(source: MacRumors)

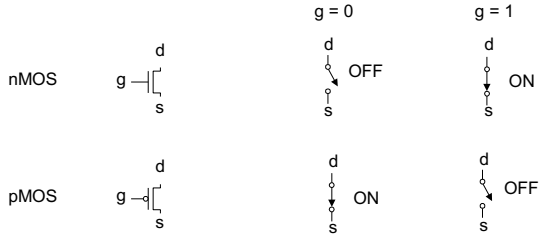
創新科技

**顯示器採用全新工藝與科技，精準貼合機身弧度的設計，一直延伸至優雅圓潤的邊角。**

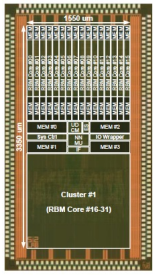
# Design Trend

- **Transistor**
- **Circuit**
- **Chip Architecture**
- **System and Application**
- **Smart Sensing + Low Power + Low Energy**
- **Data generation (IoT) and processing (AI or Learning)**
- **Toward Si-Civilization**

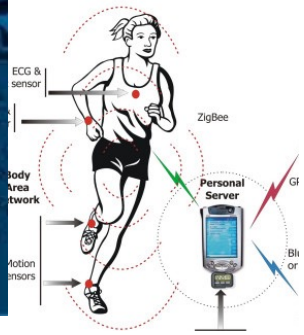




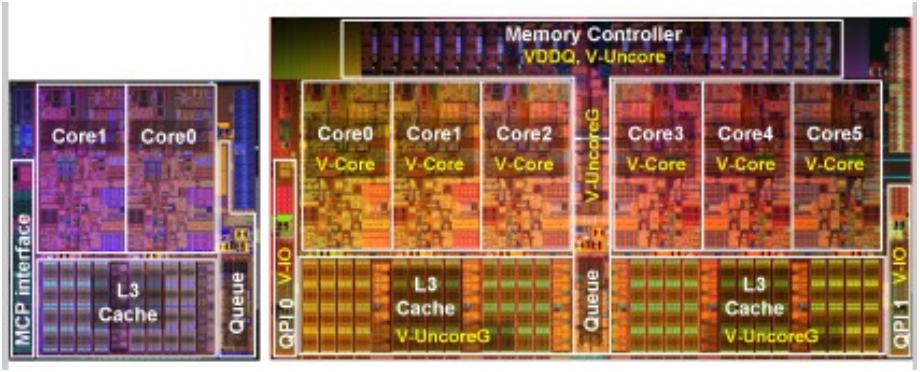
| RBM-P Chip Summary | |
|---|---|
| Technology | UMC 65nm 1P10M CMOS |
| Chip Size | 4.0mm x 2.2mm |
| Gate Count | 2.2M Gates |
| On-chip Memory | 128kB SRAM |
| Working Frequency | 210 MHz @ 1.2V |
| **Machine Learning Spec.** | |
| Applied Algorithm | Neural Network |
| Model Training | Restricted Boltzmann Machine |
| Number of Cores | 32 RBM Cores in 2 Clusters |
| Data Dimension | 4096 Neurons / Layer |
| Classification | 128 Candidates / sample |
| **On-chip Learning Performance @CD2** | |
| Throughput | 7.53G NWs / sec (GNWPS) |
| Energy Efficiency | 41.31 pJ / NW |
| **On-chip Inference Performance** | |
| Throughput | 11.63G NWs / sec (GNWPS) |
| Energy Efficiency | 26.74 pJ / NW |

# Westmere: A Family of 32nm IA Processors (ISSCC'2010->2019)

- The 6-core design has 1.17B transistors including the 12MB shared L3 Cache
- supports new instructions for accelerating encryption/decryption algorithms,
- speeds up performance under virtualized environments, and contains a host of other targeted performance features.
- AI engines for data-driven applications

# Westmere: A Family of 32nm IA Processors (ISSCC'2010)

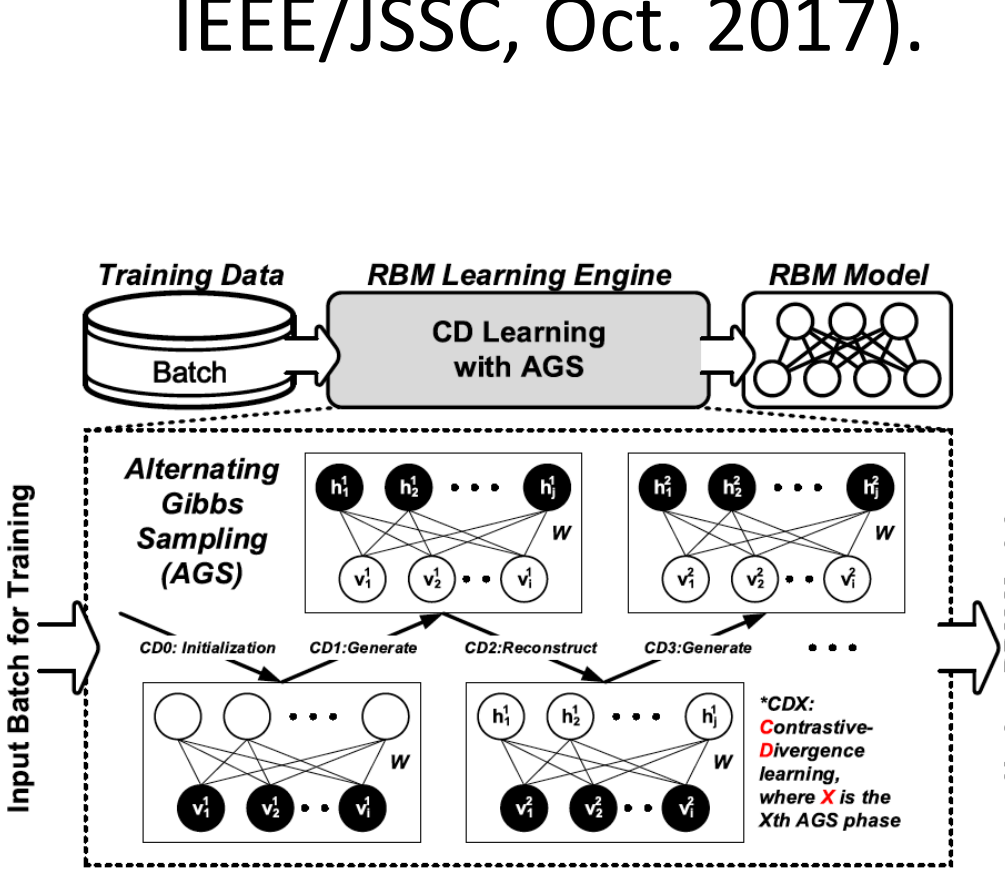


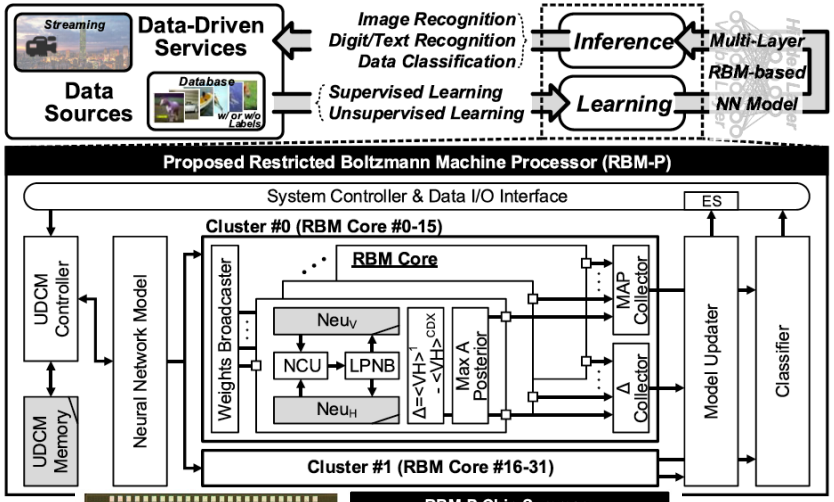

| Processor Name | Process Technology | Number of Cores | L3 Cache Size | Die Size | Transistor Count | Core Voltage Range | TDP Range |
|---|---|---|---|---|---|---|---|
| Nehalem - 4Core | 45 nm | 4 | 8 MB | 262 mm2 | 731 Million | 0.75V-1.25V | 60-130 Watts |
| Westmere - 6Core | 32 nm | 6 | 12 MB | 240 mm2 | 1.17 Billion | 0.72V-1.20V | 60-130 Watts |
| Westmere - 2Core | 32 nm | 2 | 4 MB | 78 mm2 | 384 Million | 0.72V-1.20V | 10-50 Watts |

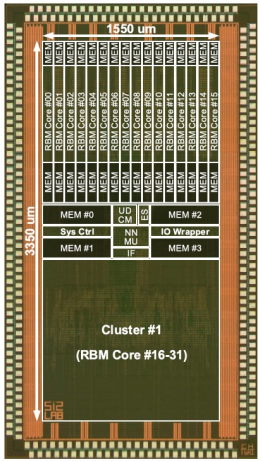
Figure 5.1.1: Westmere 6-Core Dual Socket Server and Westmere 2-Core Client Configurations.

# Data Processor for AI-based Applications

- AI Chip for training and inference (Tsai et.al., IEEE/JSSC, Oct. 2017).

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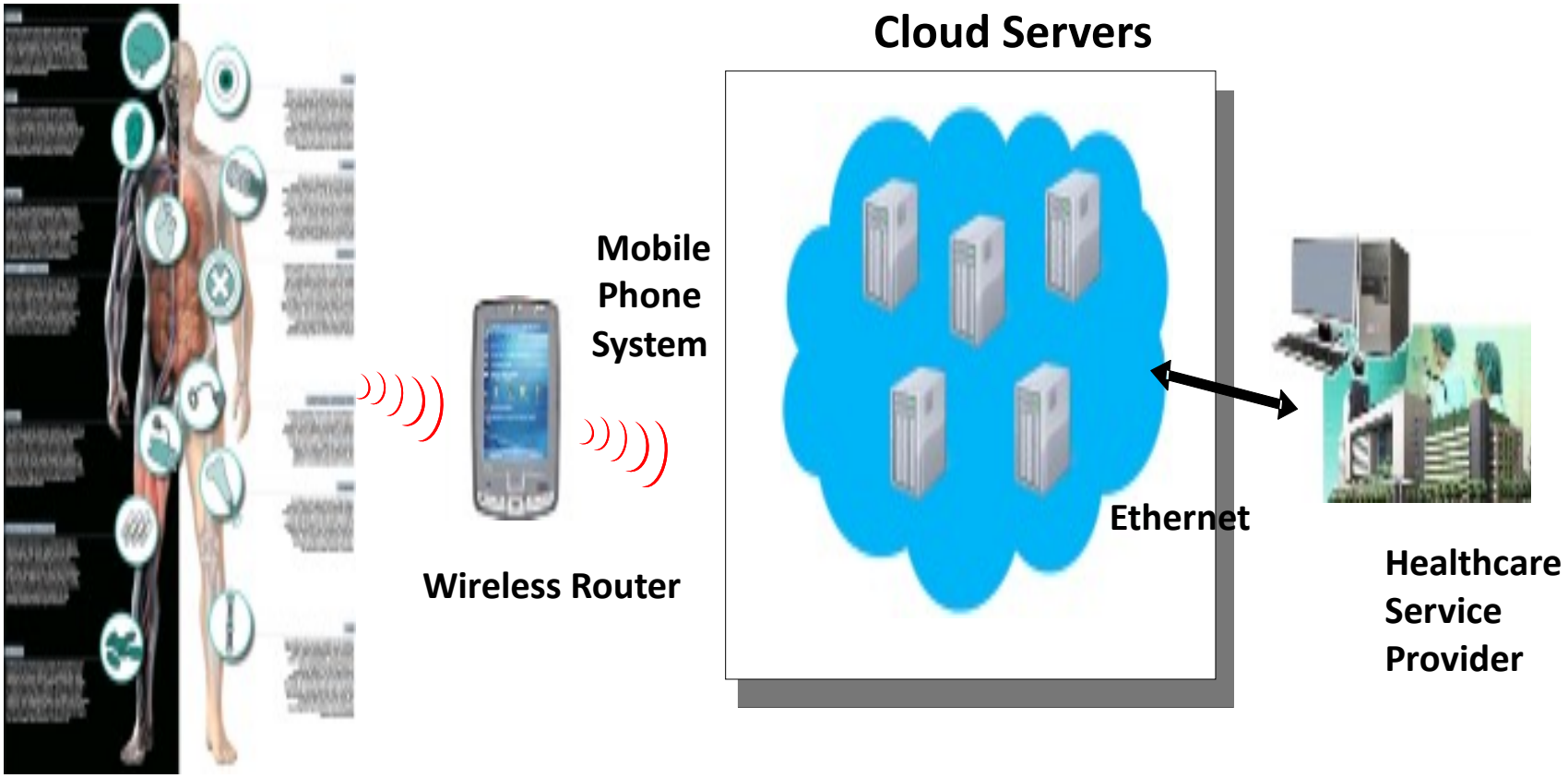
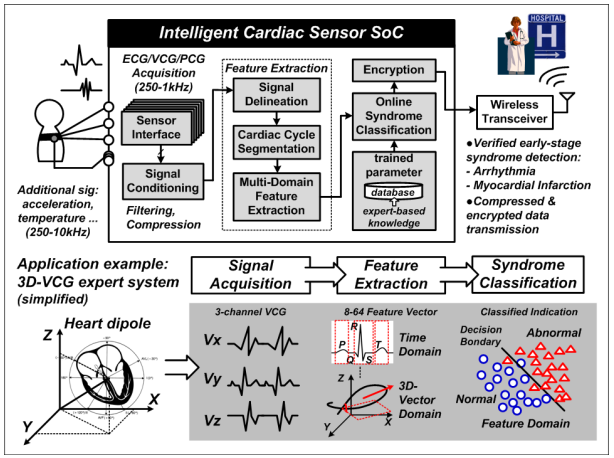
# Intelligent Processors for Bio (1/2)

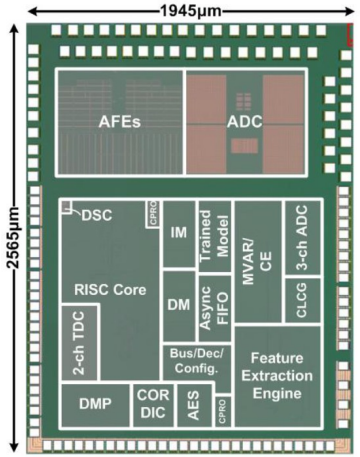
- New Opportunities for Academic Research/Industrial Applications Toward Better Life



# Intelligent Processor for BioMedical Applications (2/2)

- ML-Assisted CSP (G3, Hsu et. al, IEEE/JSSC2014)

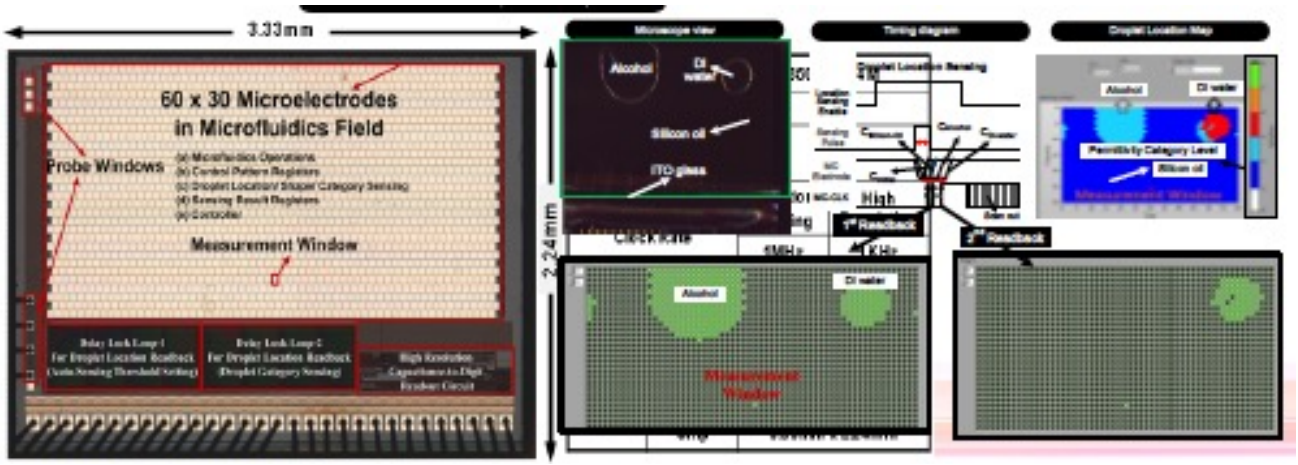



| | |
|---|---|
| Technology | UMC 90nm Standard CMOS |
| Chip Area | 2565mm×1945mm |
| Supply Voltage | 0.5-1.0V (0.7-1.0V for SRAM) |
| CLCG Frequency | 8-32kHz (System)<br>25/40MHz (Signal Processing) |
| Sensor Interface | 8/12-bit, 250-10kS/s<br>BW: 0.5-160Hz (tunable)<br>AFE Gain: 26-46dB (tunable) |
| Input Signal | 3-ch ECG/VCG, 1-ch PCG,<br>Other support signal |
| SoC Power | 19.4µW (CLCG)<br>7-32.8µW (Digital)<br>9.1-53µW (Sensor Interfaces) |
| ML-Assisted Statistical Analysis | MVAR Coefficient Estimator<br>SA (Skewness/Kurtosis)<br>MLC/SVM Classifications |
| Latency | 1 cardiac cycle (<2s@30bpm) |
| Detection Rate | >95.8% (Arrhythmia*)<br>>99% (MI†) |

*Verified using in-house recorded data (707 ECG records)
†Verified using MIT-PTB database (448 VCG records)

- Lab-on-a-Chip (Li et.al., IEEE/TCAD, TBMCAS)



# Deep Learning SoC's (AI)

- De-clouding: intelligence can be achieved in local devices, instead of cloud (data center)
  - See iLi technology.
- Various deep learning chips have been published in conferences/journals
- Performance depends on how many neurons and memory-bandwidth are allowed, especially dealing with real-time tests (inference).
- See iLi Wearable translator in Japan.

# Lab Contents (Part-I)

- A Top-Down Design Flow
  - Design methodology
  - CAD tools
- Behavioral (Abstract) Level Design
  - System design
  - Architecture design
  - Logic design
- Front-end simulation and synthesis tools
  - Behavioral correctness in different levels
  - Performance indices
  - testability

# Lab Contents (Cont'd)

- Physical Design
  - Floorplanning
  - Placement
  - Routing
- Back-end Simulation and Verification Tools
  - Back annotation
  - Timing closure
  - Manufacturability
  - …

# Lectures on Design Issues

- Modern IC Design Flow
  - Learn the current design flow
  - Complete an IC project in reasonable time
- Low-Power Low-Voltage Design
  - Mainly driven by mobile devices due to limited battery life
  - Remain a critical design issue in complex IC's
- Power Integrity in System-Level Design
  - IC design should take package model into account
  - Ensure functional in working environment

# Modern IC Design Flow

- Building blocks: IP-based/cell-based functional units, sensors, processors, storage units, I/O interfaces, …
- Simulation: timing and power
- Verification: equivalence checking
- Testability: design for testing and manufacturing
- Exploit design tools efficiently and effectively

# Low-Power Low-Voltage Design

- Mainly for mobile and sensing devices
- Exploit system behavior to reduce computational redundancy (i.e. switching activity)
- Explore architecture to reduce operational frequency and supply voltage
- Investigate circuit topology to save energy
- Innovate electron devices having better $I_{on}/I_{off}$

# Power Integrity in System-Level Design

- Voltage drop will affect timing and hence operational speed $V(t) = I(t)*R + C*dv/dt*R + L*di/dt$
- Package model should be included in design phase
- Decoupling circuits should be included to reduce dynamic voltage drop
- Apply a set of power pads to minimize transient currents through bonding wires

# Scoring Rules and TA's

**TA List:**

| Name | Email | Ext | Office |
|---|---|---|---|
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| 張庭瑜 | tim.jeffrey10.ee12@nycu.edu.tw | 54238 | ED430 |
| 翁沐昀 | henryrabbit0.st11@nycu.edu.tw | 54238 | ED430 |
| 連紹華 | eed0810766.eed08@nctu.edu.tw | 54238 | EIC213 |
| 莊彥騰 | austin.311.111.ee11@nycu.edu.tw | 54238 | ED317A |
| 李家毓 | maggie8905121.ee11@nycu.edu.tw | 54238 | ED317A |

# Other Issues

- Lecture
  - In-Person at ED415 (On-line or Hybrid if needed)
- Circuit/Chip trend
  - Refer ISSCC and IEEE/JSSC
- EDA trend
  - Refer DAC/ICCAD and IEEE/TCAD
- Office Hours
  - Wed. 15:30~17:00 (ED538, via email booking)

# Just a Reminder

哈佛圖書館的二十條訓言：

**20 maxims at Harvard Library,**

**1.**此刻打盹，你將做夢；而此刻學習，你將圓夢。

**Fall asleep, you'll make a dream; study hard, the dream will be realized.**

**…**