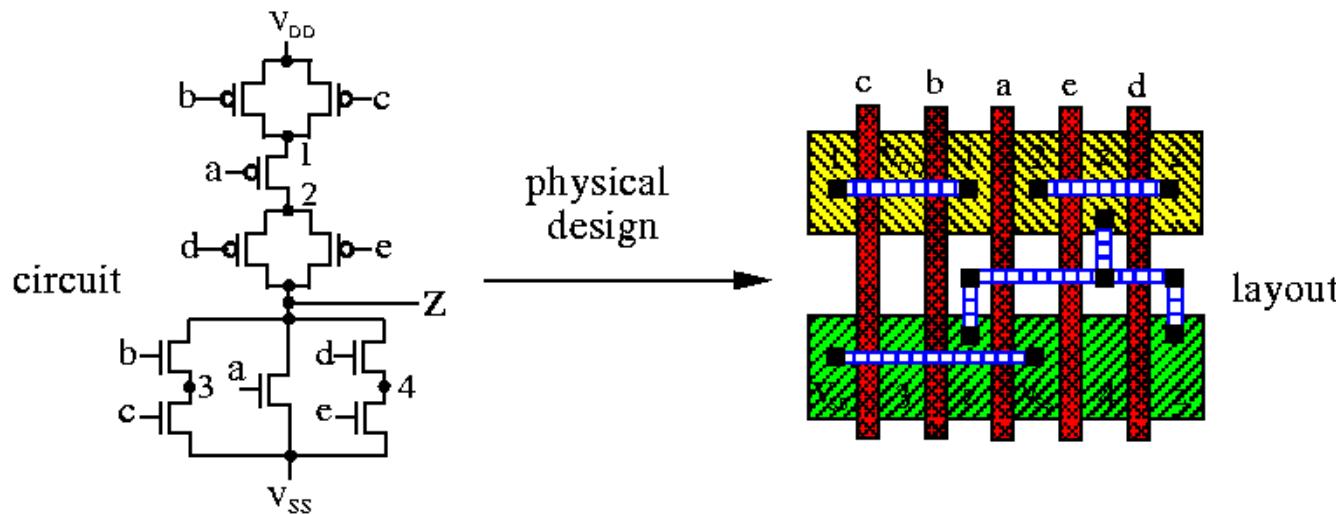
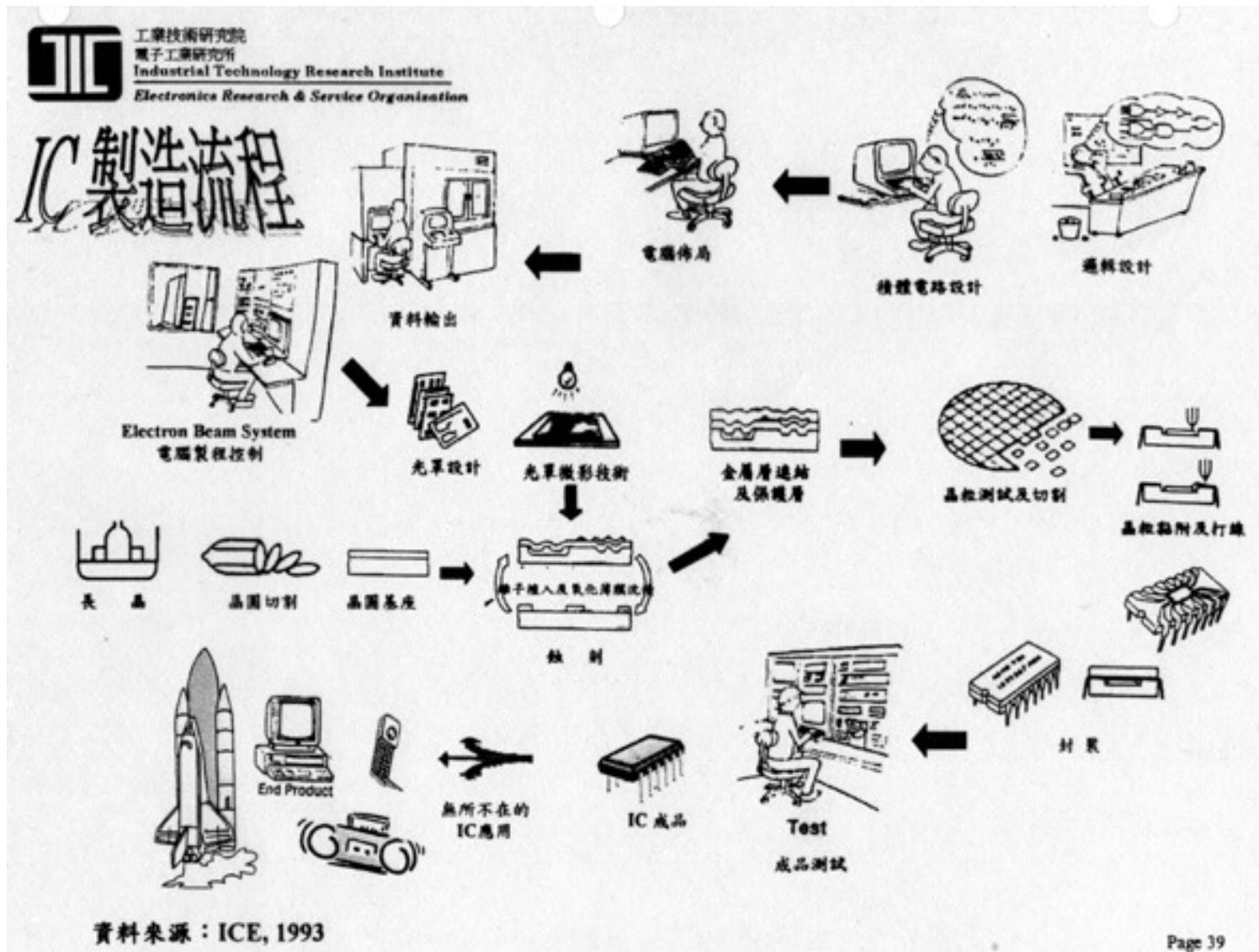


Unit 1: Introduction

- Course contents:
 - Introduction to VLSI design flow
 - Introduction to physical design automation
 - Semiconductor technology roadmap
- Readings
 - W&C&C: Chapter 1
 - S&Y: Chapter 1



IC Design & Manufacturing Process



From Wafer to Chip

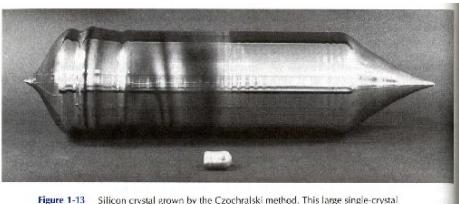


Figure 1-13 Silicon crystal grown by the Czochralski method. This large single-crystal ingot provides 20-cm (8-in.)-diameter wafers when sliced using a diamond saw; for size comparison, a small ingot (less than one inch in diameter) from the 1950s is also shown. (Photograph courtesy of MLMIC Electronic Materials, Inc.)

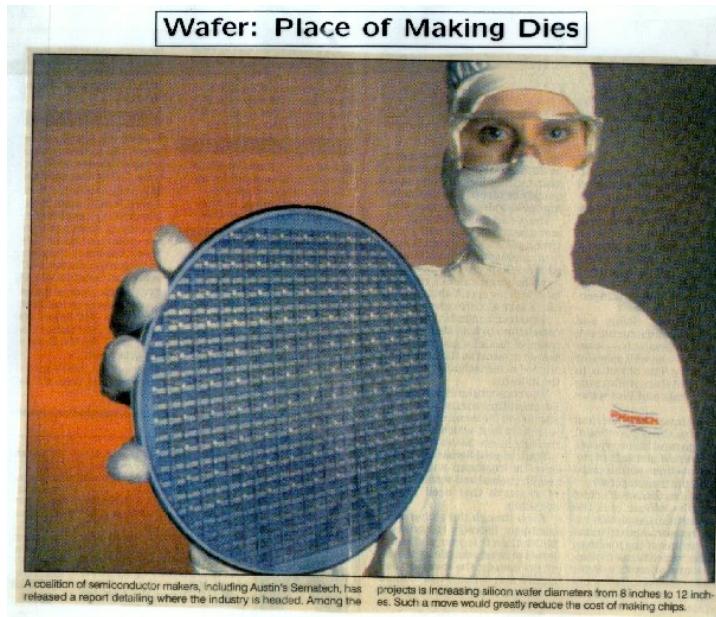
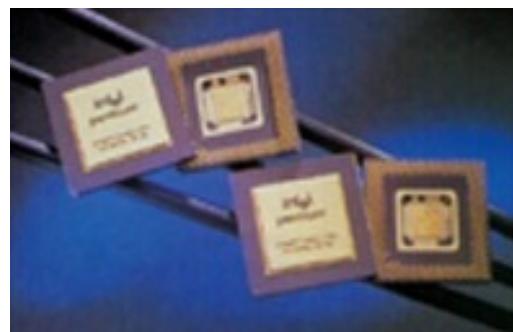


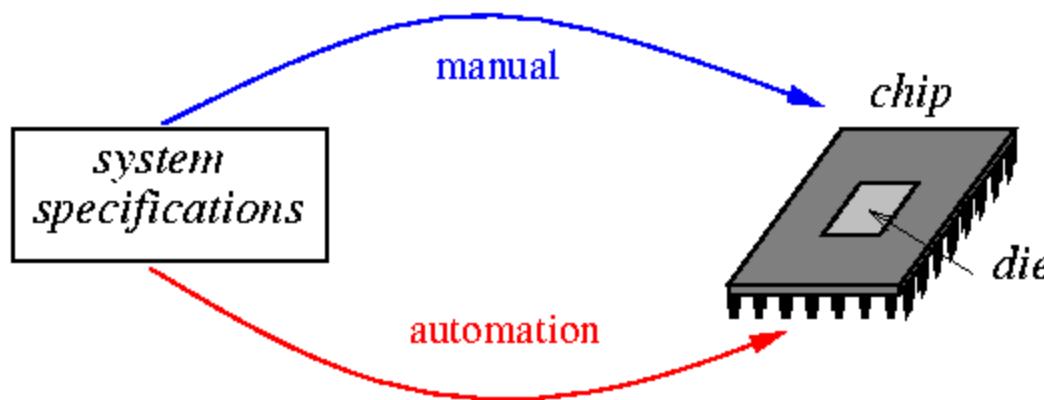
Figure 9-34
Attachment of leads from the Al pads on the periphery of the chip to posts on the package.
Photograph courtesy of Motorola, Inc.)



Wk P.-H. Lin [Courtesy of Y.-W. Chang, H.-M Chen]



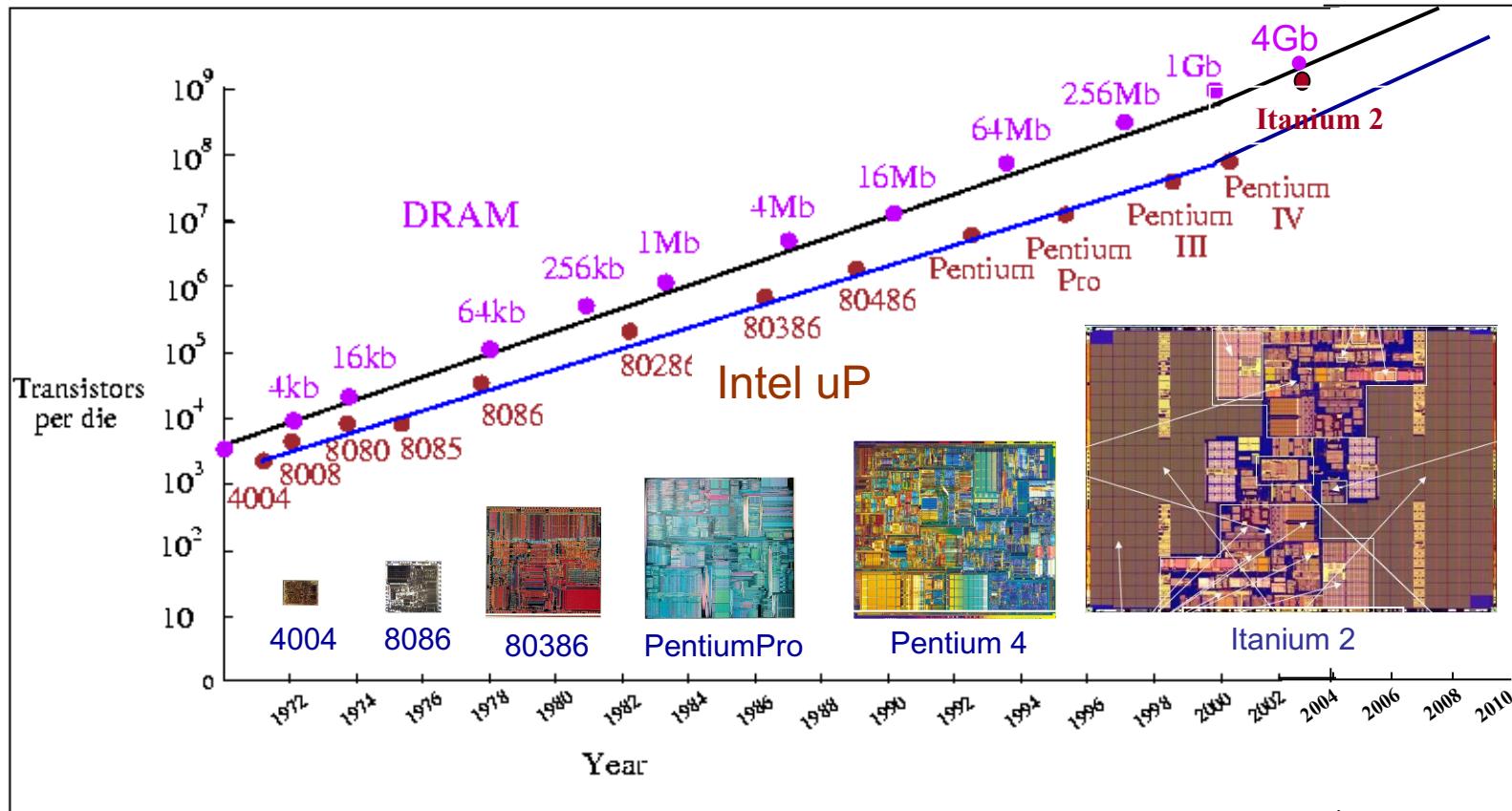
IC Design Considerations



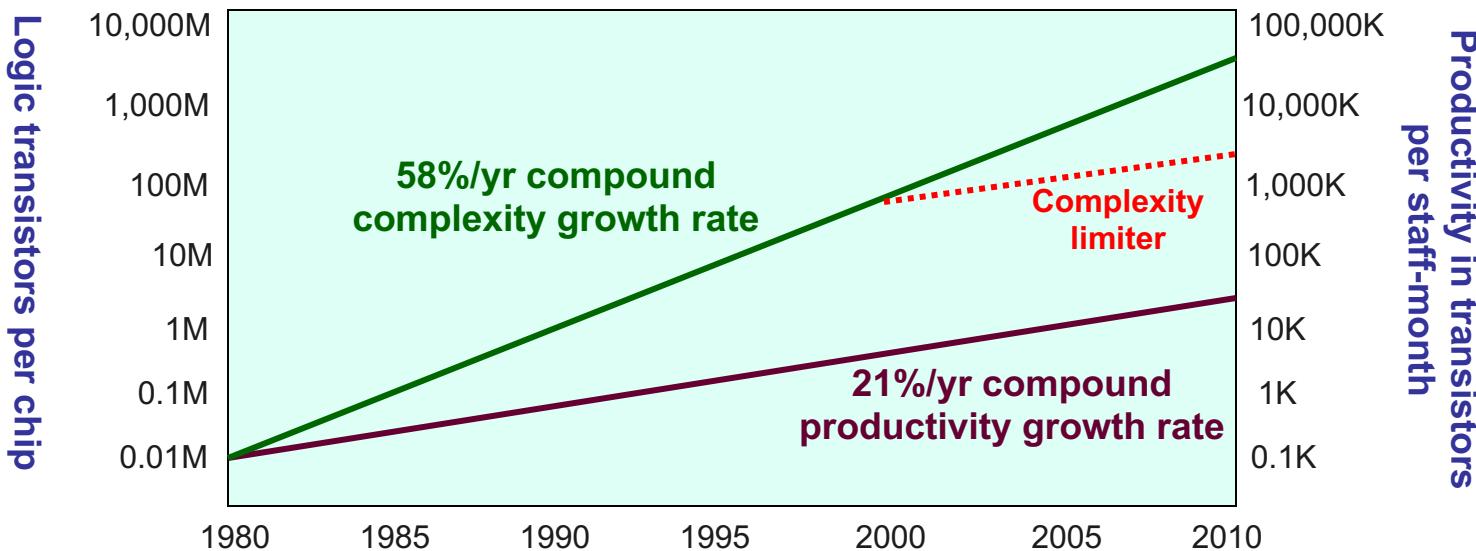
- Several conflicting considerations:
 - **Design Complexity:** large number of devices/transistors
 - **Performance:** optimization requirements for high performance
 - **Time-to-market:** about a 15% gain for early birds
 - **Cost:** die **area**, packaging, testing, etc.
 - Others: power, signal integrity (noise, etc.), testability, reliability, manufacturability, etc.

“Moore’s” Law: Driving Technology Advances

- Logic capacity doubles per IC at a regular interval (say, 18 months).
 - G. Moore: Logic capacity doubles per IC every two years (1975).
 - D. House: Computer performance doubles every 18 months (1975)



Design Productivity Crisis



- Human factors may limit design more than technology.
- Keys to solve the productivity crisis: **CAD (tool & methodology)**, hierarchical design, abstraction, IP reuse, platform-based design, etc.

Technology Roadmap for Semiconductors

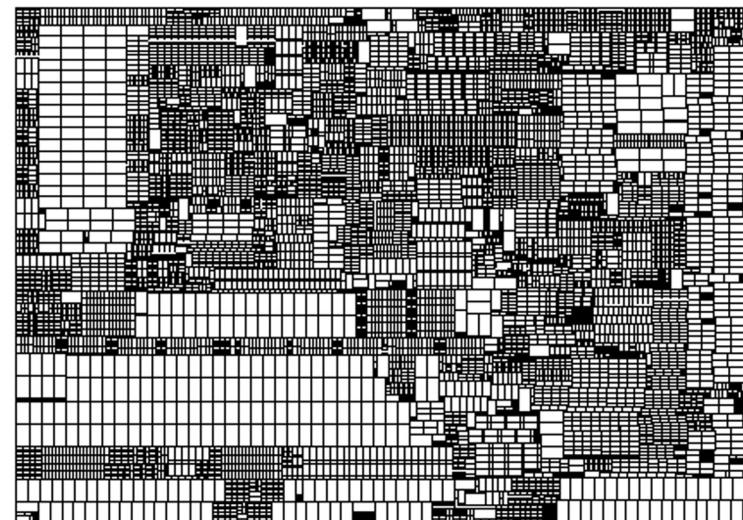
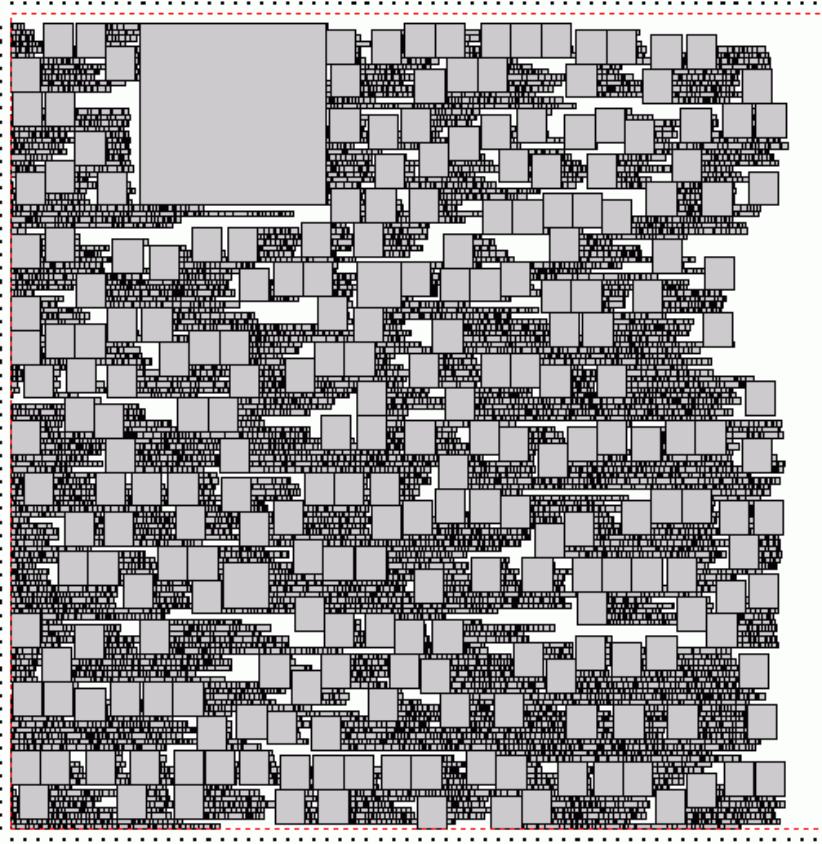
Year	1997	1999	2002	2005	2008	2011	2014
Technology node (nm)	250	180	130	100	70	50	35
On-chip local clock (GHz)	0.75	1.25	2.1	3.5	6.0	10	16.9
Microprocessor chip size (mm^2)	300	340	430	520	620	750	901
Microprocessor transistors/chip	11M	21M	76M	200M	520M	1.40B	3.62B
Microprocessor cost/transistor ($\times 10^{-8}$ USD)	3000	1735	580	255	110	49	22
DRAM bits per chip	256M	1G	4G	16G	64G	256G	1T
Wiring level	6	6–7	7	7–8	8–9	9	10
Supply voltage (V)	1.8–2.5	1.5–1.8	1.2–1.5	0.9–1.2	0.6–0.9	0.5–0.6	0.37–0.42
Power (W)	70	90	130	160	170	175	183

- Source: International Technology Roadmap for Semiconductors (easier to see the past & trend with the older version; for more recent update, see <http://www.itrs.net/>).
- Deep submicron technology: node (**feature size**) $< 0.25 \mu m$.
- Nanometer Technology: node $< 0.1 \mu m$.

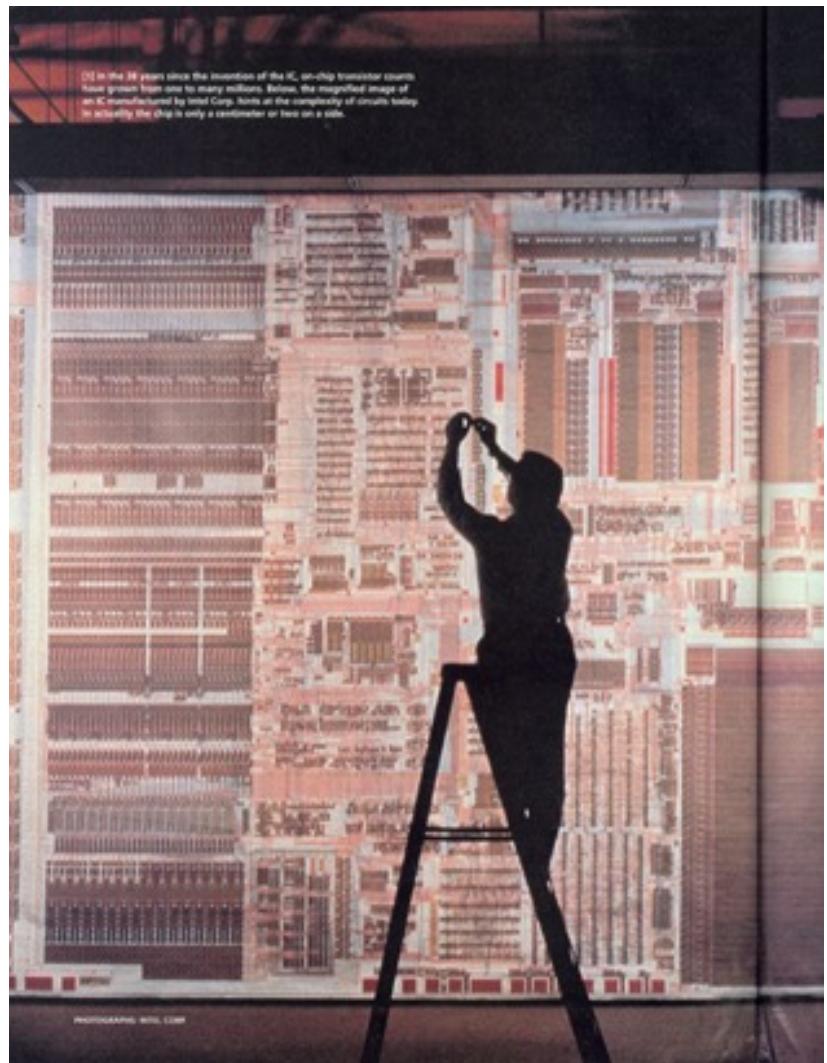
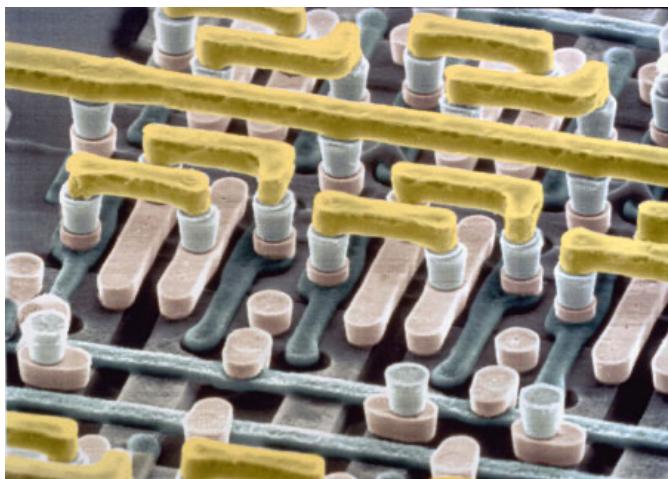
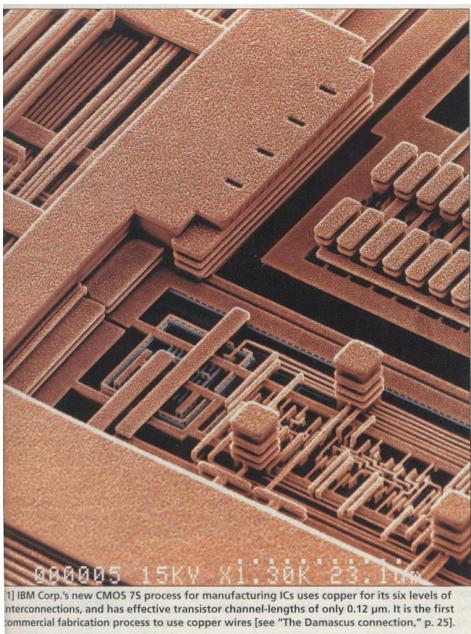
Nanometer Design Challenges

- Intel Core 2 Extreme X6800: feature size $\approx 65 \text{ nm}$, μP frequency $\approx 3.47 \text{ GHz}$ (over), die size $\approx 143 \text{ mm}^2$, μP transistor count per chip $\approx 291\text{M}$, wiring level ≈ 10 layers, supply voltage $\approx 1.28 \text{ V}$, power consumption $\approx 232 \text{ W}$ (full load)
 - **Feature size \downarrow** : sub-wavelength lithography (impacts of process variation)? reliability? noise? wire coupling?
 - **Frequency \uparrow , dimension \uparrow** : interconnect delay? electromagnetic field effects? timing closure?
 - **Chip complexity \uparrow** : large-scale system design methodology?
 - **Supply voltage \downarrow** : signal integrity (noise, IR drop, etc)?
 - **Wiring level \uparrow** : manufacturability? yield? 3D layout?
 - **Power consumption/density \uparrow** : power & thermal issues?

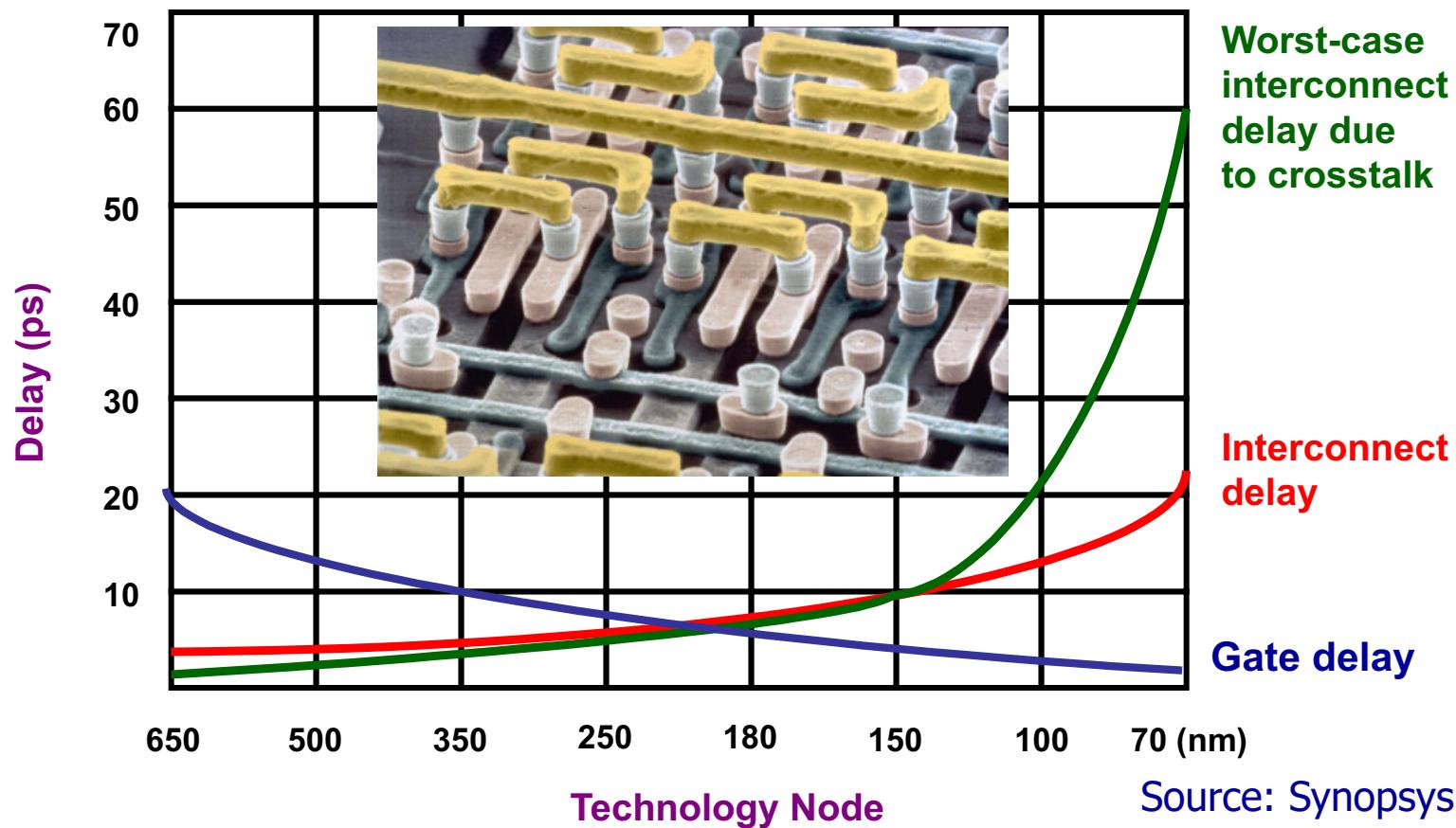
Design Complexity Increases Dramatically!!



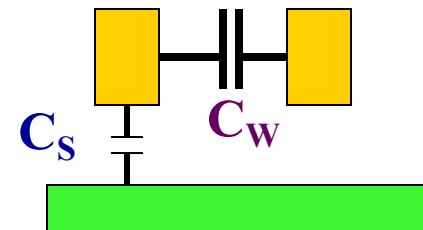
High IC Complexity



Interconnect Dominates Circuit Performance!!

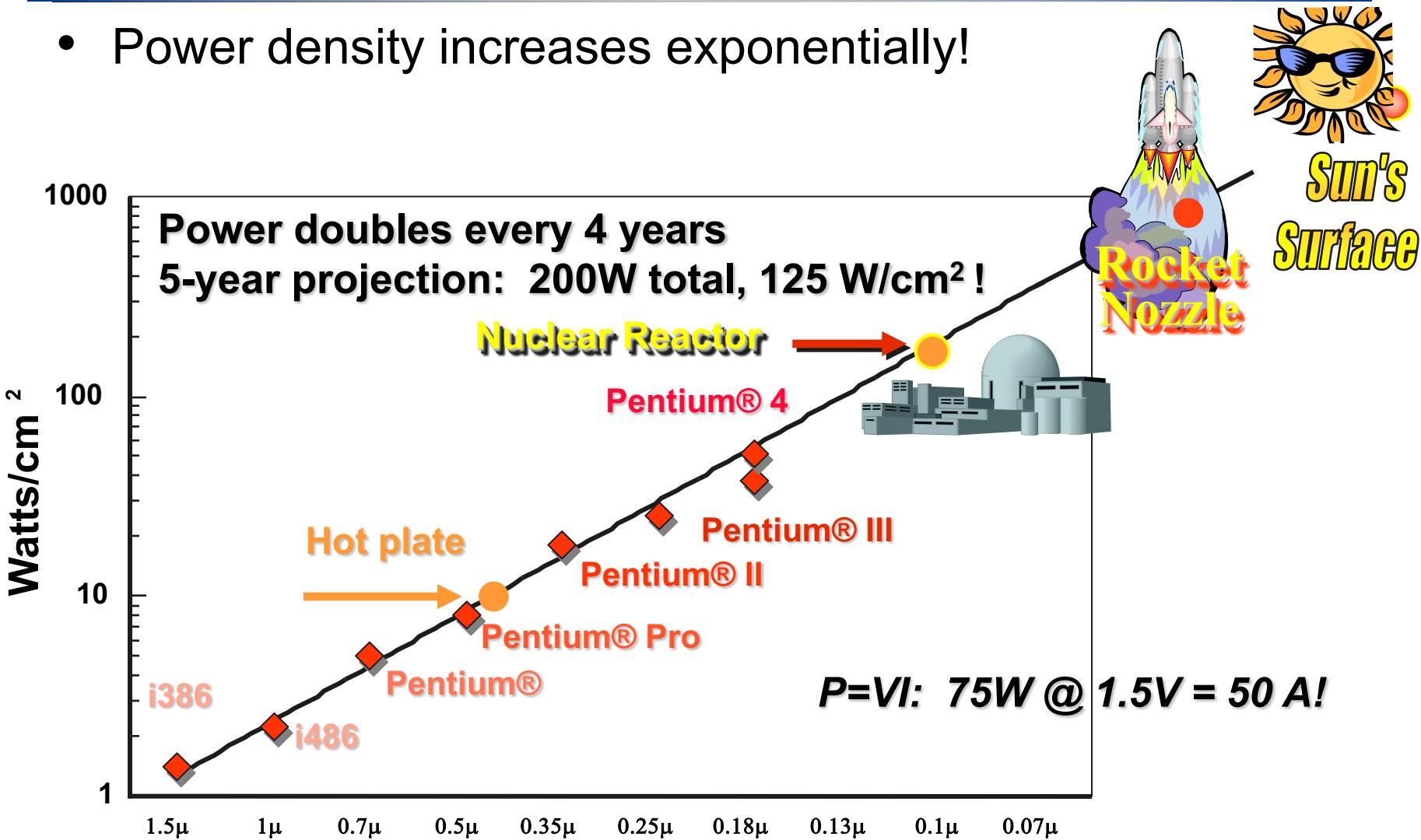


In $\leq 0.18\mu\text{m}$ wire-to-wire
capacitance dominates ($C_W \gg C_S$)



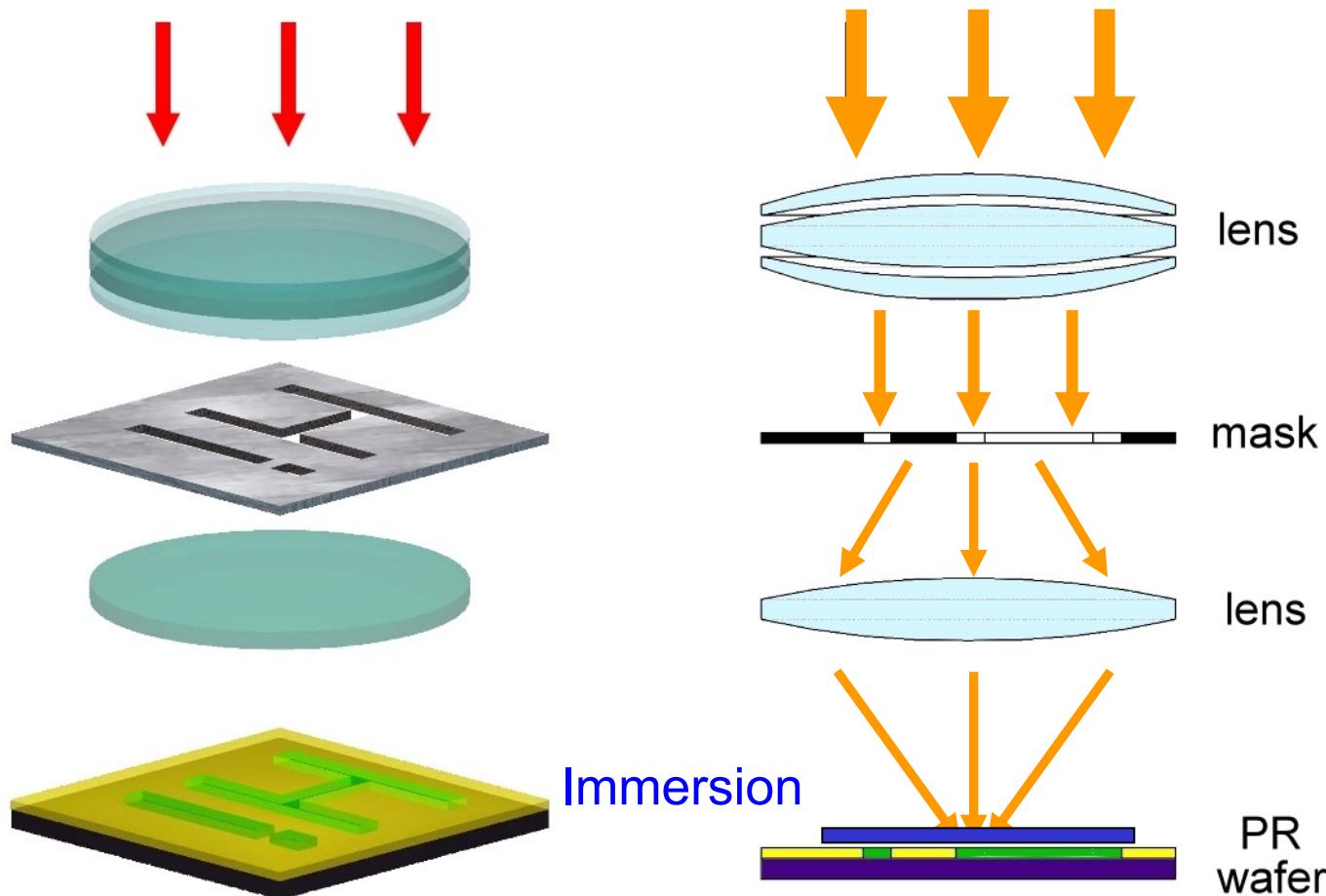
Power/Thermal Is Another Big Problem!!

- Power density increases exponentially!



Fred Pollack, "New Microarchitecture Challenges in the Coming Generations of CMOS Process Technologies," 1999 Micro32 Conference keynote. Courtesy Avi Mendelson, Intel.

Lithography System

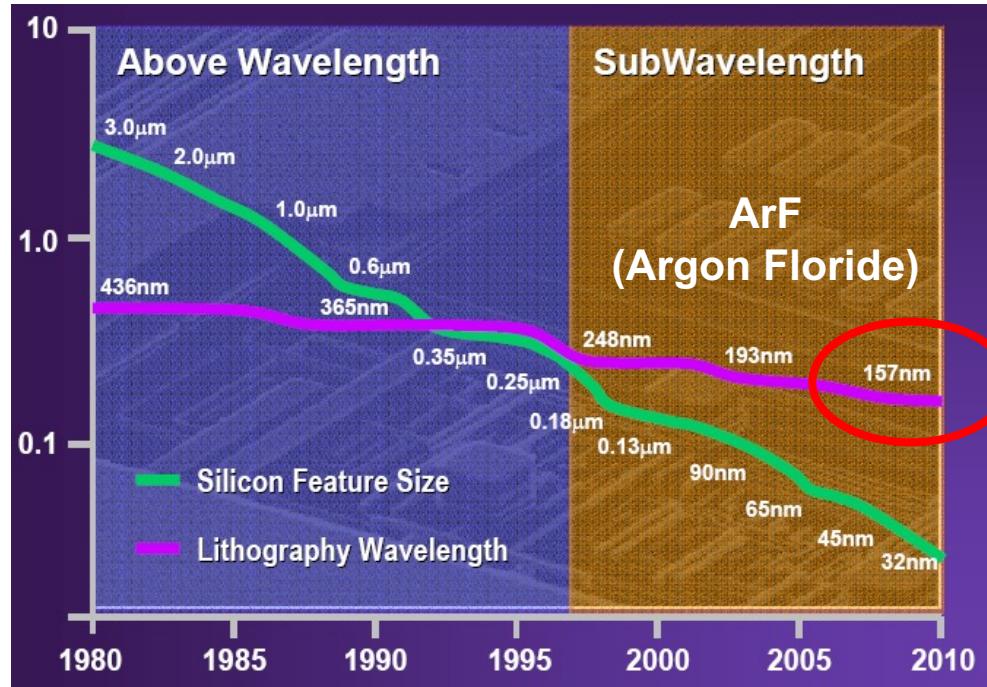


$$R = k_1 \lambda / NA$$

R: resolution; k_1 : resolution constant; λ : wavelength
NA: numerical aperture = $f(\text{lens, refraction index})$

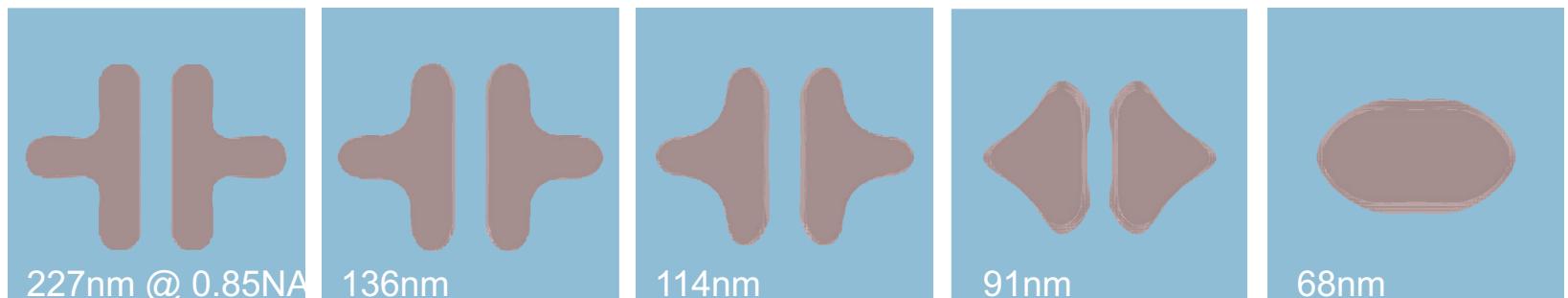
Subwavelength Lithography Gap

- Printed feature size is smaller than the wavelength of the light shining through the mask

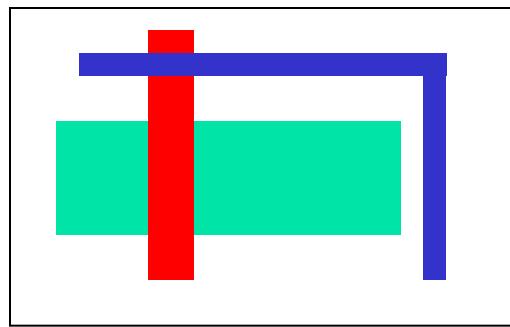


157nm will not
be feasible in
the near future!

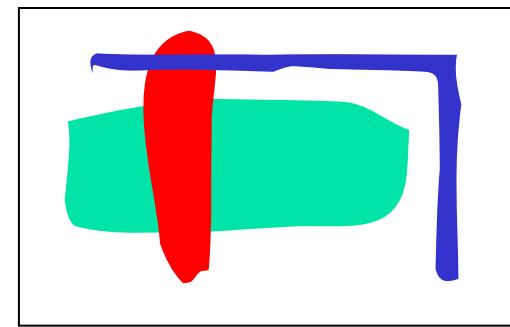
Numerical Technologies



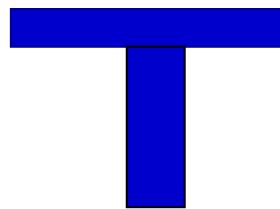
Sub-wavelength Lithography Problems!!



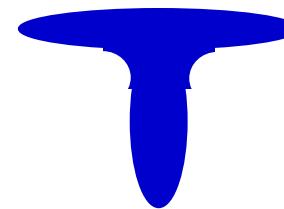
Mask patterns



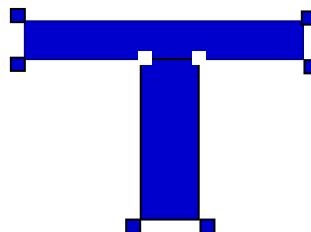
Printed layout



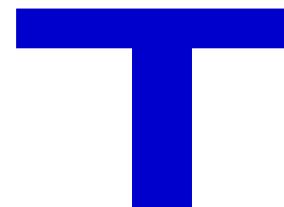
Drawn layout



Printed wafer



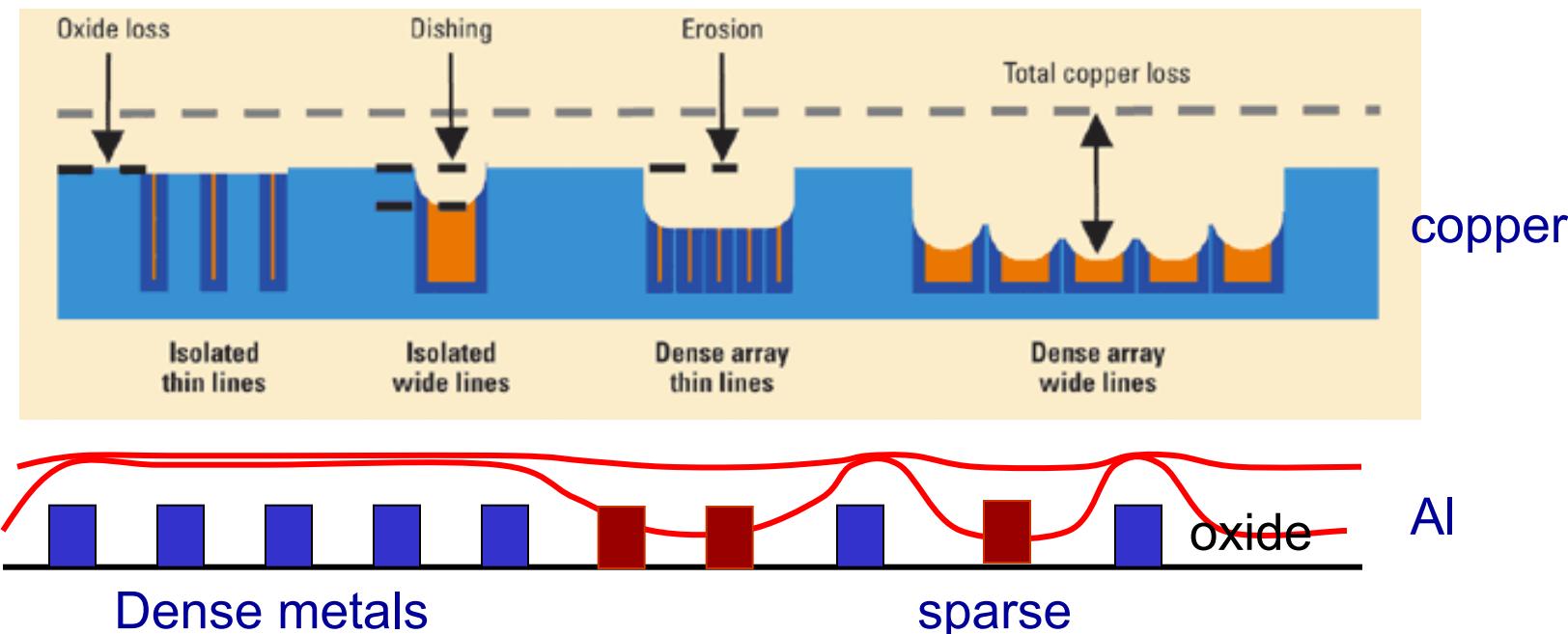
Proximity corrected layout



Printed wafer

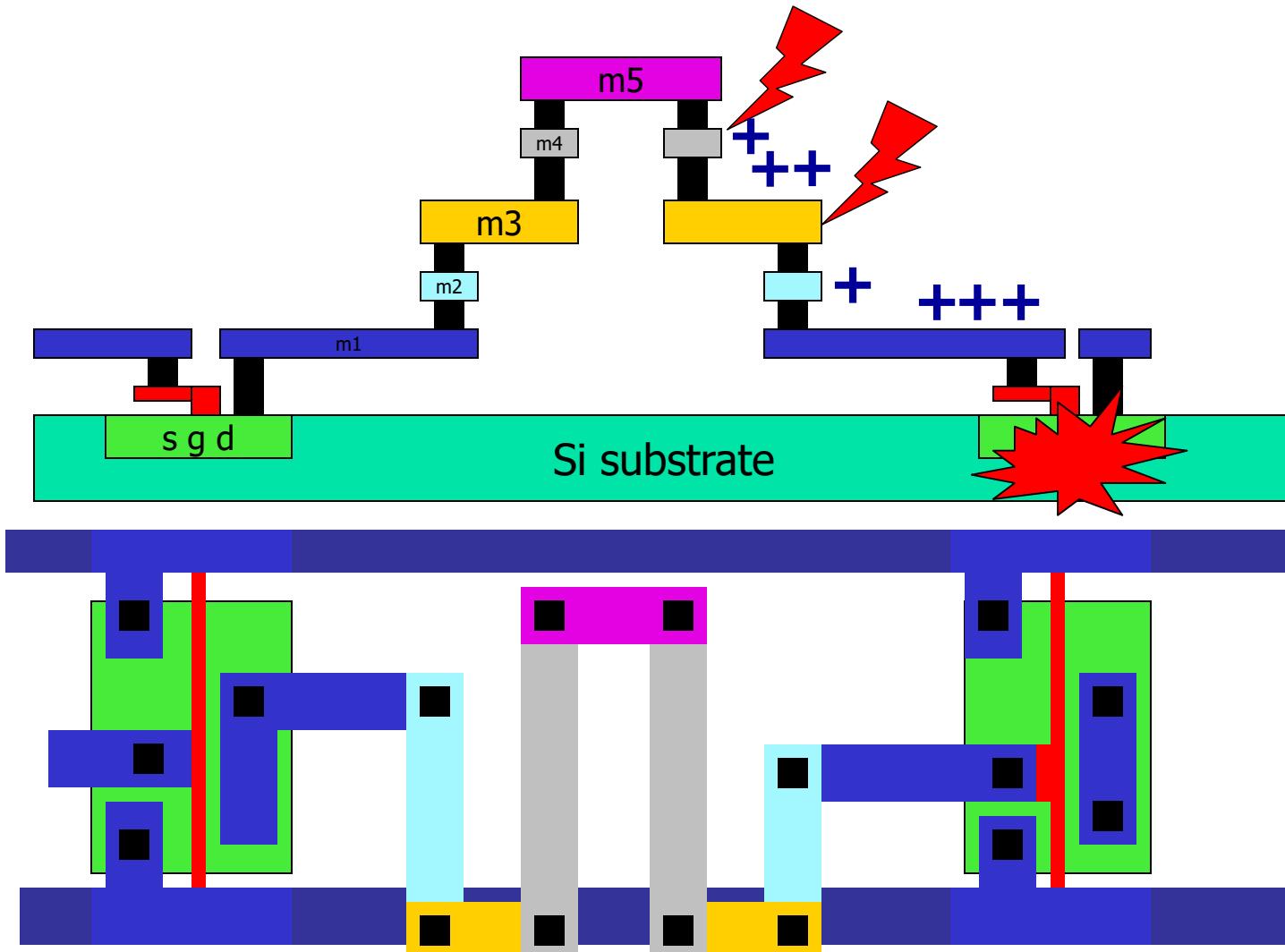
Manufacturability Becomes a 1st-Order Effect!!

- Manufacturability with 10-layer metal?
- Post Chemical-Mechanical Polishing (CMP) topography variation induces yield loss
 - Dielectric erosion and metal dishing
 - Electromigration due to large resistance variation
 - Inaccurate RC timing analysis



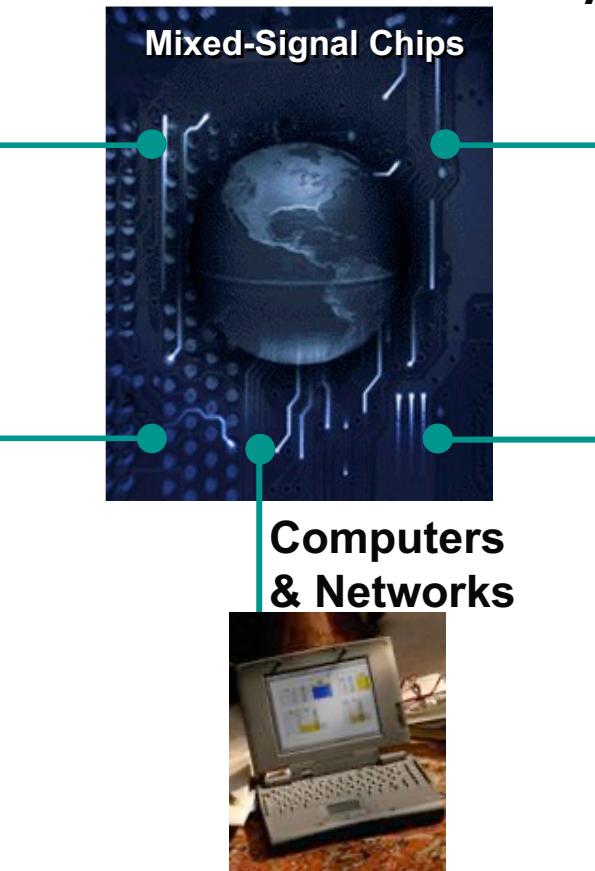
Reliability Becomes a 1st-Order Effect!!

- Manufacturability and reliability with 10-layer metal?



More and More “Mixed-Signal” ICs

Telecom



Automotive



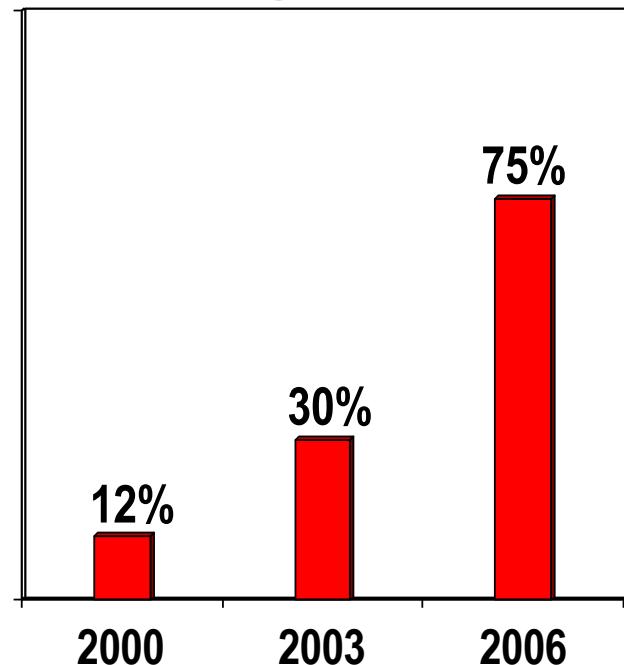
Consumer



Medical

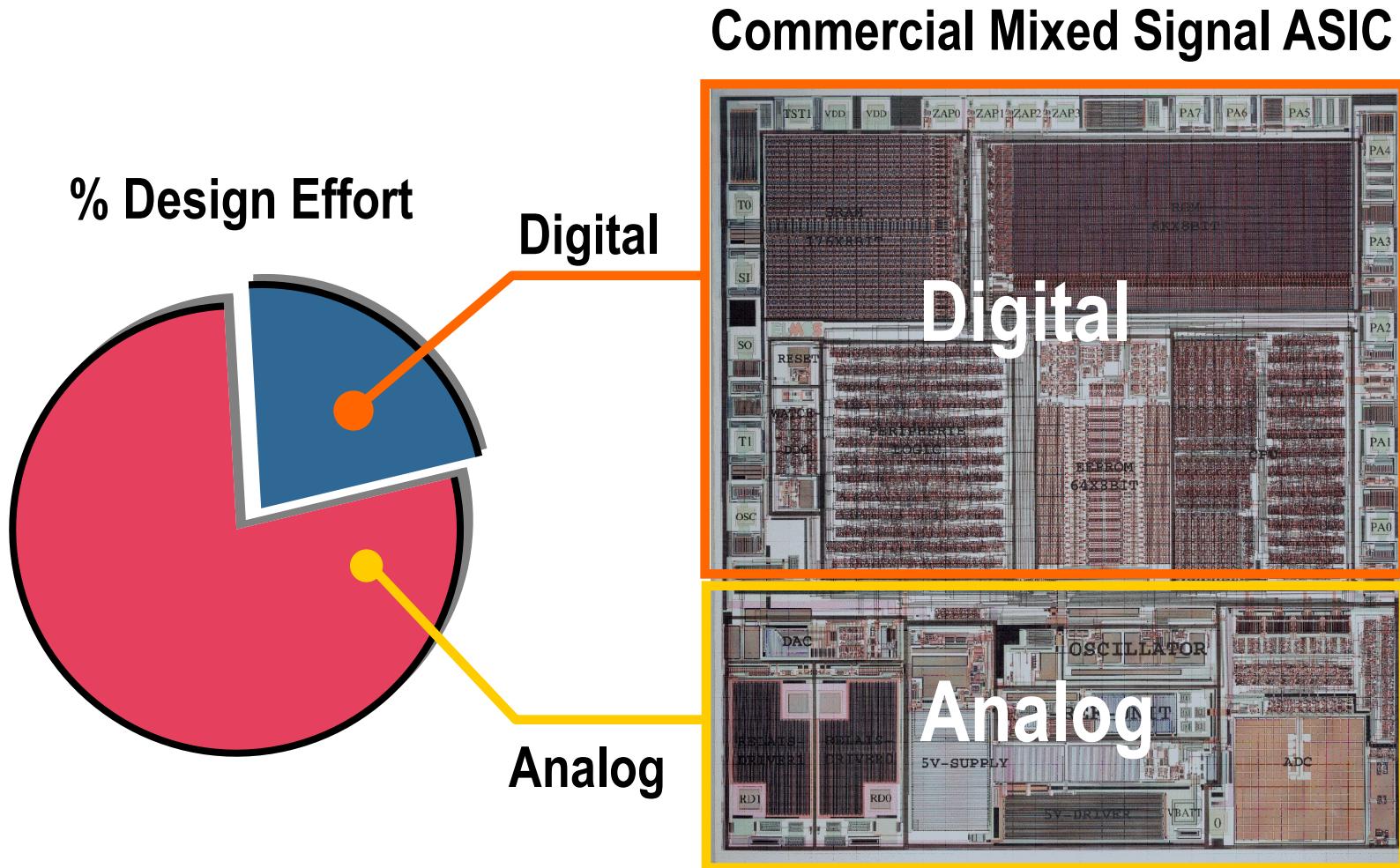


**% Digital Chips with
Analog Content**



[Source: IBS 2003]

Mixed-Signal Design Problem

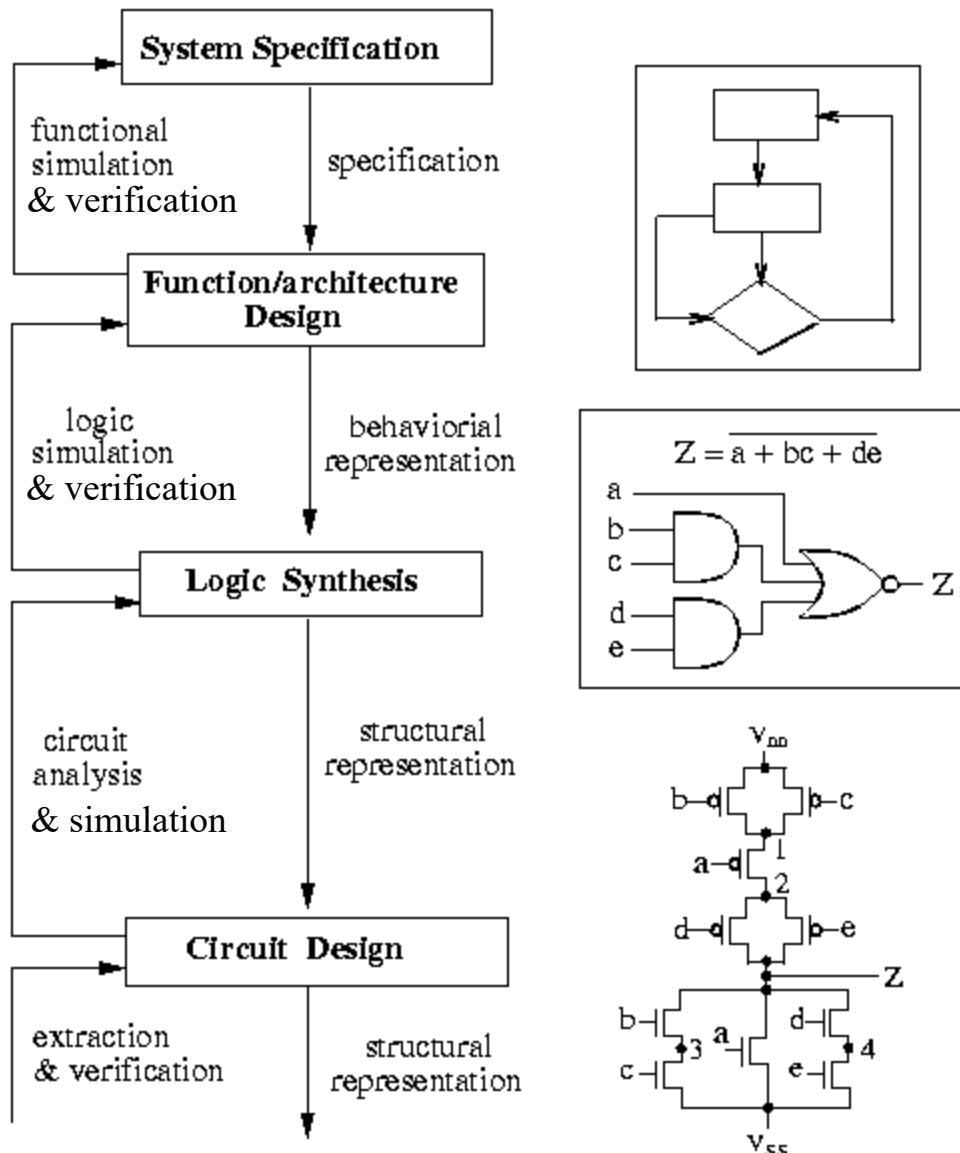


[Source: R. A. Rutenbar, ICCAD 2006]

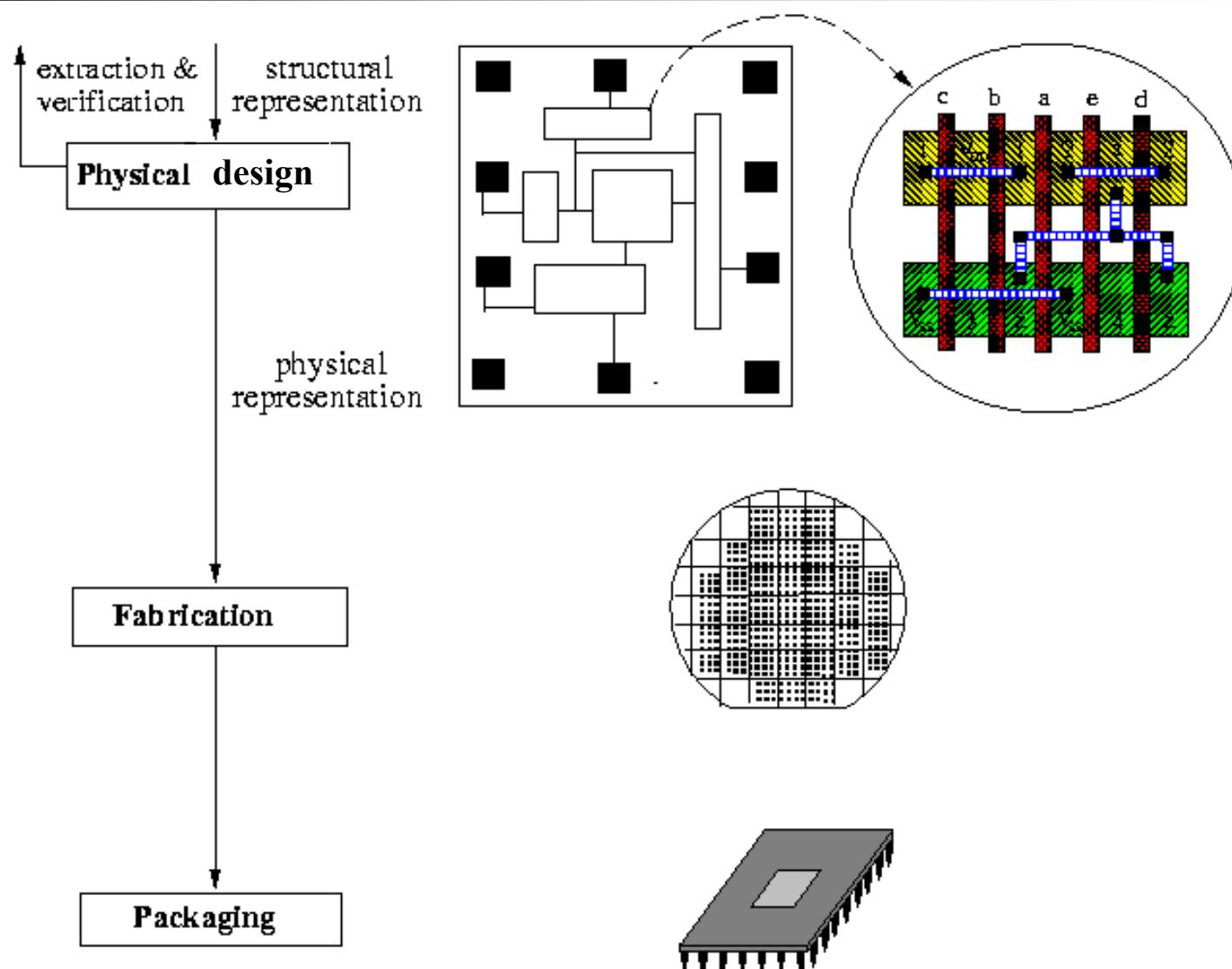
Traditional VLSI Design Cycles

1. System specification
 2. Functional design
 3. Logic synthesis
 4. Circuit design
 - 5. Physical design**
 6. Fabrication
 7. Packaging
- Other tasks involved: verification, simulation, testing, etc.
 - Design metrics: area, speed, **power dissipation**, noise, **manufacturability**, **reliability**, **testability**, design time, etc.
 - Design revolution: **interconnect (not gate) delay dominates circuit performance in deep submicron era.**
 - Interconnects are determined in physical design.
 - Shall consider interconnections in early design stages.

Traditional VLSI Design Cycle

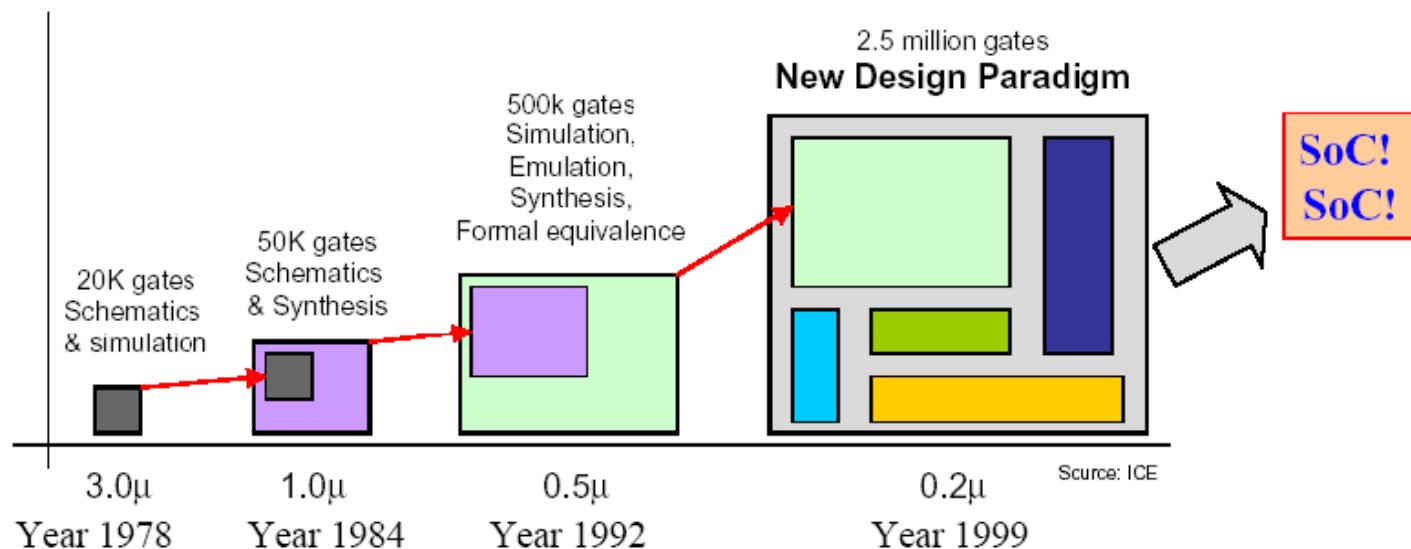


Traditional VLSI Design Flow (Cont'd)

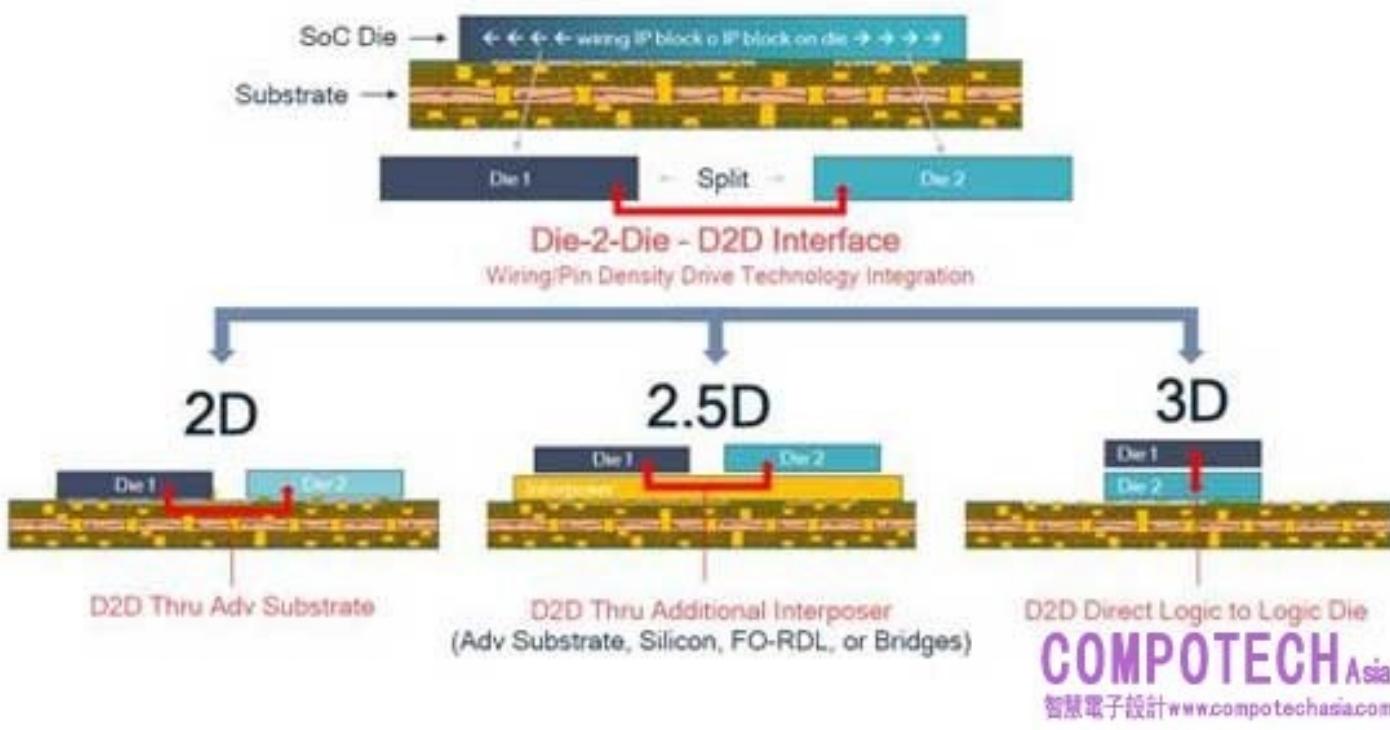


Evolution of Microelectronics

- Today's Silicon process technology
 - $0.13\mu\text{m}$ CMOS
 - $\sim 100 \text{ M}$ of devices, 3GHz internal clock
- Yesterday's chips are today's functional blocks



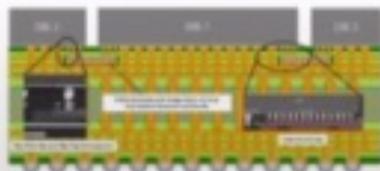
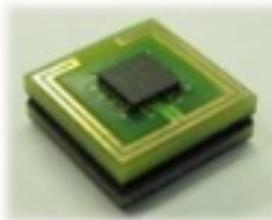
3DIC - 2D/2.5D/3D Integration



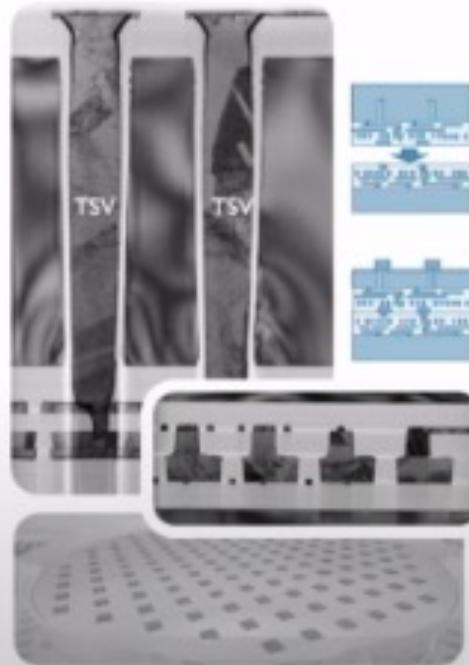
3DIC - 2D/2.5D/3D Integration

3D SYSTEM INTEGRATION

Package



Die/Wafer level



Device level
Stacking

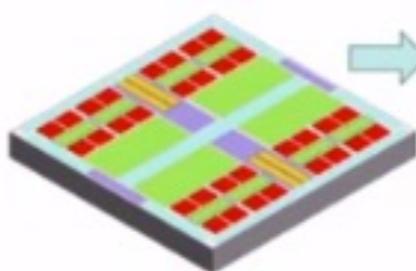


3DIC - 2D/2.5D/3D Integration

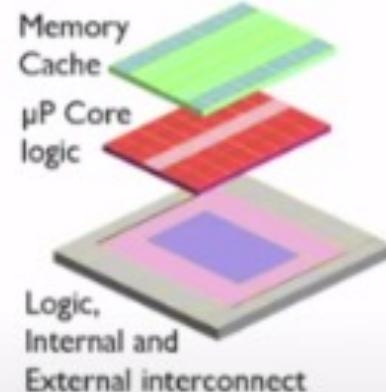
3D-SOC: FUNCTIONAL PARTITIONING

MULTI-CORE PROCESSOR PARTITIONING

2D Multi-core processor



3D functional partitioning

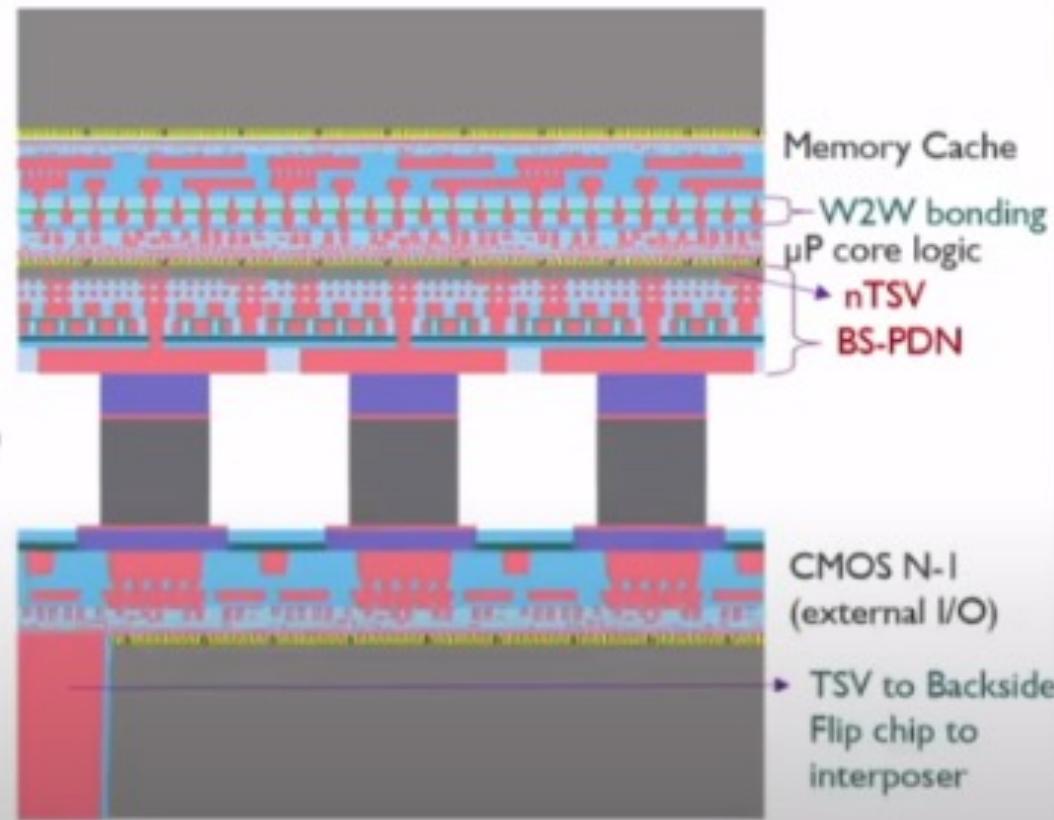


Cost effective

Memory: strongly reduced FEOL and BEOL complexity

Logic: reduced BEOL, top layers moved to backside

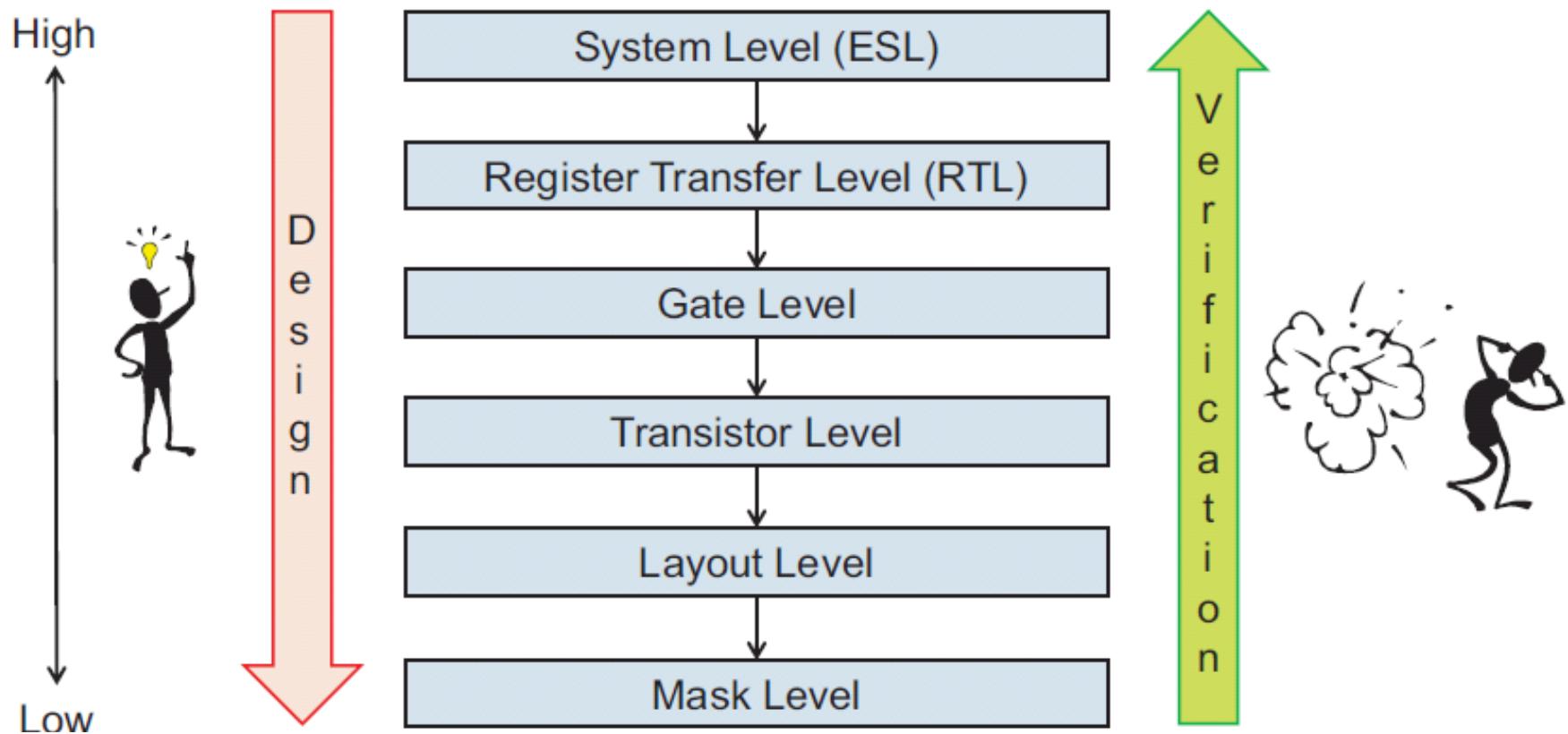
I/O chip: lower cost process node



imec

Abstraction Levels

- Synthesis / design: high to low
- Verification: low to high or same



System Level

- **Abstract algorithmic description of high-level behavior**
 - ▣ e.g. C-Programming language

```
Port*
compute_optimal_route_for_packet(Packet_t *packet,
                                  Channel_t *channel)
{
    static Queue_t *packet_queue;

    packet_queue = add_packet(packet_queue, packet);
    ...
}
```

- ▣ abstract because it does not contain any implementation details for timing or data
- ▣ efficient to get a compact execution model as first design draft
- ▣ difficult to maintain throughout project because no link to implementation

Register-Transfer Level (RTL)

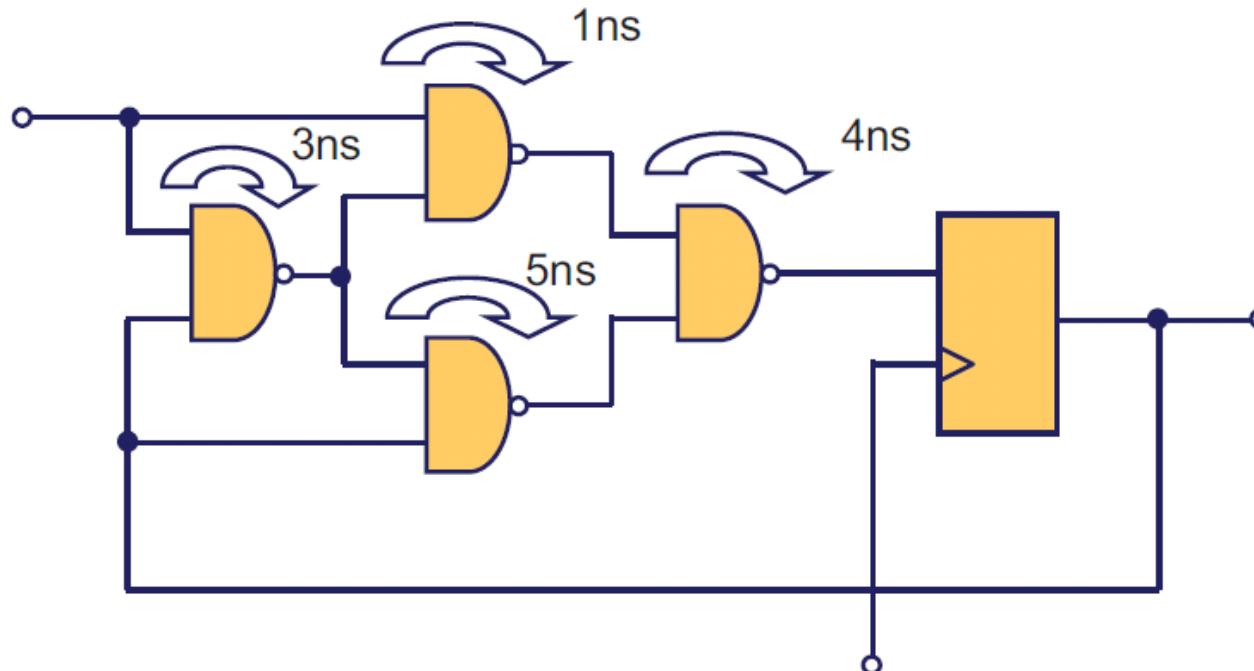
- **Cycle accurate model “close” to the hardware implementation**
 - ▣ bit-vector data types and operations as abstraction from bit-level implementation
 - ▣ sequential constructs (e.g. if - then - else, while loops) to support modeling of complex control flow

```
module mark1;
    reg [31:0] m[0:8192];
    reg [12:0] pc;
    reg [31:0] acc;
    reg[15:0] ir;

    always
        begin
            ir = m[pc];
            if(ir[15:13] == 3b'000)
                pc = m[ir[12:0]];
            else if (ir[15:13] == 3'b010)
                acc = -m[ir[12:0]];
            ...
        end
endmodule
```

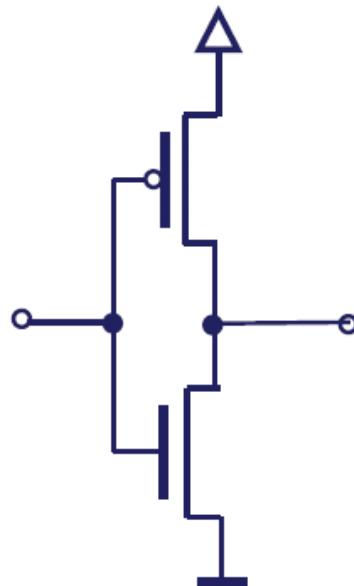
Gate Level

- Model on finite-state machine level
 - models function in Boolean logic using registers and gates
 - various delay models for gates and wires



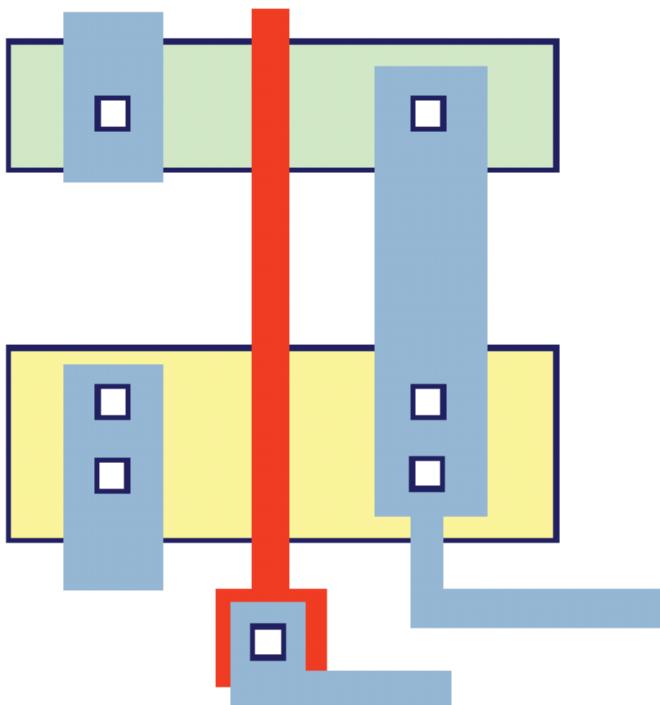
Transistor Level

- Model on CMOS transistor level
 - ▣ depending on application function modeled as resistive switches
 - used in functional equivalence checking
 - ▣ or full differential equations for circuit simulation
 - used in detailed timing analysis



Layout Level

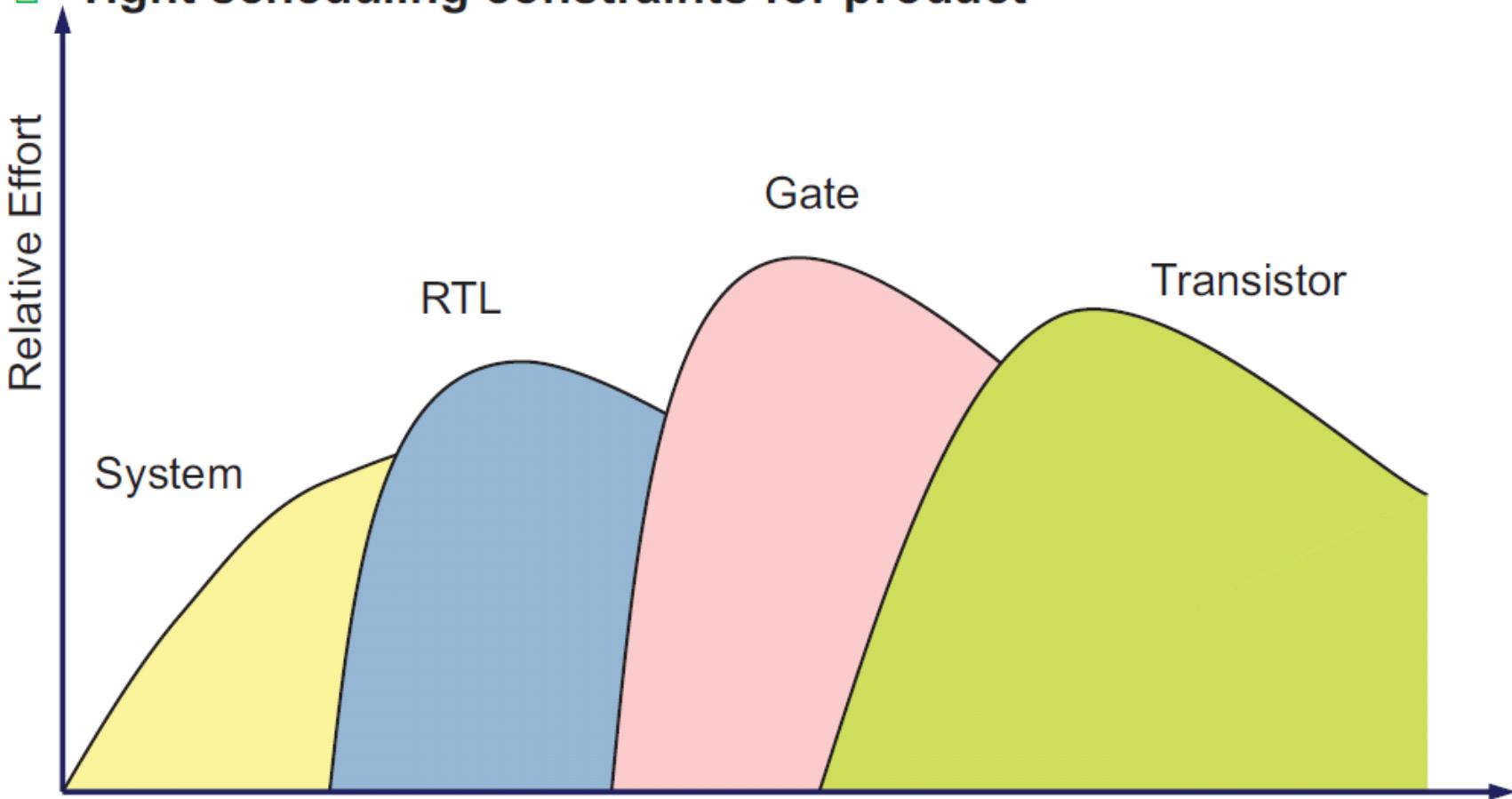
- Transistors and wires are laid out as polygons in different technology layers such as diffusion, poly-silicon, metal, etc.
 - Base layers (diffusion, polysilicon): transistors
 - Metal layers: wires



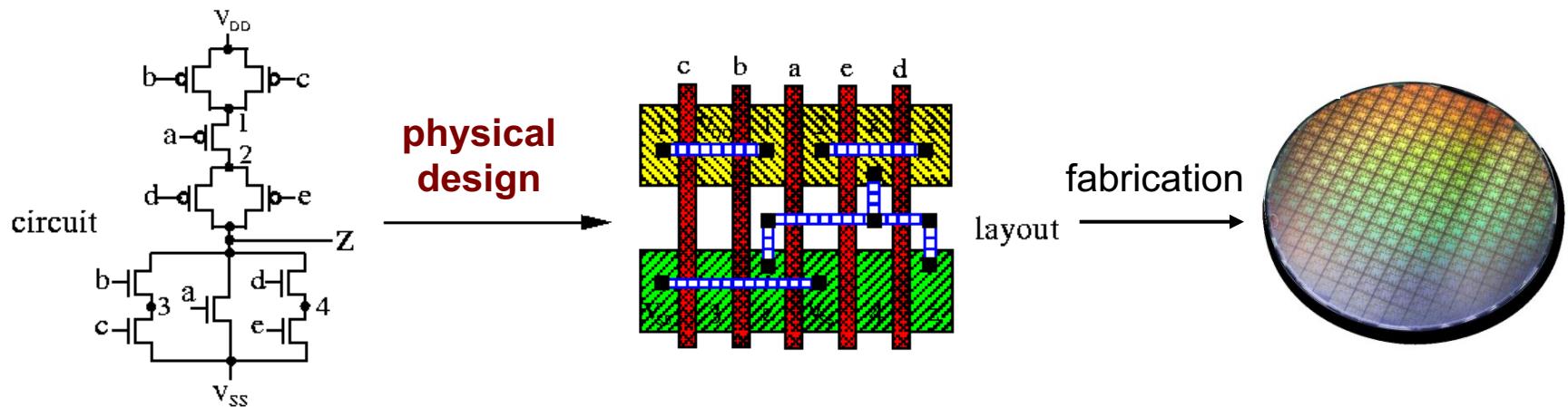
One color corresponding one layer

Design of Integrated Systems

- Design phases overlap to large degrees
- Parallel changes on multiple levels, multiple teams
- Tight scheduling constraints for product

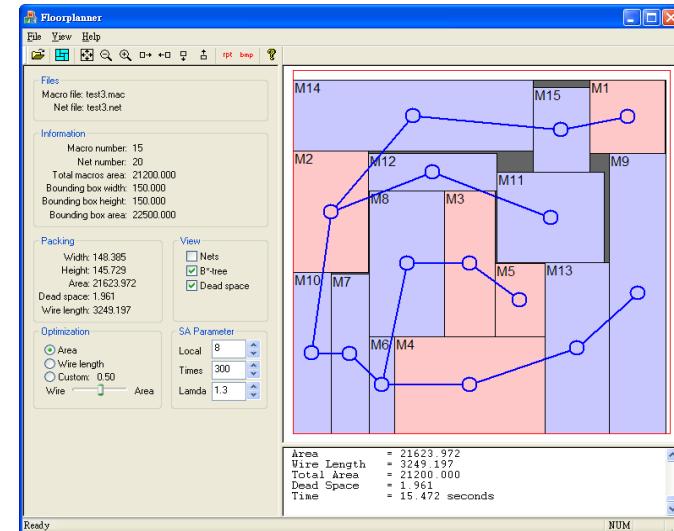
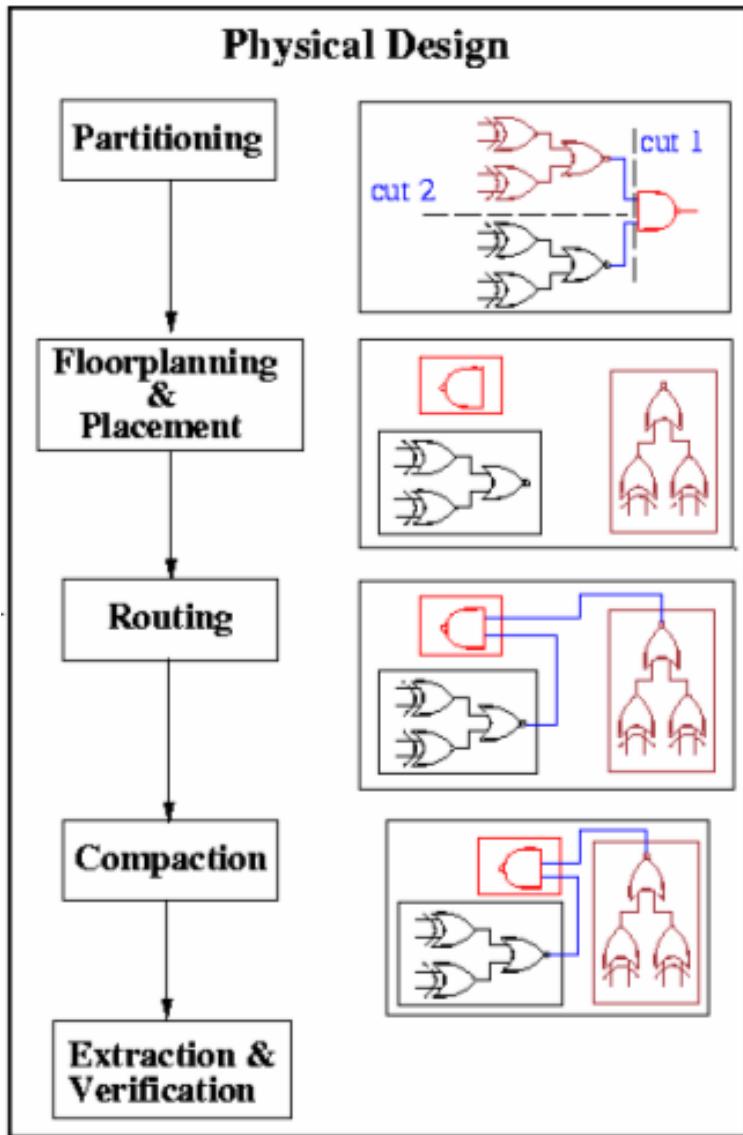


Physical Design (PD)



- PD converts a circuit description into a geometric description.
- The description is used to manufacture a chip.
- Physical design cycle:
 1. Partitioning
 2. Floorplanning
 3. Placement
 4. Routing
 5. Post-layout optimization (buffering, sizing, etc.)
- Others: circuit extraction, timing verification and design rule checking

Physical Design Flow

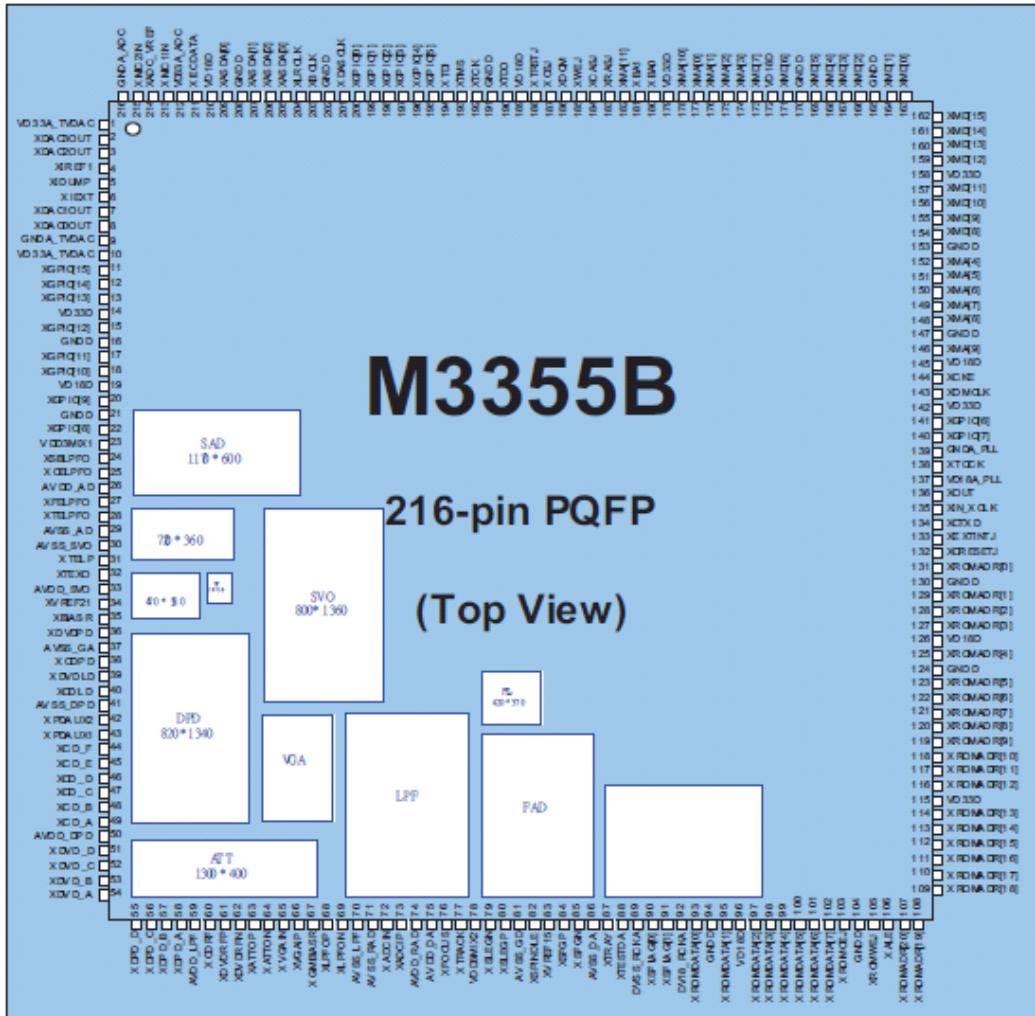


B*-tree based floorplanning system



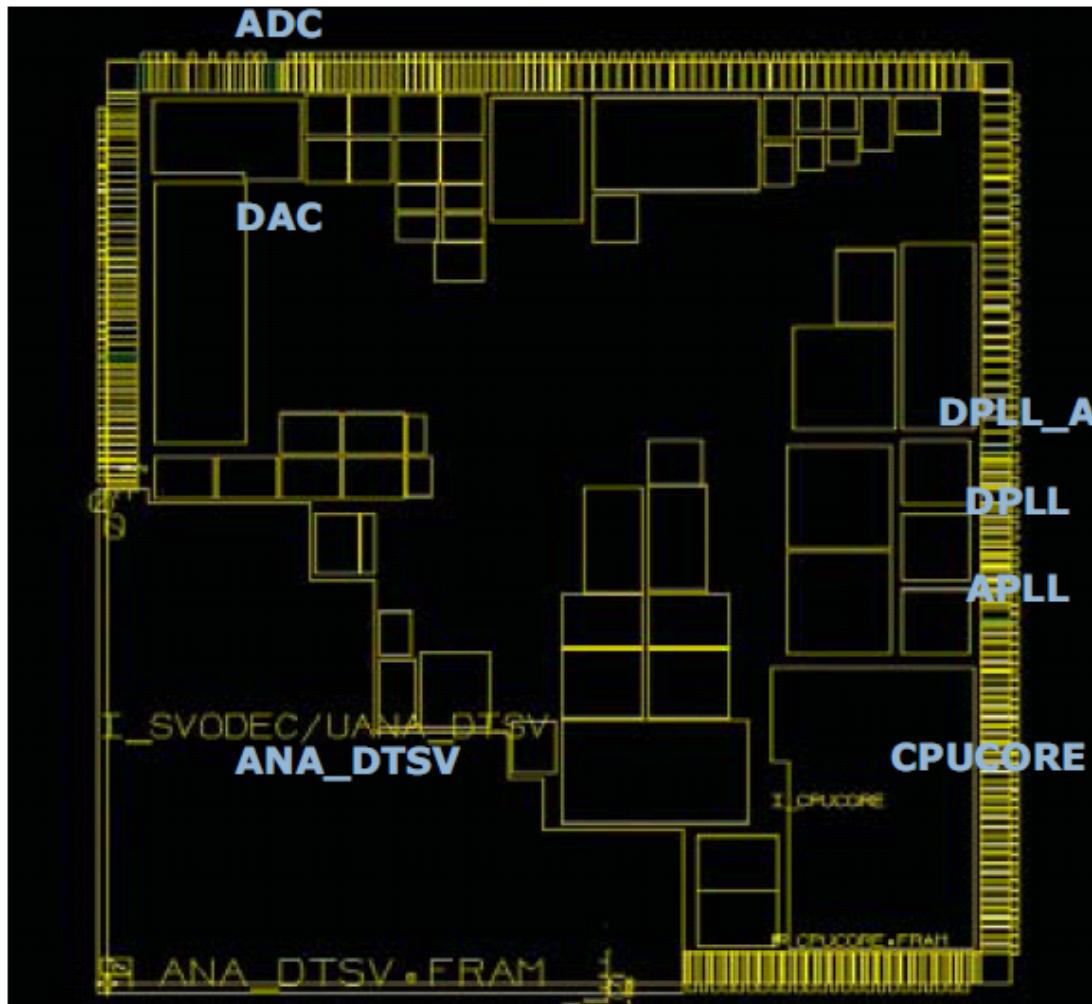
A routing system

PAD Assignment

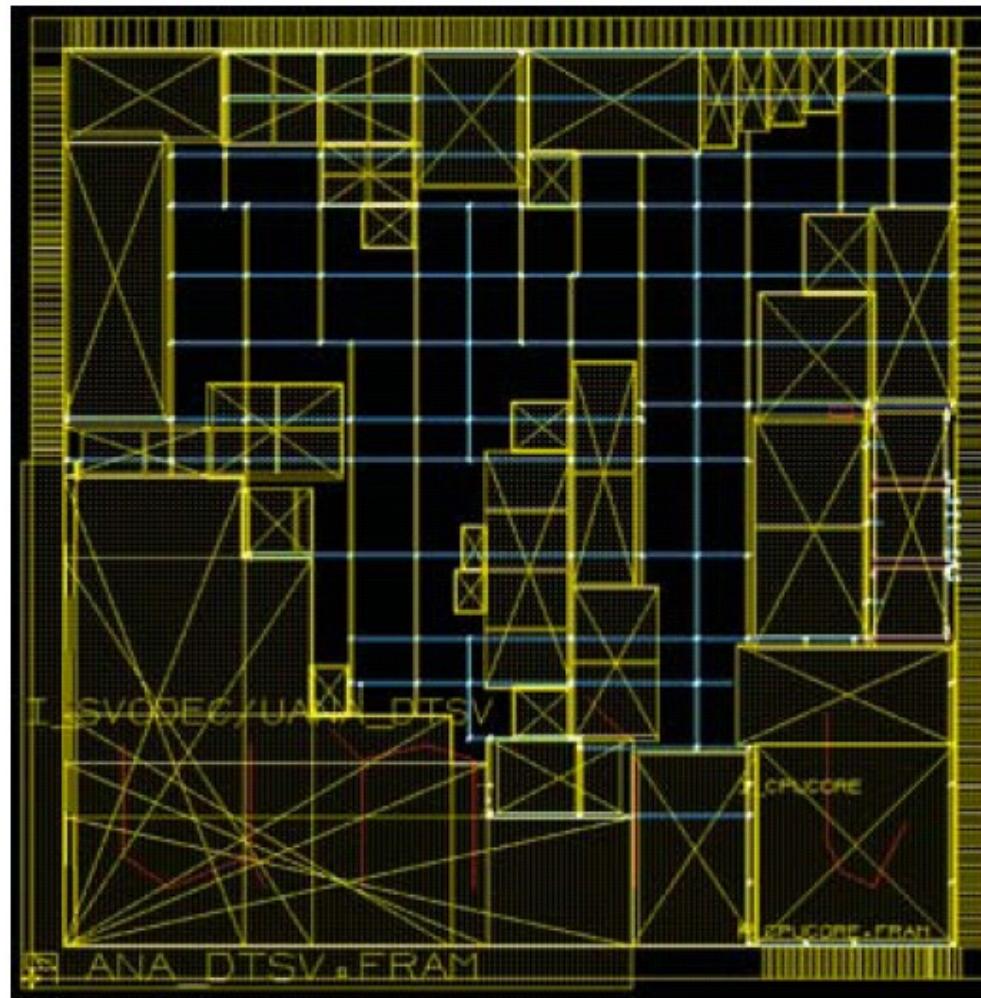


Mark P.-H. Lin [Courtesy of Y.-W. Chang, H.-M Chen]

Floorplanning

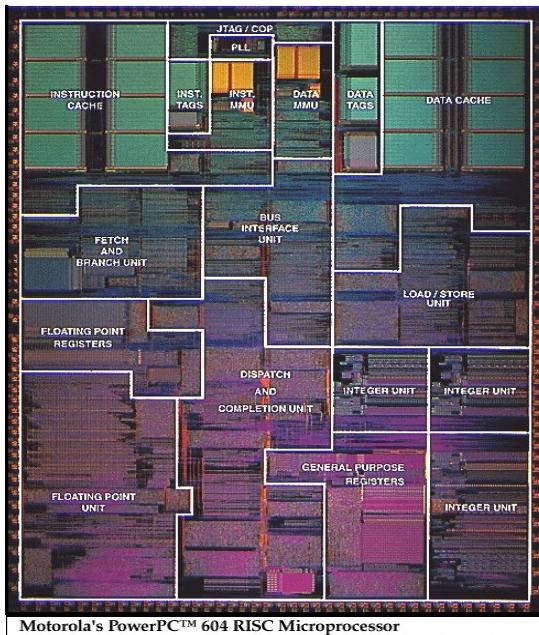


Power Planning

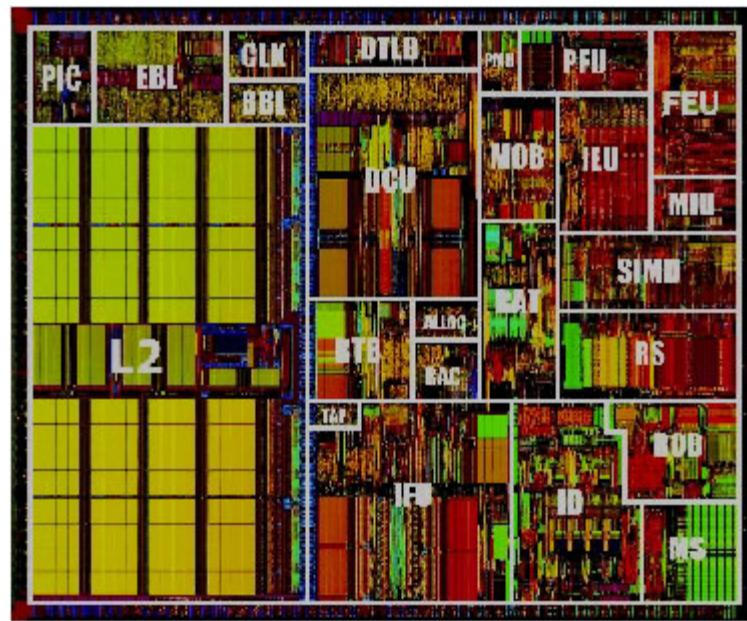


Floorplan Examples

PowerPC
604

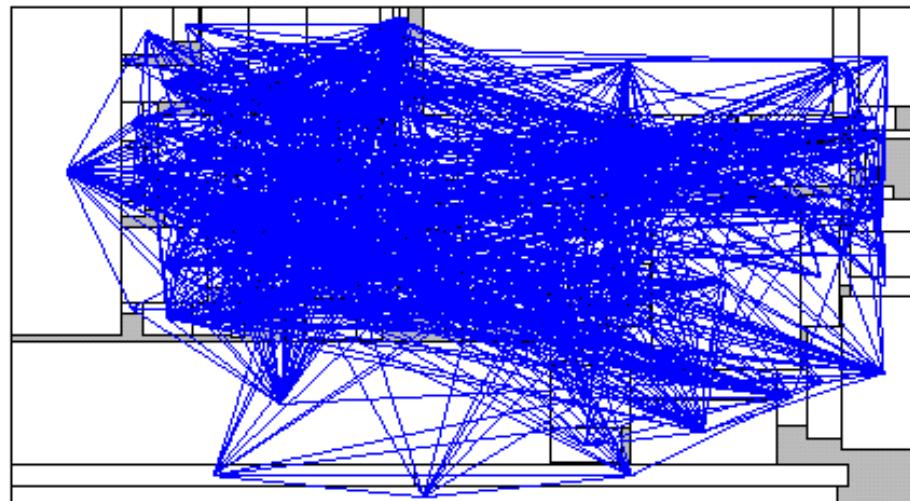


Motorola's PowerPC™ 604 RISC Microprocessor

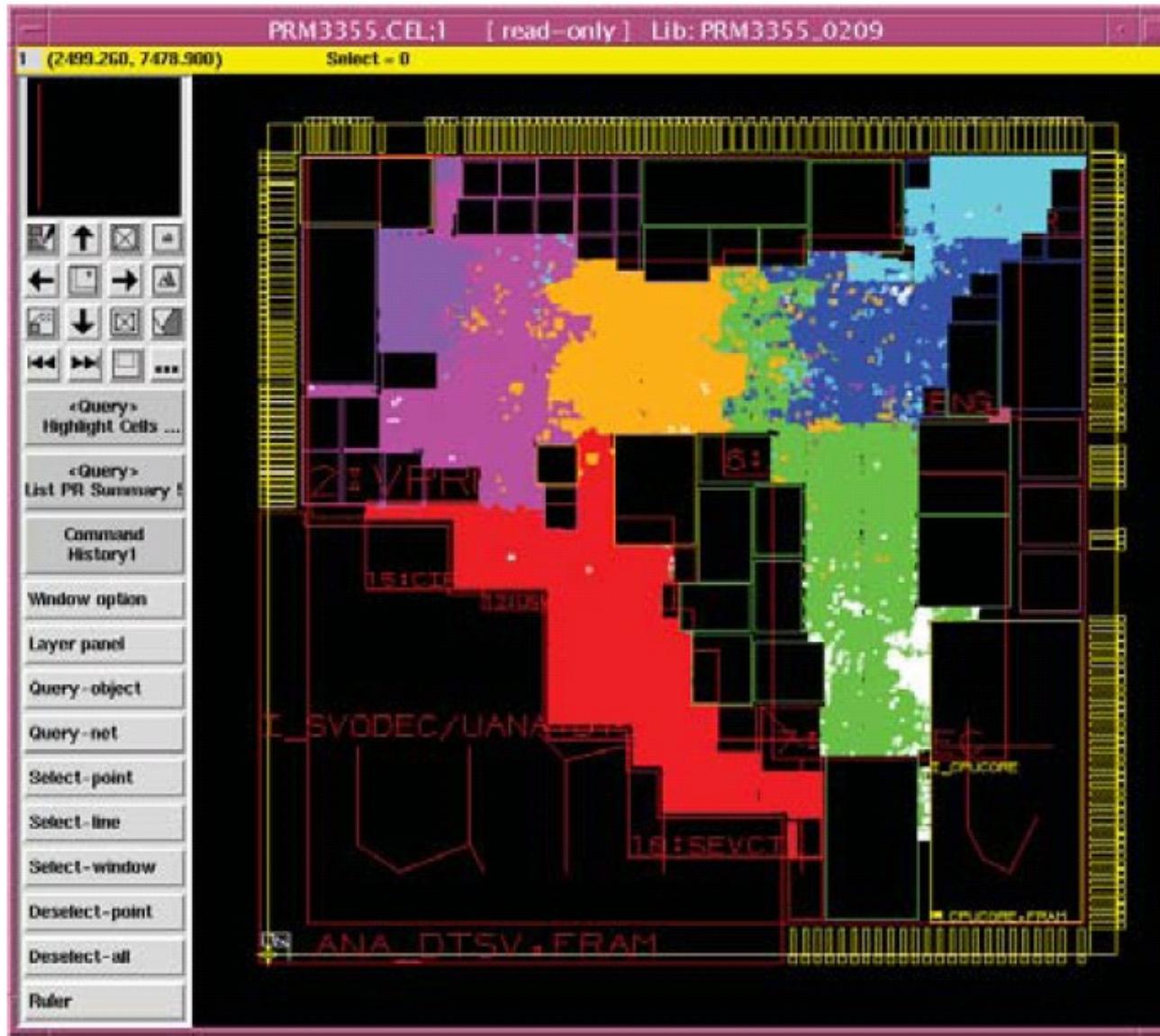


Intel
Pentium 4

A floorplan
with
interconnections

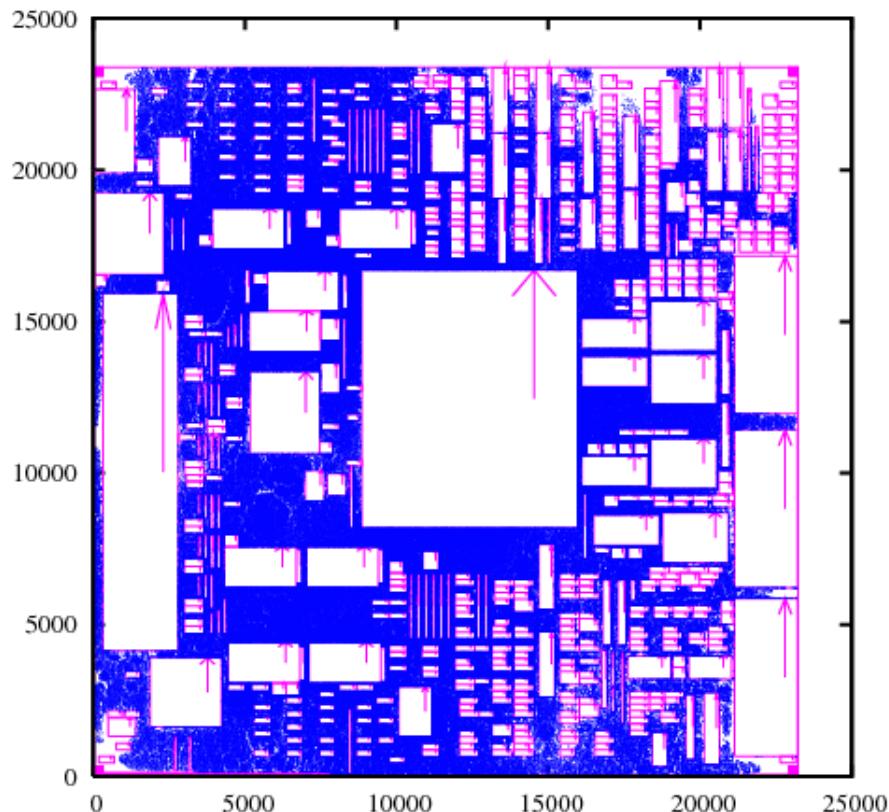


Placement



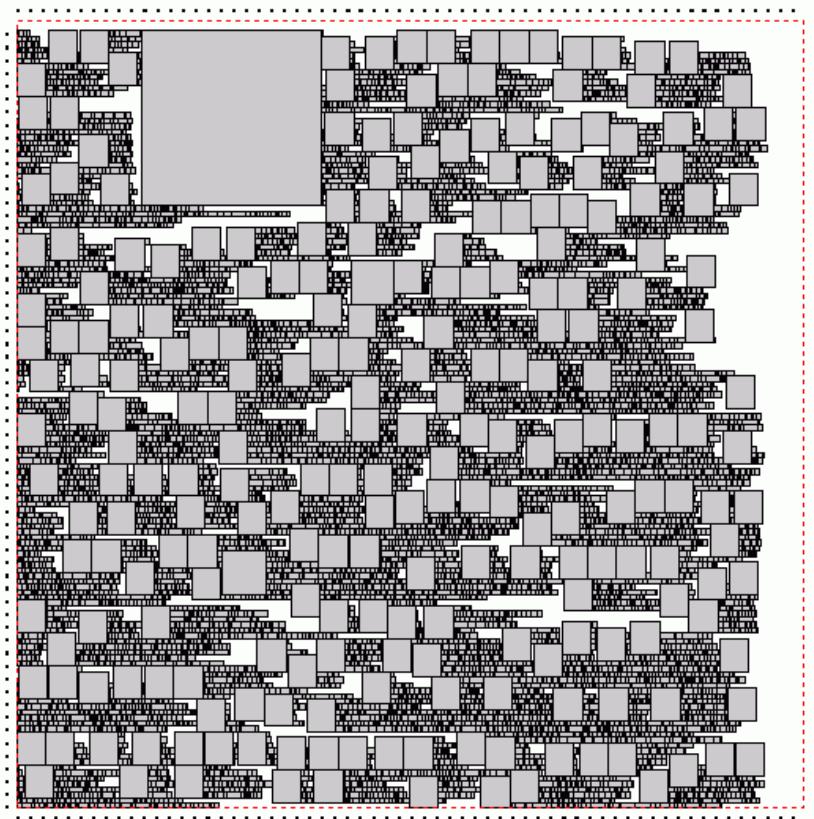
Placement Examples

adaptec5.plt, block= 843224, net= 867798, HPWL= 387222315



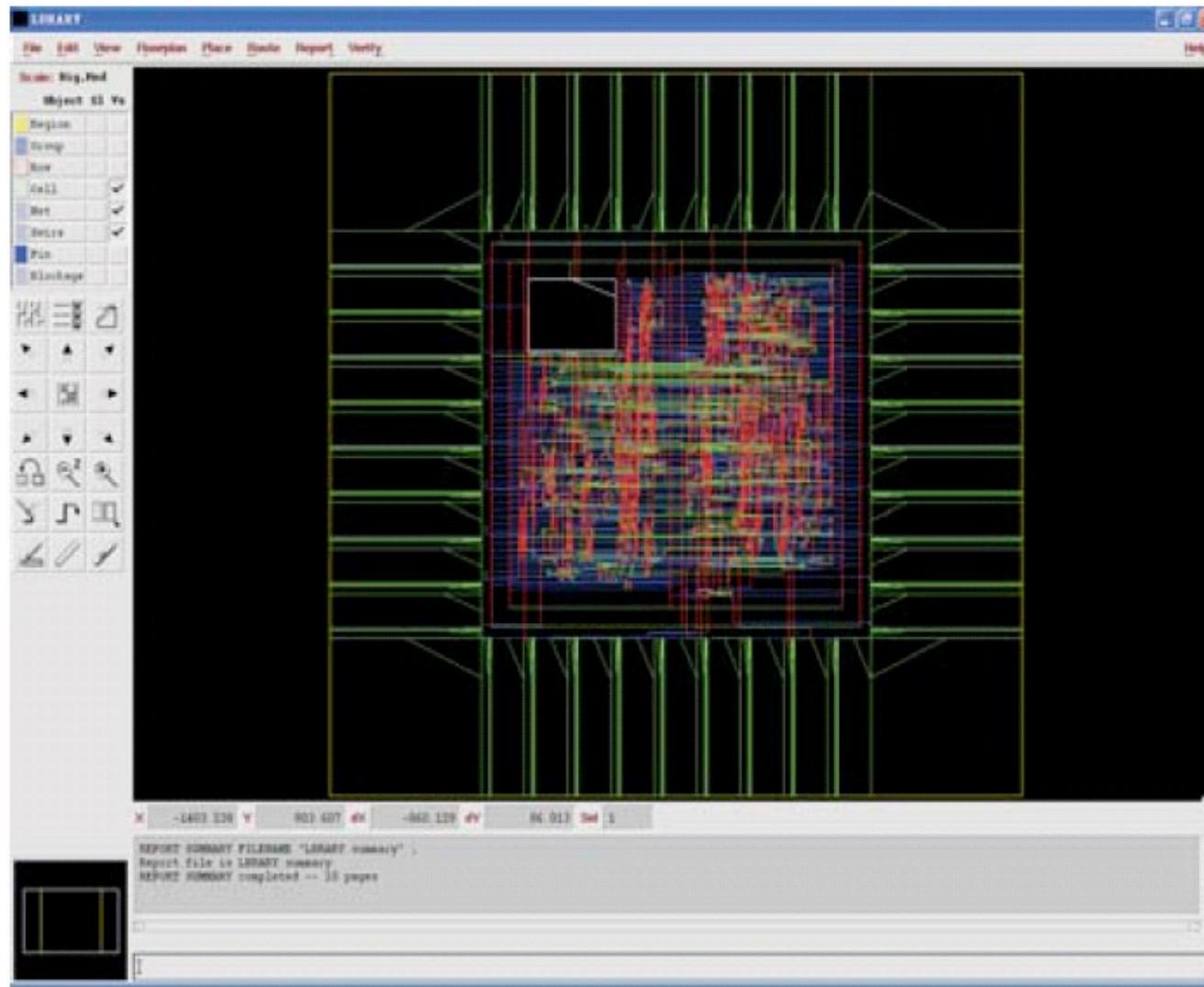
842K movable cells
646 fixed macros
868K nets

ISPD98 ibm01



12,752 cells, 247 macros
 $A_{\max}/A_{\min} = 8416$

Routing



Routing Example

- 0.18um technology, two layers, pitch = 1 um, 8109 nets.

