# NI 622x Specifications

Specifications listed below are typical at 25 °C unless otherwise noted. Refer to the *M Series User Manual* for more information about NI 622x devices.

このドキュメントの日本語版については、ni.com/manuals を参照してください。 (For a Japanese language version, go to ni.com/manuals.)

# **Analog Input**

Number of channels		Input impedance	
NI 6220/6221	8 differential or	Device on	
	16 single ended	AI+ to AI GND	>10 GΩ in parallel
NI 6224/6229			with 100 pF
	32 single ended	AI- to AI GND	>10 G $\Omega$ in parallel
NI 6225			with 100 pF
	80 single ended	Device off	
ADC resolution	16 bits	AI+ to AI GND	820 Ω
DNL	No missing codes	AI- to AI GND	820 Ω
	guaranteed	Input bias current	±100 pA
INL	Refer to the AI Absolute	Crosstalk (at 100 kHz)	
	Accuracy Table	Adjacent channels	75 dB
Sampling rate		Non-adjacent channels	90 dB <sup>1</sup>
Maximum	250 kS/s single channel, 250 kS/s multi-channel	Small signal bandwidth (-3 dB)	700 kHz
	(aggregate)	Input FIFO size	4,095 samples
Minimum	No minimum	Scan list memory	4,095 entries
Timing accuracy	50 ppm of sample rate	Division	
Timing resolution	50 ns	Data transfers	DMM ( w d )
Input coupling	DC	PCI/PXI devices	DMA (scatter-gather), interrupts,
Input range	±10 V. ±5 V.		programmed I/O
	±1 V, ±0.2 V	USB devices	USB Signal Stream, programmed I/O
Maximum working voltage for an (signal + common mode)	C 1		
CMRR (DC to 60 Hz)	92 dB		



<sup>&</sup>lt;sup>1</sup> For USB-6225 devices, channel AI <0..15> crosstalk to channel AI <64..79> is -71 dB; applies to channels with 64-channel separation, for example, AI (x) and AI (x + 64).

Overvoltage protection (AI <0..79>, AI SENSE, AI SENSE 2) **Typical Performance Graphs** 

Device on .....±25 V for up to two AI pins Device off .....±15 V for up to two AI pins

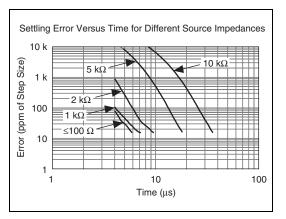
Input current during

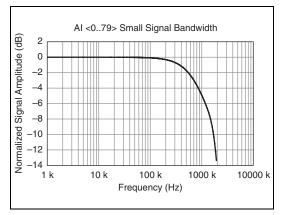
overvoltage condition ......±20 mA max/AI pin

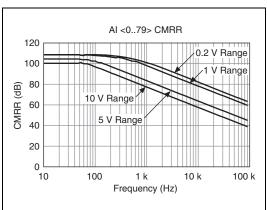
#### **Settling Time for Multichannel Measurements**

Accuracy, full scale step, all ranges

±90 ppm of step (±6 LSB) ......4 μs convert interval ±30 ppm of step (±2 LSB) .......5 μs convert interval ±15 ppm of step (±1 LSB)......7 μs convert interval







# **Analog Output**

rmaiog output	
Number of channels	
NI 6220/6224	.0
NI 6221/6225	. 2
NI 6229	. 4
DAC resolution	. 16 bits
DNL	±1 LSB
Monotonicity	. 16 bit guaranteed
Maximum update rate	
1 channel	.833 kS/s
2 channels	.740 kS/s per channel
3 channels	.666 kS/s per channel
4 channels	.625 kS/s per channel
Timing accuracy	.50 ppm of sample rate
Timing resolution	.50 ns
Output range	±10 V
Output coupling	.DC
Output impedance	. 0.2 Ω
Output current drive	.±5 mA
Overdrive protection	±25 V
Overdrive current	. 10 mA
Power-on state	±20 mV <sup>1</sup>
Power-off glitch	.400 mV for 200 ms
Output FIFO size	8,191 samples shared among channels used
Data transfers	
PCI/PXI devices	DMA (scatter-gather),
	interrupts,
	programmed I/O
USB devices	USB Signal Stream, programmed I/O

Settling time, full scale step	
15 ppm (1 LSB)	6 µs
Slew rate	15 V/μs
Glitch energy	
Magnitude	100 mV
Duration	2.6 us

# Calibration (Al and AO)

Recommended warm-up time	15 minutes
Calibration interval	1 year

- · Non-periodic waveform
- Periodic waveform regeneration mode from onboard FIFO
- Periodic waveform regeneration from host buffer including dynamic update

AO waveform modes:

<sup>&</sup>lt;sup>1</sup> For all USB-6221/6229 Screw Terminal devices, when powered on, the analog output signal is not defined until after USB configuration is complete.

# Al Absolute Accuracy Table

Nomina	Nominal Range	:			Residual					
Positive Full Scale	Negative Full Scale	Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Reference Tempco	Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	INLError (ppm of Range)	Random Noise, σ (μVrms)	Absolute Accuracy at Full Scale <sup>1</sup> (μV)	$Sensitivity^2 \atop (\mu V)$
10	-10	75	25	5	20	57	92	244	3,100	9.76
5	5	85	25	5	20	09	92	122	1,620	48.8
1	-1	95	25	5	25	62	92	30	360	12.0
0.2	-0.2	135	25	5	08	175	92	13	112	5.2

AbsoluteAccuracy = Reading · (GainError) + Range · (OffsetError) + NoiseUncertainty

 $GainError = ResidualAIGainError + GainTempco \cdot (TempChangeFromLastInternalCal) + ReferenceTempco \cdot (TempChangeFromLastExternalCal) + ReferenceTempco \cdot (TempChangeFromLastExternalCal) + ReferenceTempco \cdot (TempChangeFromLastExternalCal) + ReferenceTempco \cdot (TempChangeFromLastExternalCal) + ReferenceTempco \cdot (TempChangeFromLastInternalCal) + ReferenceTempco \cdot (TempChangeFromCh$ 

 $OffsetError = Residual AIOffsetError + OffsetTempco \cdot (TempChangeFromLastInternalCal) + INL\_Error$ 

Noise Uncertainty =  $\frac{\text{RandomNoise} \cdot 3}{\frac{1}{12000}}$  For a co

For a coverage factor of 3  $\sigma$  and averaging 100 points.

Absolute accuracy at full scale on the analog input channels is determined using the following assumptions:

TempChangeFromLastExternalCal = 10 °C TempChangeFromLastInternalCal = 1 °C

number\_of\_readings = 100

number\_or\_readings = 100 CoverageFactor =  $3 \sigma$  For example, on the 10 V range, the absolute accuracy at full scale is as follows: GainError = 75 ppm + 25 ppm  $\cdot$  1 + 5 ppm  $\cdot$  10 GainError = 150 ppm

GainError = 75 ppm + 25 ppm  $\cdot$  1 + 5 ppm  $\cdot$  10 OffsetError = 20 ppm + 57 ppm  $\cdot$  1 + 76 ppm

OffsetError = 153 ppm

NoiseUncertainty =  $\frac{244 \, \mu \text{ V} \cdot 3}{\sqrt{r \cdot c \cdot c}}$  NoiseUncertainty = 73  $\mu \text{ V}$ 

Absolute Accuracy =  $10 \text{ V} \cdot (\text{GainError}) + 10 \text{ V} \cdot (\text{OffsetError}) + \text{NoiseUncertainty}$  Absolute Accuracy =  $3,100 \, \mu\text{V}$ 

<sup>2</sup> Sensitivity is the smallest voltage change that can be detected. It is a function of noise.

Accuracies listed are valid for up to one year from the device external calibration.

# **AO Absolute Accuracy Table**

Nomina	lominal Range				Residual			Absolute
Positive	Negative	Residual Gain Error (ppm of	Gain Tempco	Reference	Offset Error (ppm of	Offset Tempco (ppm of	INL Error (ppm of	Accuracy at Full Scale <sup>1</sup>
Full Scale	Full Scale	Reading)	(ppm/°C)	Tempco	Range)	Range/°C)	Range)	(μV)
10	-10	06	10	5	40	S	128	3,230

<sup>1</sup> Absolute Accuracy at full scale numbers is valid immediately following internal calibration and assumes the device is operating within 10 °C of the last external calibration. Accuracies listed are valid for up to one year from the device external calibration.

 $AbsoluteAccuracy = OutputValue \cdot (GainError) + Range \cdot (OffsetError)$ 

 $GainError = Residual GainError + GainTempco \cdot (TempChangeFromLastInternalCal) + Reference Tempco \cdot (TempChangeFromLastExternalCal) + Reference Tempco \cdot (TempChangeFromChangeFromLastExternalCal) + Reference Tempco \cdot (TempChangeFromChangeFromCh$  $OffsetError = Residual OffsetError + AOOffsetTempco \cdot (TempChangeFromLastInternalCal) + INL\_Error + AOOffsetError + AOOOffsetError + AOOOffsetError + AOOOffsetError + AOOOffset$ 

# Digital I/O/PFI

#### **Static Characteristics**

Number of channels	
NI 6220/6221 (68-pin)/6225	.24 total
	8 (P0.<07>)
	16 (PFI <07>/P1,
	PFI <815>/P2)
PCI-6221 (37-pin)	.10 total
_	2 (P0.<0, 1>)
	8 (PFI <07>/P1)
NI 6224/6229	.48 total
	32 (P0.<031>)
	16 (PFI <07>/P1,
	PFI <815>/P2)
Ground reference	.D GND
Direction control	.Each terminal
	individually
	programmable
	as input or output
Pull-down resistor	.50 kΩ typical,
	20 kΩ minimum

# Waveform Characteristics (Port 0 Only)

Terminals used

Input voltage protection1 .....±20 V on up to two pins

Terrimais used
NI 6220/6221 (68-pin)/6225Port 0 (P0.<07>)
PCI-6221 (37-pin)Port 0 (P0.<0, 1>)
NI 6224/6229Port 0 (P0.<031>)
Port/sample size
NI 6220/6221 (68-pin)/6225Up to 8 bits
PCI-6221 (37-pin)Up to 2 bits
NI 6224/6229Up to 32 bits
Waveform generation (DO) FIFO 2,047 samples
Waveform acquisition (DI) FIFO2,047 samples
DO or DI Sample Clock

frequency<sup>2</sup>......0 to 1 MHz

#### Data transfers

PCIPXI devices	DMA (scatter-gather),
	interrupts,
	programmed I/O
USB devices	USB Signal Stream,
	programmed I/O
DO or DI Sample Clock source <sup>3</sup>	Any PFI, RTSI,
	AI Sample or
	Convert Clock,
	AO Sample Clock,
	Ctr n Internal Output,
	and many other signals

## PFI/Port 1/Port 2 Functionality<sup>4</sup>

Functionality	Static digital input, static digital output, timing input, timing output
Timing output sources	Many AI, AO, counter, DI, DO timing signals
Debounce filter settings	125 ns, 6.425 μs, 2.56 ms, disable; high and low transitions; selectable per input

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<sup>&</sup>lt;sup>1</sup> Stresses beyond those listed under *Input voltage protection* may cause permanent damage to the device.

<sup>&</sup>lt;sup>2</sup> Performance can be dependent on bus latency and volume of bus activity.

<sup>3</sup> The digital subsystem does not have its own dedicated internal timing engine. Therefore, a sample clock must be provided from another subsystem on the device or an external source.

<sup>&</sup>lt;sup>4</sup> Port 2 is not available on PCI-6221 (37-pin) devices.

# **Recommended Operation Conditions**

PCI/PXI devices

Level	Min	Max
Input high voltage (V <sub>IH</sub> )	2.2 V	5.25 V
Input low voltage (V <sub>IL</sub> )	0 V	0.8 V
Output high current (I <sub>OH</sub> )		
P0.<031>	_	-24 mA
PFI <015>/P1/P2	_	-16 mA
Output low current (I <sub>OL</sub> )		
P0.<031>	_	24 mA
PFI <015>/P1/P2	_	16 mA

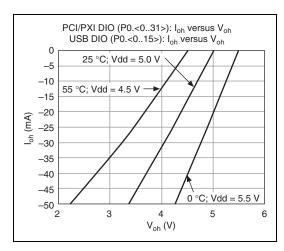
#### USB devices

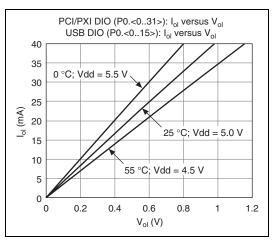
Level	Min	Max
Input high voltage (V <sub>IH</sub> )	2.2 V	5.25 V
Input low voltage (V <sub>IL</sub> )	0 V	0.8 V
Output high current (I <sub>OH</sub> )		
P0.<015>	_	-24 mA
P0.<1631>	_	-16 mA
PFI <015>/P1/P2	_	-16 mA
Output low current (I <sub>OL</sub> )		
P0.<015>	_	24 mA
P0.<1631>	_	16 mA
PFI <015>/P1/P2	_	16 mA

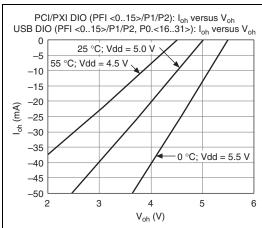
## **Electrical Characteristics**

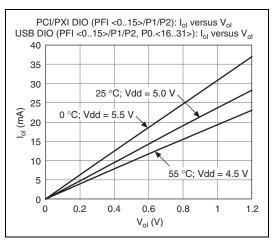
Level	Min	Max
Positive-going threshold (VT+)	_	2.2 V
Negative-going threshold (VT–)	0.8 V	_
Delta VT hysteresis (VT+ – VT–)	0.2 V	_
$I_{IL}$ input low current ( $V_{in} = 0 \text{ V}$ )	_	-10 μA
$I_{IH}$ input high current ( $V_{in} = 5 \text{ V}$ )	_	250 μΑ

#### **Digital I/O Characteristics**









General-Purpose Counter/Timers		Phase-Locked Loop (PLL)	
Number of counter/timers	2	Number of PLLs	1
Resolution	32 bits	Reference signal	PXI_STAR,
Counter measurements	Edge counting		PXI_CLK10,
Counter measurements	pulse,		RTSI <07>
	semi-period,	Output of PLL	
	period,		other signals derived
	two-edge separation		from 80 MHz Timebase
Position measurements	X1, X2, X4 quadrature		including 20 MHz and 100 kHz Timebases
	encoding with		100 kmz Timebases
	Channel Z reloading;	Evtornal Digital Trigge	<b>*</b> 0
	two-pulse encoding	External Digital Trigge	
Output applications	Pulse, pulse train with	Source	
F	dynamic updates,		PXI_TRIG,
	frequency division,		PXI_STAR
	equivalent time sampling	Polarity	Software-selectable for
Internal base clocks	80 MHz		most signals
	20 MHz,	Analog input function	Start Trigger.
	0.1 MHz	8 <del>-</del>	Reference Trigger,
External base clock frequency	0 MHz to 20 MHz		Pause Trigger,
External base clock frequency	U MITZ 10 20 MITZ		Sample Clock,
Base clock accuracy	50 ppm		Convert Clock,
Inputs	Gate Source HW Arm		Sample Clock Timebase
iiiputs	Aux, A, B, Z, Up_Down	Analog output function	Start Trigger,
<b></b>	•		Pause Trigger,
Routing options for inputs	•		Sample Clock,
	PXI_TRIG, PXI_STAR,		Sample Clock Timebase
	analog trigger,	Counter/timer functions	Gate, Source, HW_Arm,
	many internal signals		Aux, A, B, Z, Up_Down,
FIFO	2 camples	Digital waveform generation	
	2 samples	(DO) function	Sample Clock
Data transfers		Digital waysfarm a aquisition	-
PCI/PXI devices		Digital waveform acquisition (DI) function	Sample Clock
	DMA controller for each counter/timer:	(D1) Tunetion	Sample Clock
	interrupts;		
	programmed I/O		
USB devices			
COD de vices	programmed I/O		
Frequency Generator			
Number of channels	1		
Base clocks	10 MHz, 100 kHz		
Divisors	1 to 16		
Base clock accuracy	50 ppm		
Output can be available on any Pl	FI or RTSI terminal.		

#### **Device-To-Device Trigger Bus**

PCI devices .....RTSI <0..7>1

PXI devices......PXI\_TRIG <0..7>,
PXI\_STAR

USB devices ......None

many internal signals

Debounce filter settings......125 ns, 6.425 μs, 2.56 ms, disabled;

high and low transitions; selectable per input

#### **Bus Interface**

USB devices ......USB 2.0 Hi-Speed or full-speed<sup>2</sup>

DMA channels

counter/timer 0,

counter/timer 1

USB Signal Stream

All PXI-622x devices support one of the following features:

- May be installed in PXI Express hybrid slots
- Or, may be used to control SCXI in PXI/SCXI combo chassis

**Table 1.** PXI/SCXI Combo and PXI Express Chassis Compatibility

M Series Device	M Series Part Number	SCXI Control in PXI/SCXI Combo Chassis	PXI Express Hybrid Slot Compatible
PXI-6220	191332B-04	No	Yes
PXI-6221	191332B-03	No	Yes
	191332B-13	Yes	No
PXI-6224	191332B-02	No	Yes
PXI-6225	192227A-01	No	Yes
PXI-6229	191332B-01	No	Yes
	191332B-11	Yes	No
Earlier versions of PXI-6220/ 6221/6224/ 6229	191332A-0 <i>x</i>	Yes	No

## **Power Requirements**

Current draw from bus during no-load condition<sup>3</sup>

+5 V	0.02 A <sup>4</sup>
+3.3 V	0.25 A <sup>4</sup>
+12 V	0.15 A

Current draw from bus during AI and AO overvoltage condition<sup>3</sup>

+5 V	$0.02 A^4$
+3.3 V	0.25 A <sup>4</sup>
+12 V	0.25 A



**Caution** USB-622x devices must be powered with NI offered AC adapter or a National Electric Code (NEC) Class 2 DC source that meets the power requirements for the device and has appropriate safety certification marks for country of use.

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<sup>&</sup>lt;sup>1</sup> In other sections of this document, RTSI refers to RTSI <0..7> for PCI devices or PXI\_TRIG <0..7> for PXI devices.

<sup>&</sup>lt;sup>2</sup> If you are using a USB M Series device in full-speed mode, device performance will be lower and you will not be able to achieve maximum sampling/update rates.

<sup>&</sup>lt;sup>3</sup> Does not include P0/PFI/P1/P2 and +5 V terminals.

<sup>&</sup>lt;sup>4</sup> PCI-6221 (37-pin) devices do not use +3.3 V from the bus. The 3.3 V current draw, shown in the *Power Requirements* section, comes from the +5 V instead.

USB power supply requirements	11 to 30 VDC, 20 W,
	locking or non-locking
	power jack with 0.080"
	diameter center pin,
	5/16-32 thread for
	locking collars

#### **Power Limits**



Caution Exceeding the power limits may cause unpredictable behavior by the device and/or PC/chassis.

PCI devices
+5 V terminal (connector 0) 1 A max <sup>1</sup>
+5 V terminal (connector 1) 1 A max <sup>1</sup>
PXI devices
+5 V terminal (connector 0) 1 A max <sup>1</sup>
+5 V terminal (connector 1) 1 A max <sup>1</sup>
P0/PFI/P1/P2 and +5 V
terminals combined 2 A max
USB devices
+5 V terminal 1 A max <sup>1</sup>
P0/PFI/P1/P2 and +5 V
terminals combined
Power supply fuse

## **Physical Requirements** Printed circuit board dimensions

PCI-6220/6221/6224/	
6225/6229	9.7 cm $\times$ 15.5 cm
	$(3.8 \text{ in.} \times 6.1 \text{ in.})$
PXI-6220/6221/6224/	
6225/6229	Standard 311 PXI

#### Er

Enclosure dimensions (includes connectors)		
USB-6221/6225/6229		
Screw Terminal	$26.67 \times 17.09 \times 4.45$ cm	
	$(10.5 \times 6.73 \times 1.75 \text{ in.})$	
USB-6221/6229 BNC	$28.6 \times 17 \times 6.9$ cm	
	$(11.25 \times 6.7 \times 2.7 \text{ in.})$	
USB-6225 Mass Termination	$18.8 \times 17.09 \times 4.45$ cm	
	$(7.4 \times 6.73 \times 1.75 \text{ in.})$	
USB-6221/6225/6229 OEM	Refer to the	
	NI USB-622x/625x OEM	

#### Weight

veight
PCI-622091 g (3.2 oz)
PCI-6221 (68-pin)92 g (3.2 oz)
PCI-6221 (37-pin)95 g (3.3 oz)
PCI-622499 g (3.5 oz)
PCI-6225103 g (3.6 oz)
PCI-6229101 g (3.5 oz)
PXI-6220158 g (5.5 oz)
PXI-6221162 g (5.7 oz)
PXI-6224170 g (5.9 oz)
PXI-6225174 g (6.1 oz)
PXI-6229171 g (6.0 oz)
USB-6221 Screw Terminal1.2 kg (2 lb 10 oz)
USB-6225/6229
Screw Terminal
USB-6225 Mass Termination907 g (2 lb)
USB-6221 OEM131 g (4.6 oz)
USB-6225/6229 OEM162 g (5.7 oz)
O connector
PCI/PXI-6220/6221 (68-pin) 1 68-pin VHDCI
PCI/PXI-6224/6225/62292 68-pin VHDCI
PCI-6221 (37-pin) 1 37-pin D-SUB
USB-6221 Screw Terminal64 screw terminals
LICD 6225/6220

#### I/C

· •	1
PCI/PXI-6224/6225/6229	2 68-pin VHDCI
PCI-6221 (37-pin)	1 37-pin D-SUB
USB-6221 Screw Terminal	64 screw terminals
USB-6225/6229	
Screw Terminal	128 screw terminals
USB-6221 BNC	20 BNCs and
	30 screw terminals
USB-6229 BNC	30 BNCs and
	60 screw terminals
USB-6225 Mass Termination	2 68-pin SCSI
JSB-6221/6225/6229 Screw Ter	minal/USB-6221/6229 BNC

# Maximum Working Voltage<sup>2</sup>

screw terminal wiring......16-28 AWG

NI 6220/6221/6224/6225/6229 Channel to earth ......11 V, Measurement Category I



Caution Do not use for measurements within Categories II, III, or IV.

User Guide

<sup>&</sup>lt;sup>1</sup> Has a self-resetting fuse that opens when current exceeds this specification.

<sup>&</sup>lt;sup>2</sup> Maximum working voltage refers to the signal voltage plus the common-mode voltage.

#### Environmental

#### Shock and Vibration (PXI Devices Only)

Operational shock	30 g peak, half-sine,
	11 ms pulse
	(Tested in accordance
	with IEC-60068-2-27.
	Test profile developed
	in accordance with
	MIL-PRF-28800F.)

# Random vibration

Operating 5 to 500 Hz, 0.5 grms	
Nonoperating	5 to 500 Hz, 2.4 g <sub>rms</sub>
(	Tested in accordance
V	with IEC-60068-2-64.
ı	Nonoperating test profile
e	exceeds the requirements
C	of MIL-PRF-28800F,
(	Class 3.)

5 to 500 Hz 0.3 g

# Safety

This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1



**Note** For UL and other safety certifications, refer to the product label or visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

# **Electromagnetic Compatibility**

This product is designed to meet the requirements of the following standards of EMC for electrical equipment for measurement, control, and laboratory use:

- EN 61326 EMC requirements; Minimum Immunity
- EN 55011 Emissions; Group 1, Class A
- CE, C-Tick, ICES, and FCC Part 15 Emissions; Class A



**Note** For EMC compliance, operate this device with shielded cables

## **CE Compliance**

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

- 73/23/EEC; Low-Voltage Directive (safety)
- 89/336/EEC; Electromagnetic Compatibility Directive (EMC)



**Note** Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

# **Environmental Management**

National Instruments is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial not only to the environment but also to NI customers.

For additional environmental information, refer to the NI and the Environment Web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as any other environmental information not included in this document.

#### Waste Electrical and Electronic Equipment (WEEE)



**EU Customers** At the end of their life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers and National Instruments WEEE initiatives, visit ni.com/environment/weee.htm.

#### 电子信息产品污染控制管理办法 (中国 RoHS)



中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于National Instruments 中国 RoHS 合规性信息,请登录 ni.com/environment/rohs\_china。(For information about China RoHS compliance, go to ni.com/environment/rohs\_china.)

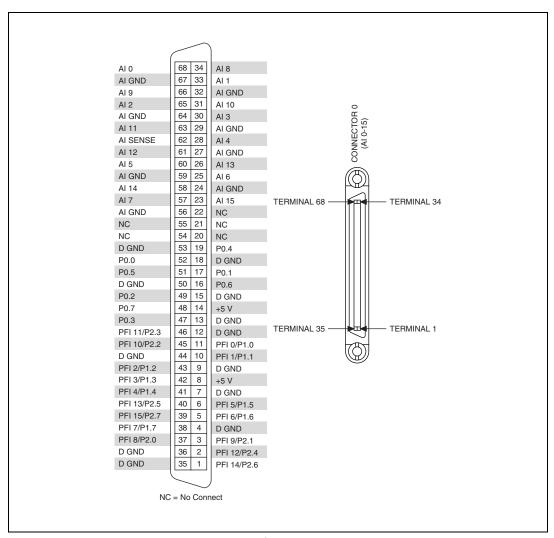


Figure 1. PCI/PXI-6220 Pinout

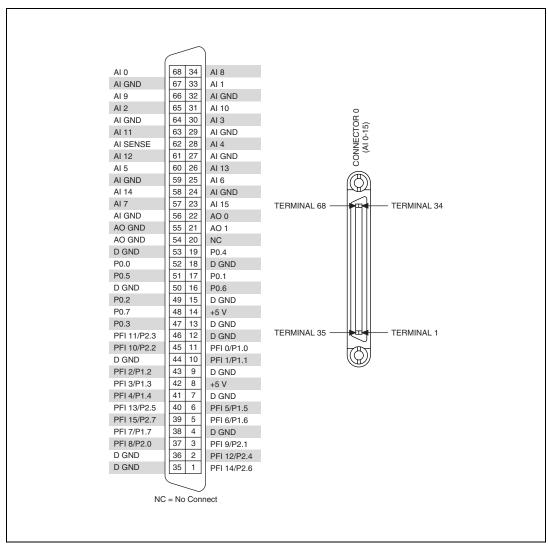


Figure 2. PCI/PXI-6221 (68-Pin) Pinout

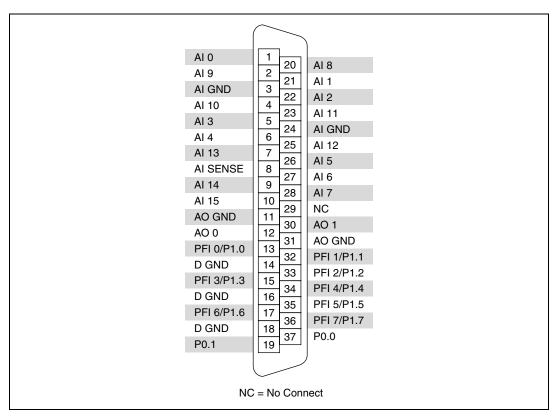


Figure 3. PCI-6221 (37-Pin) Pinout

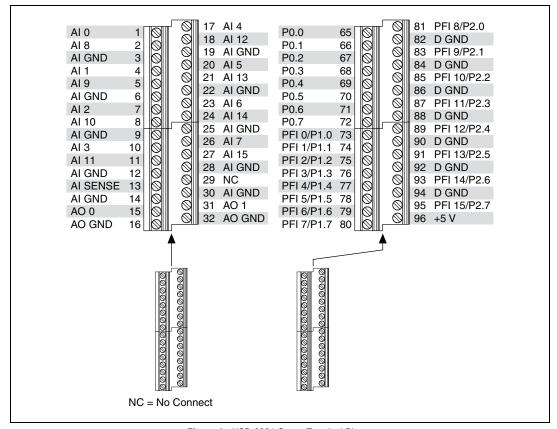


Figure 4. USB-6221 Screw Terminal Pinout

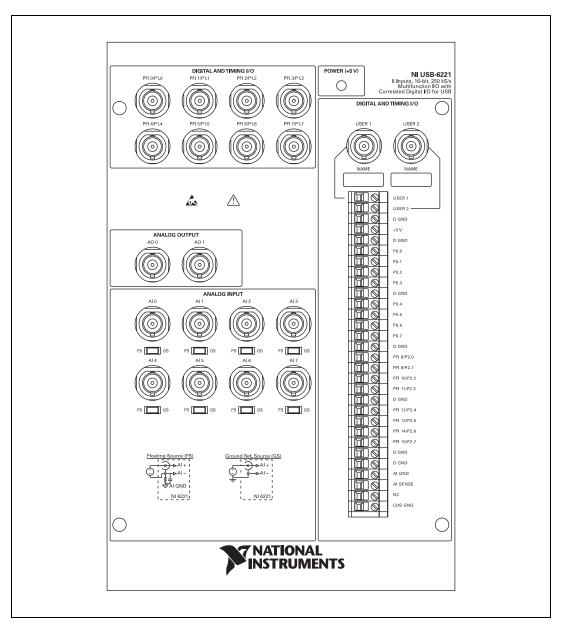


Figure 5. USB-6221 BNC Top Panel and Pinout

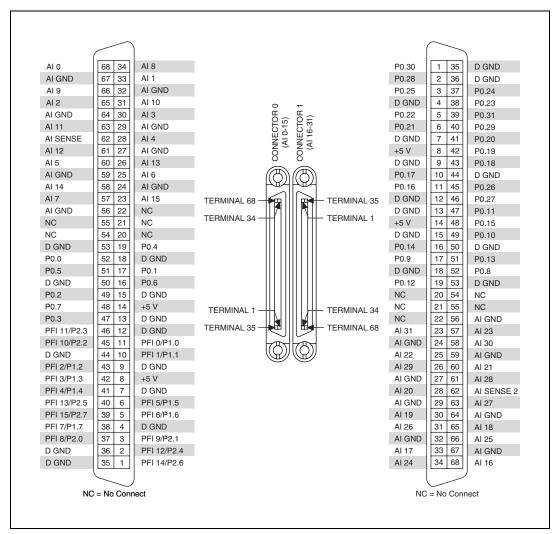


Figure 6. PCI/PXI-6224 Pinout

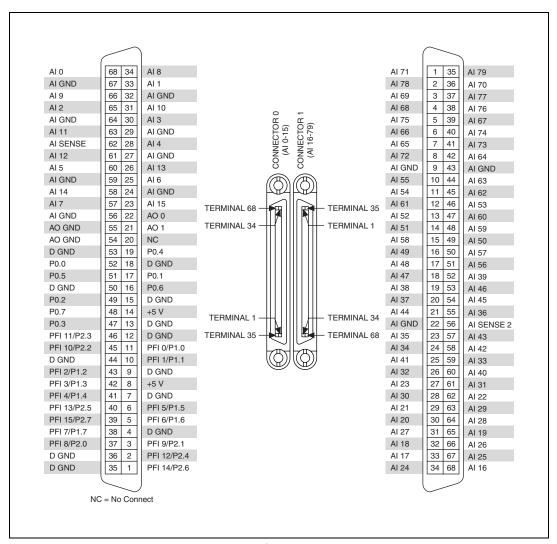


Figure 7. PCI/PXI-6225 Pinout

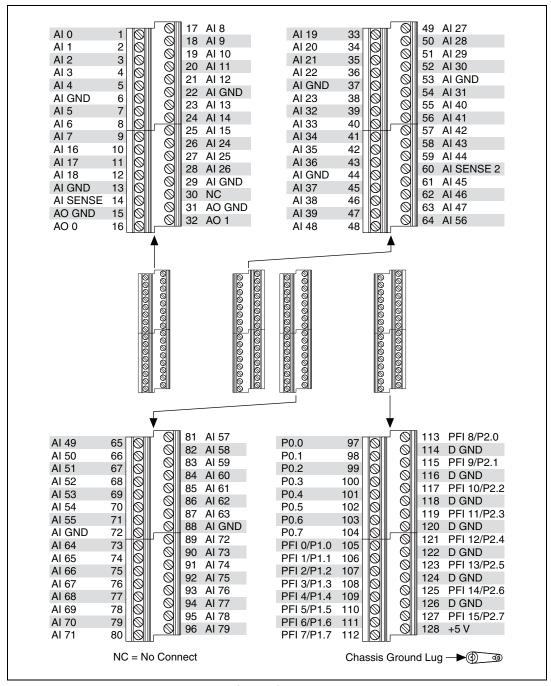


Figure 8. USB-6225 Screw Terminal Pinout

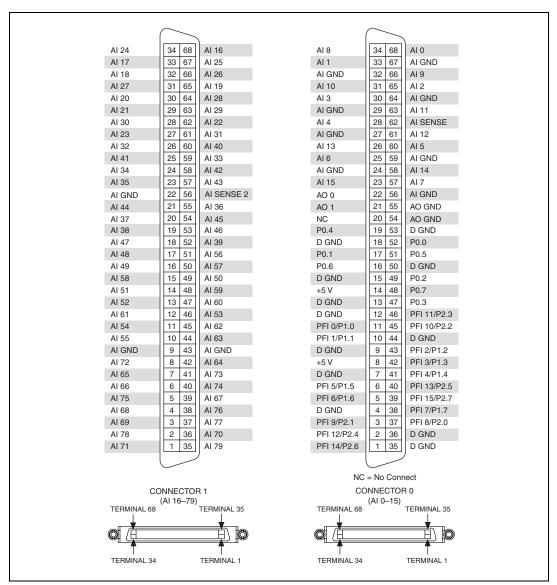


Figure 9. USB-6225 Mass Termination Pinout

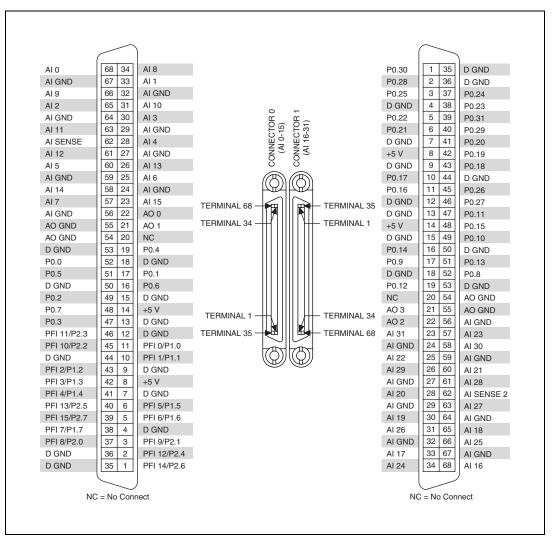


Figure 10. PCI/PXI-6229 Pinout

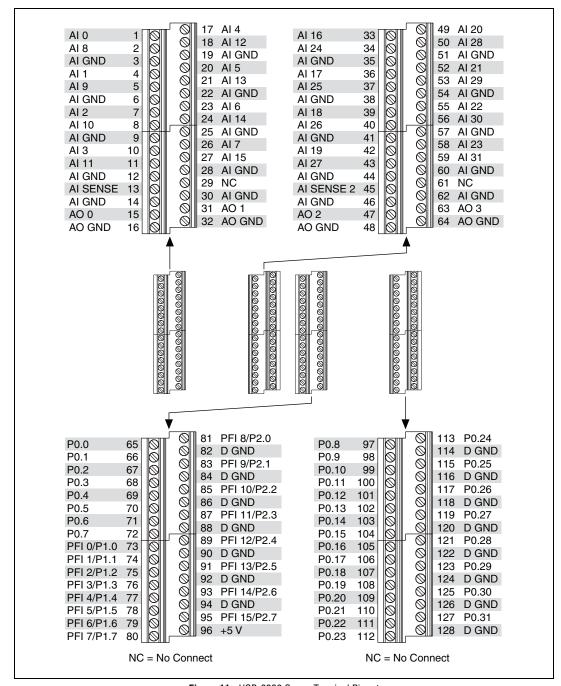


Figure 11. USB-6229 Screw Terminal Pinout

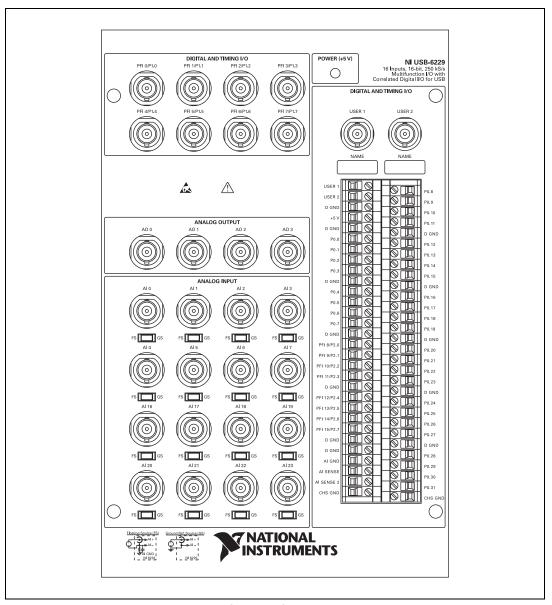


Figure 12. USB-6229 BNC Top Panel and Pinout

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