

BUG2 WIFI

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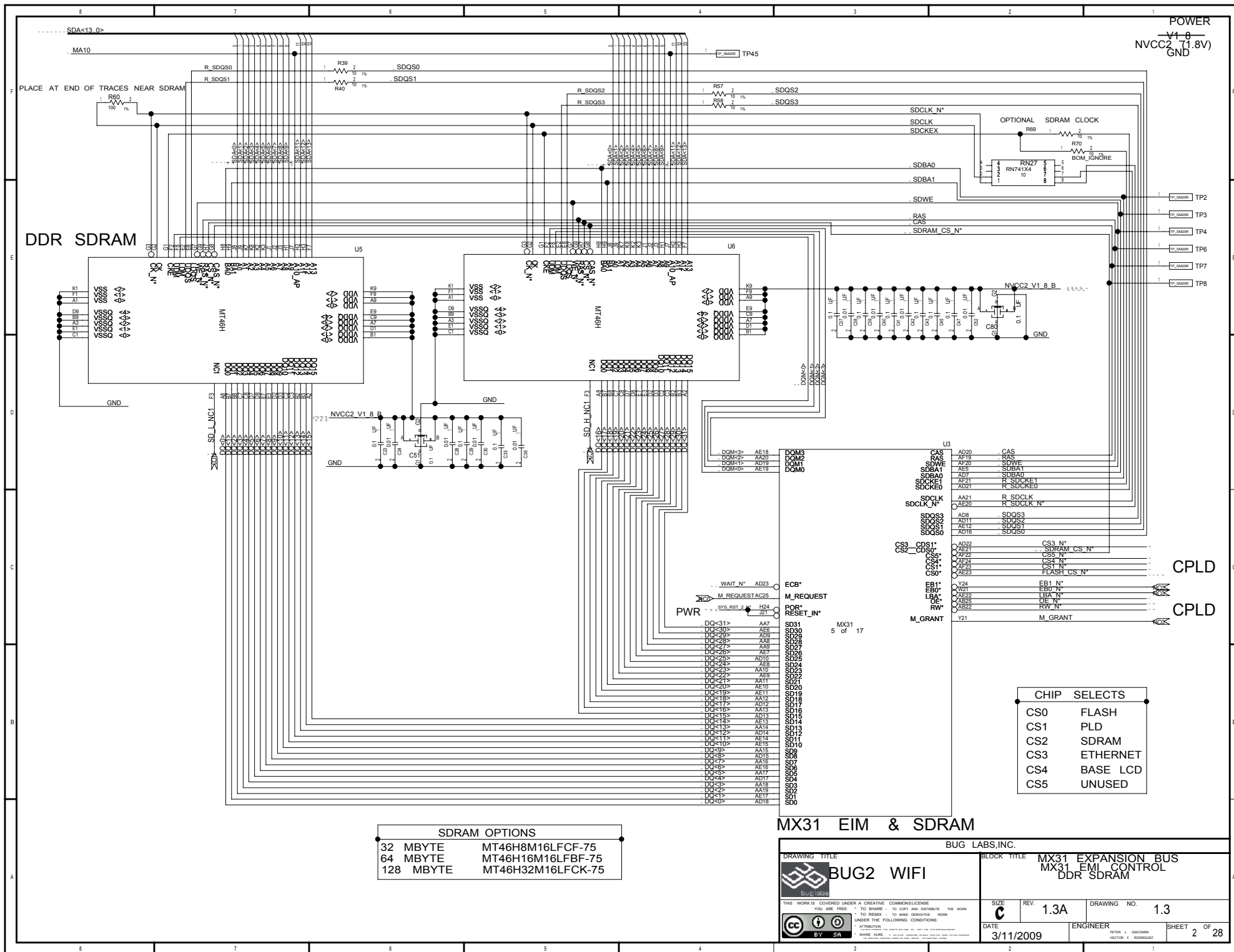
BUG LABS, INC.

BLOCK TITLE MX31 EXPANSION BUS
MX31 EMI ADDRESS & DATA BUSES
BUS BUFFERS & NOR FLASH

SIZE C **REV.** 1.3A **DRAWING NO.** 1.3

DATE 3/11/2009 **ENGINEER** ENCADIS **PETIT J.** **DESIGNER** ENCADIS **RECTOR F.** **REVIEWER**

SHEET 1 **OF** 28



POWER
V3 3
NVCC8 (2.8V)
NVCC7 (2.8V)
NVCC1 (2.8V)
GND

BOOT MODE CONTROL
DEFAULT = 16-BIT CS0 EXTERNAL
SEE MX31 DOCUMENTATION

CPLD

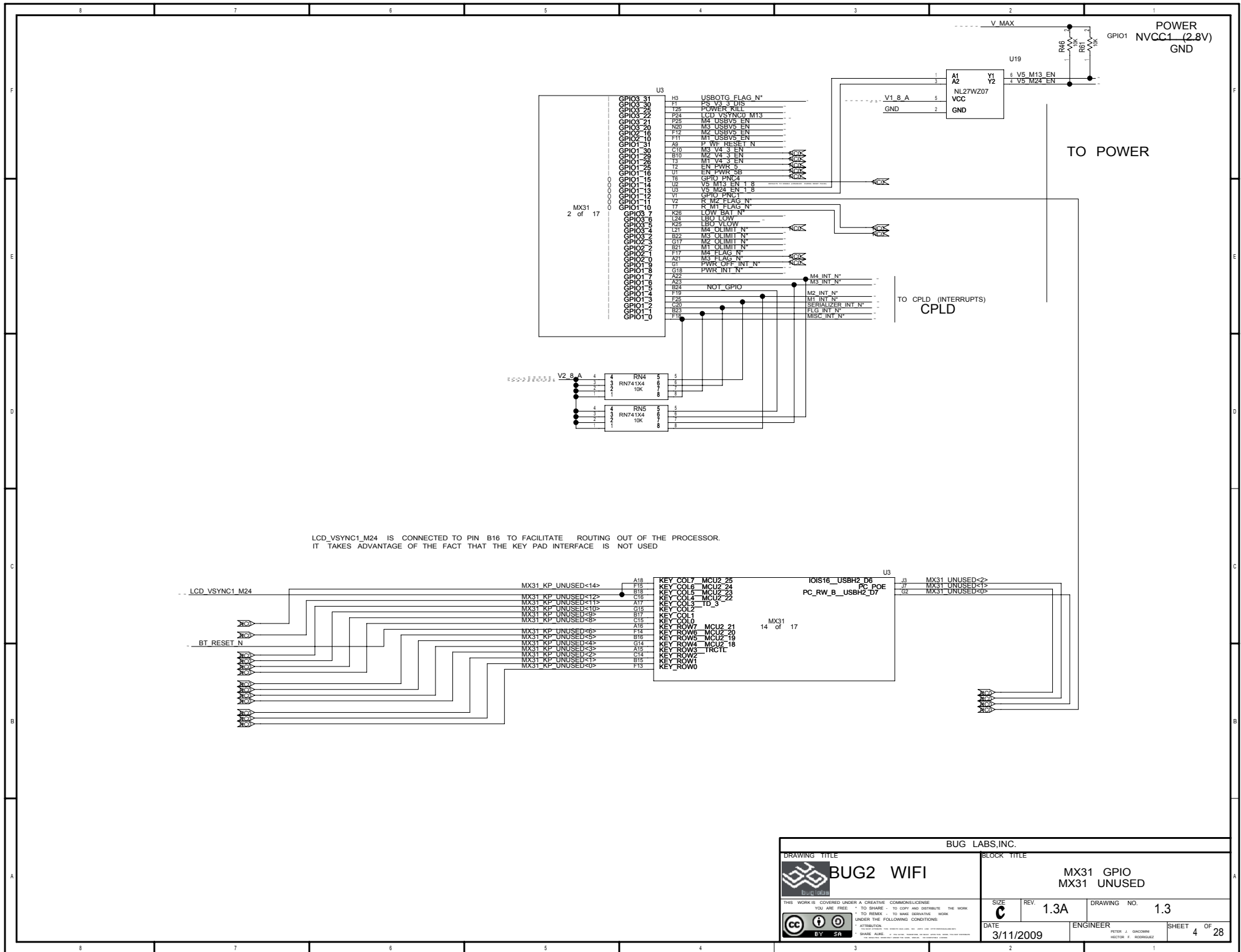
CKIH IS REFERENCE CLOCK
FPM IS DEFAULT REFERENCE CLOCK
SEE MX31 DOCUMENTATION

BOTTOM GROUND LANDS FOR SHIELD

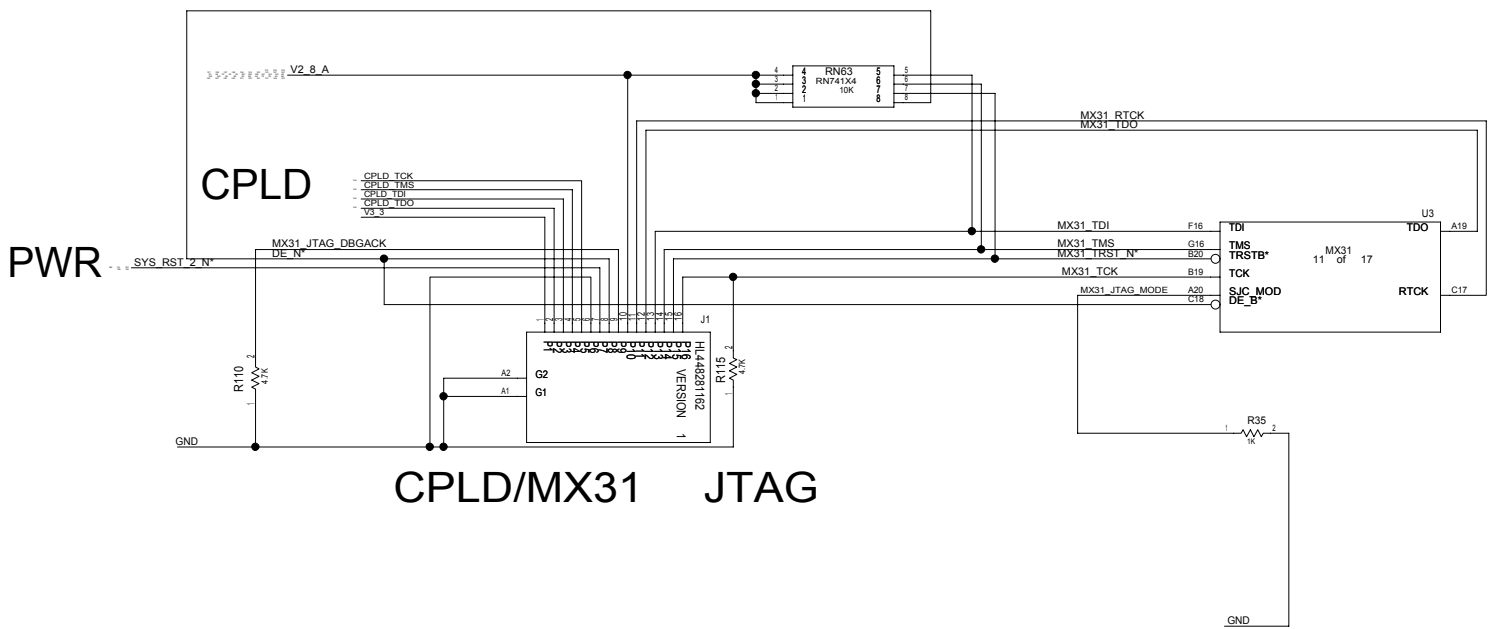
GROUNDING BOARD MOUNTING HOLES

TOP GROUND LANDS FOR SHIELD



DRAWING TITLE BUG2 WIFI		BLOCK TITLE MX31 BOOT & CE CONTROL MX31 CLOCKING OSCILLATORS & CLOCKS	
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DATE 3/11/2009		ENGINEER PETER J. GONCANN NICHOLAS F. RODRIGUEZ	DRAWING NO. 1.3
		SHEET 3	OF 28



POWER
 $V2 \frac{8}{NVCC69} (2.8V)$
 GND



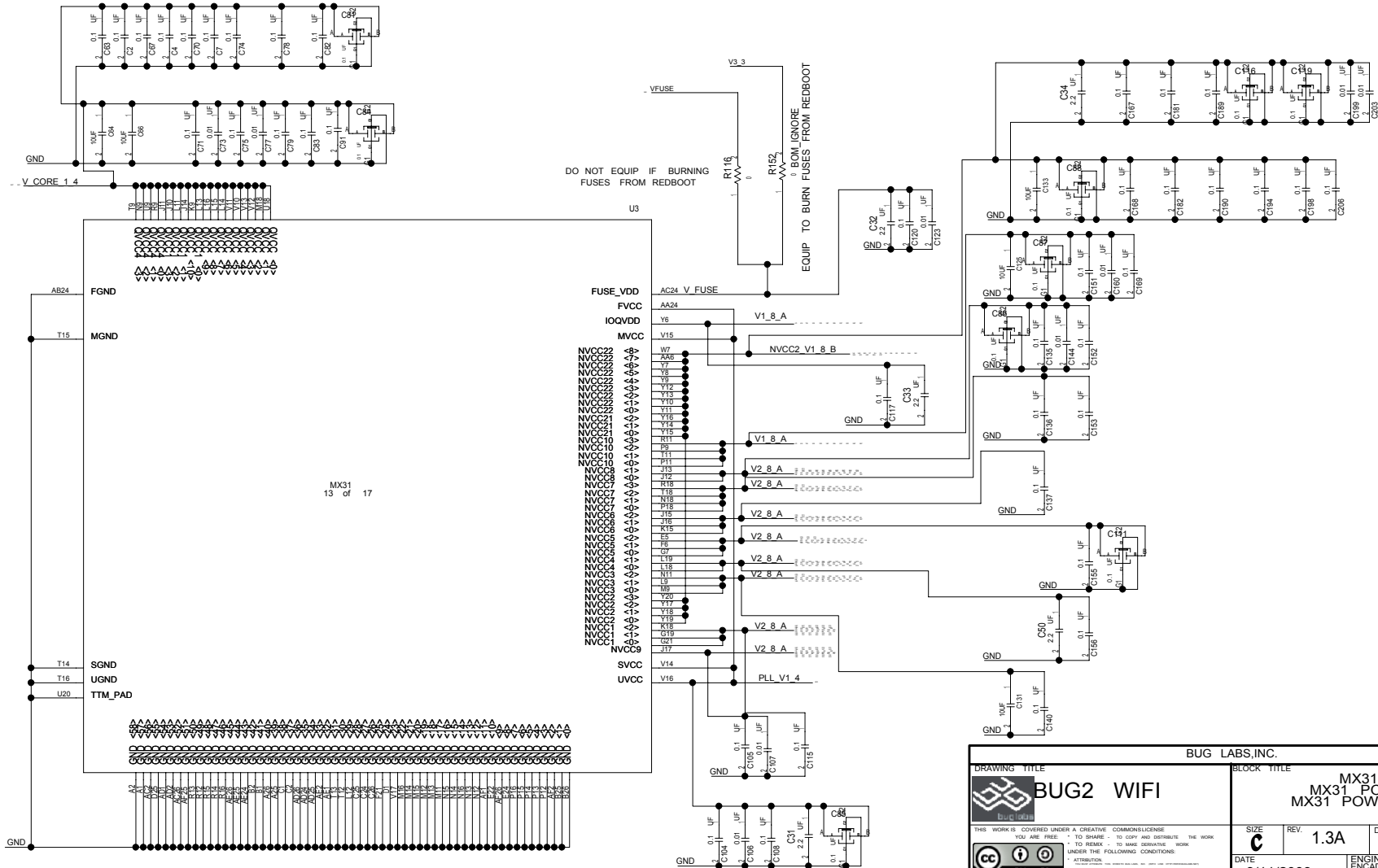
CPLD/MX31 JTAG

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2. SHARE Alike		DATE	ENGINEER	SHEET
3. BY SA		3/11/2009	ENCADIS DESIGN, INC. PETER A. GARDNER, DIRECTOR P. RODRIGUEZ	5 OF 28

PWR
CPLD

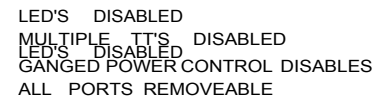
CPLD

POWER
V_FUSE(3.3V/1.8V)
V3 3
NVCC8(2.8V)
NVCC7(2.8V)
NVCC6(2.8V)
NVCC5(2.8V)
NVCC4(2.8V)
NVCC3(2.8V)
NVCC1(2.8V)
NVCC9(2.8V)
NVCC10(1.8V)
NVCC2(1.8V)
XVCC(1.5V)
QVCC(1.3V)
GND



DRAWING TITLE		BLOCK TITLE	
BUG2 WIFI		MX31 POWER CONTROL MX31 POWER DECOUPLING	
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POWER
V5 0
WIFI_PWR (5.0V)
V3 3
GND



CPLD

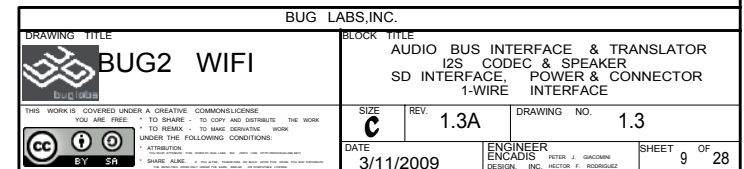
ROUTE USB BUSSES AS 90 OHM DIFFERENTIAL

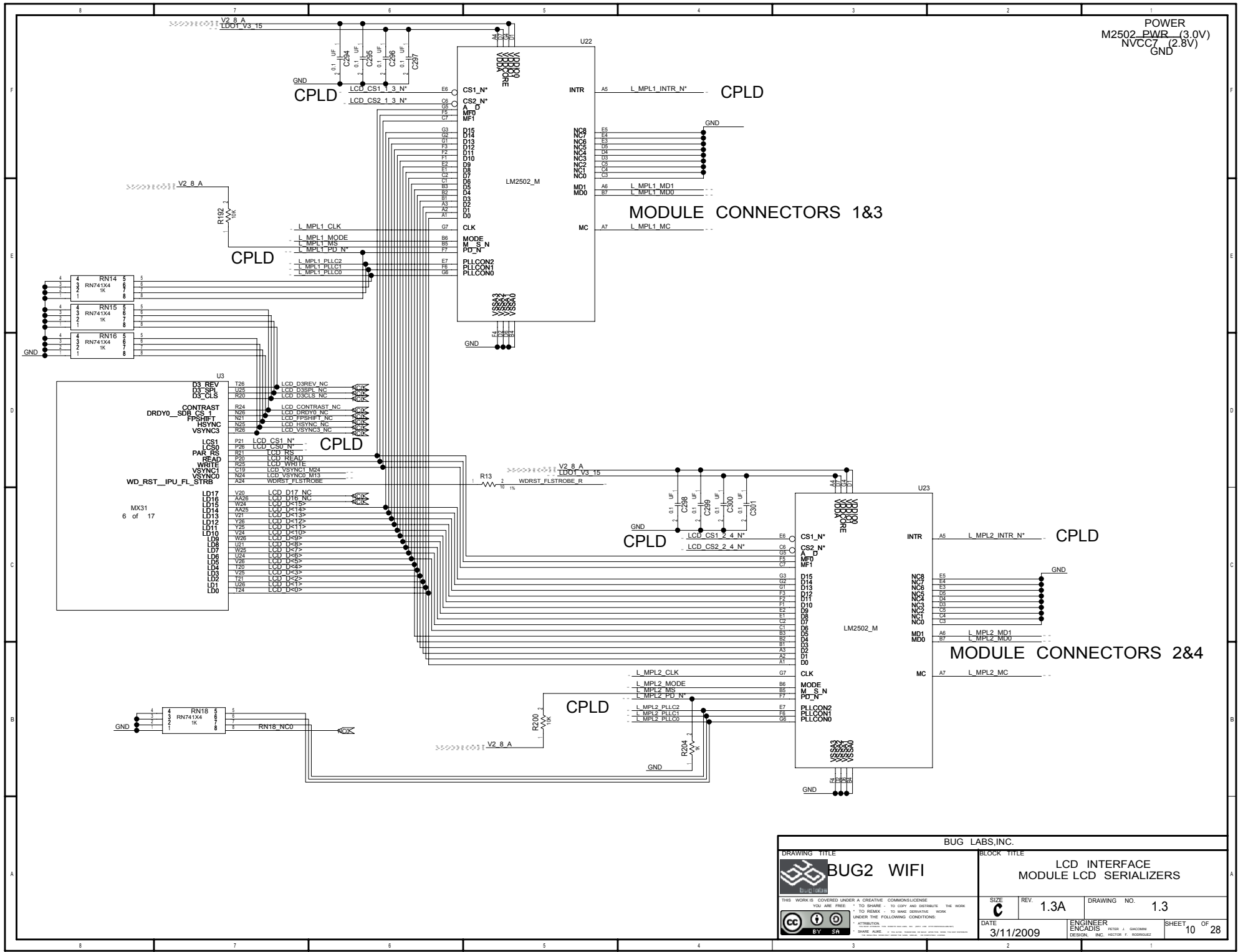
MODULE 1
MODULE 2
MODULE 3
MODULE 4



DRAWING TITLE						BLOCK TITLE					
 BUG2 WIFI						USB HOST HUB SD POWER					
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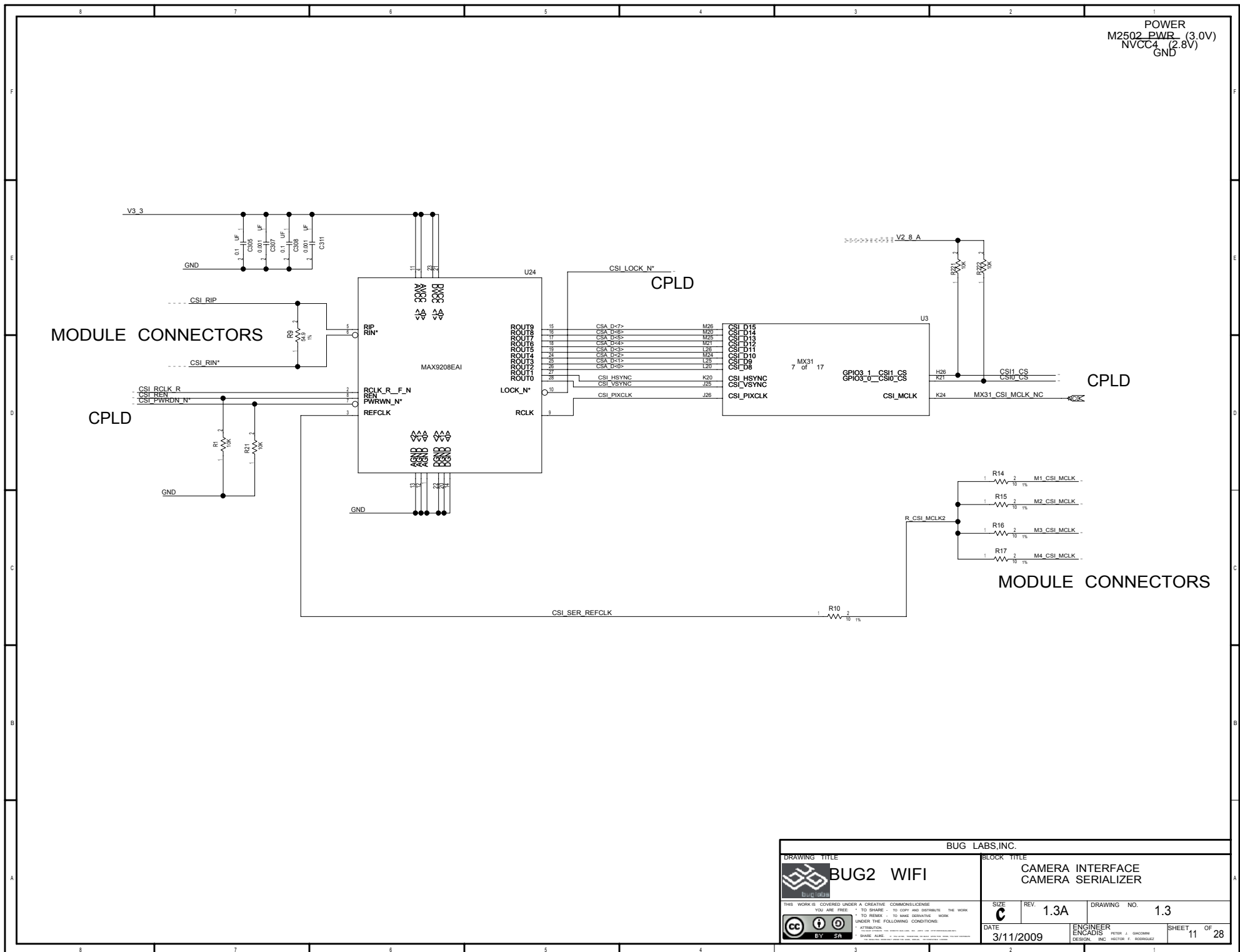
POWER

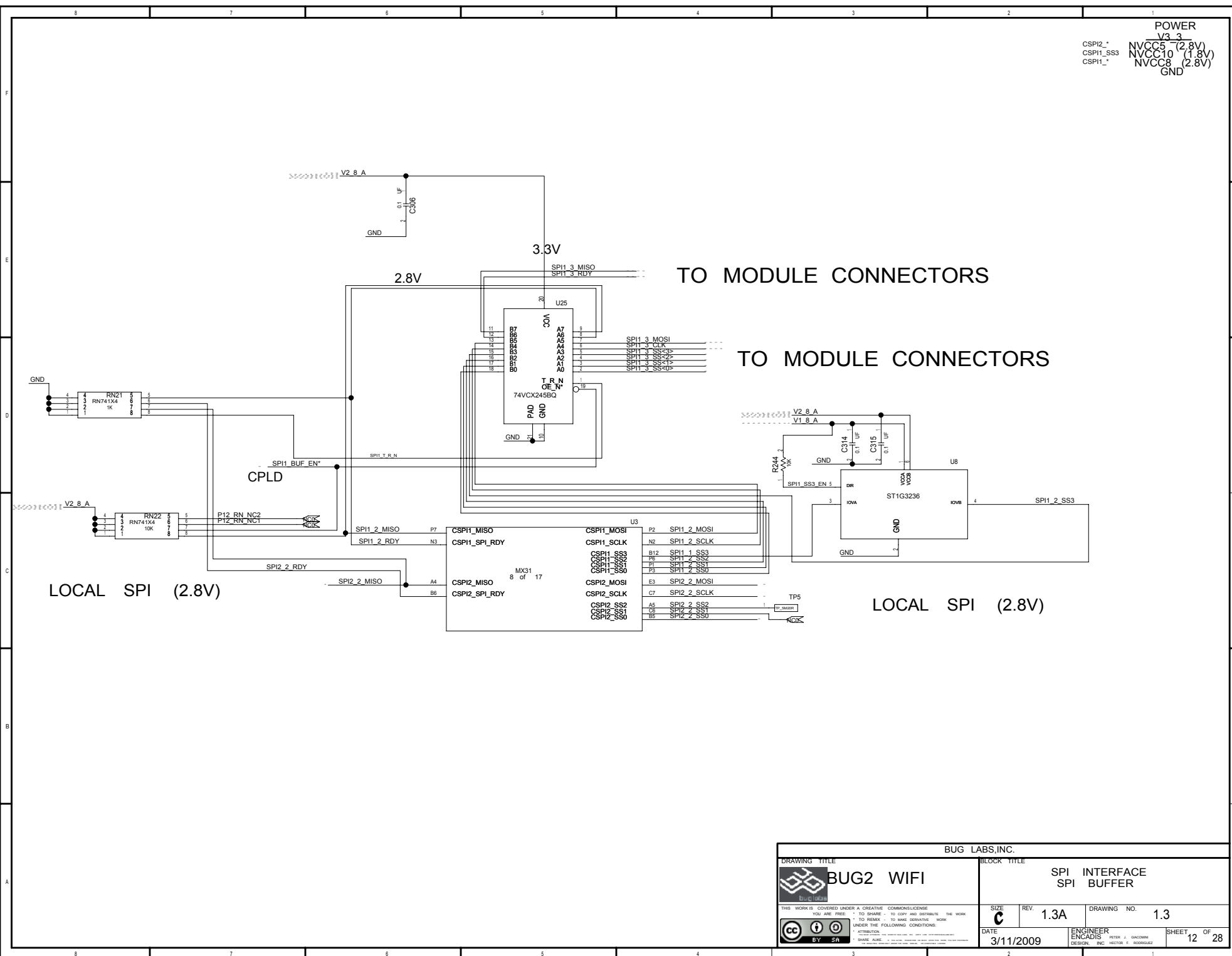
SD	V3_3
NVCC5	(V2.8)
NVCC3	(V2.8)
V1_8	A
GND	



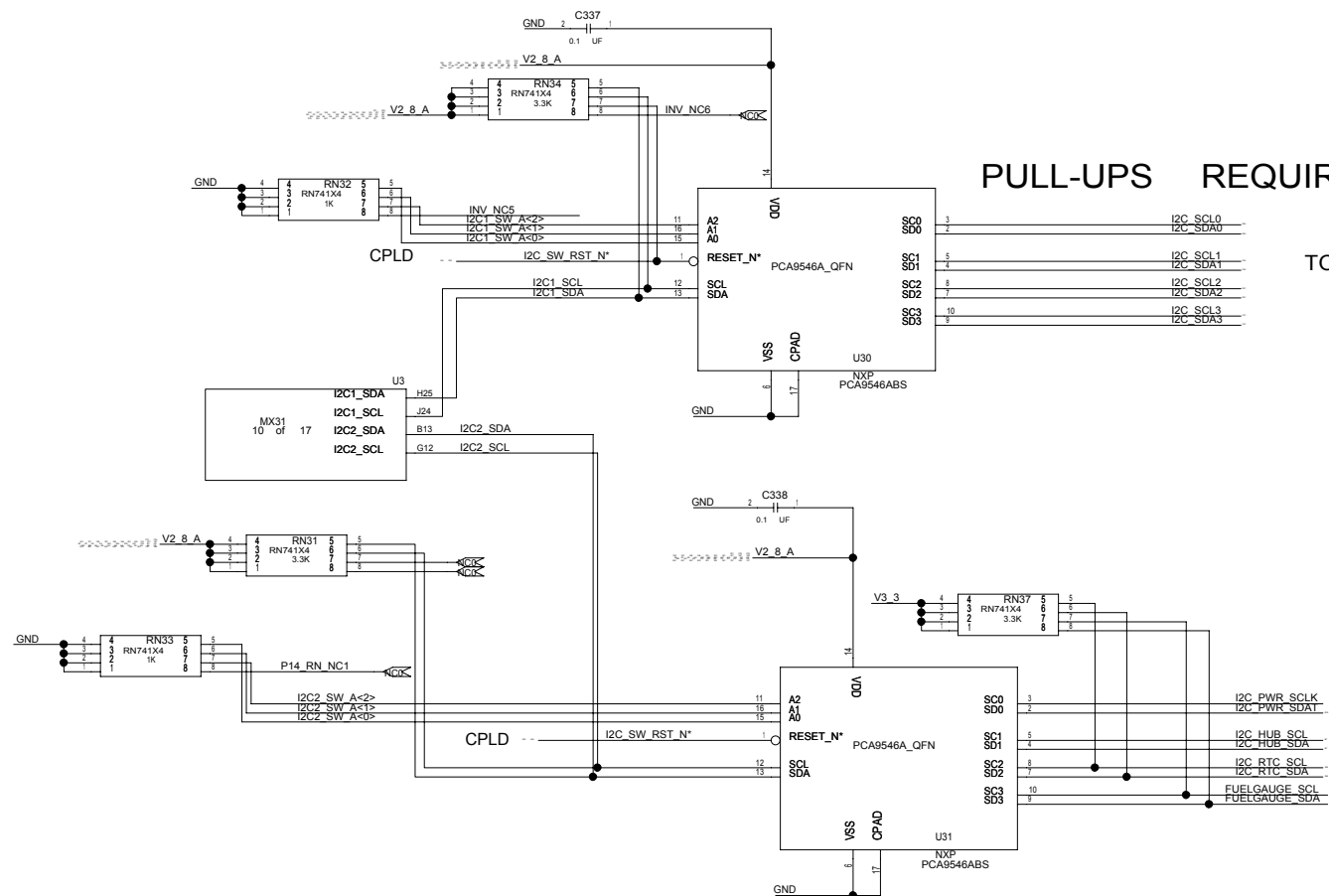


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<small>DATE: 3/11/2009</small>		<small>ENGINEER: ENCADIS DESIGN, INC. PETER J. GARCIA RODRIGUEZ</small>	
DATE		REV.	DRAWING NO.
3/11/2009		1.3A	1.3
SHEET 10		OF 28	
3		1	





POWER
V3_3
I2C1_* NVCC4 (2.8V)
I2C2_* NVCC8 (2.8V)
GND



PULL-UPS REQUIRED ON PLUG-IN MODULE

TO MODULE CONNECTORS

TO LOCAL I2C

DRAWING TITLE				BLOCK TITLE			
BUG2 WIFI				I2C INTERFACES I2C SWITCH			
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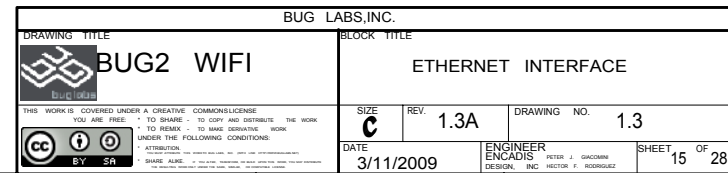
```

      POWER
      V3_3
BYPASS ONLY E_PLL_V1_8
BYPASS ONLY E_CORE_V1_8
FILTERED V3_3 E_VDDA
          GND

```

ROUTE EXT_PWR TRACE TO HANDLE AT LEAST 8A

J14





CPLD

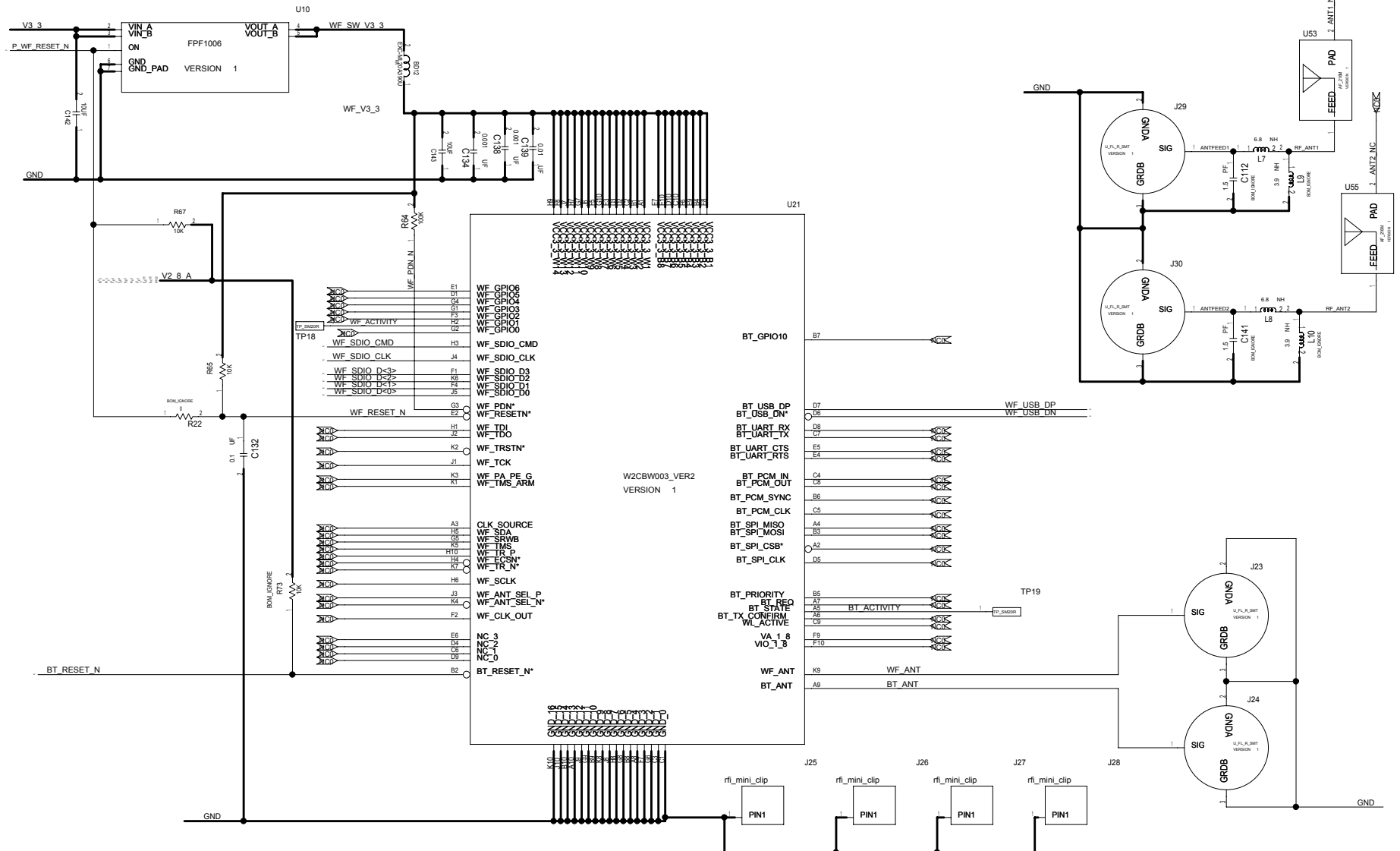
POWER
V3_3
GND

CPLD

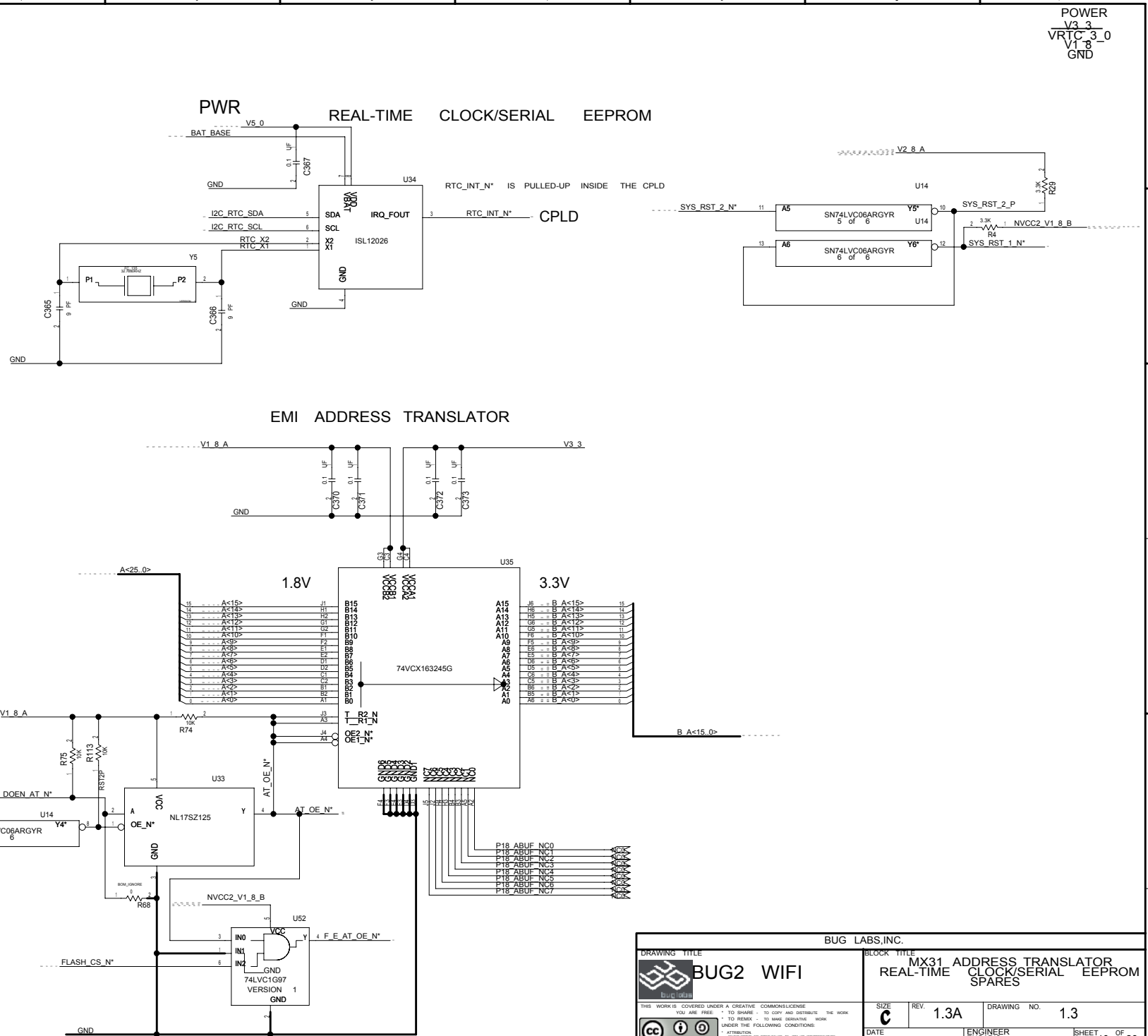
CPLD

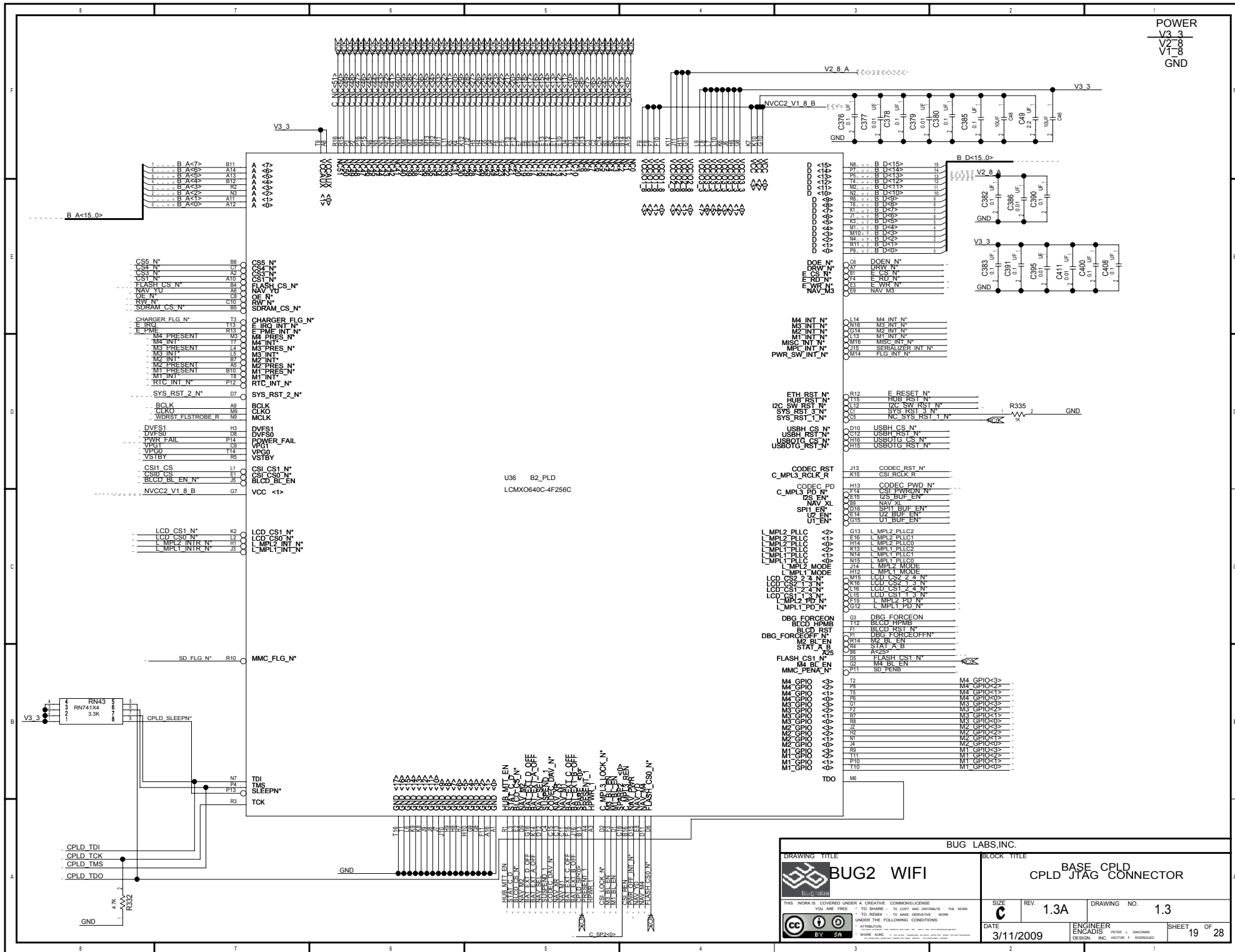
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DRAWING TITLE		BLOCK TITLE	
 BUG2 WIFI		BASE LCD BUTTONS	
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DESIGNER ENCADIS		PETTER J. GONCALVES	SHEET 16 OF 28

802.11 INTERFACE (BASED ON W12W1 MODULE USING SDIO INTERFACE)



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BUG2 WIFI				802.11 INTERFACE			
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DATE				ENGINEER ENCLOSURE			
DATE				SHEET 17 OF 28			

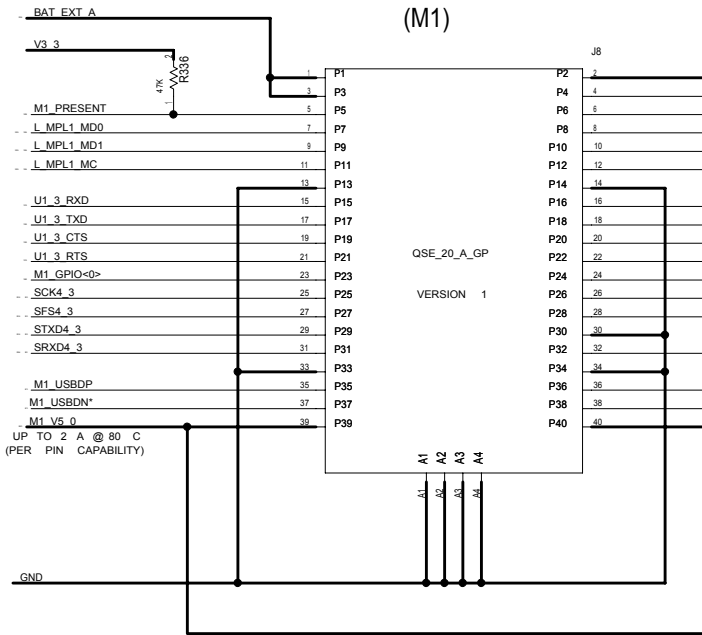




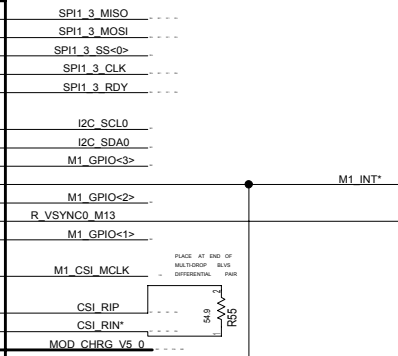
DRAWING TITLE		BLOCK TITLE	
BUG2 WIFI		BASE CPLD CPLD JTAG CONNECTOR	
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ENGINEER ENCADIS		SHEET 19 OF 28	

MODULE 1

UP TO 4 AMPS AT 80 C

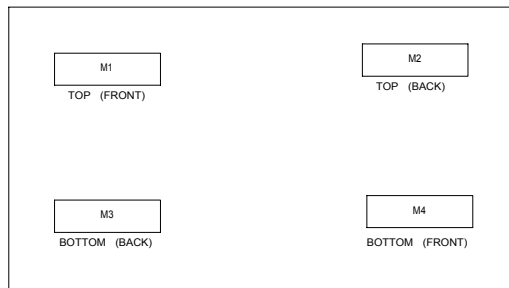


UP TO 2 A @ 80 C
(PER PIN CAPABILITY)



POWER
V3_3
GND

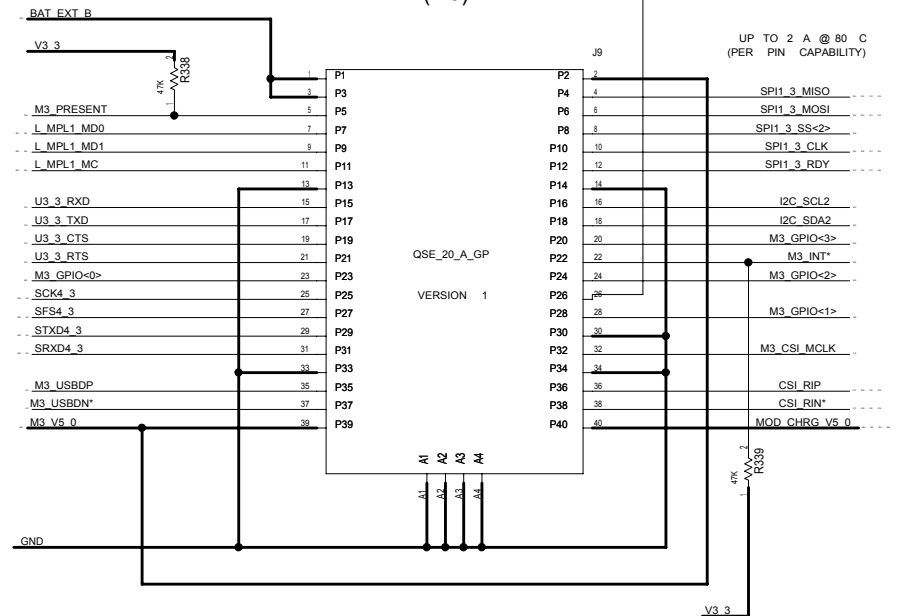
PLACE M1 AND M3 ON SAME VERTICAL HALF
OF BASE ON OPPOSITE SIDES



MODULE 3

(M3)

UP TO 2 A @ 80 C
(PER PIN CAPABILITY)



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DRAWING TITLE



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BLOCK TITLE

MODULE CONNECTORS
PORTS 1 & 3

SIZE

C

REV.

1.3A

DRAWING NO.

1.3

DATE

3/11/2009

ENGINEER

ENCADIS

PETER J. GONCALVES

DESIGN, INC. NECTON, MA 01936

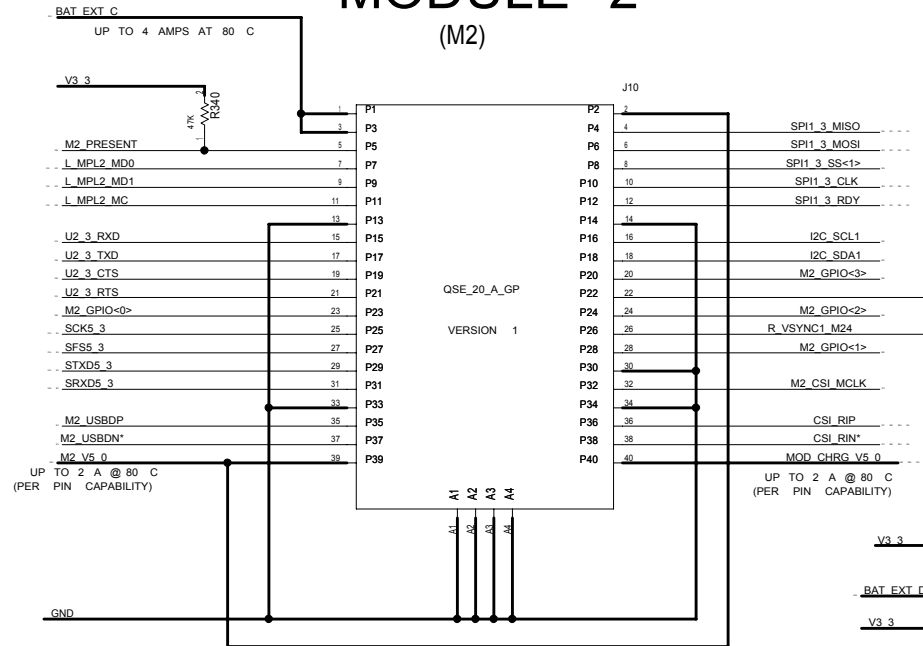
SHEET

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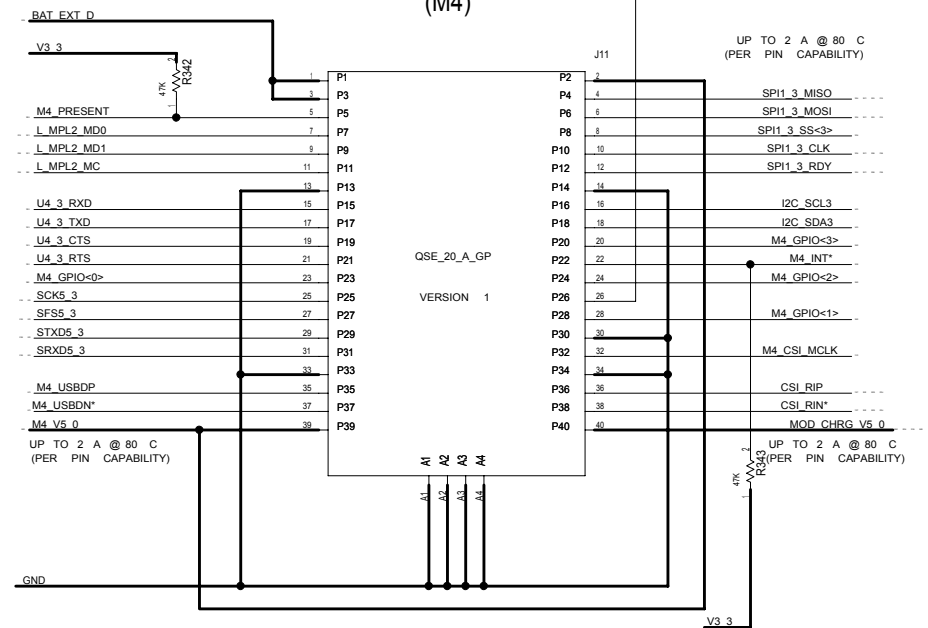
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28

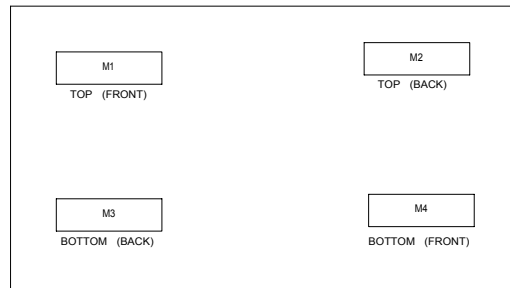
MODULE 2 (M2)



MODULE 4 (M4)

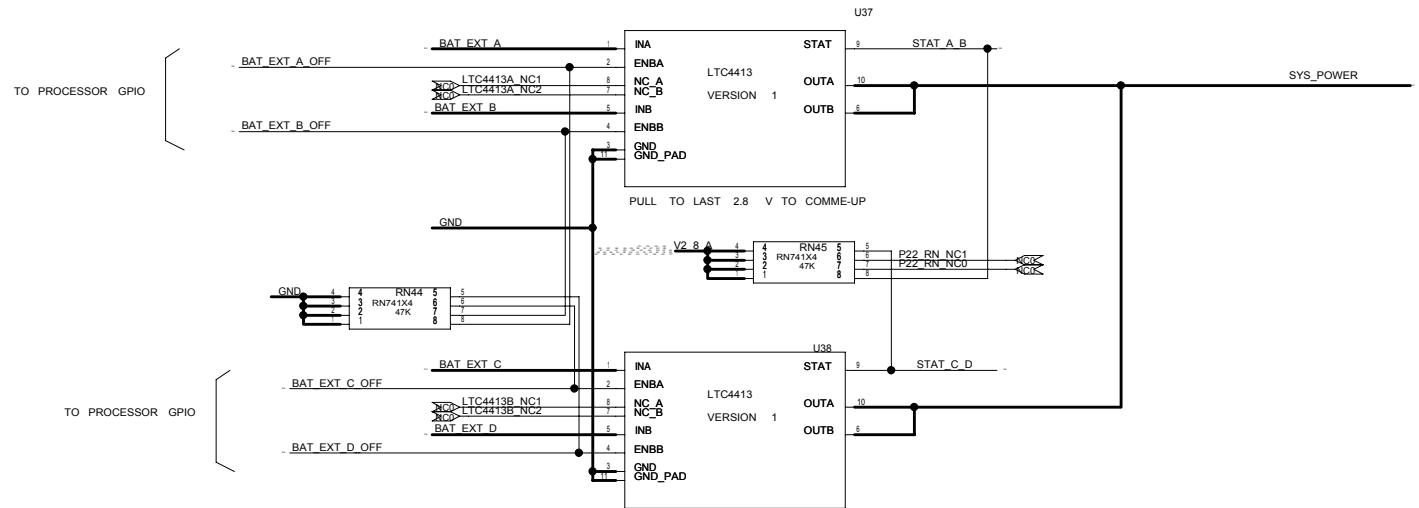


PLACE M2 AND M4 ON SAME VERTICAL HALF
(RIGHT) OF BASE ON OPPOSITE SIDES



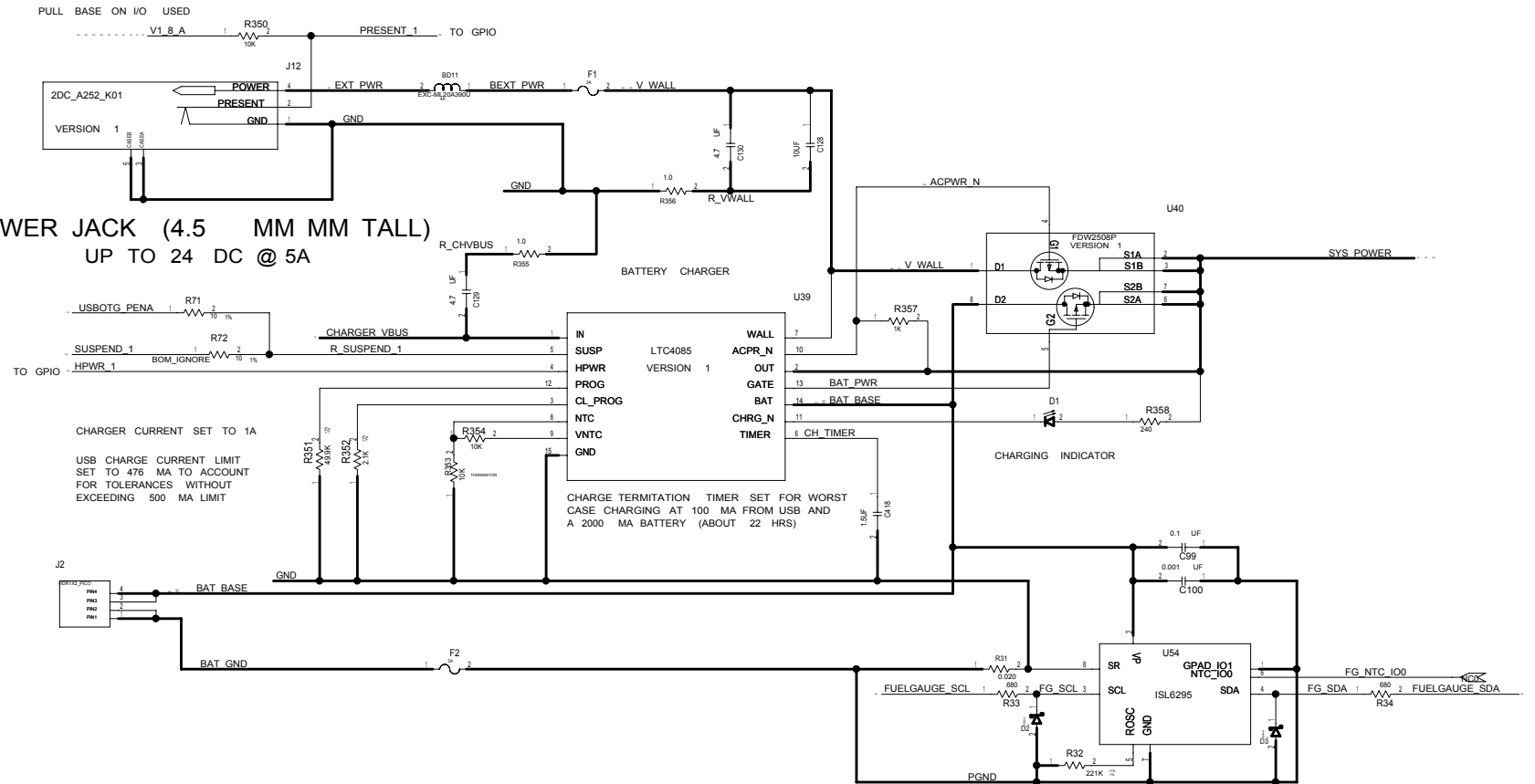
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EXTERNAL BATTERY SHARING CONTROL



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DRAWING TITLE				BLOCK TITLE					
BUG2 WIFI				MULTI-BATTERY LOAD SHARING UP TO FOUR BATTERIES & MODULES BATTERY SHARING					
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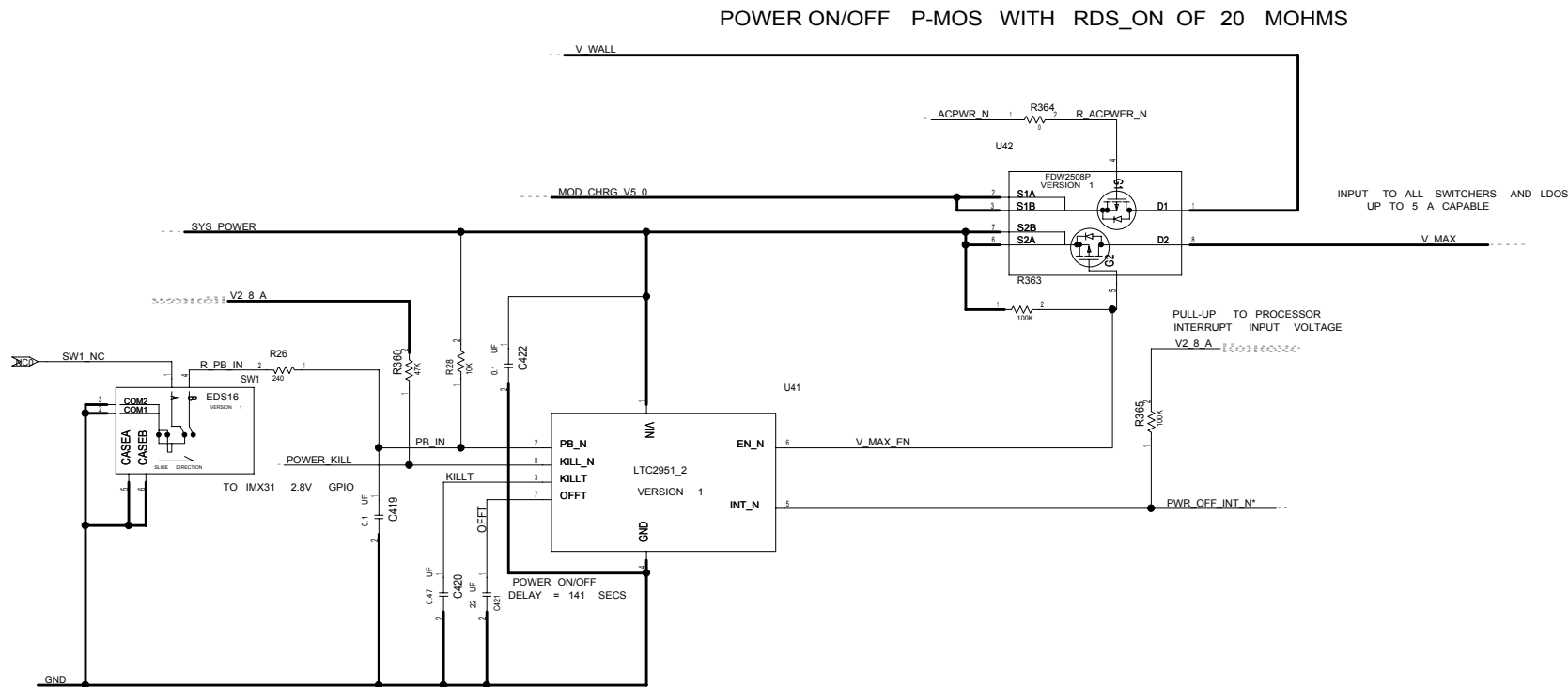
POWER JACK (4.5 MM MM TALL) UP TO 24 DC @ 5A



BATTERY CONNECTOR

THIS A TWO PIN HEADER PHYSICALLY WITH TWO CONTACT PADS PER PIN
PINS 1 AND 2 REPRESENT THE LEFT PIN WHEN FACING THE HEADER
WHEN FACING MATING PLUG, RIGHTMOST PIN SHOULD ATTACH TO BATTERY GROUND

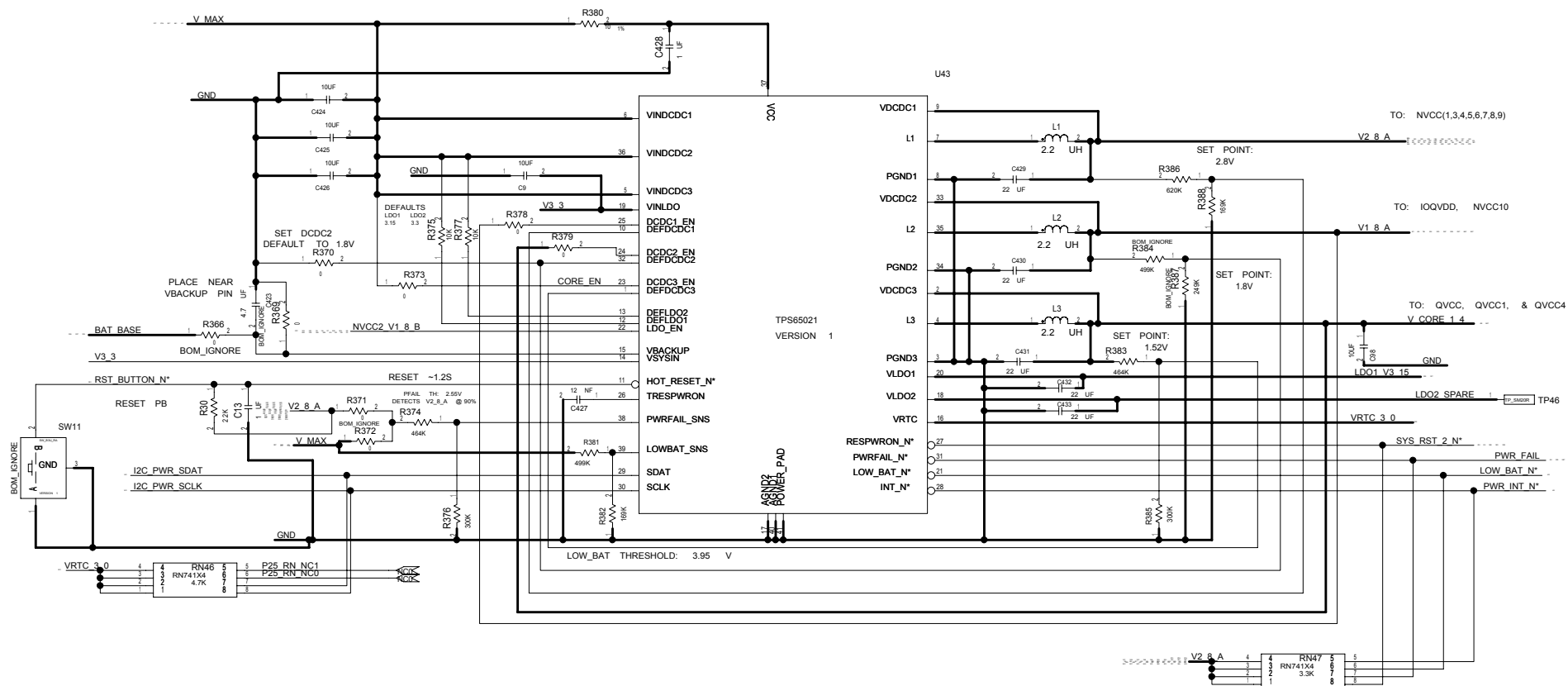
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BUG2 BASE		AC/USB BATTERY CHARGER	
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DATE 7/13/06		ENGINEER H. F. RODRIGUEZ	DRAWING NO. 1.0
		SHEET 23	OF 28



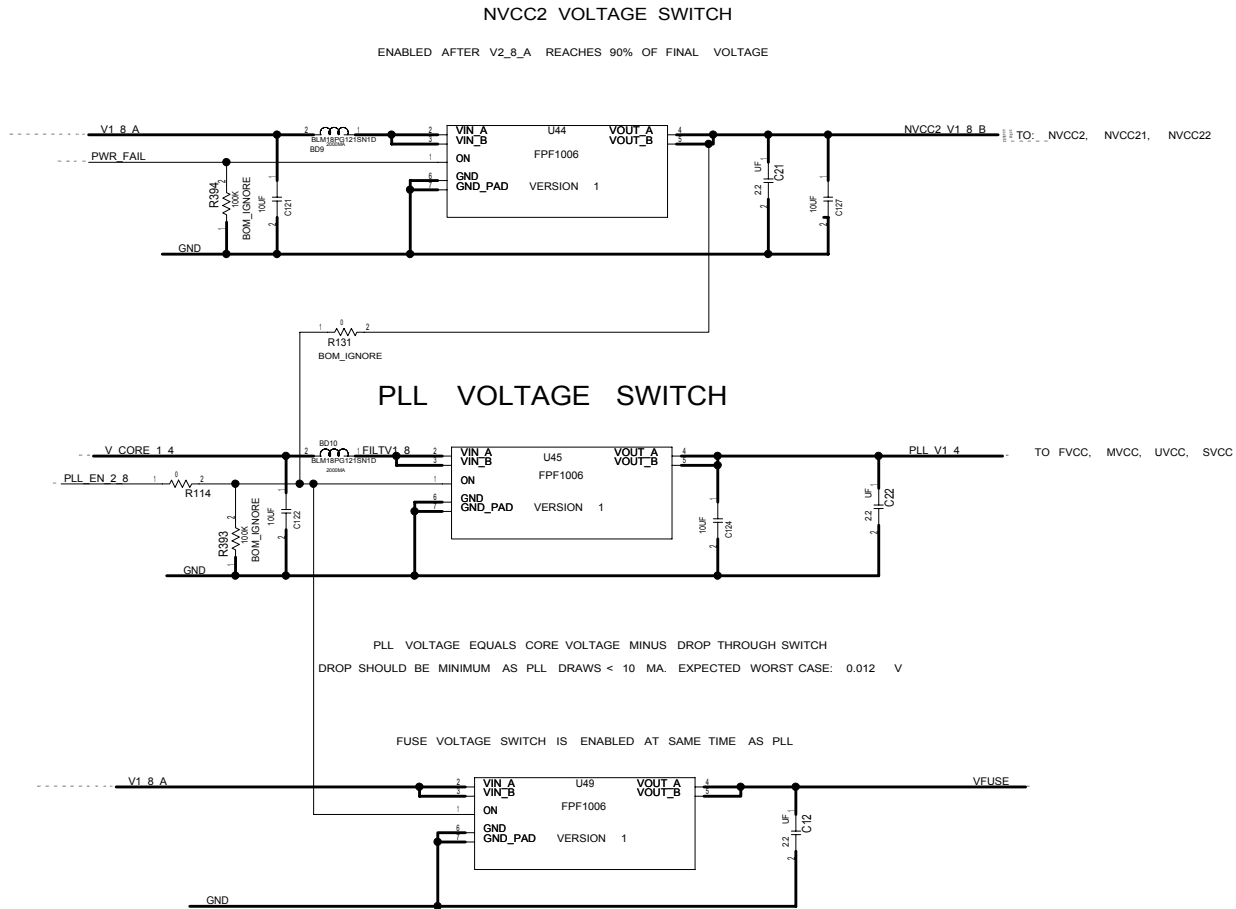
POWER ON/OFF SWITCH TIMING AND DEBOUNCING



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SHEET 24		OF 28	

PLACE A 10 UF CAP NEAR EACH VINDCDCX PIN

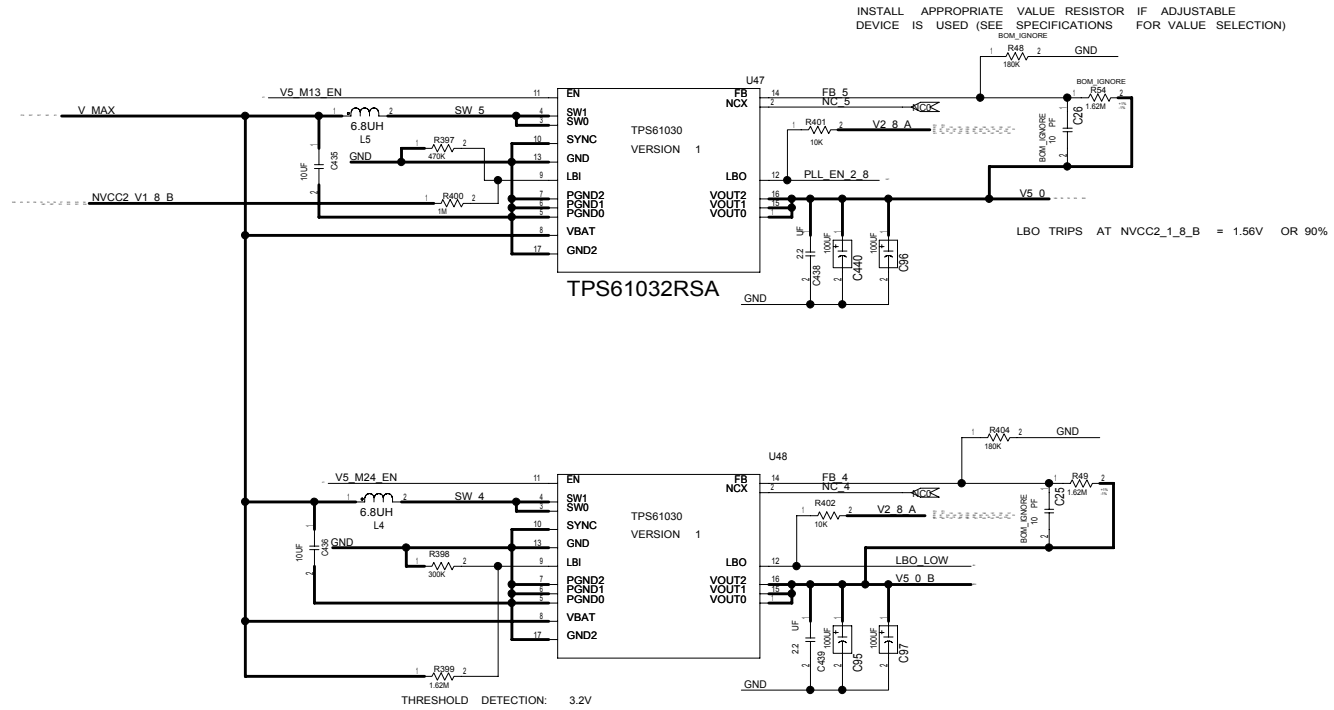


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BUG2 WIFI				PROGRAMMABLE POWER SUPPLY			
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DESIGNER, INC. PETER J. GONZALEZ				SHEET 25 OF 28			

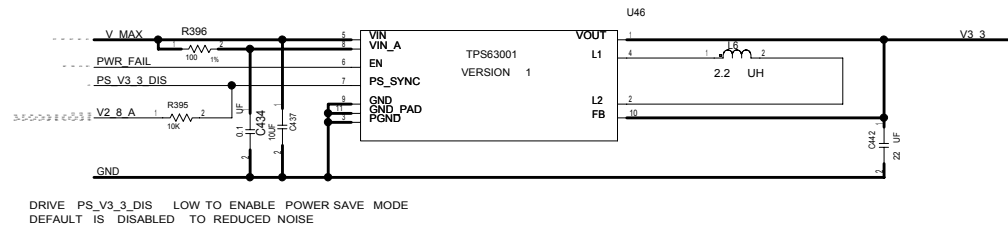


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 BUG2 WIFI		NVCC2 AND PLL POWER SWITCHES	
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MODULES 5 VOLTS SUPPLIES

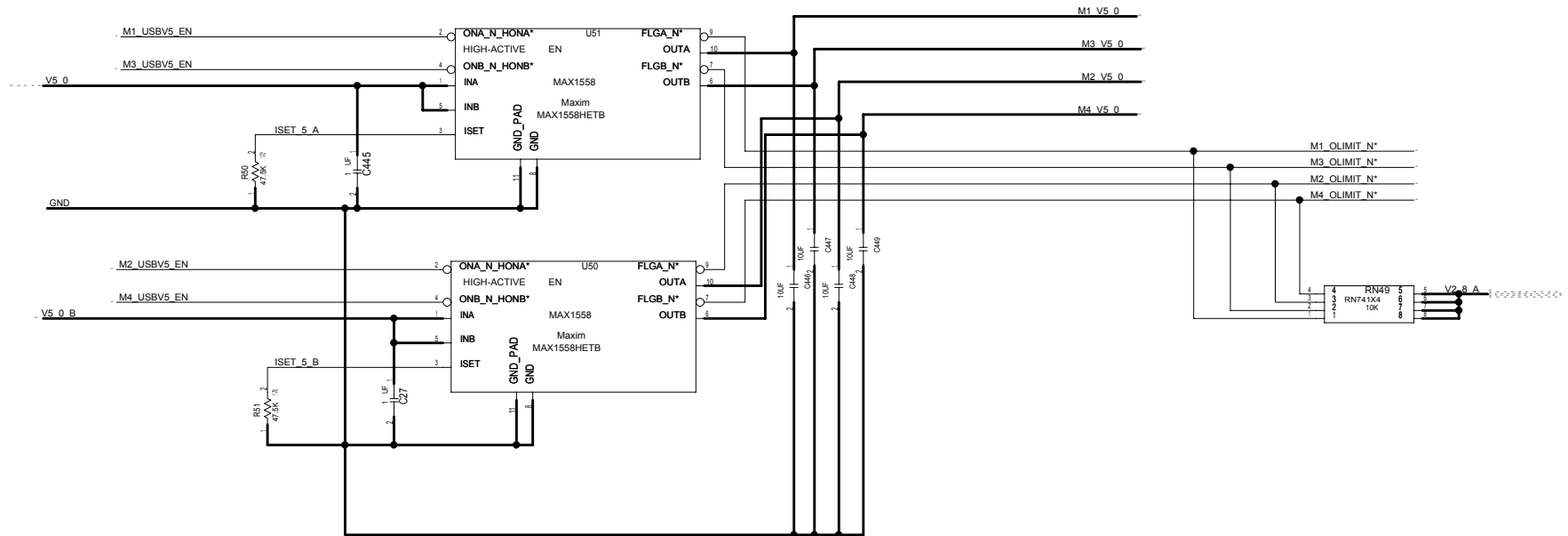


3.3V SUPPLY (BUCK-BOOST UP TO 1.5A)



DRAWING TITLE				BLOCK TITLE			
BUG2 WIFI				HIGH VOLTAGE SUPPLIES (5.0, 4.3, & 3.3 VOLTS)			
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DATE 3/11/2009		ENGINEER		SHEET OF 27 OF 28		DRAWING NO. 1.3	

MODULES 5 VOLTS SWITCHES



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3/11/2009		C	1.3A
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ENCADIS		1.3	
DESIGN, INC.		PETER J. GARCIA	
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SHEET		OF	
28		28	

